AN90030

Paralleling of Nexperia GaN FETs in half-bridge topology

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Document information

Information	Content
Keywords	NX-HB7000EV, GaN FET, TO-247, half-bridge, converter, paralleling, circuit design, PCB layout
Abstract	This appplication note explains the recommendations for circuit design and PCB layout when paralleling Nexperia TO-247 GaN FETs in a half-bridge configuration.

nexperia

1. Introduction

GaN FETs are becoming increasingly important for modern power conversion systems, examples being inverters, power supplies and on-board chargers. The fundamental building block for many applications is the half-bridge as shown in Fig. 1 below.

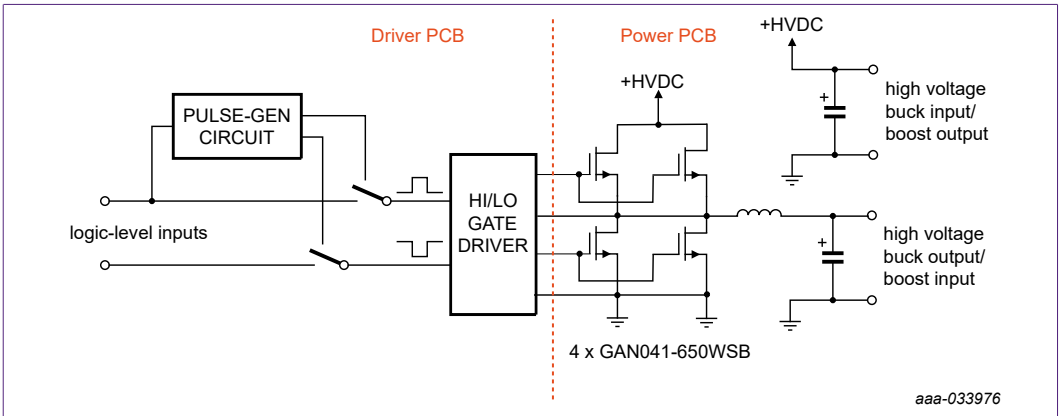

Fig. 1. Half-bridge with paralleled GaN FETs functional block diagram

To realise the power levels demanded by the growing number of high-power applications, designs using multiple GaN FETs in parallel are becoming more widespread.

With both the high currents in conjunction with the fast-switching speeds that are possible when utilising GaN FETs in these systems, these combinations of factors do present some challenges for the designer that will be discussed here.

One of the main challenges is current sharing between GaN FETs and associated switching stability. We will show how to parallel leaded TO-247 GaN FETs used for the high-side and low-side of a half-bridge driving an inductive load effectively.

It is obviously very important for paralleled GaN FETs to share current equally to prevent any individual device suffering from excessive power dissipation that could compromise reliability and lifetime. It is also very important that switching is stable without excessive oscillation which would in turn result in higher switching losses than are acceptable.

2. Half-bridge current sharing topology

For the purposes of this application note two paralleled GAN041-650WSB [1] GaN FETs in a side-by-side configuration for both the high-side and low-side have been selected for the half-bridge test circuit, which provides the following design benefits:

- Compact switching node
- Optimised current flow path

In addition to this, a separate PCB is utilised for the Gate drivers, which provides the following design benefits:

- Short and balanced gate drives

Symmetry is the key factor so that the effective impedance paths are matched as much as possible.

3. Gate drive design considerations

In this study we use a common gate driver for the paralleled GaN FETs. This means that the normal requirement for short gate-drive loops is complicated by the need for matched switching behaviour. Gate drive loops give the best performance when the Gate-Source loops are equalised in terms of path length (effective impedance) for each device being paralleled.

The drivers should be physically as close to the gates as possible to limit the track lengths, which provides the following benefits:

- Current shared equally by linear design
- Gate track lengths equal (as highlighted by the red rectangles in Fig. 2).

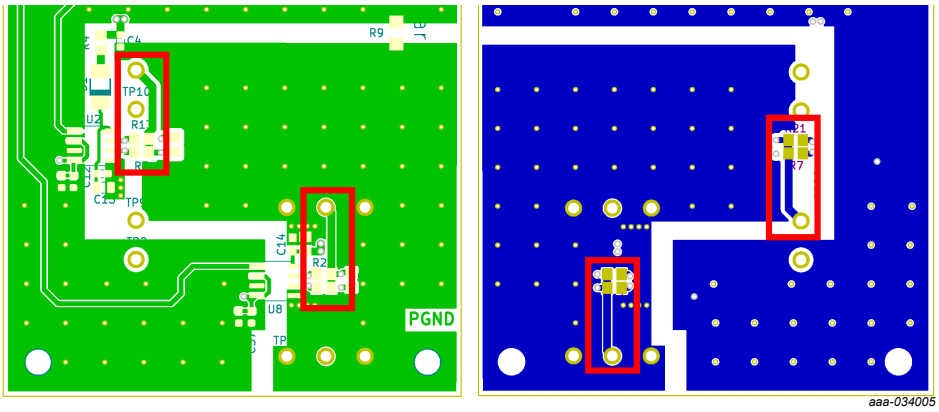

Fig. 2. Gate driver PCB track lengths

Best design practice is for the driver to be placed on the same PCB as the GaN FETs so that the inductance between the Source pin and driver are reduced as much as practically possible.

However, where this is not feasible due to design, placement or packaging constraints, and a separate driver board must be used, then the use of short wide tracks or ideally multiple signal planes on both boards, in association with large gauge terminals soldered between the boards, is advised. This will reduce the inductance between the GaN FET Source pin and driver as much as practically possible. Use of non-soldered connectors, such as plugs and sockets, are not recommended in the Gate-Source loop as these typically increase the inductance, leading to an increased risk of oscillation.

Also, for best Gate signal integrity, it is recommended that the connection between the Source pin and driver are to a “quiet” ground connection, where none of the main current is able to flow.

3.1. Gate driver IC considerations

Isolated driver ICs offer packaging benefits as transformer isolation is a standard requirement for most designers to use between the controller and the power electronics and driver.

The gate driver IC utilized for the half-bridge test circuit is from the Silicon Labs Si827x series, specifically the Si8271[2].

Features which make these gate drivers an appropriate choice include:

- high dv/dt immunity of 200 kV/µs CMTI
- fully isolated
- high output source/sink current capability

Similar features are available in gate driver ICs from other manufacturers also.

3.2. Gate Ferrite beads and resistors

Due to the extremely fast dv/dt that occurs during switching, this increases the possibility of oscillation in the half-bridge test circuit, which can very quickly lead to device damage or destruction. However, with very careful selection of the Gate ferrite bead and resistors for each connection to the GaN FETs, the possibility of oscillation can be minimised.

The GAN041-650WSB GaN FETs do not have an internal ferrite bead and as such allows the designer much more flexibility in selecting the optimal component required. As specified in the Nexperia GAN041-650WSB data sheet [1], the recommended ferrite bead is the BLM18AG221SN1D, supplied by Murata. This ferrite has a typical impedance of 220 Ω at 100 MHz and has been found to be extremely effective in suppressing any gate circuit instability in the half-bridge test circuit.

Along with the ferrite bead, the value of the resistor(s) in the gate circuit also contributes significantly to the switching stability. Nexperia recommends that initial stability tests are conducted with a gate resistance of 15 Ω. However, the final value(s) chosen will depend on the driver used and its respective current source/sink capabilities.

For the half-bridge test circuit, resistances of 15 Ω and 7.5 Ω are connected to the active high and low outputs of the drivers respectively.

While individual ferrite beads should be used in series with each gate, a single gate resistor can be used at the driver output. Refer to the schematics Fig. 21 and Fig. 26 for further details.

4. DC bus snubbers and decoupling

DC bus snubbers must be connected between the high voltage and ground planes (very large voltage overshoots are seen without appropriate suppression) and should be located as close as possible to each GaN FET. Typically, these DC Bus snubbers would consist of a 10 Ω resistor in series with 10 nF capacitor.

Also, decoupling capacitances of 10 nF and 100 nF value should be located as close as possible to each GaN FET and be connected between the high voltage and ground planes. See Fig. 3 and Fig. 4.

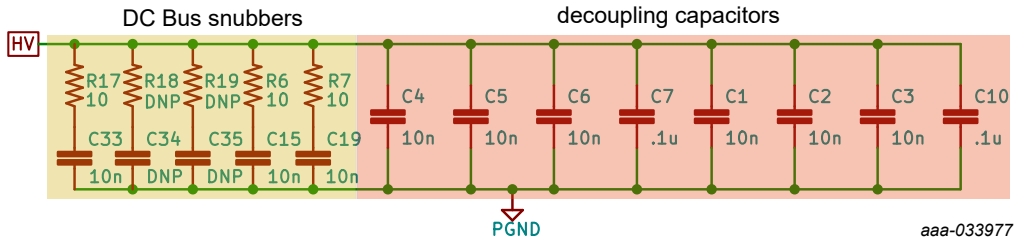

Fig. 3. Bus snubber RC networks and decoupling capacitors schematic

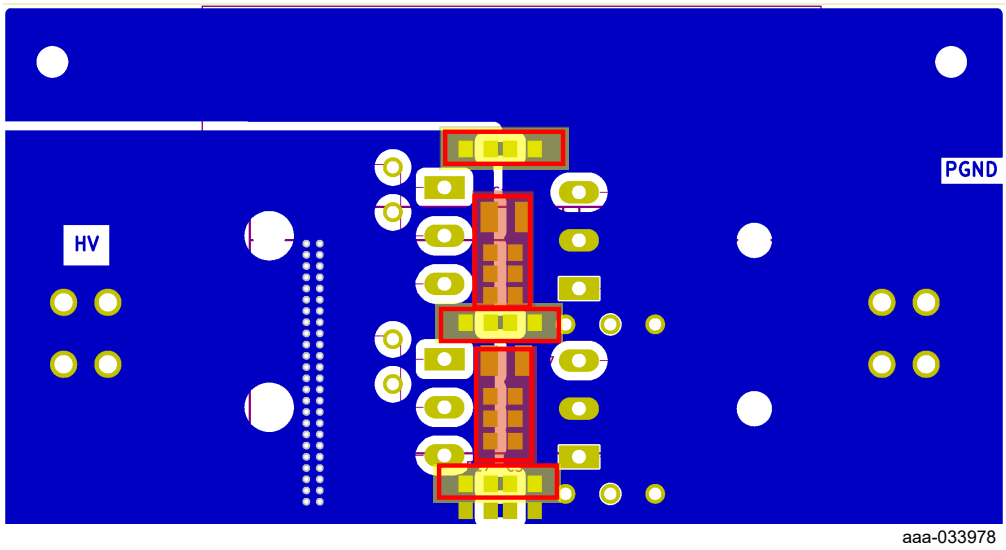

Fig. 4. Bus snubber RC networks and decoupling capacitors PCB layout

4.1. Switching node snubber

Switching node snubbers are only recommended to achieve maximum stability at high switching currents. These will increase the switching loss and are only recommended at high power levels where the losses are a very small percentage of the total power.

Although provision has been made in the half-bridge test circuit for multiple snubbers between the DC bus and switch node and between the Switch Node and Ground, none were required to be populated to achieve switching stability and excellent switch node voltage overshoot control and damping.

4.2. Thermal considerations

The R_{DSon} of the cascode GaN HEMT has a positive temperature coefficient. The $V_{GS(th)}$ of the GaN FET has a negative temperature coefficient which means that the device with the higher junction temperature will turn on first and therefore be subjected to a higher share of the current. However, the GaN FETs have been mounted so that even heat distribution is achieved, which results in even current sharing between devices. So, when paralleling GaN FETs, it is very important for them to be effectively heatsinked and implicitly very well connected thermally together.

5. Layout optimisation for current Sharing

Testing has shown that current sharing can be improved by positioning the devices in line with the current and load path to keep the distances between the inputs and outputs symmetrical.

The current path is much better with balanced copper flood planes. For balanced operation, a layout should aim to have the parallel devices in line with the load and power as shown in Fig. 5, keeping the current loop as small as possible.

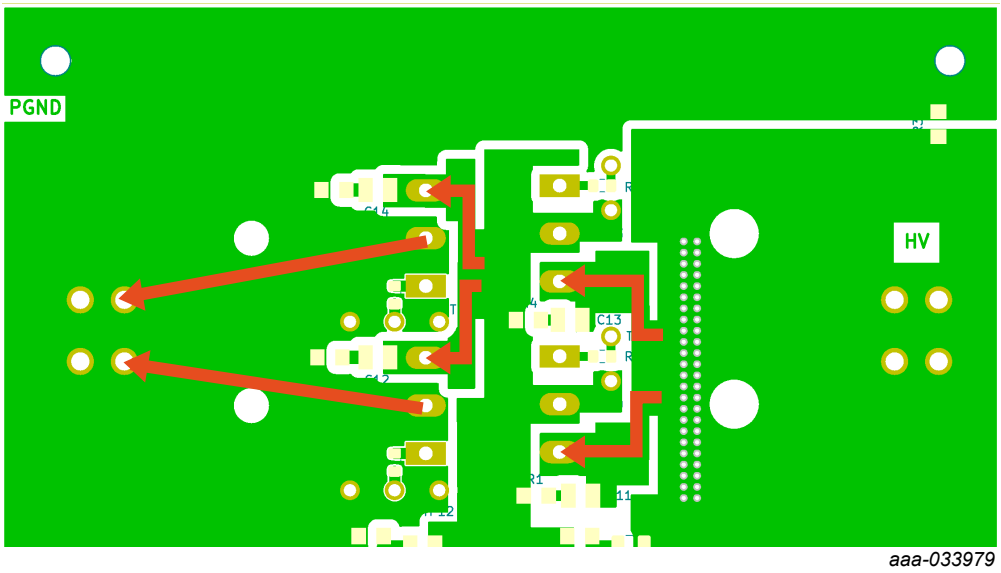

Fig. 5. PCB current paths

6. Captured waveforms from single-shot staircase test

In this section are shown the test results from performing a seven pulse, single-shot staircase test at 100 kHz. The inductor is connected to the BUS voltage set at 400 V and the current flows through the low-side GaN FETs and recirculates through the high-side GaN FETs. Each pulse has a width of 1.9 µs, leading to a peak inductor current of 114 A.

See Fig. 6, the oscilloscope channel identifications are as follows:

- C1 – low-side GaN FET Q2 gate signal
- C2 – low-side GaN FET Q4 gate signal
- C3 – inductor current
- C4 – switch node voltage

aaa-033980

Fig. 6. Single-Shot staircase test waveforms

Note : An air-cored non-overlapped inductor is used, avoiding saturation and keeping winding parasitic capacitance low.

aaa-033981

Fig. 7. Zoom of final pulse

Notice how closely matched the gate signals are, and that they are nicely damped at switch off - as such there is no risk of sustained oscillation.

The impedance of the ferrite bead permits the ringing on the internal Source inductance to be visible at the Gate pin. This is a natural consequence of the decoupling effect of the ferrite. If the Gate potential were held rigidly, then instead of observable voltage oscillations, there would be unobservable current oscillations which would be coupled and amplified.

Fig. 8 shows the individual GaN FET currents measured in the same seven pulse, 100 kHz, staircase test.

The oscilloscope channel identification are as follows:

- C1 – low-side GaN FET Q2 gate signal
- C2 – switch node voltage
- C3 – low-side GaN FET Q2 device current
- C4 – low-side GaN FET Q4 device current

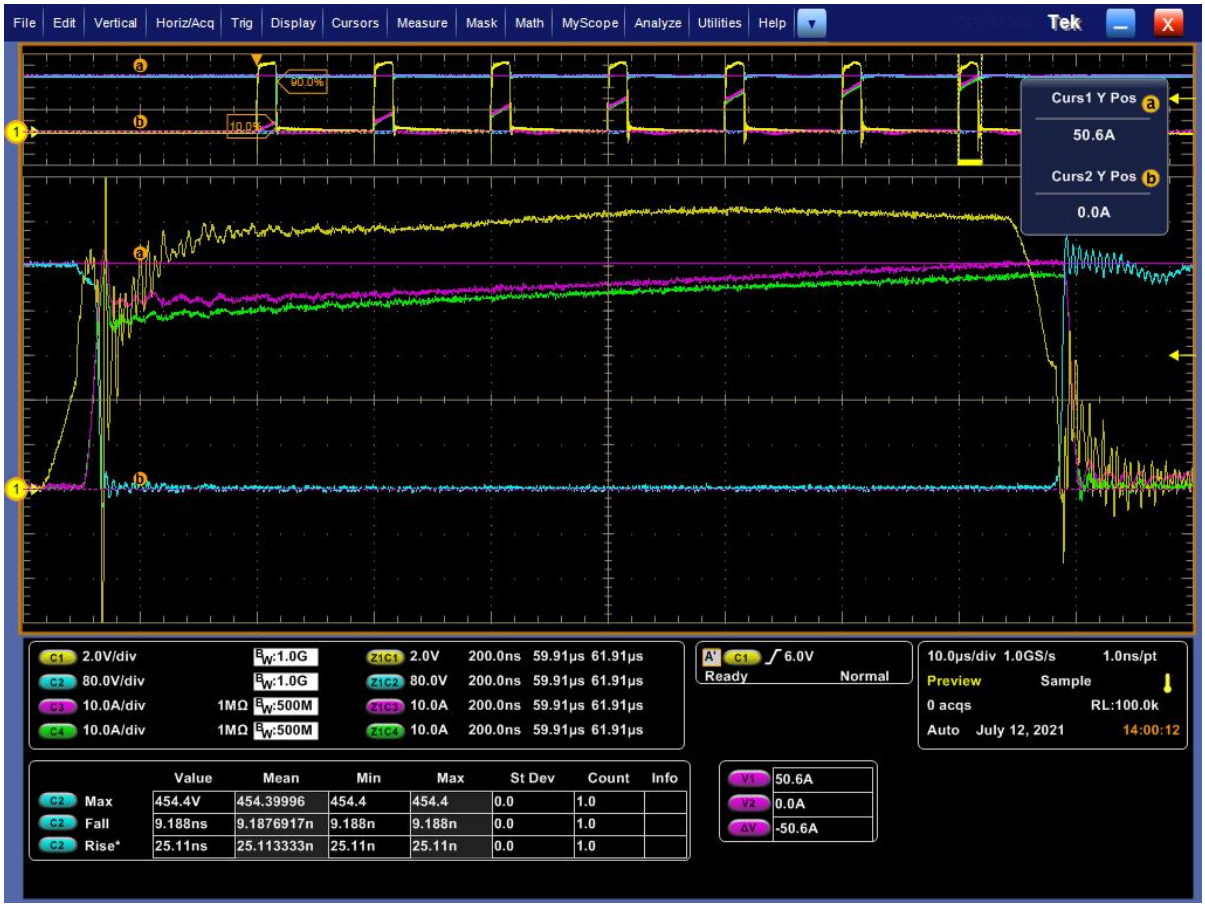

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Fig. 8. Individual GaN FET currents

Note - the magenta and green traces are measured GaN FET currents, showing excellent current sharing between devices.

7. System performance running in BUCK mode

In this section are shown the captured oscilloscope traces and test results when the system is running in BUCK mode. The operating conditions are as follows:

- Input voltage = 400 V
- Output voltage = 225 V
- Output power = 6.6 kW
- Switching frequency = 100 kHz
- Ambient temperature = 34 °C

In Fig. 9 the oscilloscope channel identification are as follows:

- C1 – low-side GaN FET Q2 Gate signal
- C2 – low-side GaN FET Q4 Gate signal
- C3 – Inductor current
- C4 – Switch Node voltage

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Fig. 9. System running in BUCK mode

Fig. 10 and Fig. 11 show zooms of the low-side GaN FETs during switch ON and switch OFF.

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Fig. 10. Zoom of Q2 and Q4 low-side GaN FETs - switch ON

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Fig. 11. Zoom of Q2 and Q4 low-side GaN FETs - switch OFF

Note that during switching events any voltage oscillations on both the Gate and Switch Node signals have been very effectively damped.

Fig. 12 shows the high-side currents, the oscilloscope channel identification are as follows:

- C1 – low-side GaN FET Q2 Gate signal
- C2 – Switch Node voltage
- C3 – high-side GaN FET Q1 device current
- C4 – high-side GaN FET Q3 device current

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Fig. 12. System running in BUCK mode - GaN FET high-side currents

Fig. 13 shows the low-side device currents, the oscilloscope channel identification are as follows:

- C1 – low-side GaN FET Q2 Gate signal
- C2 – Switch Node voltage
- C3 – low-side GaN FET Q2 device current
- C4 – low-side GaN FET Q4 device current

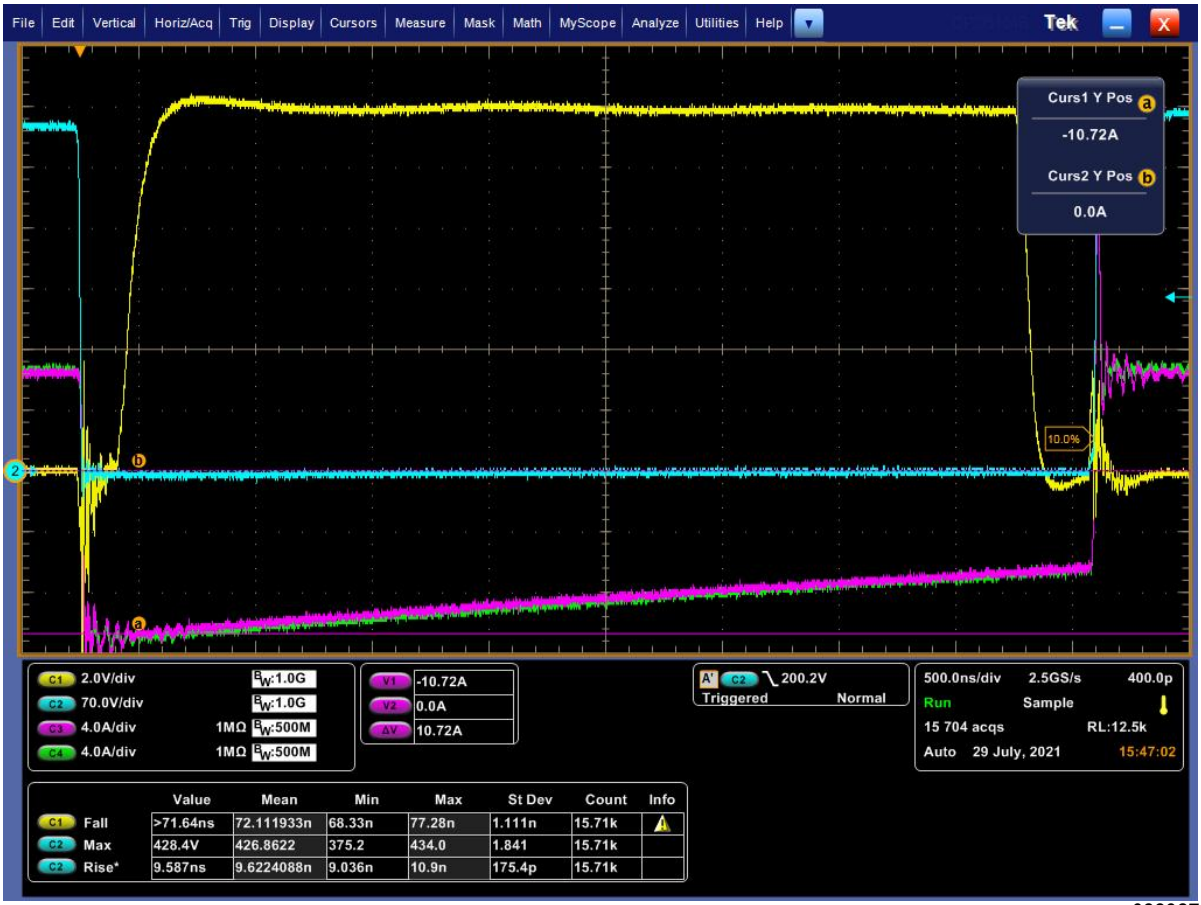

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Fig. 13. System running in BUCK mode - GaN FET low-side currents

7.1. Efficiency sweep and device temperatures

Fig. 14 shows the measured efficiency of the circuit using 2 parallel GAN041-650WSB GaN FETs while operating in BUCK mode.

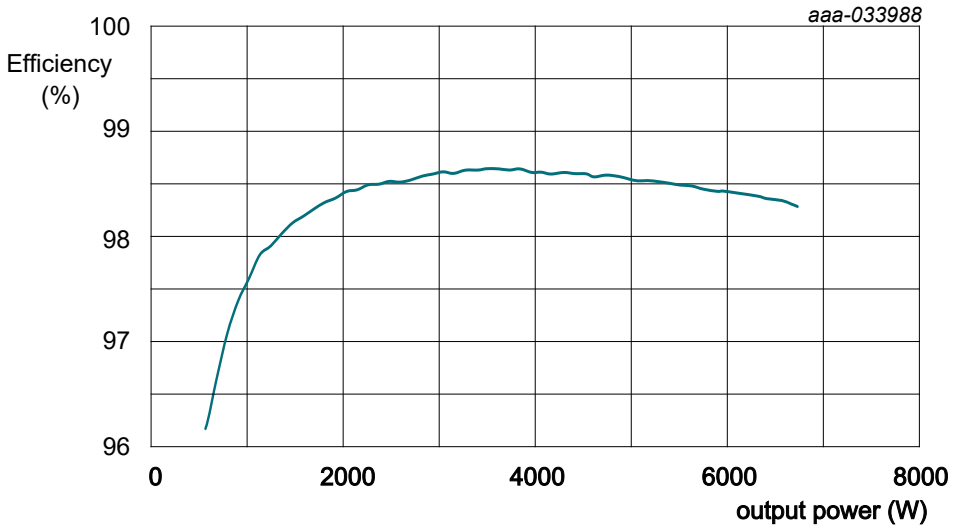

Fig. 14. Efficiency as a function of output power, BUCK mode

Device temperatures were measured using thermocouples bonded to the front face of the mounting bases and are all very close to each other:

- high-side GaN FET Q1 = 69.6 °C
- high-side GaN FET Q3 = 74.9 °C
- low-side GaN FET Q2 = 72.3 °C
- low-side GaN FET Q4 = 69.1 °C

These results confirm excellent current sharing and thermal connection of all devices.

8. System performance running in BOOST mode

In this section are shown the captured oscilloscope traces and test results when the system is running in BOOST mode. The operating conditions are as follows:

- Input voltage = 225 V
- Output voltage = 400 V
- Output power = 6.6 kW
- Switching frequency = 100 kHz
- Ambient temperature = 32 °C

In Fig. 15 the oscilloscope channel identification are as follows:

- C1 – low-side GaN FET Q2 Gate signal
- C2 – low-side GaN FET Q4 Gate signal
- C3 – Inductor current
- C4 – Switch Node voltage

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Fig. 15. System running in BOOST mode

Fig. 16 and Fig. 17 show zooms of the low-side GaN FETs during switch ON and switch OFF.

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Fig. 16. Zoom of Q2 and Q4 low-side GaN FETs - switch ON

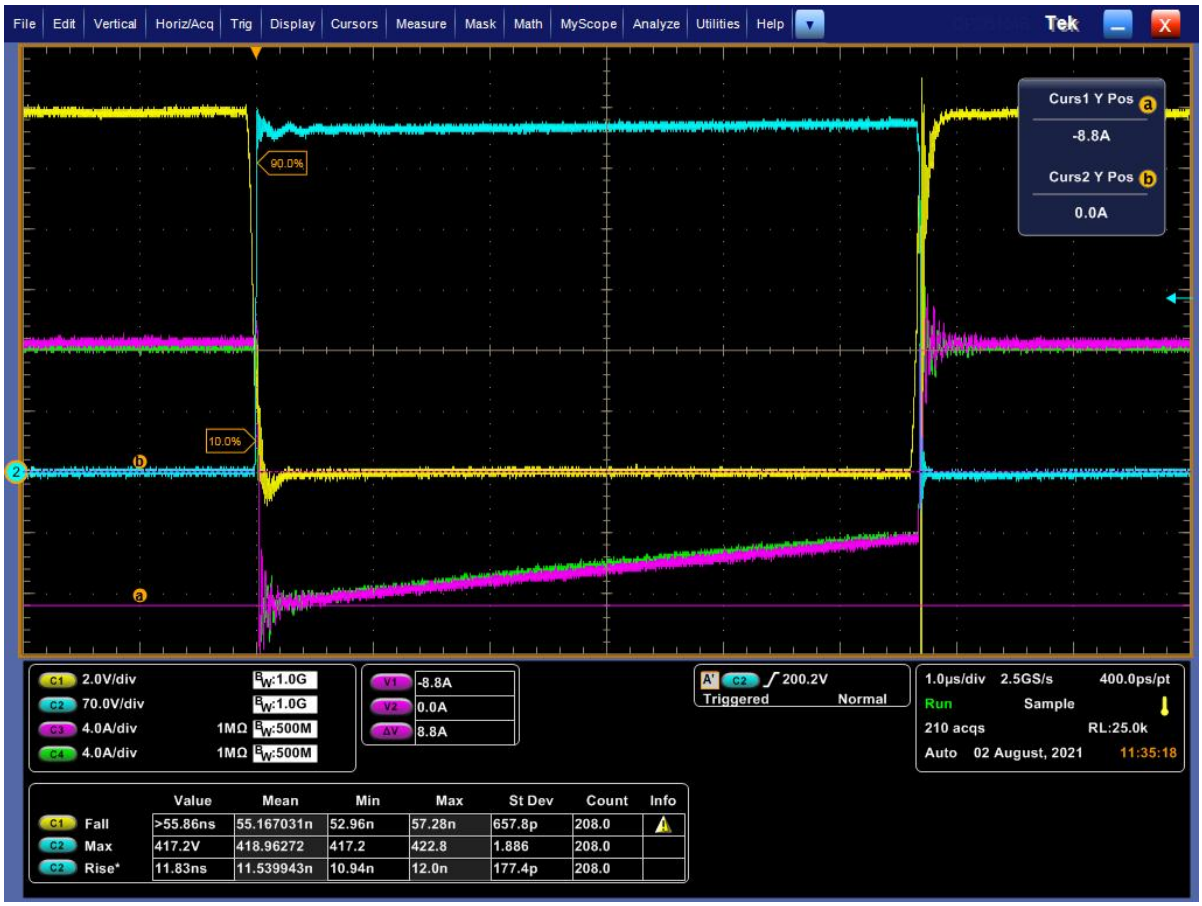
aaa-0339915

Fig. 17. Zoom of Q2 and Q4 low-side GaN FETs - switch OFF

Note that during switching events any voltage oscillations on both the Gate and Switch Node signals have been very effectively damped.

Fig. 18 shows the high-side currents, the oscilloscope channel identification are as follows:

- C1 – low-side GaN FET Q2 Gate signal
- C2 – Switch Node voltage
- C3 – high-side GaN FET Q1 device current
- C4 – high-side GaN FET Q3 device current



aaa-033992

Fig. 18. System running in BOOST mode - GaN FET high-side currents

Fig. 19 show the low-side device currents, the oscilloscope channel identification are as follows:

- C1 – low-side GaN FET Q2 Gate signal
- C2 – Switch Node voltage
- C3 – low-side GaN FET Q2 device current
- C4 – low-side GaN FET Q4 device current

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Fig. 19. System running in BOOST mode - GaN FET low-side currents

8.1. Efficiency sweep and device temperatures

Fig. 20 shows the measured efficiency of the circuit using 2 parallel GAN041-650WSB GaN FETs while operating in BOOST mode.

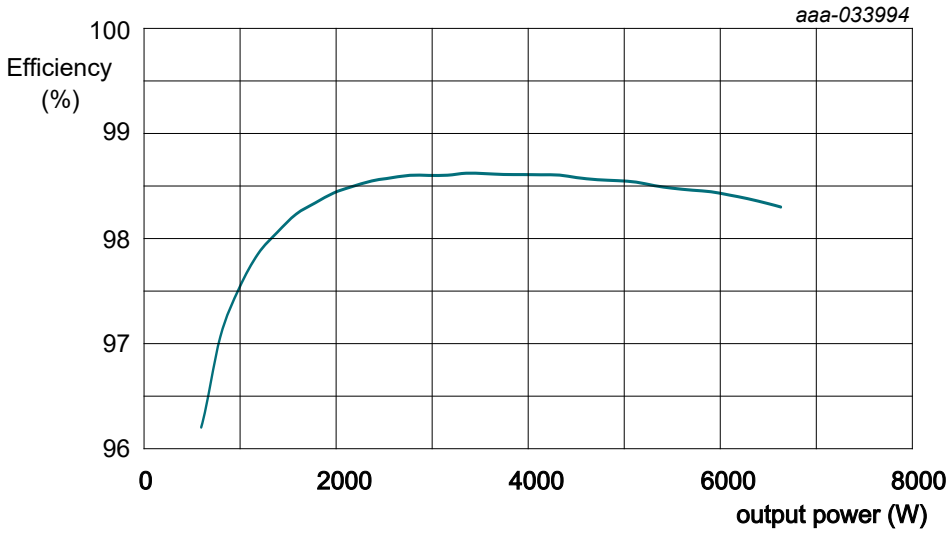

Fig. 20. Efficiency as a function of output power, BOOST mode

Device temperatures were measured using thermocouples bonded to the front face of the mounting bases and are all very close to each other:

- high-side GaN FET Q1 = 60.3 °C
- high-side GaN FET Q3 = 67.2 °C
- low-side GaN FET Q2 = 78.0 °C
- low-side GaN FET Q4 = 71.0 °C

These results confirm excellent current sharing and thermal connection of all devices.

9. Probing considerations

Nexperia application note AN90004[3], "*Probing considerations for fast switching applications*" should be followed to ensure accurate measurement of any switching circuits.

Additionally, the low-side ground spring should either be soldered directly to the Source pin on the package or alternatively to a "quiet" ground connection, where none of the main current is able to flow.

10. Design Details

The half-bridge converter circuit detailind in this application note has been implemented on two 4-layer PCBs with 2oz copper for the outer layers and 1.5 oz copper for the inner layers.

The circuit schematic, PCB layout and Bill of Material for the two PCBs are shown in the next sections.

10.1. Power board schematic

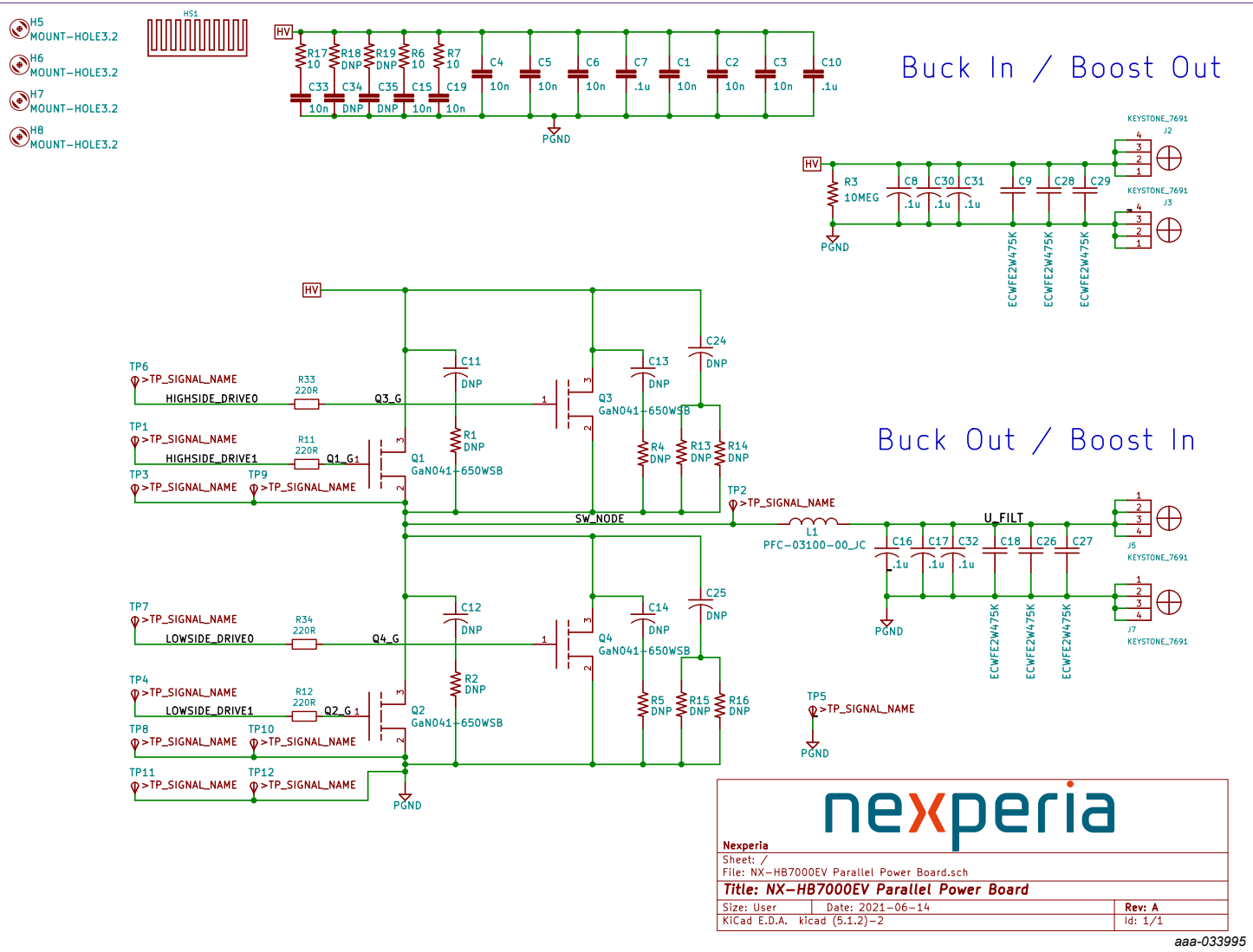

Fig. 21. Power board schematic

10.2. Power board PCB layout, planes and tracking

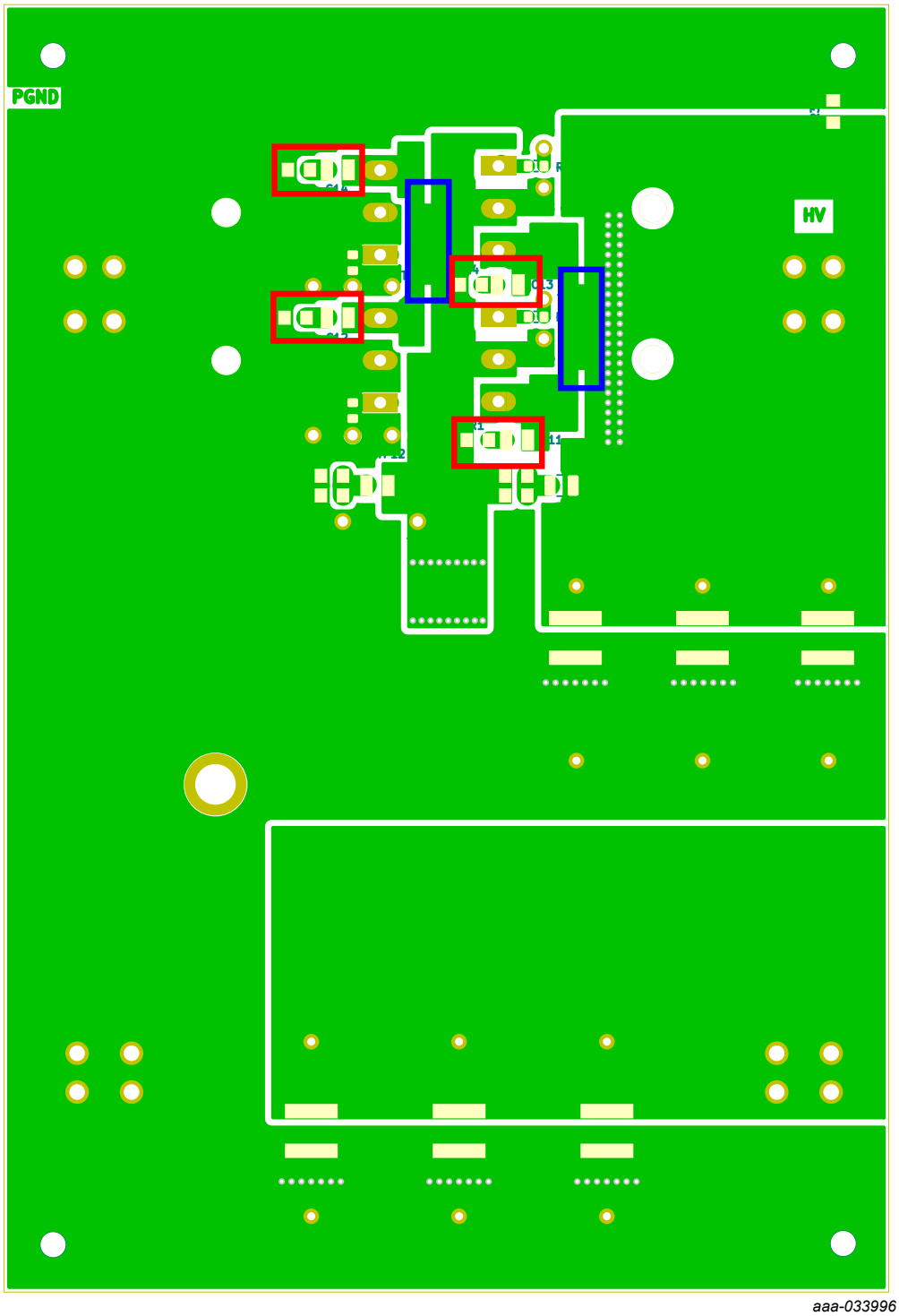

Fig. 22. Power board - top layer

Note how the Drain connections identified by the blue rectangles have been made symmetrically to Switch Node and HV, the snubbers identified by the red rectangles are placed directly on the Drain pins and the use of stitch vias between planes.

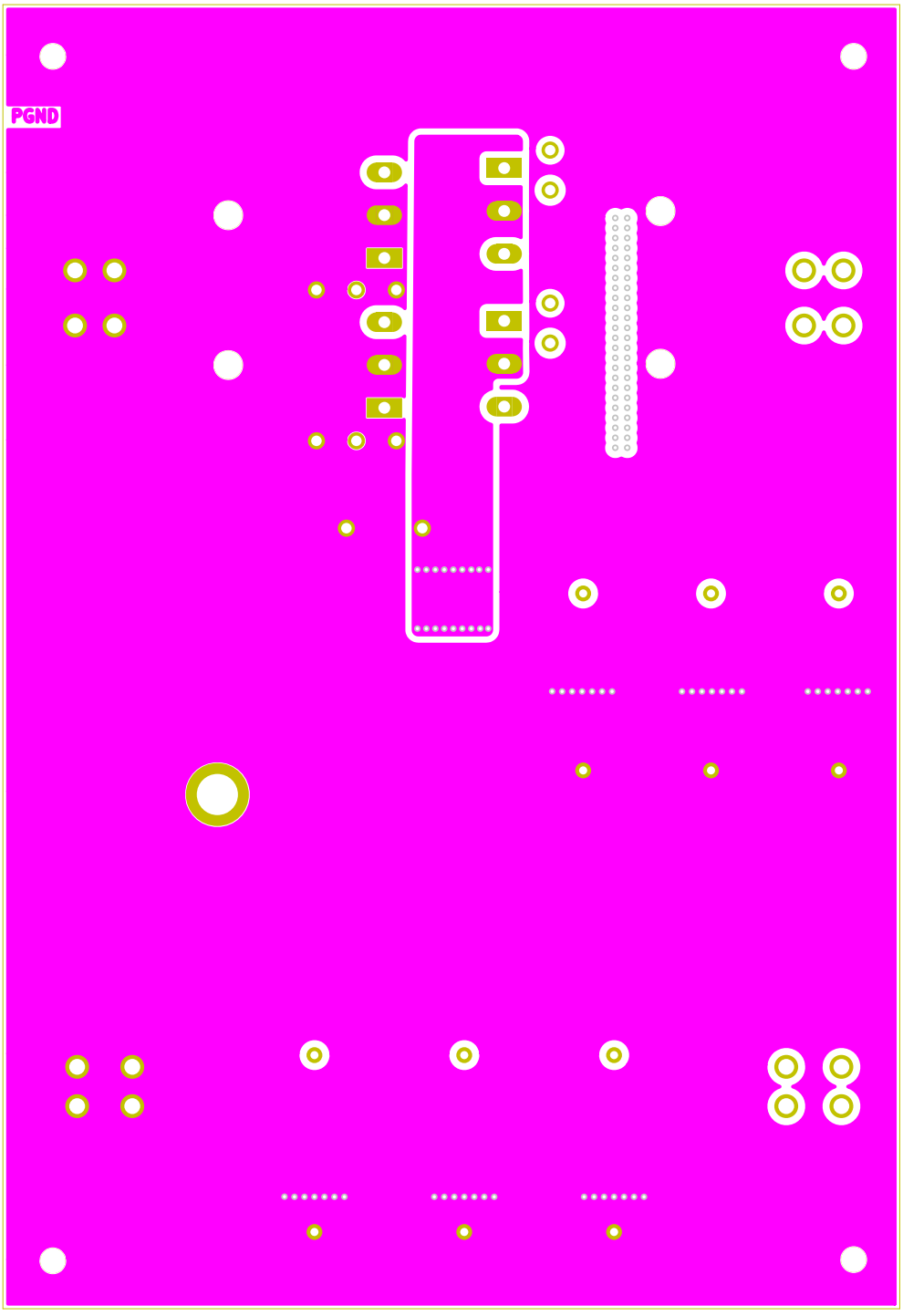

Fig. 23. Power board - inner layer 1 - Switch node and Ground plane

Note the extremely compact Switch Node.

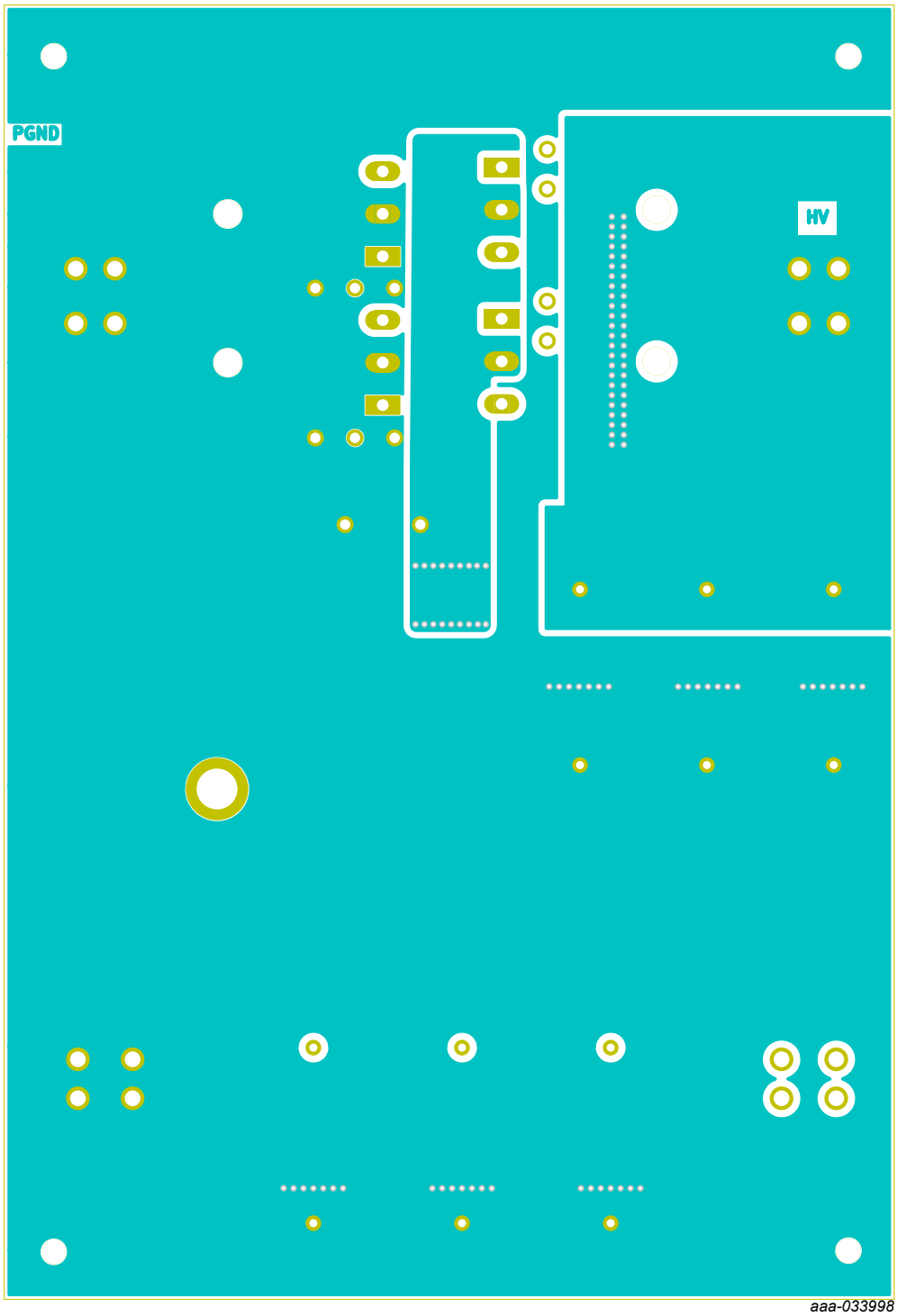

Fig. 24. Power board - inner layer 2 - Switch node, HV and Ground planes

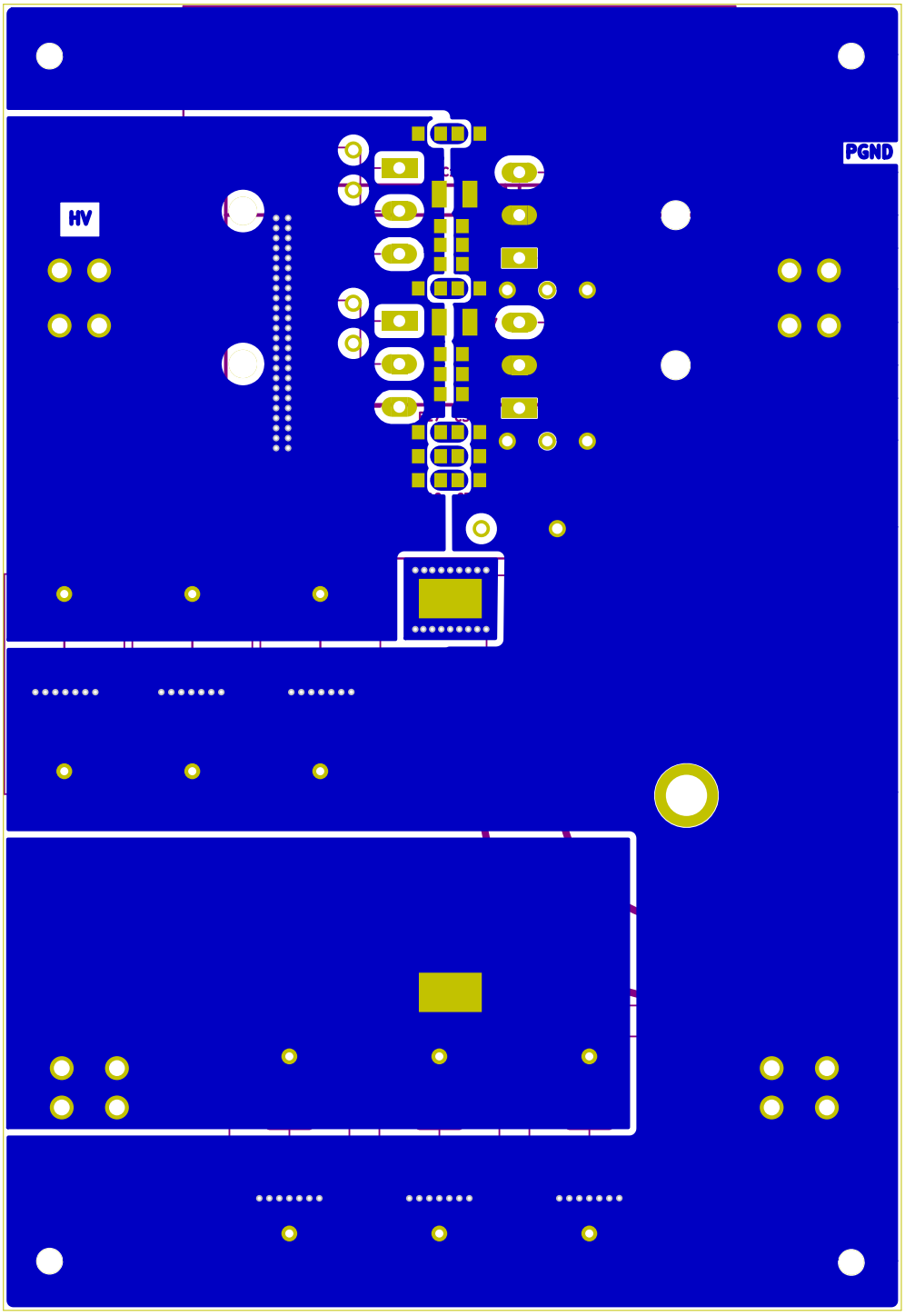

Fig. 25. Power board - bottom layer

10.3. Power board Bill of Materials

Table 1. Power board Bill of Material

Part	Value	Voltage	Package	Description	Supplier	Supplier P/N
C1	10n	630V	C1206	Capacitor, Ceramic	Farnell	1759518
C2	10n	630V	C1206	Capacitor, Ceramic	Farnell	1759518
C3	10n	630V	C1206	Capacitor, Ceramic	Farnell	1759518
C4	10n	630V	C1206	Capacitor, Ceramic	Farnell	1759518
C5	10n	630V	C1206	Capacitor, Ceramic	Farnell	1759518
C6	10n	630V	C1206	Capacitor, Ceramic	Farnell	1759518
C7	100n	1kV	C1812	Capacitor, Ceramic	Farnell	2085218
C8	100n	1kV	C2225	Capacitor, Ceramic	Farnell	1838767 or 2896821
C9	2.2uF	630V	PHE450_2U	Capacitor, PP Film	RS	105-1057
C10	100n	1kV	C1812	Capacitor, Ceramic	Farnell	2085218
C11	-	-	C1210	Capacitor, Ceramic	-	-
C12	-	-	C1210	Capacitor, Ceramic	-	-
C13	-	-	C1210	Capacitor, Ceramic	-	-
C14	-	-	C1210	Capacitor, Ceramic	-	-
C15	10n	630V	C1206	Capacitor, Ceramic	Farnell	1759518
C16	100n	1kV	C2225	Capacitor, Ceramic	Farnell	1838767 or 2896821
C17	100n	1kV	C2225	Capacitor, Ceramic	Farnell	1838767 or 2896821
C18	2.2uF	630V	PHE450_2U	Capacitor, PP Film	RS	105-1057
C19	10n	630V	C1206	Capacitor, Ceramic	Farnell	1759518
C24	-	-	C1210	Capacitor, Ceramic	-	-
C25	-	-	C1210	Capacitor, Ceramic	-	-
C26	2.2uF	630V	PHE450_2U	Capacitor, PP Film	RS	105-1057
C27	2.2uF	630V	PHE450_2U	Capacitor, PP Film	RS	105-1057
C28	2.2uF	630V	PHE450_2U	Capacitor, PP Film	RS	105-1057
C29	2.2uF	630V	PHE450_2U	Capacitor, PP Film	RS	105-1057
C30	100n	1kV	C2225	Capacitor, Ceramic	Farnell	1838767 or 2896821
C31	100n	1kV	C2225	Capacitor, Ceramic	Farnell	1838767 or 2896821
C32	100n	1kV	C2225	Capacitor, Ceramic	Farnell	1838767 or 2896821
C33	10n	630V	C1206	Capacitor, Ceramic	Farnell	1759518
C34	-	-	C1210	Capacitor, Ceramic	-	-
C35	-	-	C1210	Capacitor, Ceramic	-	-
HS1			COOL_INNO_1	Heatsink	Cool Innovations	
J2			KEYSTONE _7691	Screw Terminal	Mouser	534-7691-SEMS
J3			KEYSTONE _7691	Screw Terminal	Mouser	534-7691-SEMS

J5			KEYSTONE _7691	Screw Terminal	Mouser	534-7691-SEMS
J7			KEYSTONE _7691	Screw Terminal	Mouser	534-7691-SEMS
L1	220uH					
Q1	GAN041-650WSB	650V	TO-247	GaN FET	Nexperia	GAN041-650WSB
Q2	GAN041-650WSB	650V	TO-247	GaN FET	Nexperia	GAN041-650WSB
Q3	GAN041-650WSB	650V	TO-247	GaN FET	Nexperia	GAN041-650WSB
Q4	GAN041-650WSB	650V	TO-247	GaN FET	Nexperia	GAN041-650WSB
R1	-	-	R1206	Resistor	-	-
R2	-	-	R1206	Resistor	-	-
R3	10MEG		R1206	Resistor	Farnell	1469973
R4	-	-	R1206	Resistor	-	-
R5	-	-	R1206	Resistor	-	-
R6	10	-	R1206	Resistor	Farnell	1738986
R7	10	-	R1206	Resistor	Farnell	1738986
R11	220		0603	Ferrite	Farnell	1515674
R12	220		0603	Ferrite	Farnell	1515674
R13	-	-	R1206	Resistor	-	-
R14	-	-	R1206	Resistor	-	-
R15	-	-	R1206	Resistor	-	-
R16	-	-	R1206	Resistor	-	-
R17	10	-	R1206	Resistor	Farnell	1738986
R18	-	-	R1206	Resistor	-	-
R19	-	-	R1206	Resistor	-	-
R33	220		0603	Ferrite	Farnell	1515674
R34	220		0603	Ferrite	Farnell	1515674
				Alumina insulator	Mouser	532-4169G
				Alumina insulator	Mouser	532-4169G
				Alumina insulator	Mouser	532-4169G
				Alumina insulator	Mouser	532-4169G
				Cooling Fan	RS	922-6248
				Standoff	Farnell	1733422
				Standoff	Farnell	1733422
				Standoff	Farnell	1733422
				Standoff	Farnell	1733422
				Screw M3 x 6mm	RS	560-754
				Screw M3 x 6mm	RS	560-754
				Screw M3 x 6mm	RS	560-754
				Screw M3 x 6mm	RS	560-754
				PCB	PCBWay	NX-HB7000EV Parallel TO-247 Current Board Rev1.1

10.4. Driver board schematics

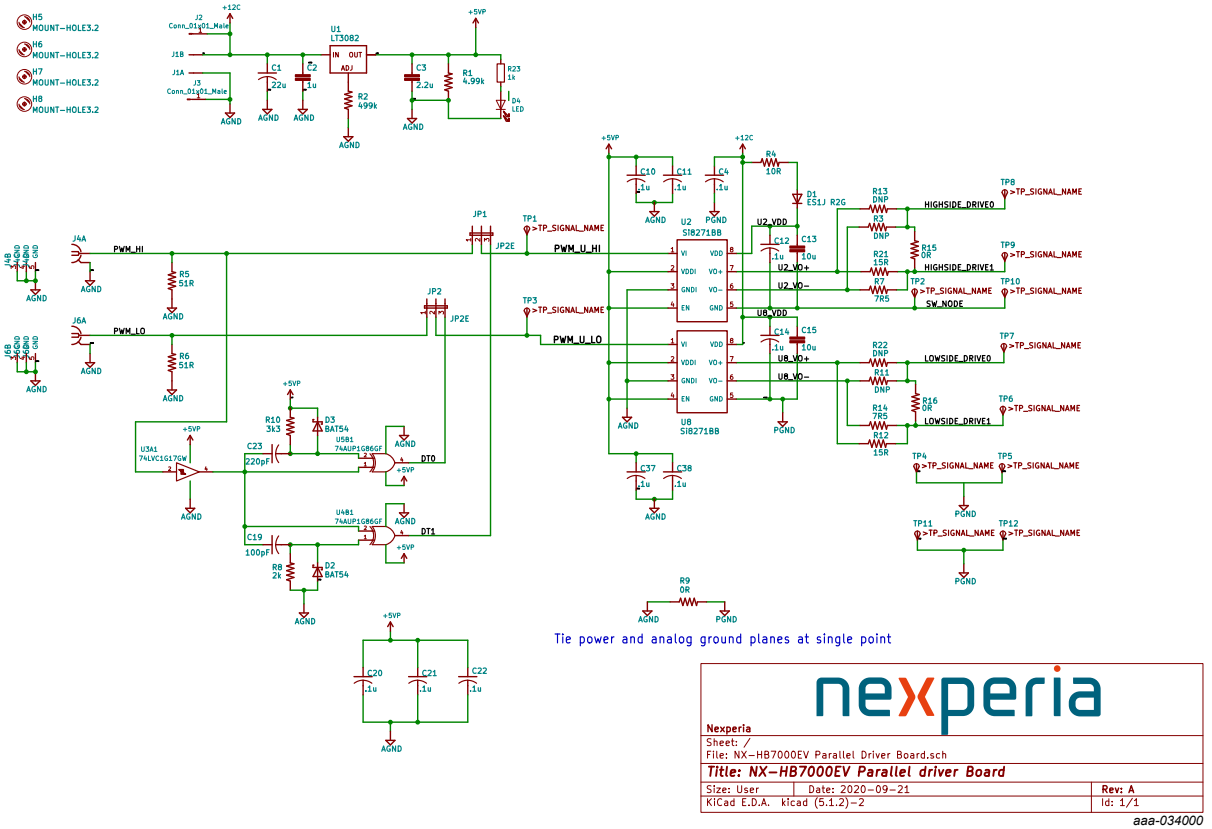

Fig. 26. Driver board schematic

10.5. Driver board PCB layout, planes and tracking

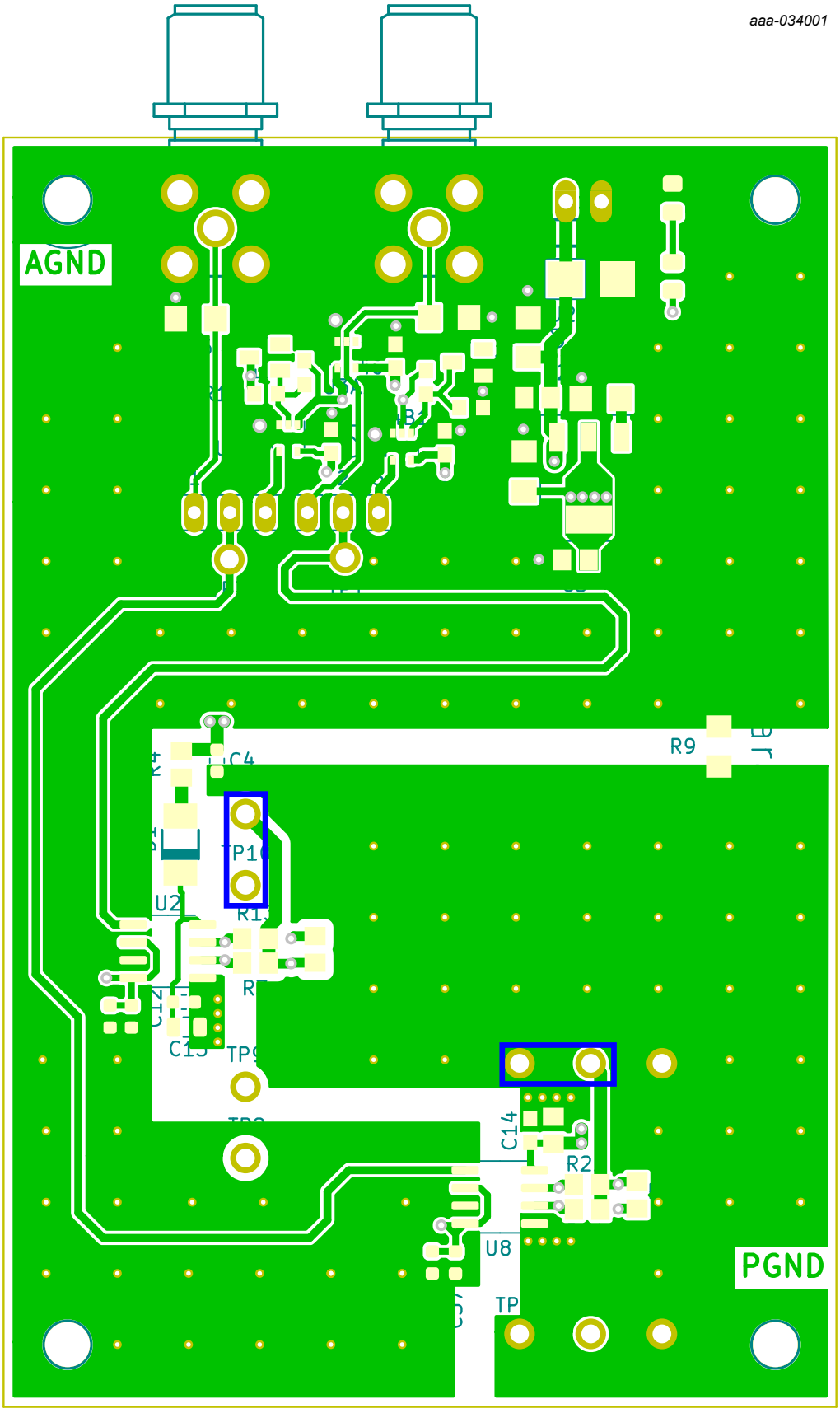

Fig. 27. Driver board - top layer

Note the top layer, (Fig. 27), uses symmetrical GaN FET Gate connections for one high-side and one low-side identified by the blue rectangles – the Gate connections for the associated paralleled GaN FET are routed on the Bottom Layer.

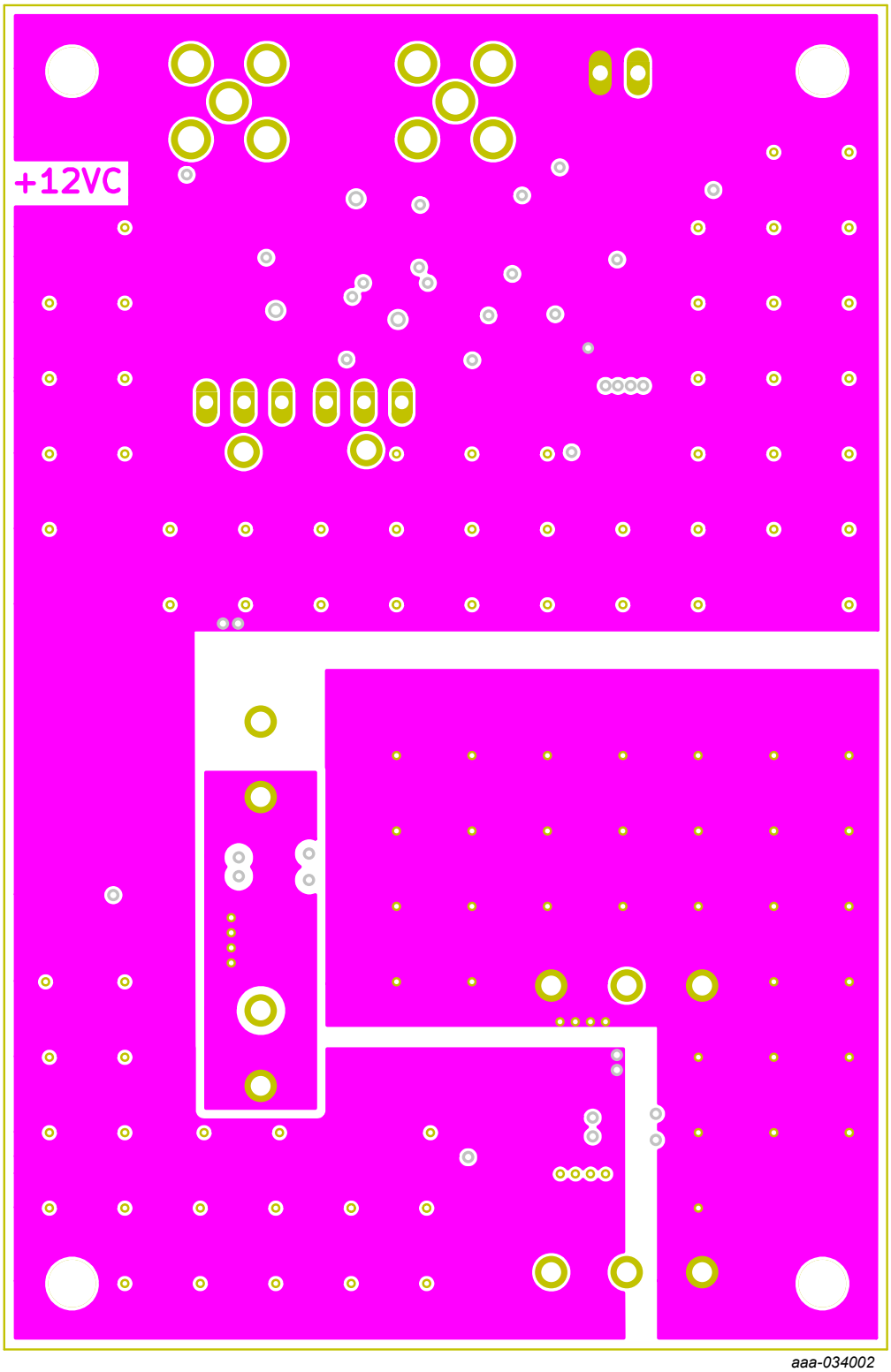

Fig. 28. Driver board - inner layer 1 – Switch Node, 12 V, Analogue Ground and Power Ground Planes

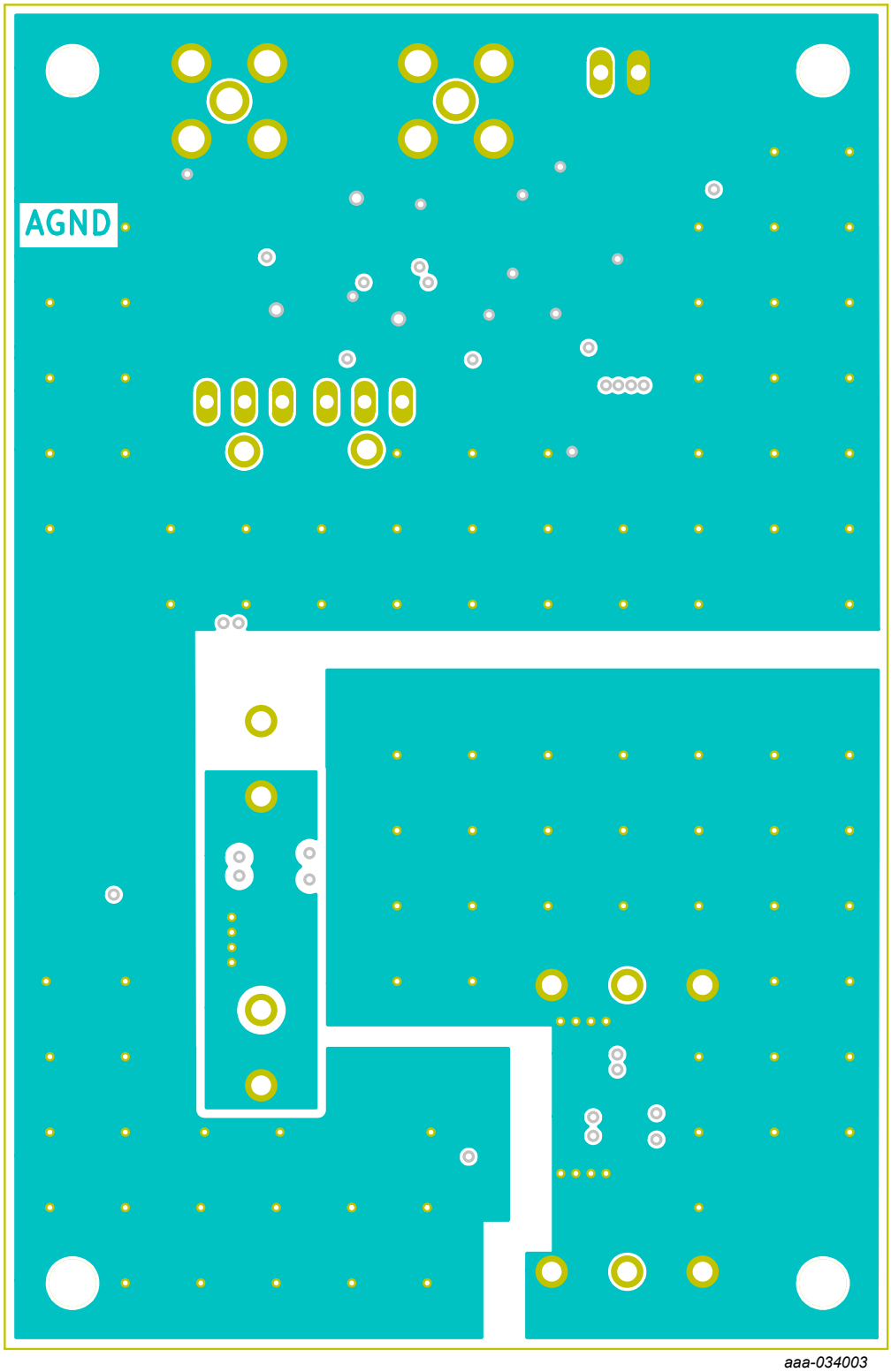

Fig. 29. Driver board - inner layer 2 – Switch Node, Analogue Ground and Power Ground Planes

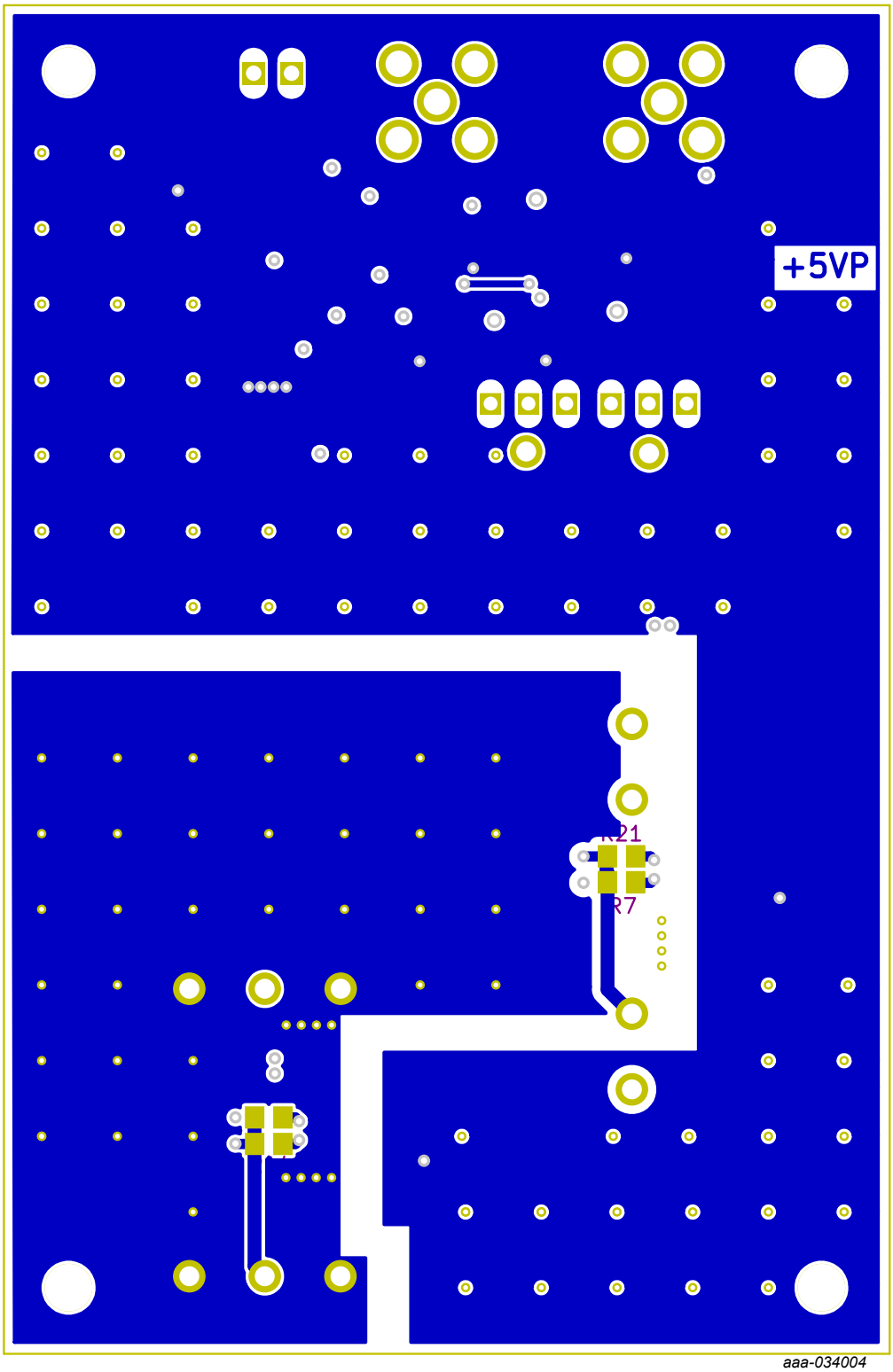

Fig. 30. Driver board - bottom layer

10.6. Driver board Bill of Materials

Table 2. Driver board Bill of Material

Part	Value	Voltage	Package	Description	Supplier	Supplier P/N
C1	22uF	35V	C1206	Capacitor, Ceramic	Farnell	2525173
C2	1uF	50V	C0805	Capacitor, Ceramic	Farnell	2094043
C3	2.2uF	50V	C0805	Capacitor, Ceramic	Farnell	2346931
C4	100nF	100V	C0603	Capacitor, Ceramic	Farnell	2749806
C10	100nF	100V	C0603	Capacitor, Ceramic	Farnell	2749806
C11	100nF	100V	C0603	Capacitor, Ceramic	Farnell	2749806
C12	100nF	100V	C0603	Capacitor, Ceramic	Farnell	2749806
C13	10uF	35V	C0805	Capacitor, Ceramic	Farnell	2547034
C14	100nF	100V	C0603	Capacitor, Ceramic	Farnell	2749806
C15	10uF	35V	C0805	Capacitor, Ceramic	Farnell	2547034
C19	100pF	100V	C0603	Capacitor, Ceramic C0G	Farnell	1740605
C20	100nF	100V	C0603	Capacitor, Ceramic	Farnell	2749806
C21	100nF	100V	C0603	Capacitor, Ceramic	Farnell	2749806
C22	100nF	100V	C0603	Capacitor, Ceramic	Farnell	2749806
C23	220pF	50V	C0603	Capacitor, Ceramic C0G	Farnell	498579
C37	100nF	100V	C0603	Capacitor, Ceramic	Farnell	2749806
C38	100nF	100V	C0603	Capacitor, Ceramic	Farnell	2749806
D1	ES1J	600V	DO-214AC	Diode	Farnell	3519291
D2	BAT54	30V	SOT23	Diode, Schottky	Nexperia	BAT54,215
D3	BAT54	30V	SOT23	Diode, Schottky	Nexperia	BAT54,215
D4	LED	-	D0805	LED, Green	Farnell	2610419
J1	22-23-2021		2.54mm	2-pin header	Farnell	1462926
J4	BU-SMA-G	-	BU-SMA-G	Female SMA Connector	Farnell	2112448
J6	BU-SMA-G	-	BU-SMA-G	Female SMA Connector	Farnell	2112448
JP1	-	-	2.54mm	3-pin header	Farnell	1248150
JP2	-	-	2.54mm	3-pin header	Farnell	1248150
R1	4.99k	-	R1206	Resistor	Farnell	1470015
R2	499k	-	R1206	Resistor	Farnell	1470019
R3	-	-	R0805	Resistor	-	-
R4	10R	-	R0805	Resistor	Farnell	2303326
R5	51R	-	R1206	Resistor	Farnell	1470021
R6	51R	-	R1206	Resistor	Farnell	1470021
R7	7R5	-	R0805	Resistor	Farnell	3235185
R8	2k	-	R0603	Resistor	Farnell	2059343
R9	0R	-	R1206	Resistor	Farnell	1469963
R10	3k3	-	R0603	Resistor	Farnell	2303173
R11	-	-	R0805	Resistor	-	-
R12	15R	-	R0805	Resistor	Farnell	1750730

R13	-	-	R0805	Resistor	-	-
R14	7R5	-	R0805	Resistor	Farnell	3235185
R15	0R	-	R0805	Resistor	Farnell	9233750
R16	0R	-	R0805	Resistor	Farnell	9233750
R21	15R	-	R0805	Resistor	Farnell	1750730
R22	-	-	R0805	Resistor	-	-
R23	1k	-	R0805	Resistor	Farnell	1469847
U1	LT3082	-	SOT223-3	Linear Regulator	Mouser	584-LT3 082EST #PBF
U2	Si8271BB-IS	-	SOIC8	HI/LO ISO Gate Driver	Farnell	2524443
U3A1	74LVC1G17GW	-	TSSOP-5	Schmitt Trigger Buffer	Nexperia	74LVC1G17GW
U4B1	74HCT1G86GW	-	TSSOP-5	2-input X-OR gate	Nexperia	74HCT1G86GW
U5B1	74HCT1G86GW	-	TSSOP-5	2-input X-OR gate	Nexperia	74HCT1G86GW
U8	Si8271BB-IS	-	SOIC8	HI/LO ISO Gate Driver	Farnell	2524443
				Shorting Link	RS	251-8503
				Shorting Link	RS	251-8503
				PCB	PCBWay	NX-HB7000EV Parallel TO-247 Driver Board Rev1.1

11. Summary

By using careful layout, short and impedance balanced gate drives, correctly placed DC Bus snubbers and decoupling, it is possible to achieve excellent current sharing in paralleled GaN FETs driving an inductive load. This has been effectively shown using leaded parts on a 4-layer FR4 PCB.

12. References

1. GAN041-650WSB data sheet.
2. Si8271 data sheet.
3. Nexperia application note AN90004.

13. Revision history

Table 3. Revision history

Revision number	Date	Description
2.0	2021-10-19	Minor changes to Section 2 and Section 4.
1.0	2021-09-21	Initial version.

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List of Tables

List of Figures

Contents

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