# AN90033

## Bidirectional multi-voltage level translator applications using Nexperia's LSF010x auto-sense devices

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**Document information**

| Information | Content |
|---|---|
| Keywords | LSF, Bidirectional multi-voltage level translation, Auto-sense |
| Abstract | This application note presents several methods of voltage level translation using parallel channels of pass transistor based voltage translators from LSF010x device family from Nexperia. |

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# 1. Introduction

This application note presents several methods of voltage level translation using parallel channels of pass transistor based voltage translators from LSF010x device family from Nexperia.

System level designers are confronted with increasing complexity of modern electronic systems in which lower power and logic voltage levels are used. This may lead to incompatibility between input and output levels if different interface voltage are required within a system. The level shifters can have different input/output (I/O) voltage levels on A and B port side which allows safe communication between various devices without damage from overvoltage or malfunction due to improper high-state levels at the higher voltage side.

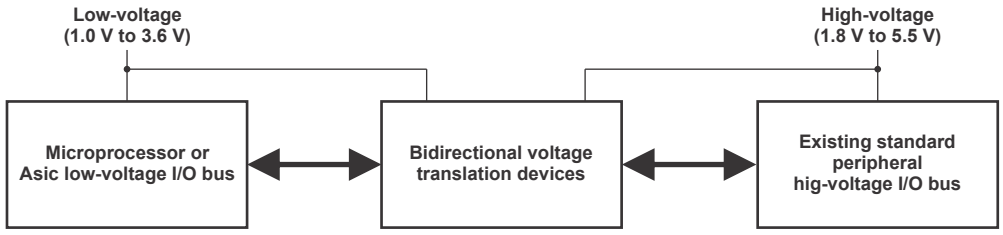



**Fig. 1. Typical application of the LSF family as voltage level translator**

The LSF010x devices are designed for logic levels as low as 0.95 V and as high as 5 V, enabling mixed low-to-high and high-to-low logic transitions. They support unidirectional as well as bidirectional level translation.

In terms of a signal path, LSF0101, LSF0102, LSF0104 and LSF0108 devices are functionally and electrically equivalent. The last number in the type name indicates the number of channels per device in addition to a so-called reference channel but it is used typically for a reference voltage for a correct biasing of LSF010x device. The reference channel is almost identical to the other data channels. An LSF010x device includes an array of matched pass transistors with their gates tied together internally at the EN pin.

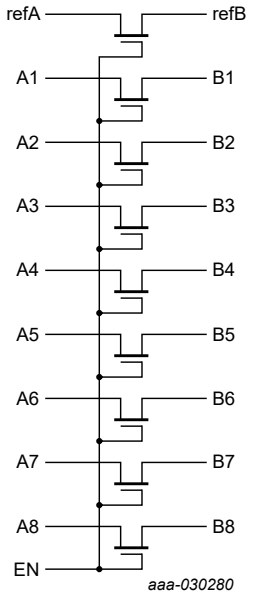



**Fig. 2. The LSF010x implements a pass transistor method of level translation**

The LSF010x device family uses internal pass transistor as switches and external pull-up resistors to translate between different voltage levels. In some specific conditions, pull-up resistors can be omitted. They are mandatory in systems with open-drain drivers. The pull-up resistors at both sides of a voltage translator IC assure that in the idle state the communication lines connected to the data ports A1, A2 to An and B1, B2 to Bn of a LSF010x device, are at the high state.

In contrast, the low state of the lines must be enforced by external drivers. The driver sink the current flowing from the supplies via pull-up resistors and the internal pass transistors to the drivers.

# 2. LSF operation

## 2.1. The reference channel

The internal structure of the LSF translator is shown in Fig. 3, as an example of an LSF0101 with one translating channel and the reference channel. The purpose of the reference channel is to control the gate voltages of all translation channel transistors in a way that both high level and low level translation is functioning even though the connected devices per channel might operate at different voltage levels. The pass transistor of a translation channel must be conducting in case of low level transmission and must be disconnecting in case of high level translation. The constant gate voltage must be configured to allow this behavior, therefore it must be high enough to enable conduction and it needs to be limited in order to enable transmission devices to drive the pass transistor into disconnection mode for high level translation.

The A-side of the reference channel is supplied by $V_{refA}$, whereas the Enable pin is recommended to be connected to the $V_{refB}$ pin via a 200 kΩ resistor, resulting in a voltage level of $V_{refA} + V_{TH}$ (~0.8 V) at the pin of $V_{refB}$ and at the gates of all pass transistors in the IC.

As a result, the gate voltage levels of all pass transistors is determined by $V_{refA}$. If the enable pin shall be controlled dynamically, the high voltage of the driver should not exceed $V_{refA} + V_{TH}$, otherwise the translation of a high level would fail.

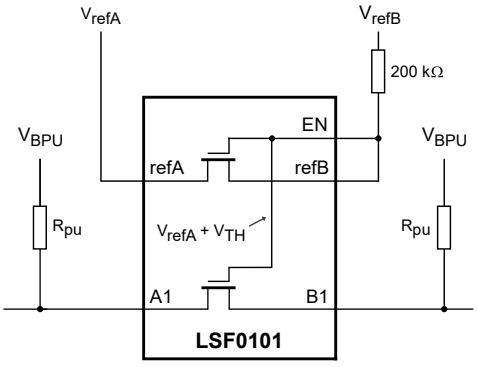



**Fig. 3. Configuration of the reference channel**

## 2.2. Basic operation principles

For the operation principles we consider the translation of both high and low level, as translation has to work properly in both directions. The low level is, naturally, not actually translated. It is pulled down by the Transmitter, causing the pass transistor to conduct and pull down the input of the receiver as well.

For the high level, the Transmitter is causing the pass transistor to disconnect. On the receiver side, the input level is generated by the pull-up of the receiver. Thus it is important that the pass transistor is properly disconnecting in case of a high level translation, and the reference channel is configured accordingly as described in the chapter above.

## 2.3. Translation scenarios for up- and down translation

The following scenarios for up- and down translation of voltage levels are describing various alternative configurations of voltages and directions of translation. The basic functional mechanisms of the LSF010x, valid for every translation scenario, are:

- If one side is driving a low level, the pass transistor is conducting and the level of the other side is pulled to low level.
- If one side is driving a high level and the other is in reception (high impedance) mode, the pass transistor is disconnecting and the pull-up at the receiver side is generating the high level for the receiver.

When either An or Bn port is driven LOW, the FET is turned ON and a low ohmic resistance connection exists between the An and Bn port.

In case of a high level transmission, the ohmic connection between participants is open and thus not connecting.

### Down translation

The scenario for a down translation is shown in Fig. 4. The device on the B-side is the driver, the device on the A-side is the receiver. Both devices have open-drain connections and external pull-up resistors and voltages are used.

### Transmitting a low level

When the B-side device is driving a low level, the input voltage at the pass transistor is pulled low and causes the pass transistor to conduct. Consequently, the voltage level at the receiver side is pulled down as well. Current is flowing through the pull-up resistors towards the driver side into the NMOS transistor of the driving device.

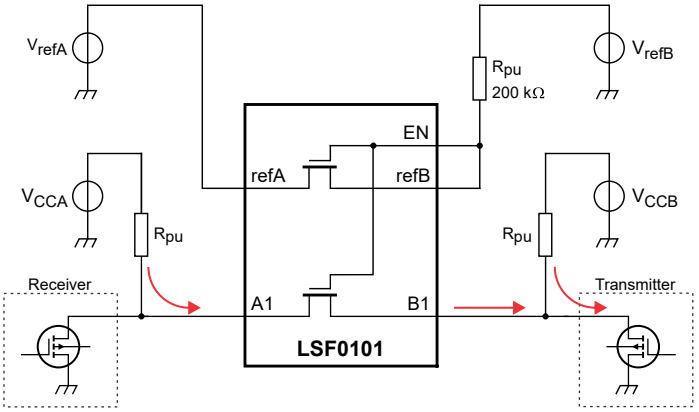



**Fig. 4. B-side is transmitting a low level**

### Transmitting a high level

The scenario for a high level translation is shown in Fig. 5. The driver on the B-side is operating it's open drain output in high impedance mode causing the voltage at the B-side to be pulled up via the pull-up resistor. The Gate voltage of the pass transistor is configured as $V_{refA} + V_{TH}$ and thus the pass transistor is disconnecting. The translated high level at the receiving A-side is generated by the A-side pull-up connection. There is no ohmic connection between the participants and the high level of the receiver is not directly driven by the B-side driver.

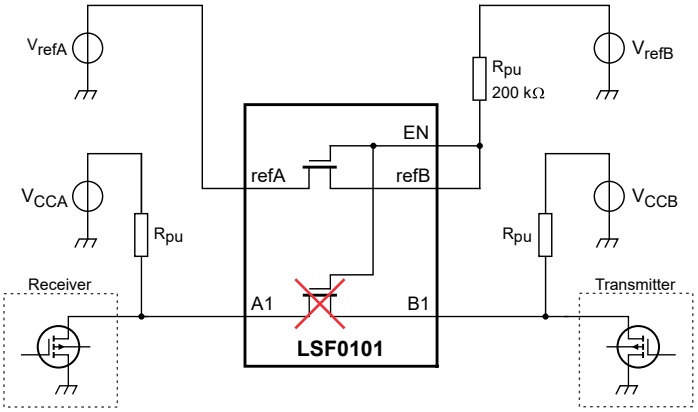



**Fig. 5. B-side is transmitting a high level**

## Up translation

In the scenario of up translation, the device supplied by the lower voltage, in our example the A-side, is the driver. As well as for the down translation scenario, we consider the low and high level translation scenarios separately.

## Transmitting a low level

As well as in the Down translation scenario, the driver is pulling down the input voltage at the pass transistor and causes the pass transistor to conduct. Consequently, the voltage level at the receiver side is pulled down as well. Current is flowing through the pull-up resistors towards the driver side into the NMOS transistor of the driving device, as illustrated in Fig. 6.

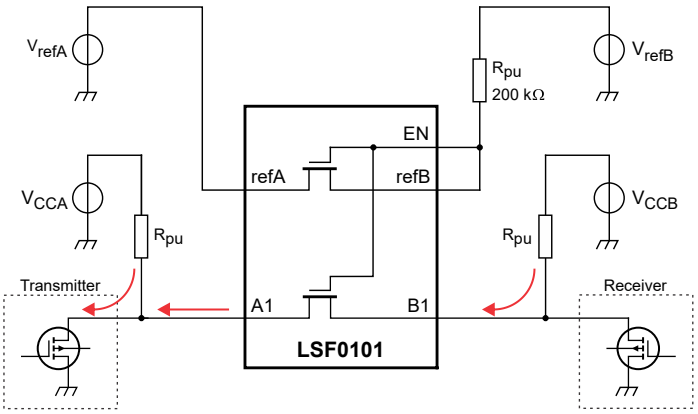



**Fig. 6. A side is transmitting a low level**

### Transmitting a high level

For the transmission of a high level, the A-side driver will disconnect it's NMOS and pull-up the voltage at the A-side, causing the pass transistor to disconnect. The voltage level at the receiver side will be pulled up by the pull-up circuit of the receiver, shown in Fig. 7.

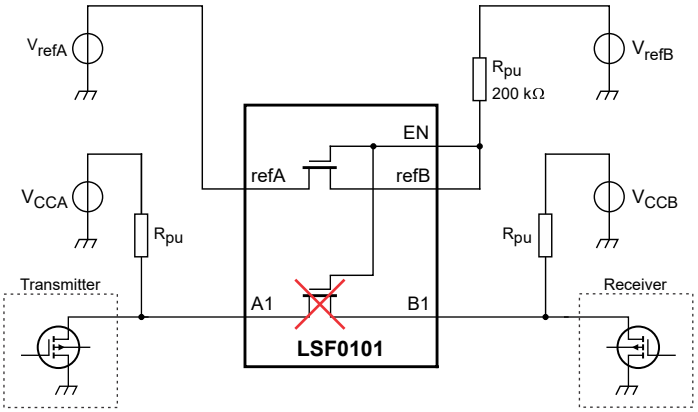



**Fig. 7. A-side is transmitting a high level**

# 3. Applications

## 3.1. Application with open-drain devices

The LSF translator is ideal for devices with open drain interface. The external pull-up supplies with associated resistors are generating the high voltage level on the receiver side. The value of the pull-up resistor has to be chosen low enough to achieve a fast enough charging of parasitic capacitors or rise time of the bus signal and on the other hand not to exceed the drive capabilities of the open drain stage for a proper low level. All scenarios considered in the chapters above are based on open drain interface devices.

## 3.2. Application with push-pull devices

It is possible to operate the signal channel with a push-pull interface, however some care needs to be taken:

1. If a push-pull device is in receive mode, it needs a pull-up circuit for generating the high input level because it is not driven by the sender via the pass transistor. This configuration is special because a pull-up is not needed by the push-pull interface to drive a high level
2. If the push-pull device is driving a high level and the device on the other side is driving a low level, the low level will be, as always, dominant. In comparison to the open-drain device with pull-up circuit, the high level drive of a push-pull is driven through the active PMOS with a relatively low $R_{DS(on)}$ (~50 Ω - 100 Ω), and therefore the current through the LSF and the low level driver will be quite high. As an example we can assume 50 Ω as resistance of the PMOS, 5 Ω ON-resistance of the LSF channel and another 50 Ω on resistance of the NMOS of the low level driver, thus in total 105 Ω. With a voltage of 3.3 V at the high level driver with push-pull interface, the current would be 31,4 mA just for one signal channel. This scenario should be prevented.
3. For certain protocols with fix data flow direction (i.e. UART or SPI), the conflict mentioned in 2. cannot occur and the LSF is a good solution.

### 3.3. Application with multiple devices with different voltages

The following example shows an application with a Microcontroller on the A-side and three Devices at the B-side. The voltage levels of the B-side devices are different, ranging from 1.2 V to 5 V. The Microcontroller is operating at 3.3 V. Fig. 8 shows the scenario. The communication is bidirectional for all 3 channels and there are pull-up circuits for all channels on both sides except for channel 2 on the B-side. The Device at channel 2 has 1.2 V supply voltage, the same as $V_{refA}$. As mentioned earlier, $V_{refA}$ must be the lowest voltage in the system in order to fulfill the condition for $V_{gate} = V_{refA} + V_{TH}$. When looking at the voltage level of the Channel 2, B-side in case of a high level driven by Device 2, the open input would not pull-up the voltage but the equation $V_{inputB} = V_{refA} + V_{TH}$ would be valid here as well and it would be sufficient to disconnect the pass transistor of channel 2. For the devices 1 and 2, the translation scenarios as described in the previous sections can be applied.

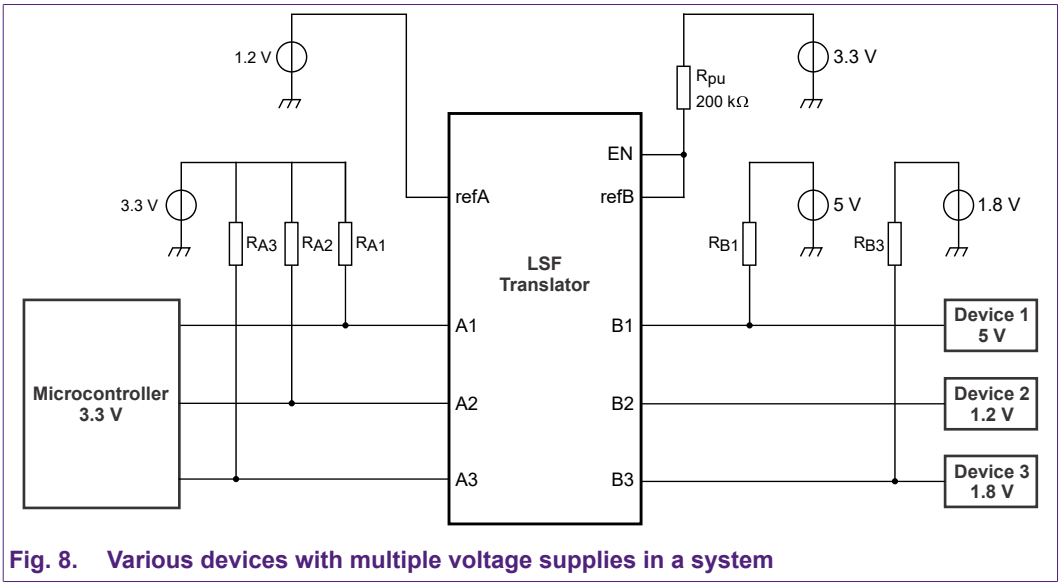



**Fig. 8. Various devices with multiple voltage supplies in a system**

## 4. Pull-up resistor calculation

As mentioned in the previous section, pull-up resistors and voltages are essential for the LSF translator functionality. There are two main influencing factors for the value of the pull-up resistors:

1. High speed of translation and fast rising edges would require a low ohmic pull-up resistor.
2. Low voltage levels and current limitation of connected devices can only be accomplished with higher ohmic resistance values.

The second criterion concludes to a calculation for the current flow in case of low level drive, as shown in Fig. 9, where the A-side is driving a low level, resulting in current flowing from the B-side via the pass transistor and additionally from the pull-up of the A-side. Connected devices have specified maximum low voltage levels ($V_{IL}$) and input current limits.

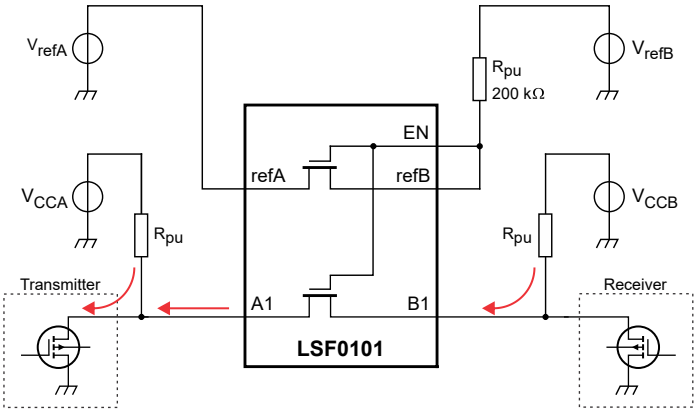



**Fig. 9. Current flow diagram for pull-up resistor calculation**

Based on specified values for the maximum $V_{IL}$ and maximum allowed I/O current of the connected devices, the equation for the current flowing into the NMOS of device A is:

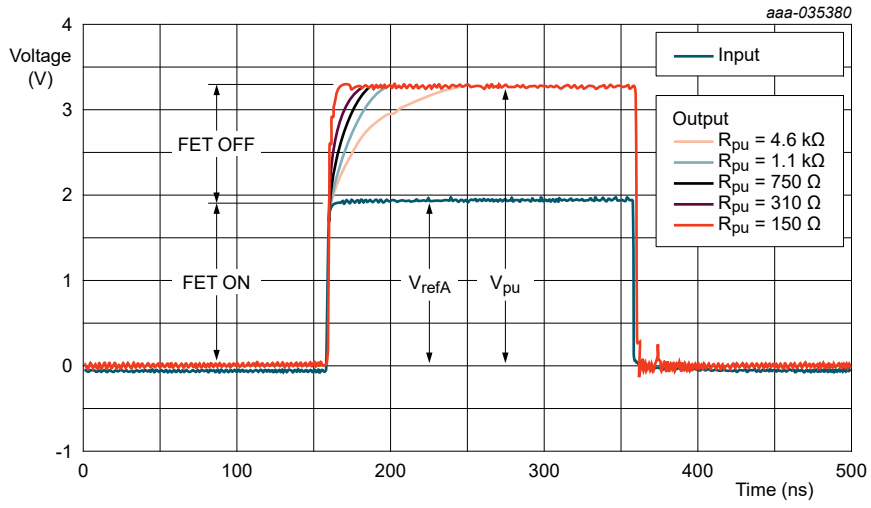
$$I_{D(A)} + I_{D(B)} = \frac{V_{CCB} - V_{IL}}{R_{PU(B)}} + \frac{V_{CCA} - V_{IL}}{R_{PU(A)}}$$

Assuming that the voltage drop in the pass transistor is neglectable and we use the same pull-up resistor values for both A-side and B-side, we can resolve the equation to $R_{PU}$:

$$R_{PU} = \frac{V_{refB} + V_{refA} - 2V_{IL}}{I_O}$$

$$R_{PU} = \frac{3.3\ V + 1.8\ V - (2 \times 0.2\ V)}{3\ mA} = 1.57\ k\Omega$$

The shape of the rising edge can be optimized by reducing the pull-up resistor value as much as allowed without conflicting with criterion 2 mentioned above. The results of various measurements with different resistor values are illustrated in Fig. 10.




As the pull-up resistor value is increased, the rise time of the output signal also increases.

**Fig. 10. The output waveforms with a capacitive load of 30 pF and different values of pull-up resistors**

# 5. Design for maximum frequency operation

The maximum frequency is dependent on translation voltages, the drive strength, the total node capacitance $C_{L(tot)}$ and the pull-up resistors $R_{PU}$ that are present on the bus.

The node capacitance is the sum of the PCB trace capacitance and the capacitance of the devices that are connected to the bus. Because of the dependency of the external components, PCB layout and the different device operating states the calculation of rise and fall times is complex and has several inflection points along the curve.

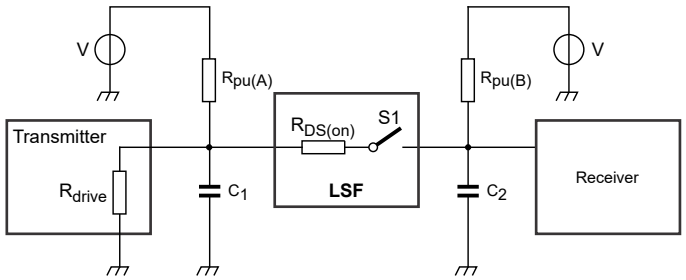



**Fig. 11. Basic diagram for an I²C circuit with transmitter, receiver and pull-up circuitry**

The frequency is mainly determined by the various RC low passes as shown in Fig. 11. There are two main cases to be considered:

1. The open-drain transmitting device is in ON-state and the LSF device turned on with a low-impedance path to the Receiver
2. The transmitting device switches to OFF-state (high-level) and the Receiver is also in OFF-state (high-level). The LSF device is initially on, the parasitic bus-capacitances (C1, C2) are charged up via the pull-up resistors. The A-side from the B-side are disconnected as soon as the port voltage VA is reaching its high-level state. The port voltage $V_B$ will reach its high level shortly delayed compared to $V_A$ due to the higher voltage level to be reached.

There are some basic guidelines to follow that will help maximize the performance of the device:

- Reduce the trace length by placing the LSF device close to the receiver.
- The signal round trip time on trace should be shorter than the rise or fall time of a signal to reduce reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher drive strength controlled by the pull-up resistor (up to 15 mA), the higher the frequency the device can use.

Fig. 12 shows the input (A1) and output (B1) voltages of LSF device translating from 1.2 V to 1.8 V with parasitic capacitances (C1 and C2 in Fig. 11) of 80 pF at each side. Pull-up resistors are 1.2 kΩ each.

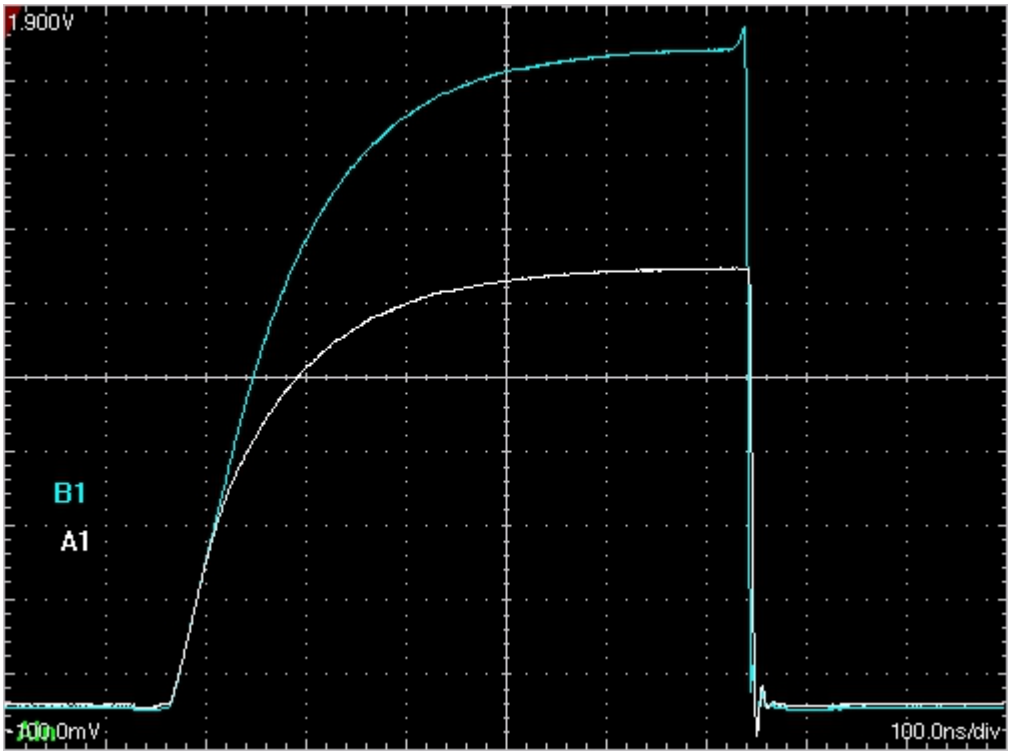



**Fig. 12. Input and output signal of an LSF translation**

The system designer must choose the pull-up resistor(s) values based on the external current drive strength and limit the node capacitance (minimize the wire, stub, connector and trace length) to get the desired operation frequency.

The minimum value of the output pull-up resistor is restricted by the maximum current-sinking capability ($I_{OL(max)}$) of the driver, whereas the maximum value is limited by maximum allowable rise time of the output signal.

# 6. Supply voltage of the reference channels

The reference channel supply voltages are controlling the Gate voltage of the pass transistor of each channel. This was explained in the operation chapter of this document. As mentioned, the voltage sources of the reference channel are assumed to be ideal in terms of internal resistance, which must not be high ohmic and must be able to sink the very small current flowing through the pass transistor. In real applications, supply voltages can also be generated by voltage converters such as buck converters or LDO's. These converters, in particular the LDO, have a limited capability to sink current in case the generated voltage is lower than the voltage at the connected output node and this might lead to an increased voltage level of the lower reference voltage. The scenario is shown in Fig. 13. We consider the two reference voltage sources $V_{refA}$ and $V_{refB}$, with a 200 kΩ resistor in the path to create the dependency of $V_{gate}$ from $V_{refA}$ is also shown in the figure. As the path transistor in the reference channel is conducting, we have an ohmic connection between the two voltage sources, causing a current flow from $V_{refB}$ towards $V_{refA}$.

The current can be estimated to:

$$\frac{V_{refB} - V_{refA} - V_{TH}}{R_{pu}} = \frac{3.3\,V - 1.8\,V - 0.5\,V}{200\,k\Omega} = 5\ \mu A$$

If $V_{refA}$ cannot sink the current, the voltage at $V_{refA}$ can be pulled up to higher a voltage level. A possible mitigation measure is to add a high ohmic pull-down resistor at pin $V_{refA}$. It's value can be calculated by dividing the desired voltage at $V_{refA}$ over the sink current:

$$\frac{1.8\,V}{5\ \mu A} = 360\ k\Omega$$

In Fig. 13, a smaller value of 330 kΩ is used which would compensate possible reductions of $V_{TH}$ in case of temperature increase, associated with increased current.

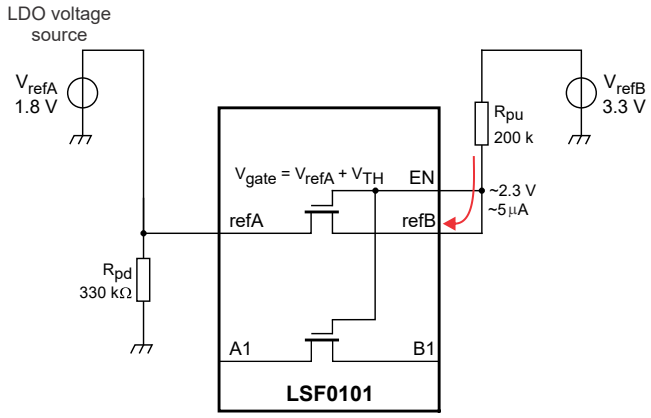



**Fig. 13. Current flow through $V_{ref}$ channel**

# 7. Revision history

**Table 1. Revision history**

| Revision number | Date | Description |
|---|---|---|
| 1.0 | 20220831 | AN90033 |

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