AN90034

Nexperia Precision Electrothermal models in SPICE and VHDL-AMS for Power MOSFETs

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Document information

Information	Content
Keywords	Electrothermal, SPICE, VHDL-AMS, simulation, model
Abstract	This application note introduces Nexperia electrothermal MOSFET models. Details are provided on how to use them in simulations. Simulation results for key MOSFET characteristics are included.

1. Introduction

Nexperia provides MOSFET electrothermal models that link the electrical and thermal performance. The models are available in SPICE and VHDL-AMS for multiple simulation platform support. They represent all the key MOSFET behaviours relevant to MOSFET applications. As such it is possible to estimate device performance quickly and accurately within widely available simulation tools before any physical prototyping. By using the latest MOSFET models errors can be spotted and designs can be optimised for cost and performance much earlier in the design cycle and changes can be implemented timelier, thus improving time to market. This application note introduces the models, how to use them, what their capabilities and limitations are, and where to find them.

The models will be available in “families” of devices – that is one model file will contain all the products of a given technology and voltage rating. For example, the Trench9 40 V Standard Level Automotive portfolio is one such model family. Importing the model file to your simulation tool should give access to all the device models i.e., each R_{DSon} value in each package type within that family. The simulation tool used will vary how this works e.g., LTspice™ or PSpice.

2. Importing models in LTspice™

Download the electrothermal model ZIP file from Nexperia.com, e.g. BUK7xxxx-40H_LTspice. The ZIP file contains the library file and symbol. The model can be viewed in a text editor, here the product models included can be seen in Fig. 1.

First place the provided symbol on the schematic, the easiest way is to have the symbol in the same directory as the schematic and then it is accessible via the component library and by changing the Top Directory to the local directory, see Fig. 2.

The easiest way is to link the symbol to the full library is to use the “.inc” command and point to the file. If the file is saved in the same location as the simulation, then only filename is needed, otherwise, the full file path is required. Finally change the value “NMOS_5Pin” to any of the models listed library file, for example “BUK7S1R0-40H”, see Fig. 3.

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**********************************************
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*5-pin Electrothermal models included:
*BUK7J1R0-40H    BUK7J1R4-40H    BUK7M11-40H
*BUK7M15-40H     BUK7M20-40H     BUK7M3R3-40H
*BUK7M4R3-40H    BUK7M5R0-40H    BUK7M6R0-40H
*BUK7M6R7-40H    BUK7M8R5-40H    BUK7M9R5-40H
*BUK7S0R5-40H    BUK7S0R7-40H    BUK7S0R9-40H
*BUK7S1R0-40H    BUK7S1R2-40H    BUK7S1R5-40H
*BUK7S2R0-40H    BUK7S2R5-40H    BUK7Y1R7-40H
*BUK7Y2R0-40H    BUK7Y2R5-40H    BUK7Y3R0-40H
*BUK7Y3R5-40H    BUK7Y7R2-40H
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Fig. 1. LTspice™ library file showing devices modelled within

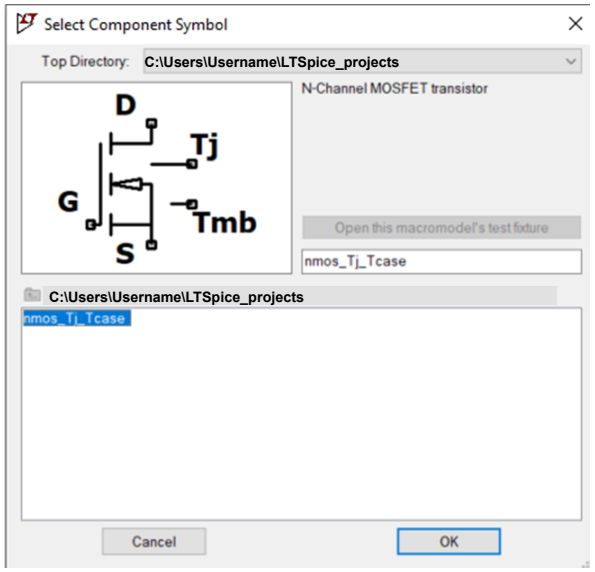


Fig. 2. Adding the symbol to a schematic

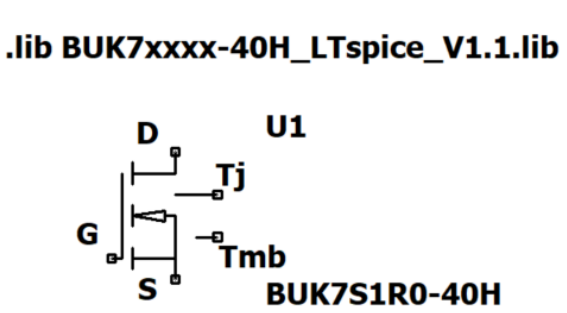


Fig. 3. Pointing a symbol to the model file

3. Using Models in Part Quest Explore

The models are also available in VHLD-AMS format which is supported by PartQuest™ Explore (https://explore.partquest.com). Here, the models are available within the partner library and are ready to be used with no additional set-up.

Further examples of models and simulations using PartQuest™ Explore can be found on Nexperia's Interactive Application Notes (https://www.nexperia.com/applications/interactive-app-notes).

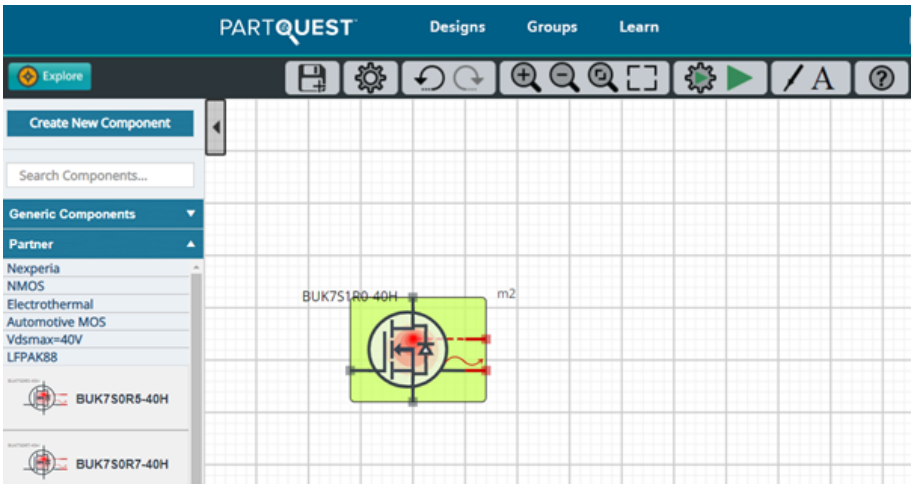


Fig. 4. Nexperia's new Precision Electrothermal models found in the partner library within PartQuest™ Explore

4. 5 pin MOSFET model

The electrothermal models have 5 pins, the 3 traditional electrical pins for Gate, Drain, and Source and two additional pins for interacting with the thermal properties of the MOSFET, see Fig. 5. These are namely the junction temperature pin, Tj and the mounting-base pin, Tmb. Tj can be probed like a voltage node and gives the junction temperature (1 V is equivalent to 1 °C). In addition, this pin can be connected to a fixed voltage source to set the junction temperature as a constant, this disables the self-heating behaviour of the model, Fig 5 a). Otherwise, it can be left open and monitored.

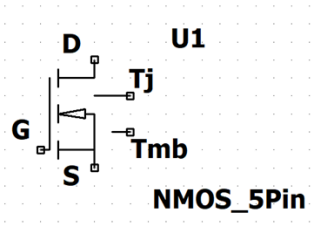
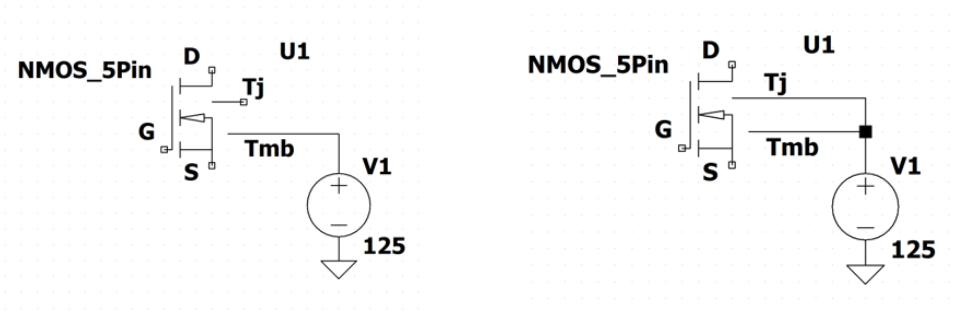


Fig. 5. Schematic symbol of the 5-pin electrothermal MOSFET model

Tmb represents the thermal connection of the device to the outside world e.g., the heat path from the mounting base of the MOSFET to a PCB or heatsink. This pin can also be connected to a fixed voltage source, this will set the ambient temperature, Fig 5 b). In addition, thermal models of PCBs can be connected to the MOSFET Tmb pin model to simulate the system thermal performance, Fig. 7.



a. setting an ambient temperature

b. fixing the junction temperature to a constant

Fig. 6. Interacting with the thermal pins

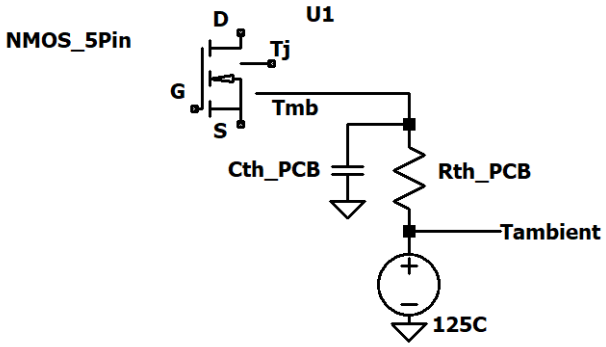


Fig. 7. Adding an external thermal network

5. Model behaviour

The following characteristics may be modelled using the 5 pin electrothermal MOSFET model:

- Gate-source threshold voltage (V_{GSth}) as a function of junction temperature (T_j)
- R_{DSon} as a function of V_{GS} and temperature
- Output characteristics (I_D as a function of V_D) vs temperature
- Transfer characteristics (I_D as a function of V_{GS}) vs temperature
- Diode forward characteristics (V_{SDS}) as a function of temperature
- Drain source leakage (I_{DSS}) as a function of temperature
- Breakdown voltage (BV_{DSS}) as a function of temperature
- Internal capacitances as a function of drain-source voltage
- Diode reverse recovery
- Package related parameters

Where possible an example circuit is shown to demonstrate each behaviour. For each of the following examples the Tj pin will be shorted to Tmb, turning off the self-heating.

Note: the characteristics are always typical values and do not represent the limits of process variation.

The device used in the simulations is BUK7S1R0-40H a 40 V, 1 mΩ power MOSFET in the LFPAK88 package. It is from the Trench9 40 V Standard Level Automotive portfolio.

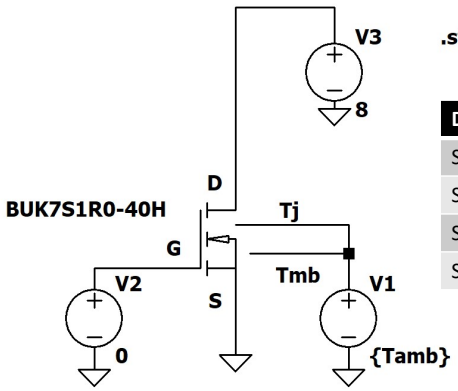
BUK7S1R0-40H

N-channel 40 V, 1.0 mΩ standard level MOSFET in LFPAK88

AUTOMOTIVE QUALIFIED ELECTROTHERMAL MODEL

5.1. Threshold voltage, I_D / V_{GS} sweep

The I_D / V_{GS} sweep fixes the V_{DS} and sweeps the V_{GS}, turning the MOSFET on, the resultant drain current (I_D) is probed. Set-up of the I_D / V_{GS} sweep is shown in Fig. 8 which also shows the ambient temperature is stepped.

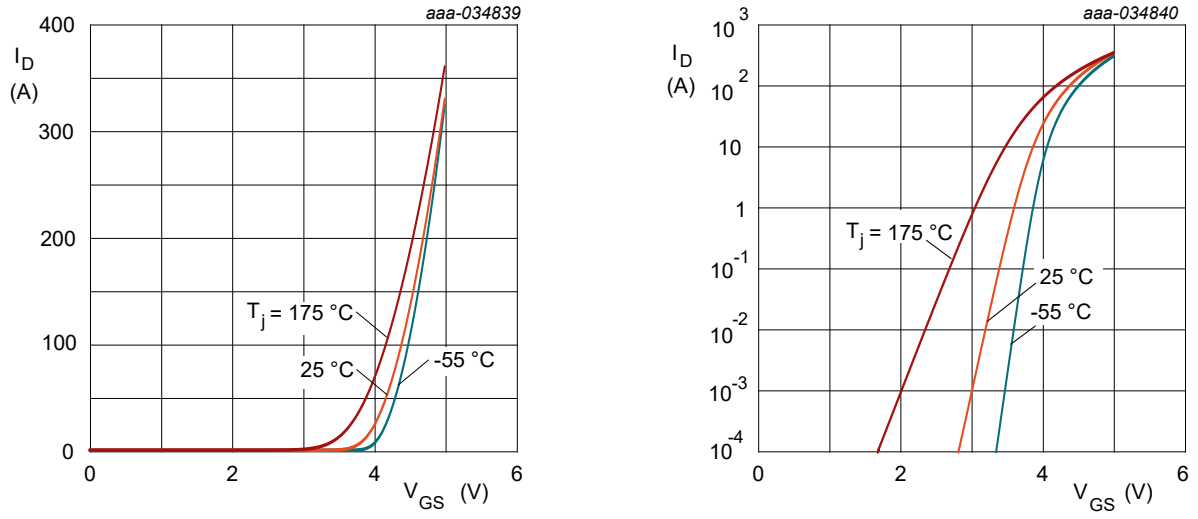


.step param Tamb list -55 25 175

DC sweep	Value	Unit
Source	V2	-
Start	0	V
Stop	5.5	V
Step	0.1	V

Fig. 8. I_D / V_{GS} schematic and simulation parameters

The waveforms in Fig. 9 shows two operating regimes, the sub-threshold slope and the transfer characteristic.



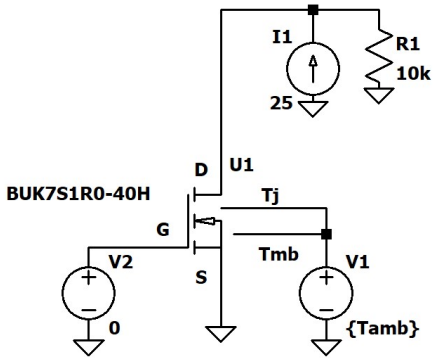
a. linear scale

b. log scale

Fig. 9. Drain current as a function of gate-source voltage; simulation results

5.2. R_{DSon}

R_{DSon} is measured with a fixed current source typically 25 A but may be less for smaller die. The V_{GS} is stepped in the same manner as I_D vs V_{GS}. The simulation set-up is in Fig. 10. Fig. 11 shows the R_{DSon} vs V_{GS}, this can be derived by dividing the drain-source voltage (V_{DS}) by the I_D.



.step param Tamb list -55 25 175

DC sweep	Value	Unit
Source	V2	-
Start	0	V
Stop	20	V
Step	0.1	V

Fig. 10. R_{DSon} schematic and simulation parameters

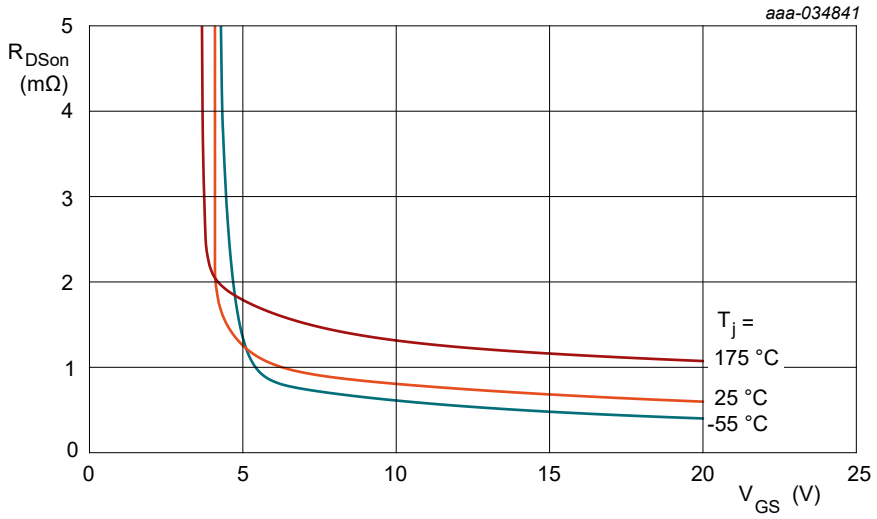
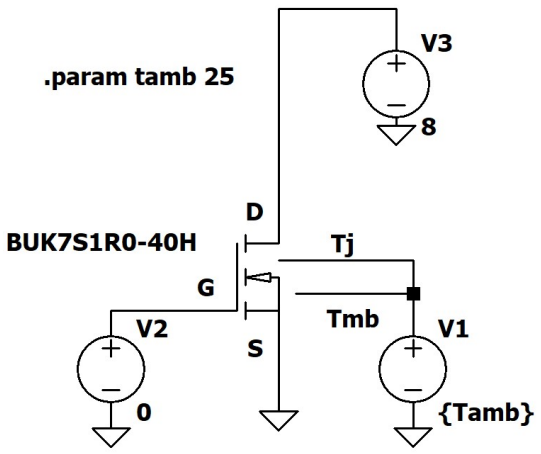


Fig. 11. R_{DSon} as a function of V_{GS}; simulation results

5.3. Output characteristics (I_D / V_{DS})

Here V_{GS} is held constant and V_{DS} is stepped. This is repeated for different V_{GS} values. The I_D is probed. The schematic set-up is shown in Fig. 12 and resultant waveforms are shown in Fig. 13.



DC sweep 1	Value	Unit
Source	V3	-
Start	0	V
Stop	2	V
Step	0.01	V

DC sweep 2	Value	Unit
Source	V2	-
list	-	-
1st value	4.0	V
2nd value	4.5	V
3rd value	5.0	V
4th value	10	V

Fig. 12. I_D / V_D schematic and simulation parameters

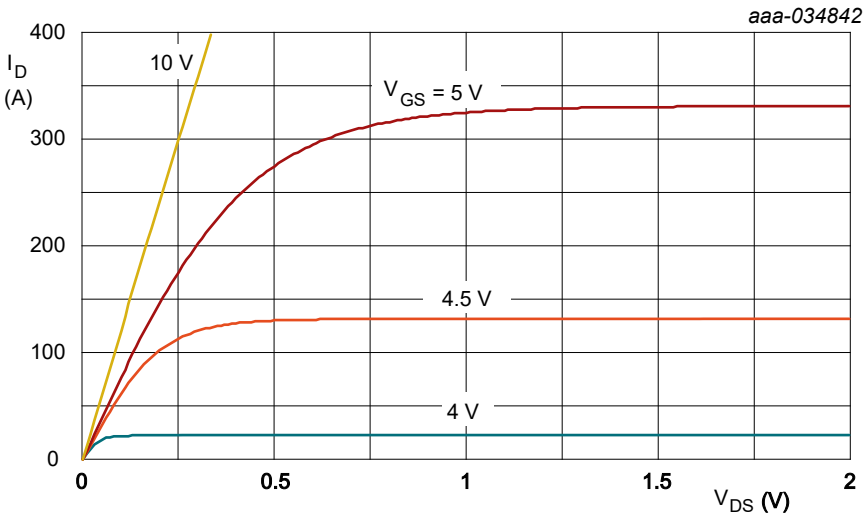
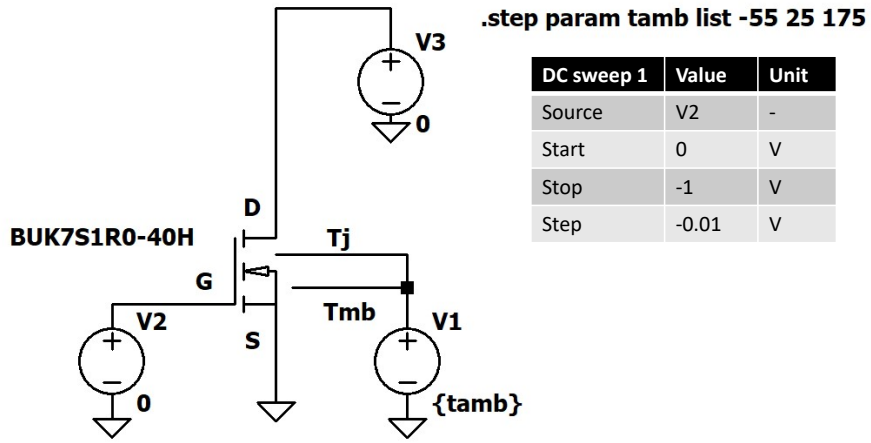


Fig. 13. I_D as a function of V_{DS}; simulation results

5.4. Diode characteristics (V_{SDS})

MOSFETs have an anti-parallel diode within the structure, as such it conducts when the source-drain voltage (V_{SD}) reaches the forward voltage drop (V_F) of the diode. This is also temperature dependent; the diode's V_F decreases with temperature and its slope resistance increases. Fig. 14 shows the test set-up and Fig. 15 shows the simulated charts.



DC sweep 1	Value	Unit
Source	V2	-
Start	0	V
Stop	-1	V
Step	-0.01	V

Fig. 14. V_{SDS} diode forward schematic and simulation parameters

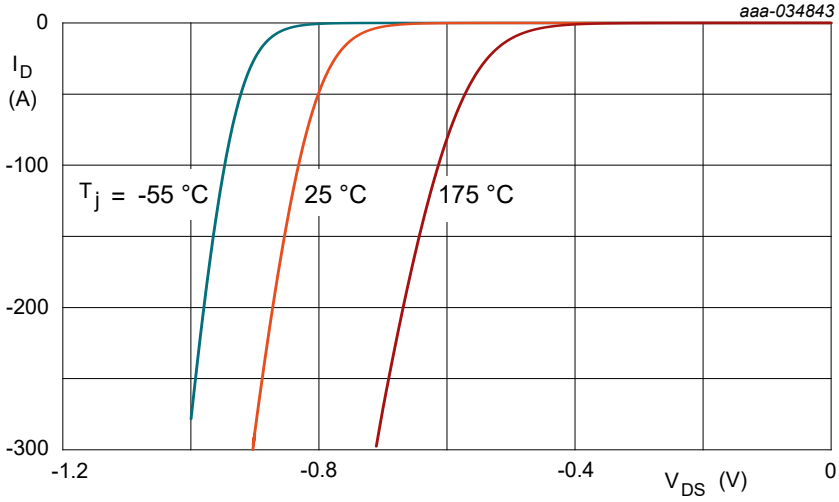


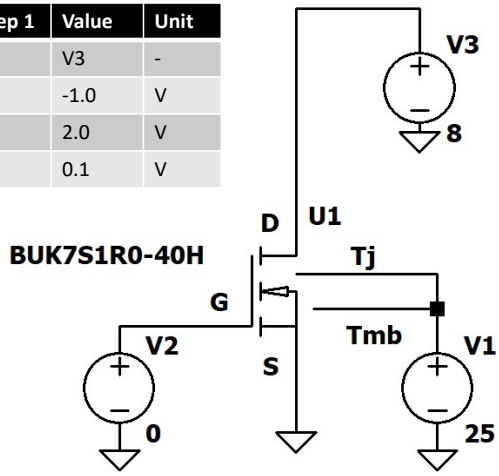
Fig. 15. Diode V_F simulation results

5.5. Body Effect

In many half-bridge applications, the MOSFET may replace the free-wheeling diode to achieve synchronous rectification. The MOSFET's R_{DSon} produces a lower voltage drop Drain to Source than the diode's V_F so power loss is reduced making the application more efficient. However, MOSFETs conducting current through the channel in reverse, such as in synchronous rectification, will have lower threshold voltage. This is known as the Body Effect and is accounted for in the models operating with negative V_{DS} and I_D. The Body Effect is also sometimes referred to as third quadrant operation.

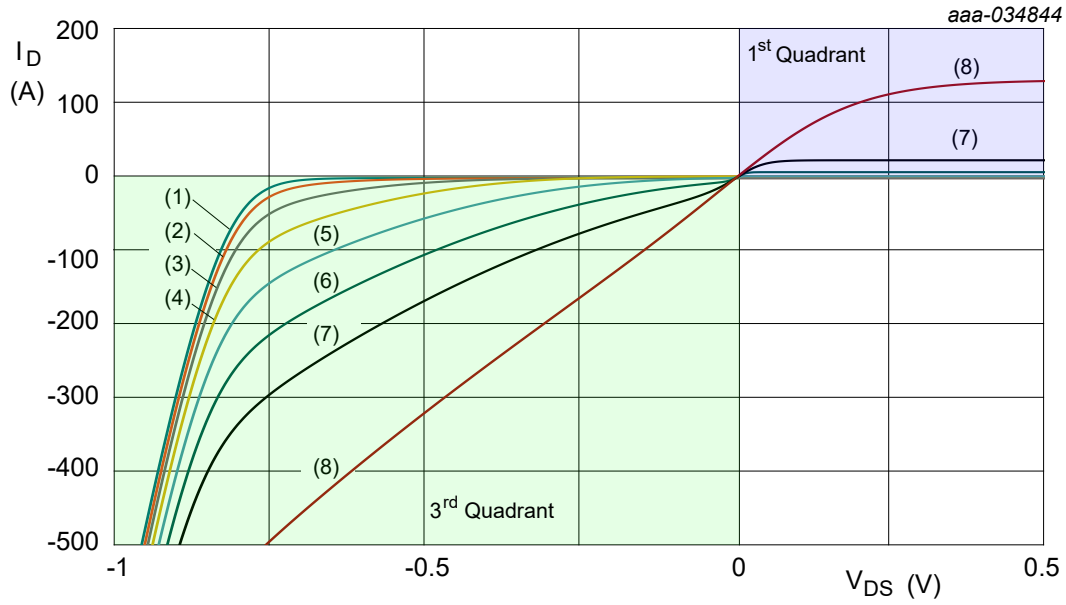
Fig. 16 shows the simulation set-up for observing the Body Effect and Fig. 17 shows both the first and third quadrant of operation. The first quadrant is I_D / V_D as previously shown and in the third quadrant when the V_{GS} = 0 is the diode curve. However, Fig. 17 also shows operating in the third quadrant with a positive V_{GS} and the increased I_D due to the Body Effect.

DC sweep 1	Value	Unit
Source	V3	-
Start	-1.0	V
Stop	2.0	V
Step	0.1	V



DC sweep 2	Value	Unit
Source	V2	-
list	-	-
1st value	0	V
2nd value	3.0	V
3rd value	3.2	V
4th value	3.4	V
5th value	3.6	V
6th value	3.8	V
7th value	4	V
8th value	10	V

Fig. 16. Body Effect schematic and simulation parameters

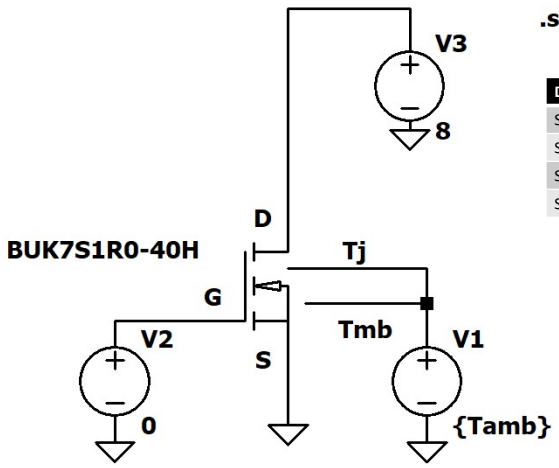


(1) V_{GS} = 0 V (V_{SDS}) (2) V_{GS} = 3.0 V (3) V_{GS} = 3.2 V (4) V_{GS} = 3.4 V
(5) V_{GS} = 3.6 V (6) V_{GS} = 3.8 V (7) V_{GS} = 4.0 V (8) V_{GS} = 10 V

Fig. 17. Full quadrant operation of a MOSFET showing I_D / V_D, V_{SDS} and the Body Effect; simulation results

5.6. Drain leakage (I_{DSS}), breakdown voltage (BV_{DSS}) and avalanche breakdown

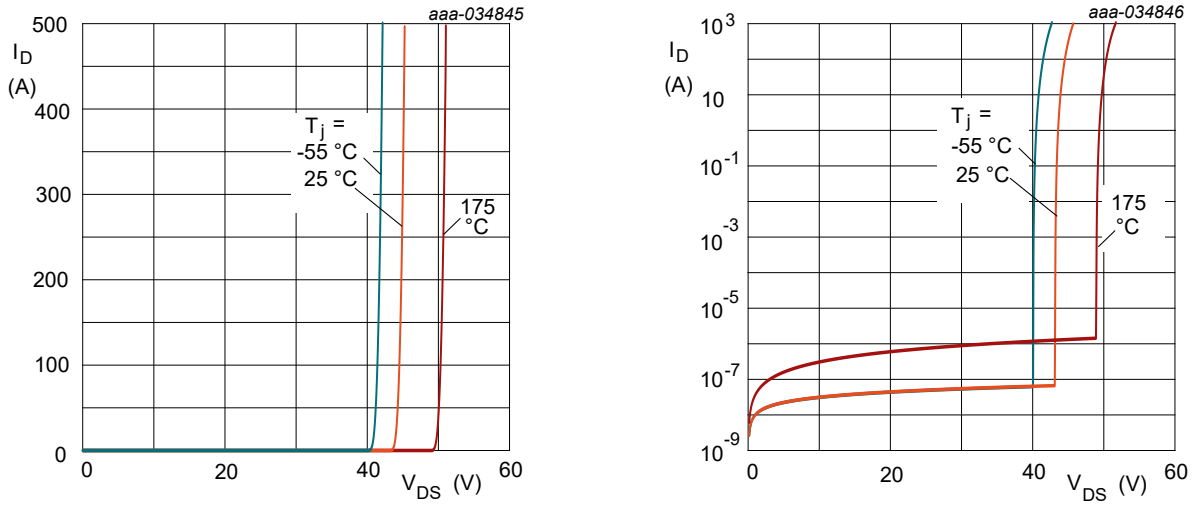
Included in the model are temperature dependant drain leakage current and breakdown voltage. In addition, the slope resistance of avalanche breakdown is modelled. Fig. 18 is the simulation set up and Fig. 19 shows the simulation results.



.step param Tamb list -55 25 175

DC sweep 1	Value	Unit
Source	V3	-
Start	0	V
Stop	55	V
Step	0.05	V

Fig. 18. I_{DSS}, BV_{DSS} and avalanche breakdown schematic and simulation parameters



a. linear scale

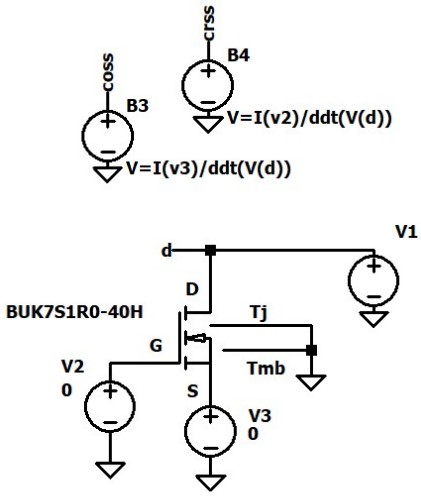
b. log scale

Fig. 19. Avalanche breakdown; I_D as a function of V_{DS} simulation results

5.7. Capacitances and gate charge

Capacitances

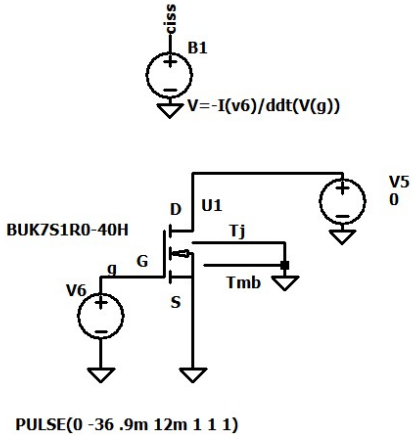
The MOSFET's internal parasitic capacitances and their voltage dependence is modelled. This is critical for accurate switching time simulations and gate charge modelling. The capacitance values have insignificant temperature dependence so in the model they are fixed with respect to temperature. The gate charge does have some temperature dependence; the Miller plateau voltage is dependent on the gain of the MOSFET which in turn is temperature dependant. To simulate the capacitance values, refer to Fig. 20 and Fig. 21 and the resultant waveforms in Fig. 22.



V1 - Pulse	Value	Unit
off	0	V
on	36	V
delay	0.99m	s
Rise time	12m	s
Fall time	1	s
On time	1	s
Period	1	s

Transient	Value	Unit
Stop time	12m	s
Time to start saving data	1m	s

Fig. 20. C_{oss} and C_{rss} schematic and simulation parameters



V6 - Pulse	Value	Unit
off	0	V
on	-36	V
delay	0.99m	s
Rise time	12m	s
Fall time	1	s
On time	1	s
Period	1	s

Transient	Value	Unit
Stop time	12m	s
Time to start saving data	1m	s

Fig. 21. C_{iss} schematic and simulation parameters

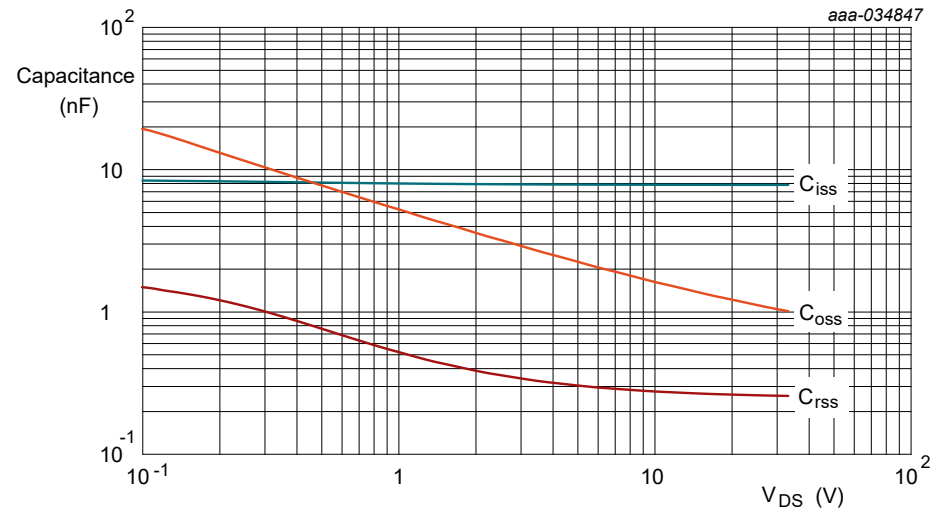
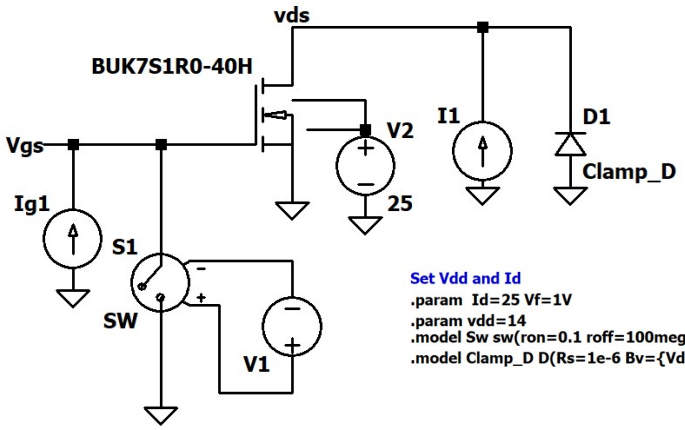


Fig. 22. Capacitances as a function of V_{DS}; simulation results

Gate charge

Fig. 23 shows the gate charge set-up and by probing the Vgs node one can see the Vgs charging with respect to time. To determine the gate charge, use the relationship in Equation (1), the gate current I_G is determined by the settings of Ig1 in the schematic set-up. The result of this is shown in Fig. 24.

$$Q = I_G \cdot t \tag{1}$$



Transient	Value	Unit
Stop time	120u	s
Time to start saving data	10u	s

V1 - Pulse	Value	Unit
off	5	V
on	0	V
delay	10u	s
Rise time	1n	s
Fall time	1n	s
On time	10	s
Period	100	s

I1 - Pulse	Value	Unit
off	0	A
on	25	A
delay	0	s
Rise time	1m	s
Fall time	1m	s
On time	1	s
Period	1	s

Ig1 - Pulse	Value	Unit
off	0	A
on	1m	A
delay	10u	s
Rise time	1n	s
Fall time	1n	s
On time	1m	s
Period	2m	s

Fig. 23. Gate charge schematic and simulation parameters

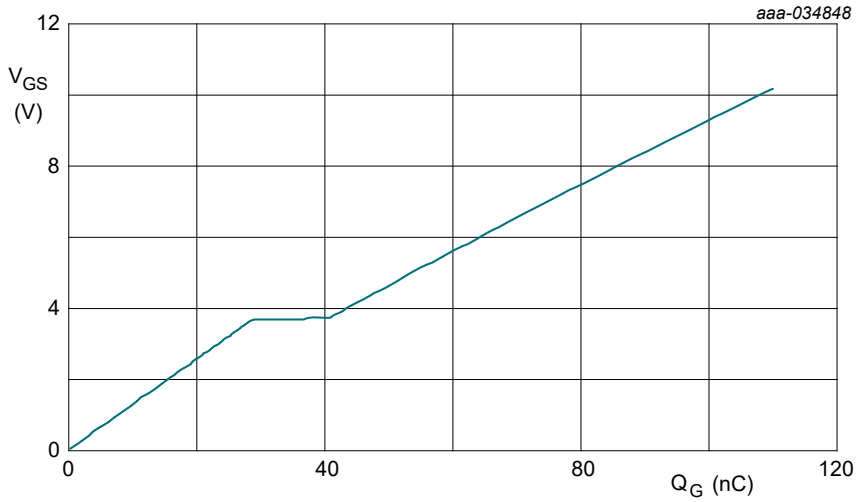


Fig. 24. Gate charge simulation results

5.8. Body diode reverse recovery charge (Q_{RR})

Q_{RR} is not solely dependent on the MOSFET but on the test circuit too. Specifically, the stray inductances of the PCB are critical in determining the Q_{RR} behaviour. As such it is difficult to represent the Q_{RR} in a simulation with a great accuracy without knowing or characterising the test bench being compared to the simulation. In addition, there are two standard methods of measuring Q_{RR} that will again yield different results. The preferred method for testing Q_{RR} is the double pulse method which more closely aligns with application uses cases, for example half-bridge topologies such as DC-to-DC convertors and motor drives.

Further information about simulating the Q_{RR} in a double pulse set-up is detailed in Nexperia application note AN90011. Further to this our paper SPICE models for predicting EMC performance of a MOSFET based half-bridge configuration details how to use the new models and double pulse simulations to predict Electromagnetic interference (EMI) behaviour before any physical testing, helping to mitigate errors sooner in the design cycle saving time and cost.

Fig. 25 shows an example Q_{RR} waveform.

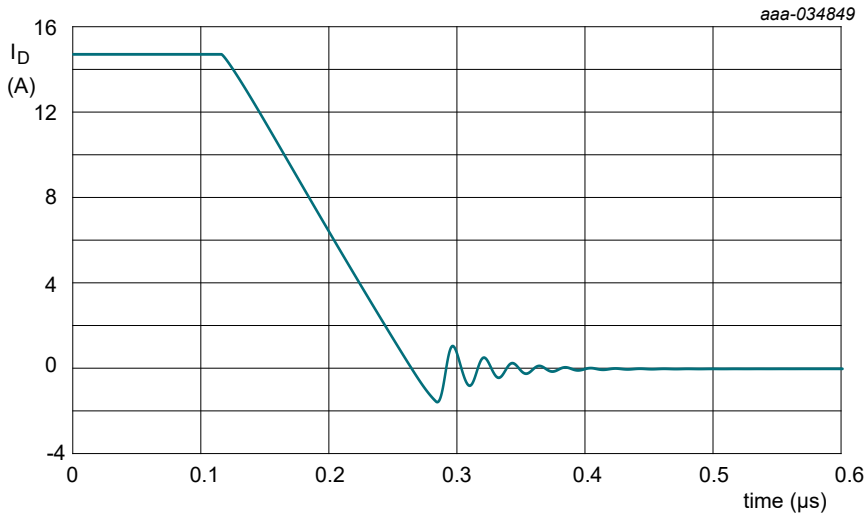


Fig. 25. Diode reverse recovery (Q_{RR}) simulation results

5.9. Package related parameters

Impedances due to the packaging are modelled, these include resistances associated with the clip and lead frame and solder interconnects etc. The package resistance also changes with temperature. Further to this the parasitic inductance is included in the model. This is critical for simulating for EMI investigations.

6. Comparing models to data sheet

Nexperia electrothermal models are based on a scalable model that takes a trend line across the parameters and die sizes in each portfolio. This means the model represents the mean device, but the data sheet represents a typical device that may not necessarily be the mean. So, whilst the model may not match the data sheet exactly, it will always be within part-to-part variation for that parameter. In general there is good alignment between the simulations and the data sheet.

A second factor where models may deviate from the data sheet is due to self-heating effects that occur on measurements. Some measurements such as diode-forward characteristics and output characteristics generate a lot of power in the device. Whilst the measurements are taken in as short a time possible the pulse is a finite period and self-heating will always occur.

Fig. 26 shows the difference caused by the self-heating within the V_{SDS} simulation. The self-heating is causing a drop in the V_F as the power increases allowing more current to flow for a given V_{DS}.

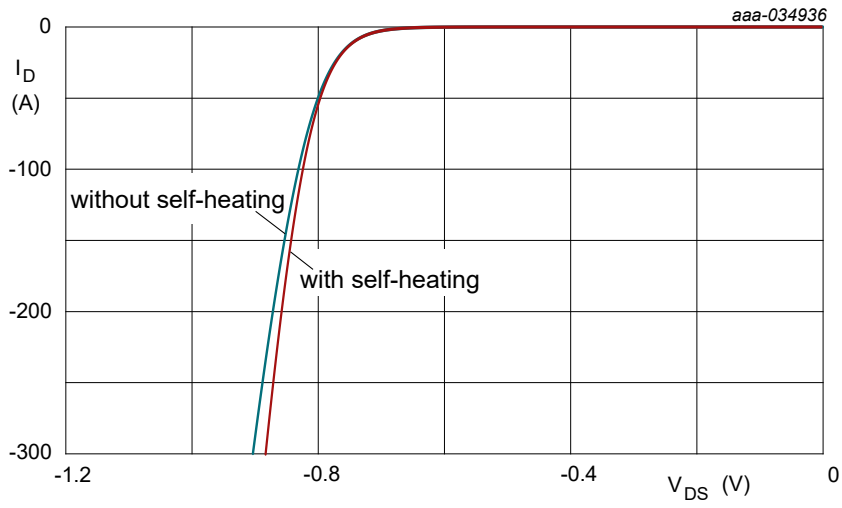


Fig. 26. V_{SDS} self-heating effects

7. Simulation tips and tricks

Whilst we endeavour to make the models as stable as possible some simulations may not converge, here are some tips and tricks:

- When using current sources to drive the pins of the model, placing a resistor to ground from the output of the current source may help, start at 1.0E9 Ω first, and go down in decades
- Changing the tolerances may help, SPICE is originally targeted at ICs with low currents so decreasing the tolerance may be acceptable for power electronics simulations
- In LTspice™ specifically using the alternate solver is often more successful in achieving convergences

8. Full simulation validity range

Table 1 shows the range over which the models are valid.

Table 1. Range over which the models are valid

Characteristics	Operating condition range	Temperature range	Comments
R_{DSon}	V_{DS} = -1.2 V to 8.0 V; V_{GS} = 0 V to $V_{GS(max)}$	-55 °C to 175 °C	
I_D/V_G	V_{DS} = 0 V to 8.0 V	-55 °C to 175 °C	
I_D/V_D	V_{DS} = 0 V to 8.0 V	-55 °C to 175 °C	
V_{SDS}	I_D ≤ pulsed drain current limit (I_{DM})	-55 °C to 175 °C	
BV_{DSS}	I_D ≤ pulsed drain current limit (I_{DM})	-55 °C to 175 °C	
Q_G and capacitance	full data sheet voltage range	-55 °C to 175 °C	not temperature dependant
Q_{RR}	V_{DS} = 0.5 x V_{DSmax}	-55 °C to 175 °C	not temperature dependant
Thermal impedance (Z_{th})	NA	-55 °C to 175 °C	worst case value as per data sheet
I_{DSS}	V_{DS} = 0 to BV_{DSS}	-55 °C to 175 °C	
I_{GSS}	NA	NA	not modelled

9. Summary

Nexperia's new electrothermal MOSFET models have been introduced and their use in LTspice™ simulations have been demonstrated. Electrothermal models will feature in future interactive application notes, please visit the Nexperia website to learn more: https://www.nexperia.com/applications/interactive-app-notes/.

10. Revision history

Table 2. Revision history

Revision number	Date	Description
1.0	2022-04-08	Initial version.

11. Legal information

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