Nexperia
Logic Translators

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EFFICIENCY WINS.

Overview

In recent years, voltage translation has become an important part of electronic design, especially in portable applications.

The latest data processors for battery-operated applications are typically produced in advanced, low-power CMOS process technologies that use a supply voltage of 1.8 V or lower. These low-voltage devices require interfacing to legacy peripherals, including memories, image sensors, relays, and RF transceivers, that are more likely to use older, lower-cost process technologies that operate at higher supply voltage. Voltage-level translators enable these different devices to work together, without producing damaging current flow or signal loss, so the system operates more efficiently and saves power. In this guide, different techniques used in translators are presented along with the products associated with them.

Introduction

Many factors have caused the existence of the number of voltage ranges in use today. The bipolar 5.0 V TTL families were replaced by lower power 5.0 V CMOS devices, introducing a need for CMOS to TTL translation. Smaller, and faster, 3.3 V devices were also introduced to improve memory access times. As the portable market grew, power became more important, 1.8 V and 1.2 V devices have been introduced to meet this.
There are now multiple voltage supply nodes that can be interfaced together. The need for voltage translation between CMOS and TTL and over different voltage nodes is inherent to ensure inter-operability.

In modular designs, devices may be at different supply voltages. For example, for a PCMCIA card, where a newer 1.8V processor is required to be interfaced to a proven 3.3V peripheral, a level translator is the solution.

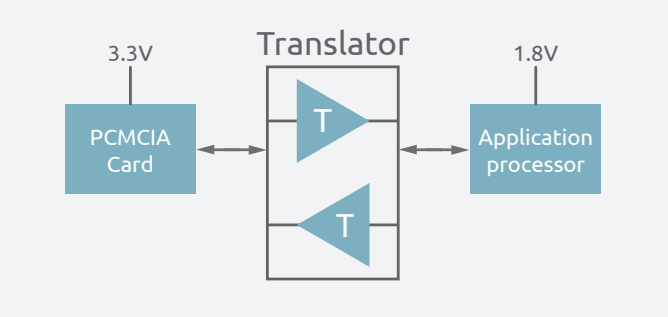

Fig. Usage of Translator

Input and output levels

Electronic devices have input levels (V_{IH} and V_{IL}) and output levels (V_{OH} and V_{OL}). Table A is an extract of a datasheet showing these levels

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} =25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8V	0.70 x V_{CC}	-	-	V
		V_{CC} = 0.9V to 1.95V	0.65 x V_{CC}	-	-	V
		V_{CC} = 2.3V to 2.7V	1.6	-	-	V
		V_{CC} = 3.0V to 3.6V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8V	-	-	0.30 x V_{CC}	V
		V_{CC} = 0.9V to 1.95V	-	-	0.35 x V_{CC}	V
		V_{CC} = 2.3V to 2.7V	-	-	0.7	V
		V_{CC} = 3.0V to 3.6V	-	-	0.9	V
V_{OH}	HIGH-level input voltage	V_I = V_{IH} or V_{IL}				
		I_O = -20 µA; V_{CC} = 0.8V to 3.6V	V_{CC} - 0.1	-	-	V
		I_O = -1.1 mA; V_{CC} = 1.1V	0.75 x V_{CC}	-	-	V
		I_O = 1.7 mA; V_{CC} =1.4V	1.11	-	-	V
		I_O = 1.9 mA; V_{CC} = 1.65V	1.32	-	-	V
		I_O = 2.3 mA; V_{CC} = 2.3V	2.05	-	-	V
		I_O = 3.1 mA; V_{CC} = 2.3V	1.9	-	-	V
		I_O = 2.7 mA; V_{CC} = 3.0V	2.72	-	-	V
		I_O = 4.0 mA; V_{CC} = 3.0V	2.6	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -20 µA; V_{CC} = 0.8V to 3.6V	-	-	0.1	V
		I_O = -1.1 mA; V_{CC} = 1.1V	-	-	0.3 x V_{CC}	V
		I_O = 1.7 mA; V_{CC} =1.4V	-	-	0.31	V
		I_O = 1.9 mA; V_{CC} = 1.65V	-	-	0.31	V
		I_O = 2.3 mA; V_{CC} = 2.3V	-	-	0.31	V
		I_O = 3.1 mA; V_{CC} = 2.3V	-	-	0.44	V
		I_O = 2.7 mA; V_{CC} = 3.0V	-	-	0.31	V
		I_O = 4.0 mA; V_{CC} = 3.0V	-	-	0.44	V

Table A. Input and output levels

V_{IH} is the high-level input voltage, if a voltage is applied that is > V_{IH}, it will be seen as a logic HIGH. V_{IL} is the low-level input voltage, if a voltage is applied that is < V_{IL}, it will be seen as a logic LOW. V_{OH} is the high-level output voltage at a specified output current. V_{OL} is the low-level output voltage at a specified output current.

Table B shows the input and output levels for TTL and CMOS products over a range of supply voltages.

Voltage	TTL				CMOS			
	Input Voltage		Output voltage		Input Voltage		Output voltage	
	V_{IH}	V_{IL}	V_{OH}	V_{OL}	V_{IH}	V_{IL}	V_{OH}	V_{OL}
5.0 - 15.0V					0.7*V_{cc}	0.3*V_{cc}		
5.0V	2.00	0.80	2.40	0.50	3.50	1.50	4.50	0.40
3.3V	2.00	0.80	2.40	0.55	2.31	0.99	2.55	0.45
1.8V					1.27	0.68	1.30	0.35
1.5V					0.98	0.78	1.30	0.35
1.2V					0.78	0.42	1.03	0.36

Table B: CMOS and TTL input and output voltage levels

As shown in table C, to guarantee functionality, the V_{OH} of the driver must be higher than the V_{IH} of the receiver. Similarly the V_{OL} of the driver must be lower than the V_{IL} of the receiver.

Device 1		Device 2	Operation
V_{OH} (min)	>	V_{IH} (min)	Function guaranteed
V_{OH} (min)	<	V_{IH} (min)	Function not guaranteed
V_{OL} (max)	>	V_{IL} (max)	Function not guaranteed
V_{OL} (max)	<	V_{IL} (max)	Function guaranteed

Table C: Input and output voltage levels and functionality

The existence of so many voltage nodes creates issues when trying to interface circuits together.
The figure below depicts H-L and L-H translation between LVC, AUP and AXP types.

When the driver's V_{OH} is lower than the receiver's V_{IH}, and/or the driver V_{OL} is greater than the receiver V_{IL}, the logic state is undefined and system behavior becomes unpredictable. While designing a system, it is critical to have parts whose outputs are compatible with the receivers' input.

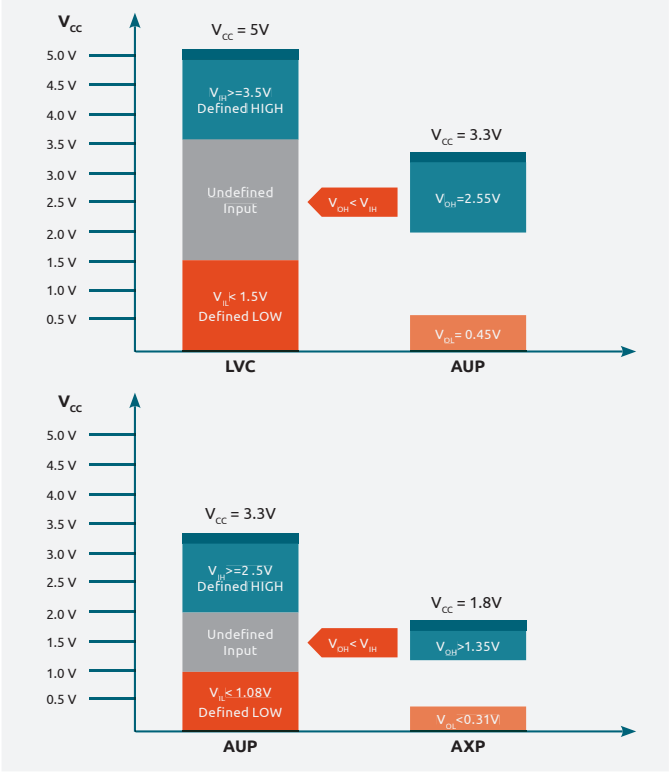

Fig. 5.0V, 3.3V and 1.8V CMOS levels

Types of translation

The following figures depict unidirectional low to high and bi-directional low to high and high to low voltage translation

Uni-directional
Suitable for either LOW to HIGH, or HIGH to LOW level translation with data transmission in one direction only.

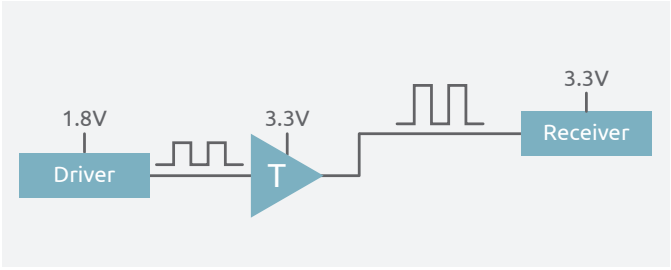

Fig. Uni-directional LOW to HIGH voltage translation

Bi-directional
Suitable for LOW to HIGH and/or HIGH to LOW level translation with data transmission and reception.

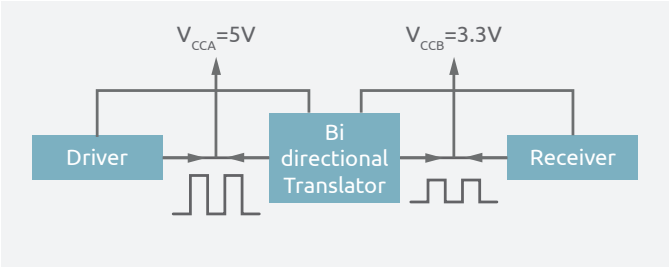

Fig. Bi-directional LOW to HIGH and HIGH to LOW voltage translation

Level translation techniques

Uni-directional HIGH to LOW level translation

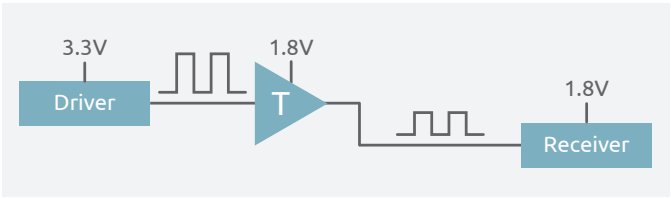

Fig. HIGH to LOW uni-directional voltage level translation

Clamp diode inputs using current-limiting resistors
By using input current limiting resistors with the internal clamp diode, HIGH to LOW voltage translation is possible. Many CMOS inputs include diodes to V_{CC} in their input ESD protection structures. Voltages higher than V_{CC} can be clamped by these diodes if current-limiting resistors are used. This provides HIGH to LOW voltage translation using current limiting resistors.

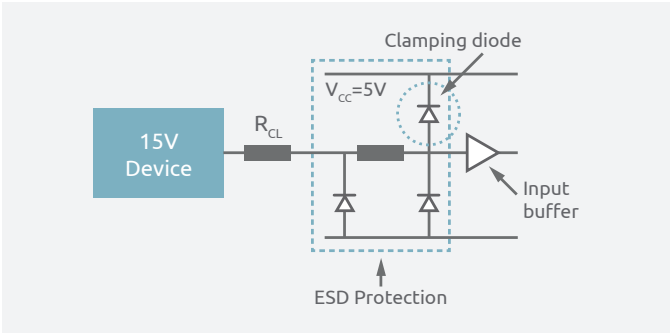

Fig. Clamp input diode using current-limiting resistors

Value of current limiting resistor R_{CL} can be calculated using V_{CC} values of driver and receiver devices. The input clamp diode also serves as an ESD protection.

Devices with input ESD diodes to V_{CC}
A device has input ESD diodes to V_{CC} if the datasheet limiting value of input clamping current (I_{IK}) includes the condition $V_I > V_{CC}$ + 0.5V and the max recommended input voltage $V_I = V_{CC}$ (see Table D).

To use the ESD diode as a clamp diode, the value of the current-limiting resistors R_{CL} should be set to ensure that the limiting value of I_{IK} is not exceeded. If there is more than one input, ensure that the combined current does not exceed the limiting value of I_{CC}.

Symbol	Parameter	Condition	Min	Max	Unit
I_{IK}	input clampingcurrent	V_I < -0.5V or $V_I > V_{CC}$ + 0.5V	-	+/-20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	supply current		-50	-	mA

Table D: Parameters indicating ESD input diodes

Advantage:
› Can be used to interface any voltage

Disadvantage:
› Requires external components

Overvoltage-tolerant inputs
Modern CMOS ESD protection circuits provide the same ESD protection without including a diode to V_{CC}. These devices have overvoltage-tolerant inputs because the recommended value of V_I is not V_{CC} but the same as the recommended maximum V_{CC}. A device specified for operation over a supply voltage range of 1.65 to 5.5V can be used at 3.3 V with 5.5 V applied to inputs. A device with overvoltage-tolerant inputs is suitable for HIGH to LOW level translation.

Devices with overvoltage-tolerant inputs:

A device has overvoltage tolerant inputs if the datasheet limiting value of I_{IK} does not include the condition $V_I > V_{CC} + 0.5V$ and the max recommended V_I is not V_{CC}.

Advantages:

- No external components required
- Lower system power than clamp diode solution

Disadvantages:

- Input can not be driven at voltages greater than the recommended maximum value of V_{CC}

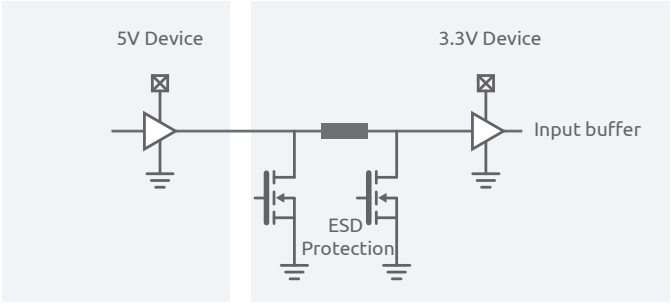

Fig. Using overvoltage tolerant inputs to enable HIGH-to-LOW level translation

Uni-directional LOW to HIGH level translation

Open-drain outputs

An open-drain output can be pulled-up to the desired voltage level in LOW to HIGH voltage translation

In devices equipped with an open-drain output, the output is pulled up to a pull-up voltage level matching the input requirements of the device it is driving. A pull-up resistor is used on the output for level translation.

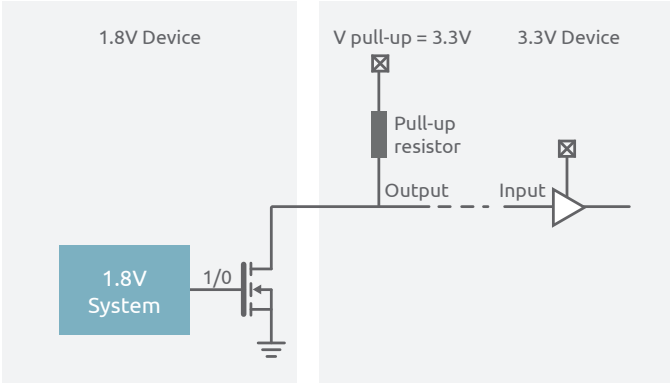

Fig. Open-drain output and pull-up resistor for level translation

Important points to note when considering open-drain outputs with pull-up resistors for level translation:

- Output rise and fall times are dependent upon the value of pull-up resistor used
- Pull-up voltage may be higher or lower than the device supply voltage
- In designs that use power-down to save battery life, use devices that include I_{OFF} in the static characteristics

Devices with open-drain outputs:

Logic devices with open-drain outputs will not have a V_{OH} parameter listed in the static characteristics of the datasheet.

Advantage:

- HIGH to LOW or LOW to HIGH translation

Disadvantages:

- Requires external components
- Additional system power

Low-threshold inputs

CMOS devices with input switching thresholds set lower than the typical $V_{CC}/2$ horizontally can be used for LOW to HIGH level translation.

The combination of N1 sizing and the drop across diode D1 determines the input threshold. The P2 PMOS reduces cross-bar current through the inverter.

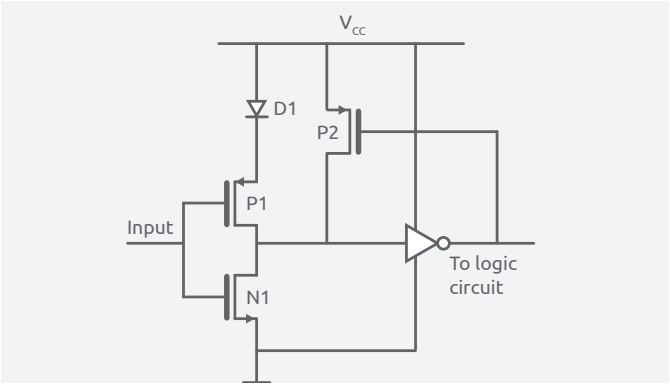

Fig. CMOS input with low threshold values

AHCT and HCT families operate at 5V and have inputs that can be interfaced to 5V TTL or 3.3V CMOS outputs. AUP1T operates at 3.3 V and can be used to interface to 1.8V CMOS outputs.

Devices with low-threshold inputs:

Logic devices with low-threshold inputs will have a ΔI_{CC} included in the static characteristics listed in the datasheet. This is the extra static current due to an input being applied that is lower than V_{CC}.
Note that to ensure power dissipation is minimized, the input should be set low as the default condition.

Smybol	Parameter	Conditions	Min	Typ	Max	Typ
ΔIcc	additional supply current	VI = VCC - 0.6 V; IO = 0 A; VCC = 3.3 V	-	-	50	µA

Table E: Parameters for devices with low-threshold inputs

Advantages:

- No external components required
- Same footprint as standard function

Disadvantage:

- Higher power dissipation due to ΔI_{CC}

Uni-directional LOW to HIGH level translation in modular design

In some cases a modular system may consist of circuits in three different voltage nodes. Control logic may be required to ensure correct functionality across all modules.

Overvoltage-tolerant inputs with open-drain outputs

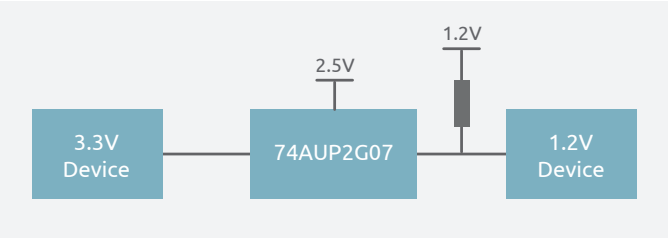

Fig. OVT input with open drain outputs

A device that includes overvoltage-tolerant inputs and open-drain outputs can be used to interface between three voltage domains. The figure below shows the 74AUP2G07 being supplied at 2.5 V and interfacing control signals between circuits at 3.3 V and 1.2 V.

Clamp diode inputs with open-drain outputs

A device that includes an ESD protection diode and open-drain outputs can be used to interface between three voltage domains. The figure below shows the 74HC3G07 being supplied at 5.0 V and interfacing control signals between circuits at 12 V and 3.3 V

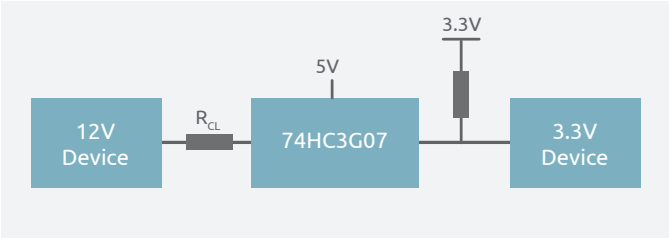

Fig. Clamp diode inputs with open drain outputs

Low-threshold inputs with open-drain outputs

A device that includes low-threshold inputs and open-drain outputs can be used to interface between three voltage domains. The Figure below shows the 74HCT3G07 being supplied at 5.0 V and interfacing control signals between circuits at 3.3 V and 1.8 V

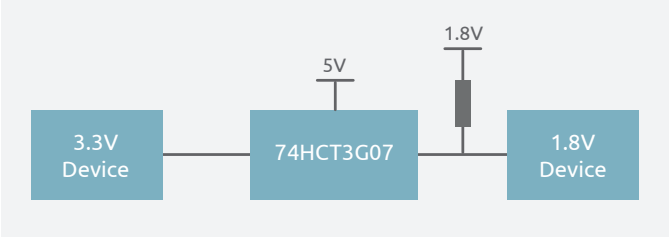

Fig. Low-threshold inputs with open drain outputs

Dual-supply voltage translators

Dual-supply devices have two supply voltages at different voltage ranges. These translators can be used for uni or bi-directional voltage level translation. Dual supply devices are designed for asynchronous communication between devices operating at different voltages and are also known as dual-supply voltage translators. Dual-supply voltage translators can be used for LOW to HIGH and HIGH to LOW voltage translation. These devices are supplied at V_{CCA} & V_{CCB} and interface data ports A & B operating in different voltage domains. They feature DIR pins to control signal direction. They are more power efficient than the single supply solutions.

Dual supply voltage translators are available in 1-, 2-, 8-, 16- and 20-bit bi-directional transceivers covering 0.8 to 3.6V and 1.2 to 5.5V, making them ideal for interfacing between supply domains of 1.2, 1.8, 2.5, 3.3 and 5.0V. Gates, buffers and shift registers also have translator function built-in.

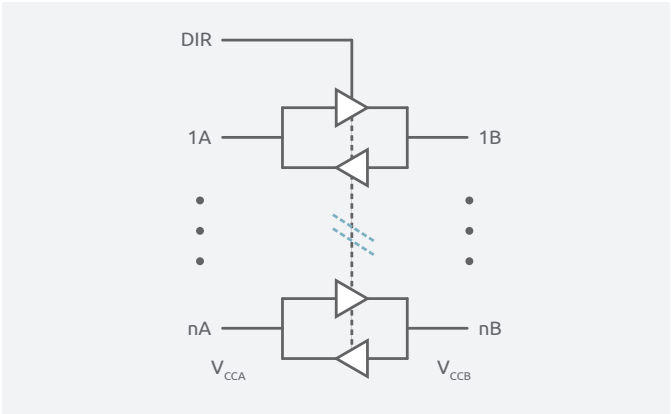

Fig. Dual –supply voltage translating transceiver

Advantages:

- No ΔIcc
- Low power consumption for battery-operated & handheld systems
- Same interface (w.r.t firmware & hardware)
- Flexibility in translating to/from a variety of voltage nodes

Disadvantages:

- Different footprint leads to change in the layout
- Larger packages are required, extra pin for second supply

CBTD & CBTLVD Switches

These are dedicated bus switches that perform level translation along with signal switching. CBTD & CBTLVD can be used to interface 5V to 3.3 systems and 3.3V to 1.8V systems respectively. CBTD is used for HIGH to LOW translation when interfacing a 5V CMOS system with a 3.3V system. They can also be used for bi-directional translation when interfacing 5V TTL system with a 3.3V system.

Similarly, CBTLVD can be used for down-translation when interfacing a 3.3V CMOS system with a 1.8V system. They can also be used for bi-directional translation when interfacing 3.3V TTL system with a 1.8V system.

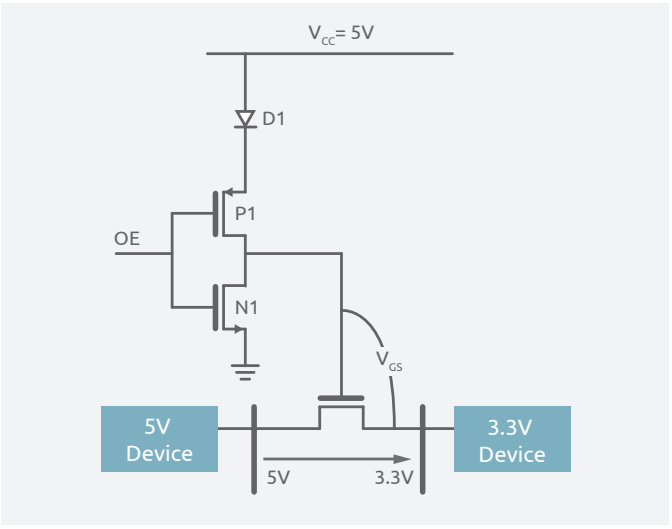

Fig. Pass transistor acting as switch

Advantage:

- Low propagation delay

Disadvantages:

- No buffering of the translated signal

For the complete Logic voltage translation portfolio, refer to data tables.

Bi-directional translators with Auto direction Sense

If bi-directional translation is needed but no direction signal by the system components is available, an auto sensing translator can be used to resolve the problem. A pair of I/O spanning voltage domains can act as either inputs or outputs depending on external stimulus without the need for a dedicated direction control pin. Internally, an extra current sensing circuit detect the direction and configures the translation circuit accordingly.

Nexperia's NXB, NXS translators are bi-directional voltage translators with integrated weak output buffer and one-shot circuits for fast switching speeds. They automatically sense the direction of the data flow. They are typically used in medium data rate interfaces with a maximum data rate up to 100Mbps. Level translators with auto-direction sensing are available in active and passive formats and can be used for both up and down translation.

- Passive devices don't have CMOS output and source and sink comes from the supply voltage. (NXS, LSF)
- Active devices have a CMOS output stage with a specific source and sink. (NXB)

Advantage:

- Offered in smaller package due to elimination of an external direction pin and the associated control logic.
- No specific power supply ramp up/ down sequencing is required.

Disadvantages:

- These translators have limited drive capability.

Active Device – NXB Level Translators

These are bi-directional push-pull type I/Os with integrated pull-ups. These are ideal for driving long traces, capacitive or high impedance loads like SPI, UART, HDMI, GPIO, USB Ports etc.

These translators can support maximum data rate of 100Mbps. It comprises of integrated one-shot blocks and 4k pull up and down resistors to accelerate the rising and falling edges in LOW to HIGH and HIGH to LOW transitions.

Figure below illustrates the architecture of one I/O channel of an NXB level translator. The translator incorporates a weak buffer with one-shot circuitry to improve switching speeds for rising and falling edges. When the A port is connected to a system driver and driven high, the weak 4 kΩ buffer drives the B port high in conjunction with the upper one shot, which becomes active when it senses a rising edge. The B port is driven high by both the buffer and the T1 PMOS, which lowers the output impedance seen on the B port while the one-shot circuit is active. On the falling edge, the lower one-shot is triggered and the buffer, along with the T2 NMOS, lowers the output impedance seen on the B port while the one-shot circuit is operating, and the output is driven low. The active circuitry in the NXB I/O channel during translations from low to high and high to low is depicted in the figure.

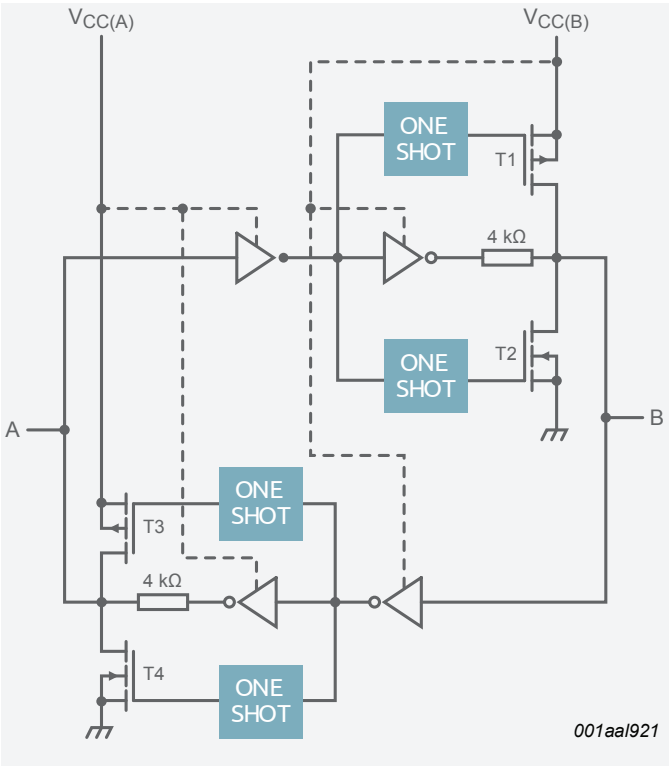

Fig. Architecture of single channel NXB Translator

Active devices – NXS Level Translators

These are bi-directional switch type translators suitable for open drain drivers used in I2C-bus, GPIO, I2C, PMBus, SMBus, Display modules, HDMI, 1-wire Bus, GPIO. The NXS has an internal pass transistor and additional one-shot circuits to accelerate rising edges of the input signals. These devices are equipped with one-shot block and 10kΩ resistor pull ups to accelerate the edges during LOW to HIGH and HIGH to LOW input transitions.

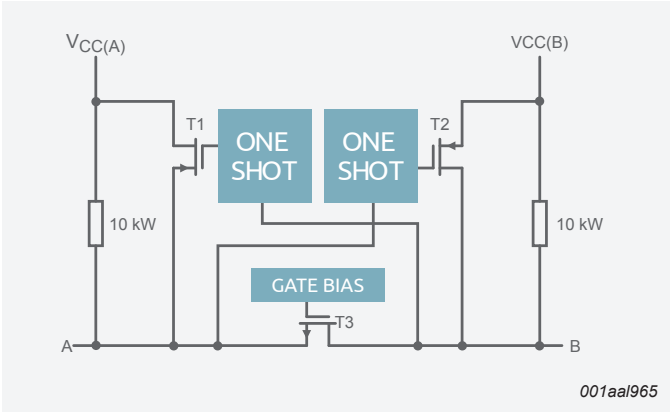

Fig. Architecture of Single Channel NXS Level Shifter

To achieve faster data rates through the device, these translators include rising edge-rate acceleration circuitry to provide stronger drive for the rising edge by bypassing the integrated 10-kΩ pull-up resistors through a low impedance path during low-to-high signal transitions. A one-shot circuit with an associated T1/ T2 PMOS transistor is used to increase switching speeds for the rising-edge input signals. When a rising edge is detected by the one-shot. circuit, the T1/T2 PMOS transistors turn on momentarily to rapidly drive the port high, effectively lowering the output impedance seen on that port and speeding up rising edge inputs.

The N-channel pass-gate transistor is used to open and close the connection between the A and B ports. When a driver connected to A or B port is low, the opposite port is, in turn, pulled low by the N2 pass-gate transistor. The gate bias voltage of the pass-gate transistor (T3) is set at approximately one threshold voltage above the VCC level of the low-voltage side.

During a low-to-high transition, the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2), bypassing the 10 kΩ pull-up resistors, and increasing current drive capability. The one-shot is activated once the input transition reaches approximately V_{CCI}/ 2 and is de-activated approximately 50 ns after the output reaches V_{CCO}/2. During the acceleration time, the driver output resistance is between approximately 50 and 70 Ω. To avoid signal contention and minimize dynamic ICC, the user should wait for the one-shot circuit to turn off before applying a signal in the opposite direction.

The pass-gate transistor T3 is on when V_{GS} is greater than $V_{T.}$ When one side of T3 is held low by an external driver, with the input to T3 at 0 V, T3 will be on and the output of T3 will be held to nearly 0 V due to the on-state resistance of T3. As the input voltage rises due to a rising edge, the output voltage of T3 tracks the input until the input voltage reaches V_{GATE} minus V_T and T3 turns off. After T3 stops conducting, the input and output ports continue to rise to their respective supply voltages due to the internal pull-up resistors. In the second case, both ports start with high levels since the integrated pull-up resistors tie the inputs to the respective supply voltages, $V_{CC(A)}$ and $V_{CC(B)}$. When the input ports are pulled low by external drivers, T3 starts to conduct when V_{GS} is greater than V_T and output starts tracking the input. The source current needed for this operation must be provided by the external driver connected to the A or B port.

Passive devices – LSF Level Translators

LSF010x translator family is a bidirectional multi-voltage level translator with an internal pass transistor. It has a reference channel and, dependent on the type, several translation channels that can be used independently. The independent usage of the channels is meant in terms of different voltage levels as well as different directions.

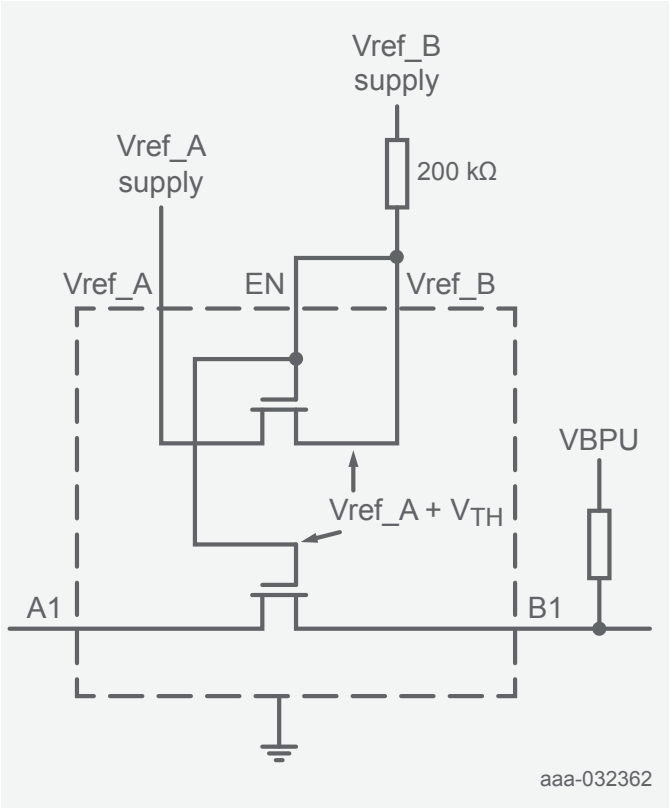

Fig. Architecture of Single Channel LSF Level Shifter using enable and reference voltage.

The internal structure of the LSF translator is shown in the above-mentioned Figure, as an example of a single channel LSF0101. The source of the reference channel is supplied by Vref_A, resulting in a voltage level of Vref_A + V_{TH} (~0.8 V) at the source of Vref_B and at the gates of all pass transistors in the IC. Thus, the gate voltage levels of all pass transistors are determined by Vref_A.

The enable pin of the LSF translator should be externally shorted to the Vref_B pin. If the enable pin shall be controlled dynamically, this pin should not be driven by a push-pull stage because in case of high-level drive, the enable pin voltage would be forced to the supply voltage level of the driver. Instead, the enable pin should be driven with an open drain driver without a pull-up resistor, as it is already provided by Vref_B.

Product Comparison – Autosense Translators

Family	NXS	NXB	LSF
Translation	Active	Active	Passive
Benefit	One-Shot improves rise time	One-Shot improves rise time	FET switch-based topology resulting in fast switching speed
Applications	Open Drain and Push-Pull, Control interfaces, I2C-bus, GPIO, I2C, PMBus, SMBus, Display modules, HDMI, 1-wire Bus, GPIO	Push Pull, Control interfaces with active drive, SPI, UART, HDMI, GPIO, USB Ports	Open Drain and Push-Pull, Control interface, I2C-bus, GPIO, I2C, PMBus, SMBus
Number of Channels	1, 2, 4, 8	1, 2, 4 ,8	1, 2, 4, 8
Signal Integrity	Better	Best	Good
Package options	GS, GM, DC, PW, GU12, BQ	GS, GM, DC, PW, GU12, BQ	GM, GX, DP, DC, PW, GU12, BQ
Temperature Range	−40 °C to +125 °C	−40 °C to +125 °C	−40 °C to +125 °C
I_{OFF}	Yes	Yes	-
Over voltage tolerant inputs	Yes	Yes	Yes
Products	NXS0101GS, NXS0101GM, NX0102DC, NXS0102DC-Q100, NXS0104PW, NXS0104PW-Q100, NXS0104BQ, NXS0104GU12, NXS0108BQ, NXS0108BQ-Q100, NXS0108PW, NXS0108PW-Q100	NXB0101GS, NXB0101GM, NX0102DC, NXB0102DC-Q100, NXB0104PW, NXB0104PW-Q100, NXB0104BQ, NXB0104GU12, NXB0108BQ, NXB0108BQ-Q100, NXB0108PW, NXB0108PW-Q100	LSF0101GM, LSF0101GX, LSF0102DP, LSF0102GX, LSF0102DC, LSF0102DC-Q100, LSF0204PW, LSF0204GU12, LSF0108PW, LSF0108PW-Q100, LSF0108BQ, LSF0108BQ-Q100

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1. Bi-directional translators with Auto direction Sense

NXS Level Translators

Type number	Description	Features						Package							
		V_{CC} (A)(V)	V_{CC}(B) (V)	Output drive capability (mA)	tpd (ns)	No of bits	No of pins	SOT886	SOT1202	SOT765-1	SOT762-1	SOT1174-1	SOT402-1	SOT764-1	SOT360-1
NXB0101GM	Dual supply translating transceiver; auto direction sensing; 3-state	1.2 - 3.6	1.65 - 5.5	± 0.02	5.5	1	6	•							
NXB0101GS	Dual supply translating transceiver; auto direction sensing; 3-state	1.2 - 3.6	1.65 - 5.5	± 0.02	5.5	1	6		•						
NXB0102DC	Dual supply translating transceiver; auto direction sensing; 3-state	1.2 - 3.6	1.65 - 5.5	± 0.02	5.5	2	8			•					
NXB0104BQ	Quad supply translating transceiver; auto direction sensing; 3-state	1.2 - 3.6	1.65 - 5.5	± 0.02	5.5	4	14				•				
NXB0104GU12	Quad supply translating transceiver; auto direction sensing; 3-state	1.2 - 3.6	1.65 - 5.5	± 0.02	5.5	4	12					•			
NXB0104PW	Quad supply translating transceiver; auto direction sensing; 3-state	1.2 - 3.6	1.65 - 5.5	± 0.02	5.5	4	14						•		
NXB0108BQ	8-bit Dual supply translating transceiver; auto direction sensing; 3-state	1.2 - 3.6	1.65 - 5.5	± 0.02	5.5	8	20							•	
NXB0108PW	8-bit Dual supply translating transceiver; auto direction sensing; 3-state	1.2 - 3.6	1.65 - 5.5	± 0.02	5.5	8	20								•

NXB Level Translators

Type number	Description	Features						Package							
		V_{CC} (A)(V)	V_{CC}(B) (V)	Output drive capability (mA)	tpd (ns)	No of bits	No of pins	SOT886	SOT1202	SOT765-1	SOT762-1	SOT1174-1	SOT402-1	SOT764-1	SOT360-1
NXS0101GM	Dual supply translating transceiver; open drain; autodi-rectionsensing	1.65 - 3.6	2.3 - 5.5	- 0.02 / 1.0	4.7	1	6	•							
NXS0101GS	Dual supply translating transceiver; open drain; autodi-rectionsensing	1.65 - 3.6	2.3 - 5.5	- 0.02 / 1.0	4.7	1	6		•						
NXS0102DC	Dual supply translating transceiver; open drain; autodi-rectionsensing	1.65 - 3.6	2.3 - 5.5	- 0.02 / 1.0	5.2	2	8			•					
NXS0104BQ	Quad supply translating transceiver; open drain; auto direction sensing	1.65 - 3.6	2.3 - 5.5	- 0.02 / 1.0	6	4	14				•				
NXS0104GU12	Quad supply translating transceiver; open drain; auto direction sensing	1.65 - 3.6	2.3 - 5.5	- 0.02 / 1.0	6	4	12					•			
NXS0104PW	Quad supply translating transceiver; open drain; auto direction sensing	1.65 - 3.6	2.3 - 5.5	- 0.02 / 1.0	6	4	14						•		
NXS0108BQ	8-bit Dual supply translating transceiver; open drain; auto direction sensing	1.2 - 3.6	1.65 - 5.5	- 0.02 / 1.0	6.3	8	20							•	
NXS0108PW	8-bit Dual supply translating transceiver; open drain; auto direction sensing	1.2 - 3.6	1.65 - 5.5	- 0.02 / 1.0	6.3	8	20								•

LSF Level Translators

Type number	Description	Features						Package									
		V_{CC} (A)(V)	V_{CC}(B) (V)	Output drive capability (mA)	tpd (ns)	No of bits	No of pins	SOT886	SOT1255-2	SOT765-1	SOT505-2	SOT1203	SOT1233-2	SOT1174-1	SOT402-1	SOT360-1	SOT764-1
LSF0101GM	1-bit bidirectional multi-voltage level translator; open-drain; push-pull	0.95 - 5.0	0.95 - 5.0	0.7	1	6	6	•									
LSF0101GX	1-bit bidirectional multi-voltage level translator; open-drain; push-pull	0.95 - 5.0	0.95 - 5.0	0.7	1	6	6		•								
LSF0102DC	2-bit bidirectional multi-voltage level translator; open-drain; push-pull	0.95 - 5.0	0.95 - 5.0	0.7	2	8	8			•							
LSF0102DP	2-bit bidirectional multi-voltage level translator; open-drain; push-pull	0.95 - 5.0	0.95 - 5.0	0.7	2	8	14				•						
LSF0102GS	2-bit bidirectional multi-voltage level translator; open-drain; push-pull	0.95 - 5.0	0.95 - 5.0	0.7	2	8	12					•					
LSF0102GX	2-bit bidirectional multi-voltage level translator; open-drain; push-pull	0.95 - 5.0	0.95 - 5.0	0.7	2	8	14						•				
LSF0108BQ	8-bit bidirectional multi-voltage level translator; open-drain; push-pull	0.95 - 5.0	0.95 - 5.0	1.4	8	20	20										•
LSF0108PW	8-bit bidirectional multi-voltage level translator; open-drain; push-pull	0.95 - 5.0	0.95 - 5.0	1.4	8	20										•	
LSF0204GU12	4-bit bidirectional multi-voltage level translator; open-drain; push-pull	0.8 - 5.0	0.8 - 5.0	0.6	4	12								•			
LSF0204PW	4-bit bidirectional multi-voltage level translator; open-drain; push-pull	0.8 - 5.0	0.8 - 5.0	0.6	4	14	20								•		

2.Standard input with clamp diode

Single Buffers

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1	SOT363
74HC1GU04	single inverter; unbuffered	2.0 - 6.0	+/- 2.6	5	36	-40~125	•	
74HC1G04	single inverter	2.0 - 6.0	+/- 2.6	7	36	-40~125	•	
74HC1G14	single inverter; Schmitt-trigger	2.0 - 6.0	+/- 2.6	10	36	-40~125	•	
74HC1G125	single buffer/line driver	2.0 - 6.0	+/- 2.6	9	36	-40~125	•	
74HC1G126	single buffer/line driver	2.0 - 6.0	+/- 2.6	9	36	-40~125	•	
74HC2GU04	single inverter; unbuffered	2.0 - 6.0	+/- 2.6	5	36	-40~125		•

Dual Buffers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT363	SOT765-1	SOT505-2
74HC2G04	dual inverter	2.0 - 6.0	+/- 5.2	8	36	-40~125	•		
74HC2G14	dual inverter; Schmitt-trigger	2.0 - 6.0	+/- 5.2	16	36	-40~125	•		
74HC2G16	dual buffer gate	2.0 - 6.0	+/- 5.2	8	36	-40~125	•		
74HC2G17	dual buffer; Schmitt-trigger	2.0 - 6.0	+/- 5.2	12	36	-40~125	•		
74HC2G34	dual buffer	2.0 - 6.0	+/- 5.2	9	36	-40~125	•		
74HC2G125	dual buffer/line driver	2.0 - 6.0	+/- 5.2	10	36	-40~125		•	•

Triple Buffers

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT765-1	SOT505-2
74HC3GU04	triple inverter; unbuffered	2.0 - 6.0	+/- 5.2	6	36	-40~125	•	•
74HC3G04	triple inverter	2.0 - 6.0	+/- 5.2	8	36	-40~125	•	•
74HC3G14	triple inverter; Schmitt-trigger	2.0 - 6.0	+/- 5.2	16	36	-40~125	•	•
74HC3G16	triple buffer gate	2.0 - 6.0	+/- 5.2	8	36	-40~125		•
74HC3G34	triple buffer	2.0 - 6.0	+/- 5.2	9	36	-40~125	•	•

Quad Buffers

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1
74HC125	quad buffer/line driver	2.0 - 6.0	+/- 7.8	9	36	-40~125	•	•
74HC126	quad buffer/line driver	2.0 - 6.0	+/- 7.8	9	36	-40~125	•	•

Hex Buffers

Type number	Description	Features					Package (suffix)				
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1	SOT109-1	SOT403-1
74HC7014	hex buffer precision; Schmitt-trigger	2.0 - 6.0	+/- 5.2	27	36	-40~125	•				
74HC04	hex inverter	2.0 - 6.0	+/- 5.2	7	36	-40~125	•	•	•		
74HC14	hex inverter; Schmitt-trigger	2.0 - 6.0	+/- 5.2	12	36	-40~125	•	•	•		
74HC365	hex buffer/line driver	2.0 - 6.0	+/- 7.8	9	36	-40~125				•	•
74HC366	hex inverter/line driver	2.0 - 6.0	+/- 7.8	10	36	-40~125				•	•
74HC367	hex buffer/line driver	2.0 - 6.0	+/- 7.8	8	36	-40~125				•	•
74HC368	hex inverter/line driver	2.0 - 6.0	+/- 7.8	9	36	-40~125				•	
74HCU04	hex inverter; unbuffered	2.0 - 6.0	+/- 5.2	5	36	-40~125	•	•	•		
74LV04	hex inverter	1.0 - 5.5	+/- 12	6	30	-40~125	•	•	•		
74LV14	hex inverter; Schmitt-trigger	1.0 - 5.5	+/- 12	13	30	-40~125	•	•	•		
HEF4049B	hex inverter/line driver	3.0 - 15.0	-3 / +20	20	10	-40~125				•	
HEF4050B	hex buffer/line driver	3.0 - 15.0	-3 / +20	40	10	-40~125				•	
HEF4069UB	hex inverter; unbuffered	3.0 - 15.0	+/- 3.4	15	10	-40~125	•	•			
HEF40098B	hex inverting buffer	3.0 - 15.0	-10 / +20	25	10	-40~125				•	
HEF40106B	hex inverter; Schmitt-trigger	4.5 - 15.5	+/- 2.4	30	10	-40~125	•	•			

Octal Buffers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1	SOT360-1	SOT764-1
74HC240	octal inverter/line driver	2.0 - 6.0	+/- 7.8	9	36	-40~125	•	•	•
74HC241	octal buffer/line driver	2.0 - 6.0	+/- 7.8	7	36	-40~125	•	•	
74HC244	octal buffer/line driver	2.0 - 6.0	+/- 7.8	9	36	-40~125	•	•	•
74HC540	octal inverter/line driver	2.0 - 6.0	+/- 7.8	9	36	-40~125	•		
74HC541	octal buffer/line driver	2.0 - 6.0	+/- 7.8	10	36	-40~125	•	•	
74HC7540	octal inverter/line driver; Schmitt-trigger	2.0 - 6.0	+/- 7.8	11	36	-40~125	•		
74HC7541	octal buffer/line driver; Schmitt-trigger	2.0 - 6.0	+/- 7.8	11	36	-40~125	•	•	
74LV244	octal buffer/line driver	1.0 - 5.5	+/- 16	8	30	-40~125	•	•	
HEF40244B	octal buffer/line driver	3.0 - 15.0	-62 / +45	30	10	-40~125	•		

Multibyte Buffers

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT362-1	SOT364-1
74ALVCH16244	16-bit buffer/line driver with bus hold	1.2 - 3.6	+/- 24	1,9	150	-40~85	•	
74ALVCH162244	16-bit buffer/line driver with bus hold	2.3 - 3.6	+/- 12	2,7	150	-40~85	•	
74ALVCH16825	18-bit buffer/line driver with bus hold	2.3 - 3.6	+/- 24	2	150	-40~85		•
74ALVCH16827	20-bit buffer/line driver with bus hold	2.3 - 3.6	+/- 24	2	150	-40~85		•
74ALVCH162827	20-bit buffer/line driver with bus hold	2.3 - 3.6	+/- 12	2,9	150	-40~85		•

FIFO Register

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT109-1	SOT403-1
74HC40105	4-bit x 16-word FIFO register	2.0 - 6.0	+/- 5.2	15	30	-40~125	•	•

Dual Flip Flops

Type number	Description	Features					Package (suffix)				
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1	SOT109-1	SOT403-1
74HC73	dual J-K flip-flop with reset	2.0 - 6.0	+/- 5.2	16	77	-40~125	•	•			
74HC74	dual D-type flip-flop with set and reset	2.0 - 6.0	+/- 5.2	14	82	-40~125	•	•	•		
74HC107	dual J-K flip-flop with reset	2.0 - 6.0	+/- 5.2	16	78	-40~125	•	•			
74HC109	dual J-/K flip-flop with set and reset	2.0 - 6.0	+/- 5.2	15	75	-40~125				•	
74HC112	dual J-K flip-flop with set and reset	2.0 - 6.0	+/- 5.2	15	66	-40~125				•	•
74LV74	dual D-type flip-flop with set and reset	1.0 - 5.5	+/- 12	11	75	-40~125	•	•			
HEF4013B	dual D-type flip-flop with set and reset	4.5 - 15.5	+/- 2.4	30	40	-40~85	•	•			
HEF4027B	dual J-K flip-flop	4.5 - 15.5	+/- 2.4	30	30	-40~85				•	

Quad Flip Flops

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT109-1	SOT403-1
74HC173	quad D-type flip-flop	2.0 - 6.0	+/- 7.8	17	88	-40~125	•	•
74HC175	quad D-type flip-flop	2.0 - 6.0	+/- 5.2	17	83	-40~125	•	•
HEF40175B	quad D-type flip-flop	4.5 - 15.5	+/- 2.4	25	45	-40~85	•	•

Hex Flip Flops

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT109-1	SOT403-1
74HC174	hex D-type flip-flop with reset	2.0 - 6.0	+/- 5.2	17	99	-40~125	•	•

Octal Flip Flops

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1	SOT360-1	SOT764-1
74HC273	octal D-type flip-flop	2.0 - 6.0	+/- 5.2	15	122	-40~125	•	•	•
74HC374	octal D-type flip-flop	2.0 - 6.0	+/- 7.8	14	83	-40~125	•	•	
74HC377	octal D-type flip-flop	2.0 - 6.0	+/- 7.8	13	83	-40~125	•	•	
74HC574	octal D-type flip-flop	2.0 - 6.0	+/- 7.8	14	133	-40~125	•	•	

Multibyte Flip Flops

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT362-1	SOT364-1
74ALVCH16374	16-bit D-type flip-flop with bus hold	1.2 - 3.6	+/- 24	2,3	350	-40~85	•	
74ALVCH16823	18-bit D-type flip-flop with bus hold	1.2 - 3.6	+/- 24	2,1	350	-40~85		•
74ALVCH16821	20-bit D-type flip-flop	2.3 - 3.6	+/- 24	2,5	350	-40~85		•

Single Gates

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1	SOT108-1	SOT402-1
74HC1G00	single 2-input NAND gate	2.0 - 6.0	+/- 2.6	7	36	-40~125	•		
74HC1G02	single 2-input NOR gate	2.0 - 6.0	+/- 2.6	7	36	-40~125	•		
74HC1G08	single 2-input AND gate	2.0 - 6.0	+/- 5.2	7	36	-40~125	•		
74HC1G32	single 2-input OR gate	2.0 - 6.0	+/- 2.6	8	36	-40~125	•		
74HC1G86	single 2-input EXCLUSIVE-OR gate	2.0 - 6.0	+/- 2.6	9	36	-40~125	•		
74HC30	8-input NAND gate	2.0 - 6.0	+/- 5.2	12	36	-40~125		•	•

Dual Gates

Type number	Description	Features					Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT765-1	SOT505-2	SOT108-1	SOT402-1
74HC21	dual 4-input AND gate	2.0 - 6.0	+/- 5.2	10	36	-40~125			•	•
74HC2G00	dual 2-input NAND gate	2.0 - 6.0	+/- 5.2	9	36	-40~125	•	•		
74HC2G02	dual 2-input NOR gate	2.0 - 6.0	+/- 5.2	9	36	-40~125	•	•		
74HC2G08	dual 2-input AND gate	2.0 - 6.0	+/- 5.2	9	36	-40~125	•	•		
74HC2G32	dual 2-input OR gate	2.0 - 6.0	+/- 5.2	9	36	-40~125	•	•		
74HC2G86	dual 2-input EXCLUSIVE-OR gate	2.0 - 6.0	+/- 5.2	9	36	-40~125	•	•		
74HC20	dual 4-input NAND gate	2.0 - 6.0	+/- 5.2	8	36	-40~125			•	•
74HC4002	dual 4-input NOR gate	2.0 - 6.0	+/- 5.2	9	36	-40~125			•	•
HEF4007UB	dual complementary pair and inverter	4.5 - 15.5	+/- 3.4	15	10	-40~85			•	
HEF4082B	dual 4-input AND gate	4.5 - 15.5	+/- 2.4	25	10	-40~85			•	

Triple Gates

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1
74HC4075	triple 3-input OR gate	2.0 - 6.0	+/- 5.2	8	36	-40~125	•		
74HC10	triple 3-input NAND gate	2.0 - 6.0	+/- 5.2	9	36	-40~125	•	•	
74HC11	triple 3-input AND gate	2.0 - 6.0	+/- 5.2	10	36	-40~125	•	•	
74HC27	triple 3-input NOR gate	2.0 - 6.0	+/- 5.2	8	36	-40~125	•	•	•
HEF4073B	triple 3-input AND gate	4.5 - 15.5	+/- 2.4	20	10	-40~85	•		

Quad Gates

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1
74HC00	quad 2-input NAND gate	2.0 - 6.0	+/- 5.2	7	36	-40~125	•	•	•
74HC02	quad 2-input NOR gate	2.0 - 6.0	+/- 5.2	7	36	-40~125	•	•	•
74HC08	quad 2-input AND gate	2.0 - 6.0	+/- 5.2	7	36	-40~125	•	•	•
74HC32	quad 2-input OR gate	2.0 - 6.0	+/- 5.2	6	36	-40~125	•	•	•
74HC86	quad 2-input EXCLUSIVE-OR gate	2.0 - 6.0	+/- 5.2	11	36	-40~125	•	•	
74HC132	quad 2-input NAND gate; Schmitt-trigger	2.0 - 6.0	+/- 5.2	11	36	-40~125	•	•	
74LV00	quad 2-input NAND gate	1.0 - 5.5	+/- 12	7	30	-40~125	•	•	•
74LV02	quad 2-input NOR gate	1.0 - 5.5	+/- 12	6	30	-40~125	•	•	•
74LV08	quad 2-input AND gate	1.0 - 5.5	+/- 12	7	30	-40~125	•	•	
74LV132	quad 2-input NAND gate; Schmitt-trigger	1.0 - 5.5	+/- 12	10	30	-40~125	•	•	•
HEF4001B	quad 2-input NOR gate	4.5 - 15.5	+/- 2.4	20	10	-40~85	•		
HEF4002B	dual 4-input NOR gate	4.5 - 15.5	+/- 2.4	20	10	-40~85	•		
HEF4011B	quad 2-input NAND gate	4.5 - 15.5	+/- 2.4	20	10	-40~85	•		
HEF4030B	quad 2-input EXCLUSIVE-OR gate	4.5 - 15.5	+/- 2.4	30	10	-40~85	•		
HEF4070B	quad 2-input EXCLUSIVE-OR gate	4.5 - 15.5	+/- 2.4	30	10	-40~85	•		
HEF4071B	quad 2-input OR gate	4.5 - 15.5	+/- 2.4	20	10	-40~125	•		
HEF4077B	quad 2-input EXCLUSIVE-NOR gate	4.5 - 15.5	+/- 2.4	30	10	-40~85	•		
HEF4081B	quad 2-input AND gate	4.5 - 15.5	+/- 2.4	20	10	-40~85	•		
HEF4093B	quad 2-input NAND gate; Schmitt-trigger	4.5 - 15.5	+/- 2.4	30	10	-40~125	•		

Quad Latches

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT109-1	SOT403-1
74HC75	quad bistable transparent latch	2.0 - 6.0	+/- 5.2	11		-40~125	•	•
HEF4043B	quad R/S latch with set and reset	4.5 - 15	+/- 2.4	25		-40~85	•	

Octal Latches

Type number	Description	Features					Package (suffix)					
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT109-1	SOT403-1	SOT763-1	SOT163-1	SOT360-1	SOT764-1
74HC259	8 bit addressable latch	2.0 - 6.0	+/- 5.2	18		-40~125	•	•	•			
74HC373	octal D-type transparent latch	2.0 - 6.0	+/- 7.8	12		-40~125				•	•	•
74HC573	octal D-type transparent latch	2.0 - 6.0	+/- 7.8	14		-40~125				•	•	•
HEF40373B	octal D-type transparent latch	4.5 - 15	-50/+62	40		-40~85				•		

Multibyte Latches

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT362-1	SOT364-1
74ALVCH16373	16-bit D-type transparent latch with bus hold	2.3 - 3.6	+/- 24	2,1		-40~85	•	
74ALVCH16843	18-bit D-type transparent latch with bus hold	2.3 - 3.6	+/- 24	2,1		-40~85		•
74ALVCH16841	20-bit D-type transparent latch with bus hold	2.3 - 3.6	+/- 24	2,4		-40~85		•

Dual and Quad Shift Registers

Type number	Description	Features					Package (suffix)
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT109-1
HEF4015B	dual 4-bit serial-in/parallel-out shift register	4.5 - 15	+/- 2.4	40	44	-40~85	•
74HC194	4-bit bidirectional serial-in/parallel-out shift register	2.0 - 6.0	+/- 5.2	14	102	-40~125	•

Octal Shift Registers

Type number	Description	Features					Package (suffix)						
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1	SOT109-1	SOT403-1	SOT763-1	SOT163-1
74HC299	8-bit universal shift register	2.0 - 6.0	+/- 7.8	19	54	-40~125							•
74HC164	8-bit serial-in/parallel-out shift register	2.0 - 6.0	+/- 5.2	12	78	-40~125	•	•	•				
74HC165	8-bit parallel or serial-in/serial-out shift register	2.0 - 6.0	+/- 5.2	16	56	-40~125				•	•	•	
74HC166	8-bit parallel or serial-in/serial-out shift register	2.0 - 6.0	+/- 5.2	15	63	-40~125				•	•		
74HC594	8-bit serial-in/parallel-out shift register	2.0 - 6.0	+/- 7.8	14	109	-40~125				•			
74HC595	8-bit serial-in/parallel-out shift register	2.0 - 6.0	+/- 7.8	16	108	-40~125				•	•	•	
74HC597	8-bit parallel or serial-in/parallel-out shift register	2.0 - 6.0	+/- 5.2	16	108	-40~125				•	•		
74HC4094	8-bit serial-in/serial or parallel-out shift register	2.0 - 6.0	+/- 5.2	15	95	-40~125				•	•		
74LV164	8-bit serial-in/parallel-out shift register	1.0 - 5.5	+/- 12	12	78	-40~125	•	•	•				
74LV165	8-bit parallel or serial-in/serial-out shift register	1.0 - 5.5	+/- 12	18	78	-40~125				•	•		
74LV165A	8-bit parallel or serial-in/serial-out shift register	1.0 - 5.5	+/- 12	7,5	115	-40~125				•	•		
74LV595	8-bit serial-in/parallel-out shift register	1.0 - 3.6	+/- 8	15	77	-40~125				•	•		
74LV4094	8-bit serial-in/serial or parallel-out shift register	1.0 - 3.6	+/- 6	14	95	-40~125				•	•		
HEF4014B	8-bit shift register	4.5 - 15	+/- 2.4	40	40	-40~85				•			
HEF4021B	8-bit shift register	4.5 - 15	+/- 2.4	40	40	-40~85				•	•		
HEF4094B	8-bit serial-in/serial or parallel-out shift register	4.5 - 15	+/- 2.4	50	28	-40~85				•			
HEF4794B	8-bit serial-in/serial or parallel-out shift register	4.5 - 15	-20	45	28	-40~85				•			

Multibyte Shift Registers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT109-1	SOT163-1	SOT360-1
HEF4894B	12-bit serial-in/serial or parallel-out shift register	4.5 - 15	-20	45	28	-40~85		•	•
HEF4557B	1-to-64 bit shift register with variable length	4.5 - 15	+/- 2.4	65	20	-40~85	•		

Octal Transceiver

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1	SOT360-1	SOT764-1
74HC245	octal transceiver	2.0 - 6.0	+/- 7.8	7	36	-40~125	•	•	•
74LV245	octal transceiver	1.0 - 5.5	+/- 16	7	30	-40~125	•	•	

Multibyte Transceiver

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT362-1	SOT364-1
74ALVCH16245	16-bit transceiver with bus hold	1.65 - 3.6	+/- 24	1,9	150	-40~85	•	
74ALVCH16543	16-bit registered transceiver with bus hold	1.65 - 3.6	+/- 24	3,8	150	-40~85		•
74ALVCH16646	16-bit registered transceiver with bus hold	1.65 - 3.6	+/- 24	2,6	150	-40~85		•
74ALVCH16652	16-bit registered transceiver with bus hold	1.65 - 3.6	+/- 24	2,6	150	-40~85		•
74ALVCH16952	16-bit registered transceiver with bus hold	1.65 - 3.6	+/- 24	3,2	150	-40~85		•
74ALVCH162245	16-bit transceiver with bus hold	1.65 - 3.6	+/- 12	2,4	150	-40~85	•	
74ALVCH16500	18-bit universal bus transceiver with bus hold	1.65 - 3.6	+/- 24	2,9	150	-40~85		•
74ALVCH16501	18-bit universal bus transceiver with bus hold	1.65 - 3.6	+/- 24	2,8	150	-40~85		•
74ALVCH16600	18-bit universal bus transceiver with bus hold	1.65 - 3.6	+/- 24	2,8	150	-40~85		•
74ALVCH16601	18-bit universal bus transceiver with bus hold	1.65 - 3.6	+/- 24	2,8	150	-40~85		•
74ALVCH162601	18-bit universal bus transceiver with bus hold	1.65 - 3.6	+/- 12	3,1	150	-40~85		•

3. Low threshold input with clamp diode

Single Buffers

Type number	Description	Features					Package (suffix)
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1
74HCT1G04	single inverter	4.5 - 5.5	+/- 2.0	8	36	-40~125	•
74HCT1G14	single inverter; Schmitt-trigger	4.5 - 5.5	+/- 2.0	15	36	-40~125	•
74HCT1G125	single buffer/line driver	4.5 - 5.5	+/- 2.0	10	36	-40~125	•
74HCT1G126	single buffer/line driver	4.5 - 5.5	+/- 2.0	10	36	-40~125	•

Dual Buffers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT363	SOT765-1	SOT505-2
74HCT2G04	dual inverter	4.5 - 5.5	+/- 4.0	10	36	-40~125	•		
74HCT2G14	dual inverter; Schmitt-trigger	4.5 - 5.5	+/- 4.0	21	36	-40~125	•		
74HCT2G16	dual buffer gate	2.0 - 6.0	+/- 5.2	10	36	-40~125	•		
74HCT2G17	dual buffer; Schmitt-trigger	4.5 - 5.5	+/- 4.0	21	36	-40~125	•		
74HCT2G34	dual buffer	4.5 - 5.5	+/- 4.0	10	36	-40~125	•		
74HCT2G125	dual buffer/line driver	4.5 - 5.5	+/- 4.0	12	36	-40~125		•	•

Triple and Quad Buffers

Type number	Description	Features					Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT765-1	SOT505-2	SOT108-1	SOT402-1
74HCT3G04	triple inverter;	4.5 - 5.5	+/- 4.0	10	36	-40~125	•	•		
74HCT3G14	triple inverter; Schmitt-trigger;	4.5 - 5.5	+/- 4.0	21	36	-40~125	•	•		
74HCT3G16	triple buffer gate	2.0 - 6.0	+/- 5.2	10	36	-40~125				
74HCT3G34	triple buffer	4.5 - 5.5	+/- 4.0	10	36	-40~125	•	•		
74HCT125	quad buffer/line driver	4.5 - 5.5	+/- 6	12	36	-40~125			•	•
74HCT126	quad buffer/line driver	4.5 - 5.5	+/- 6	11	36	-40~125			•	•

Hex Buffers

Type number	Description	Features					Package (suffix)				
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1	SOT109-1	SOT403-1
74HCT04	hex inverter	4.5 - 5.5	+/- 4.0	8	36	-40~125	•	•	•		
74HCT14	hex inverter; Schmitt-trigger	4.5 - 5.5	+/- 4	17	36	-40~125	•	•	•		
74HCT365	hex buffer/line driver	4.5 - 5.5	+/- 6	11	36	-40~125				•	•
74HCT366	hex inverter/line driver	4.5 - 5.5	+/- 6	11	36	-40~125				•	•
74HCT367	hex buffer/line driver	4.5 - 5.5	+/- 6	11	36	-40~125				•	•
74HCT368	hex inverter/line driver	4.5 - 5.5	+/- 6	11	36	-40~125				•	•

Octal Buffers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1	SOT360-1	SOT764-1
74HCT240	octal inverter/line driver	4.5 - 5.5	+/- 6	9	36	-40~125	•	•	•
74HCT241	octal buffer/line driver	4.5 - 5.5	+/- 6	11	36	-40~125	•	•	
74HCT244	octal buffer/line driver	4.5 - 5.5	+/- 6	11	36	-40~125	•	•	•
74HCT540	octal inverter/line driver	4.5 - 5.5	+/- 6	11	36	-40~125	•		
74HCT541	octal buffer/line driver	4.5 - 5.5	+/- 6	12	36	-40~125	•	•	
74HCT7540	octal inverter/line driver; Schmitt-trigger	4.5 - 5.5	+/- 6	16	36	-40~125	•		
74HCT7541	octal buffer/line driver; Schmitt-trigger	4.5 - 5.5	+/- 6	16	36	-40~125	•	•	

Dual Flip Flops

Type number	Description	Features					Package (suffix)				
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1	SOT109-1	SOT403-1
74HCT74	dual D-type flip-flop with set and reset	4.5 - 5.5	+/- 4	15	59	-40~125	•	•	•		
74HCT107	dual J-K flip-flop with reset	4.5 - 5.5	+/- 4	16	73	-40~125	•				
74HCT109	dual J-/K flip-flop with set and reset	4.5 - 5.5	+/- 4	17	61	-40~125				•	•
74HCT112	dual J-K flip-flop with set and reset	4.5 - 5.5	+/- 4	19	70	-40~125				•	•

Quad and Hex Flip Flops

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT109-1	SOT403-1
74HCT173	quad D-type flip-flop	4.5 - 5.5	+/- 6	17	88	-40~125	•	
74HCT175	quad D-type flip-flop with reset	4.5 - 5.5	+/- 4	16	54	-40~125	•	•
74HCT174	hex D-type flip-flop with reset	4.5 - 5.5	+/- 4	18	69	-40~125	•	•

Octal Flip Flops

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1	SOT360-1	SOT764-1
74HCT273	octal D-type flip-flop with reset	4.5 - 5.5	+/- 4	15	36	-40~125	•	•	•
74HCT374	octal D-type flip-flop	4.5 - 5.5	+/- 6	13	48	-40~125	•	•	
74HCT377	octal D-type flip-flop	4.5 - 5.5	+/- 6	14	53	-40~125	•	•	
74HCT574	octal D-type flip-flop	4.5 - 5.5	+/- 6	15	76	-40~125	•	•	

Single Gates

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1	SOT108-1	SOT402-1
74HCT1G00	single 2-input NAND gate	4.5 - 5.5	+/- 2	10	36	-40~125	•		
74HCT1G02	single 2-input NOR gate	4.5 - 5.5	+/- 2.0	9	36	-40~125	•		
74HCT1G08	single 2-input AND gate	4.5 - 5.5	+/- 2	11	36	-40~125	•		
74HCT1G32	single 2-input OR gate	4.5 - 5.5	+/- 2.0	10	36	-40~125	•		
74HCT1G86	single 2-input EXCLUSIVE-OR gate	4.5 - 5.5	+/- 2.0	10	36	-40~125	•		
74HCT30	8-input NAND gate	4.5 - 5.5	+/- 4	12	36	-40~125		•	•

Dual Gates

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT765-1	SOT505-2	SOT108-1
74HCT2G00	dual 2-input NAND gate	4.5 - 5.5	+/- 4	12	36	-40~125	•	•	
74HCT2G02	dual 2-input NOR gate	4.5 - 5.5	+/- 4	12	36	-40~125	•	•	
74HCT2G08	dual 2-Input AND gate	4.5 - 5.5	+/- 4	14	36	-40~125	•	•	
74HCT2G32	dual 2-input OR gate	4.5 - 5.5	+/- 4	13	36	-40~125	•	•	
74HCT2G86	dual 2-input EXCLUSIVE-OR gate	4.5 - 5.5	+/- 4	11	36	-40~125	•		
74HCT20	dual 4-input NAND gate	4.5 - 5.5	+/- 4	13	36	-40~125			•
74HCT4002	dual 4-input NOR gate	4.5 - 5.5	+/- 4	11	36	-40~125			•

Triple Gates

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1
74HCT10	triple 3-input NAND gate	4.5 - 5.5	+/- 4	11	36	-40~125	•	•	
74HCT11	triple 3-input AND gate	4.5 - 5.5	+/- 4	11	36	-40~125	•	•	
74HCT27	triple 3-input NOR gate	4.5 - 5.5	+/- 4	10	36	-40~125	•	•	•
74HCT4075	triple 3-input OR gate	4.5 - 5.5	+/- 4	10	36	-40~125	•		

Quad Gates

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1
74HCT00	quad 2-input NAND gate	4.5 - 5.5	+/- 4	10	36	-40~125	•	•	•
74HCT02	quad 2-input NOR gate	4.5 - 5.5	+/- 4	9	36	-40~125	•	•	•
74HCT08	quad 2-input AND gate	4.5 - 5.5	+/- 4	11	36	-40~125	•	•	•
74HCT32	quad 2-input OR gate	4.5 - 5.5	+/- 4	9	36	-40~125	•	•	•
74HCT86	quad 2-input EXCLUSIVE-OR gate	4.5 - 5.5	+/- 4	14	36	-40~125	•	•	
74HCT132	quad 2-input NAND gate; Schmitt-trigger	4.5 - 5.5	+/- 4	17	36	-40~125	•	•	

Octal Latches

Type number	Description	Features					Package (suffix)					
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT109-1	SOT403-1	SOT763-1	SOT163-1	SOT360-1	SOT764-1
74HCT259	8-Bit addressable latch	4.5 - 5.5	+/- 4	20		-40~125	•	•	•			
74HCT373	octal D-type transparent latch	4.5 - 5.5	+/- 6	14		-40~125				•	•	•
74HCT573	octal D-type transparent latch	4.5 - 5.5	+/- 6	17		-40~125				•	•	•

Octal Shift Registers

Type number	Description	Features					Package (suffix)					
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1	SOT109-1	SOT403-1	SOT763-1
74HCT164	8-bit serial-in/parallel-out shift register	2.0 - 6.0	+/- 5.2	12	78	-40~125	•	•	•			
74HCT165	8-bit parallel or serial-in/serial-out shift register	4.5 - 5.5	+/- 4	14	48	-40~125				•	•	•
74HCT166	8-bit parallel or serial-in/serial-out shift register	4.5 - 5.5	+/- 4.0	23	50	-40~125				•		
74HCT594	8-bit serial-in/parallel-out shift register	4.5 - 5.5	+/- 6	15	100	-40~125				•		
74HCT595	8-bit serial-in/parallel-out shift register	4.5 - 5.5	+/- 6	25	57	-40~125				•	•	•
74HCT597	8-bit parallel or serial-in/parallel-out shift register	4.5 - 5.5	+/- 4	20	83	-40~125				•		
74HCT4094	8-bit serial-in/serial or parallel-out shift register	4.5 - 5.5	+/- 4	19	86	-40~125				•		

Octal Transceivers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1	SOT360-1	SOT764-1
74HCT245	octal transceiver	4.5 - 5.5	+/- 6	10	36	-40~125	•	•	•

4. Standard over-voltage tolerant inputs

Single Buffers

Type number	Description	Features					Package (suffix)			
		V_{CC} (V)	I_o (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1	SOT1226	SOT886	SOT1202
74AHC1GU04	single inverter; unbuffered	2.0 - 5.5	+/- 8	2,6	60	-40~125	•			
74AHC1G04	single inverter	2.0 - 5.5	+/- 8	6,1	60	-40~125	•		•	
74AHC1G14	single inverter; Schmitt-trigger	2.0 - 5.5	+/- 8	3,2	60	-40~125	•			
74AHC1G17	single buffer; Schmitt-trigger	2.0 - 5.5	+/- 8	3,2	60	-40~125	•			
74AHC1G125	single buffer/line driver	2.0 - 5.5	+/- 8	3,4	60	-40~125	•		•	
74AHC1G126	single buffer/line driver	2.0 - 5.5	+/- 8	3,4	60	-40~125	•		•	
74AUP1G04	single inverter	1.1 - 3.6	+/- 1.9	4	70	-40~85	•	•	•	•
74AUP1G14	single inverter; Schmitt-trigger	1.1 - 3.6	+/- 1.9	4,7	70	-40~85	•	•	•	•
74AUP1G16	single buffer/line driver	1.1 - 3.6	+/- 1.9	3,9	70	-40~85	•		•	
74AUP1G17	single buffer; Schmitt-trigger	1.1 - 3.6	+/- 1.9	7,8	70	-40~85	•	•	•	•
74AUP1G34	single buffer	1.1 - 3.6	+/- 1.9	3,9	70	-40~85	•	•	•	•
74AUP1G125	single buffer/line driver	1.1 - 3.6	+/- 1.9	4,3	70	-40~85	•	•	•	•
74AUP1G126	single buffer/line driver	1.1 - 3.6	+/- 1.9	4,3	70	-40~85	•	•	•	•
74AUP1G240	single inverter/line driver	1.1 - 3.6	+/- 1.9	4,2	70	-40~85	•	•	•	•
74AUP1GU04	single inverter; unbuffered	1.1 - 3.6	+/- 1.9	2,3	70	-40~85	•	•	•	•
74AXP1G04	single inverter	0.7 - 2.75	+/- 4.5	2,6	70	-40~85		•	•	•
74AXP1G14	single inverter; Schmitt-trigger	0.7 - 2.75	+/- 4.5	2,9	70	-40~85		•	•	•
74AXP1G17	single buffer; Schmitt trigger	0.7 - 2.75	+/- 4.5	2,8	70	-40~85		•	•	•
74AXP1G125	single buffer/line driver	0.7 - 2.75	+/- 4.5	2,7	70	-40~85		•	•	•
74LVC1G04	single inverter	1.65 - 5.5	+/- 32	2	175	-40~125	•	•	•	•
74LVC1G14	single inverter; Schmitt-trigger	1.65 - 5.5	+/- 32	3	175	-40~125	•	•	•	•
74LVC1G16	single buffer	1.65 - 5.5	+/- 32	4,1	175	-40~125	•		•	
74LVC1G17	single buffer; Schmitt-trigger	1.65 - 5.5	+/- 32	3	175	-40~125	•	•	•	•
74LVC1G34	single buffer	1.65 - 5.5	+/- 32	2	175	-40~125	•	•	•	•
74LVC1G125	single buffer/line driver	1.65 - 5.5	+/- 32	2,1	175	-40~125	•		•	•
74LVC1G126	single buffer/line driver	1.65 - 5.5	+/- 32	2	175	-40~125	•		•	•
74LVC1GU04	single inverter; unbuffered	1.65 - 5.5	+/- 32	1,6	175	-40~125	•	•	•	•
XC7SH04	single inverter	2.0 - 5.5	+/- 8	3,5	60	-40~125	•			
XC7SH14	single inverter; Schmitt-trigger	2.0 - 5.5	+/- 8	3,2	60	-40~125	•			
XC7SH125	single buffer/line driver	2.0 - 5.5	+/- 8	3,4	60	-40~125	•		•	
XC7SHU04	single inverter; unbuffered	2.0 - 5.5	+/- 8	3,5	60	-40~125	•			

Dual Buffers

Type number	Description	Features					Package (suffix)								
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT886	SOT1202	SOT363	SOT1255	SOT765-1	SOT505-2	SOT1203	SOT833-1	SOT1233
74AHC2G125	dual buffer/line driver	2.0 - 5.5	+/- 8	3,4	60	-40~125					•	•			
74AHC2G126	dual buffer/line driver	2.0 - 5.5	+/- 8	3,4	60	-40~125					•	•			
74AHC2G241	dual buffer/line driver	2.0 - 5.5	+/- 8	3,4	60	-40~125					•	•			
74AUP2G04	dual inverter	1.1 - 3.6	+/- 1.9	4	70	-40~85	•	•	•	•					
74AUP2G14	dual inverter; Schmitt-trigger	1.1 - 3.6	+/- 1.9	4,7	70	-40~85	•	•	•	•					
74AUP2G16	dual buffer	1.1 - 3.6	+/- 1.9	3,9	70	-40~85	•		•						
74AUP2G17	dual buffer; Schmitt-trigger	1.1 - 3.6	+/- 1.9	7,8	70	-40~85	•	•	•						
74AUP2G34	dual buffer	1.1 - 3.6	+/- 1.9	3,9	70	-40~85	•	•	•	•					
74AUP2G125	dual buffer/line driver	1.1 - 3.6	+/- 1.9	4,3	70	-40~85					•		•	•	•
74AUP2G126	dual buffer/line driver	1.1 - 3.6	+/- 1.9	4,3	70	-40~85					•		•	•	•
74AUP2G240	dual inverter/line driver	1.1 - 3.6	+/- 1.9	4,2	70	-40~85					•		•	•	
74AUP2G241	dual buffer/line driver	1.1 - 3.6	+/- 1.9	4,3	70	-40~85					•		•	•	
74AUP2GU04	dual inverter; unbuffered	1.1 - 3.6	+/- 1.9	2,3	70	-40~85	•	•	•						
74AXP2G14	dual inverter; Schmitt trigger	0.7 - 2.75	+/- 4.5	2,9	70	-40~85	•	•		•					
74AXP2G17	dual buffer; Schmitt trigger	0.7 - 2.75	+/- 4.5	2,9	70	-40~85	•	•							
74AXP2G34	dual buffer	0.7 - 2.75	+/- 8	2,5	70	-40~85	•	•							
74AXP2G3404	single buffer and single inverter	0.7 - 2.75	+/- 4.5	2,9	70	-40~85	•	•							
74LVC2G04	dual inverter	1.65 - 5.5	+/- 32	2,7	175	-40~125	•	•	•	•					
74LVC2G14	dual inverter; Schmitt-trigger	1.65 - 5.5	+/- 32	3,9	175	-40~125	•	•	•						
74LVC2G16	dual buffer gate	1.65 - 5.5	+/- 24	2,2	175	-40~125	•		•						
74LVC2G17	dual buffer; Schmitt-trigger	1.65 - 5.5	+/- 32	3,6	175	-40~125	•	•	•						
74LVC2G34	dual buffer	1.65 - 5.5	+/- 32	2,2	175	-40~125	•	•	•	•					
74LVC2G125	dual buffer/line driver	1.65 - 5.5	+/- 32	2,3	175	-40~125					•	•	•	•	
74LVC2G126	dual buffer/line driver	1.65 - 5.5	+/- 32	2,4	175	-40~125					•	•	•	•	
74LVC2G240	dual inverter/line driver	1.65 - 5.5	+/- 32	2,5	175	-40~125					•	•	•	•	
74LVC2G241	dual buffer/line driver	1.65 - 5.5	+/- 32	2,6	175	-40~125					•	•	•	•	
74LVC2GU04	dual inverter; unbuffered	1.65 - 5.5	+/- 32	2,3	175	-40~125	•	•	•						
XC7WH126	dual buffer/line driver	2.0 - 5.5	+/- 8	3,4	60	-40~125					•	•			

Triple Buffers

Type number	Description	Features					Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT765-1	SOT505-2	SOT1203	SOT833-1
74AHC3GU04	triple inverter; unbuffered	2.0 - 5.5	+/- 8	2,5	60	-40~125	•	•		
74AHC3G04	triple inverter	2.0 - 5.5	+/- 8	3,1	60	-40~125	•	•		
74AHC3G14	triple inverter; Schmitt-trigger	2.0 - 5.5	+/- 8	3,2	60	-40~125	•	•		•
74AUP3G04	triple inverter	1.1 - 3.6	+/- 1.9	4	70	-40~85	•		•	•
74AUP3G14	triple inverter; Schmitt-trigger	1.1 - 3.6	+/- 1.9	4,7	70	-40~85	•		•	•
74AUP3G16	triple buffer	1.1 - 3.6	+/- 1.9	3,9	70	-40~85	•			
74AUP3G17	triple buffer; Schmitt-trigger	1.1 - 3.6	+/- 1.9	4,7	70	-40~85	•		•	•
74AUP3G34	triple buffer	1.1 - 3.6	+/- 1.9	3,9	70	-40~85	•		•	•
74LVC3G04	triple inverter	1.65 - 5.5	+/- 32	2,7	175	-40~125	•	•	•	•
74LVC3G14	triple inverter; Schmitt-trigger	1.65 - 5.5	+/- 32	3,2	175	-40~125	•	•	•	•
74LVC3G16	triple buffer	1.65 - 5.5	+/- 24	1,9	175	-40~125		•		
74LVC3G17	triple buffer; Schmitt-trigger	1.65 - 5.5	+/- 32	3,6	175	-40~125	•	•	•	•
74LVC3G34	triple buffer	1.65 - 5.5	+/- 32	2,2	175	-40~125	•	•	•	•
74LVC3GU04	triple inverter; unbuffered	1.65 - 5.5	+/- 32	2,3	175	-40~125	•	•	•	•
XC7WH14	triple inverter; Schmitt-trigger	2.0 - 5.5	+/- 8	3,2	60	-40~125	•	•		•

Quad Buffers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1
74AHC125	quad buffer/line driver	2.0 - 5.5	+/- 8	3	60	-40~125	•	•	•
74AHC126	quad buffer/line driver	2.0 - 5.5	+/- 8	3,3	60	-40~125	•	•	•
74ALVC125	quad buffer/line driver	1.65 - 3.6	+/- 24	1,8	145	-40~85	•	•	•
74LVC125A	quad buffer/line driver	1.2 - 3.6	+/- 24	2,4	175	-40~125	•	•	•
74LVC126A	quad buffer/line driver	1.2 - 3.6	+/- 24	2,4	175	-40~125	•	•	•
74LVT126	quad buffer/line driver with bus hold	2.7 - 3.6	-32 / +64	2,4	150	-40~125	•	•	•
74LVT125	quad buffer/line driver with bus hold	2.7 - 3.6	-32 / +64	2,9	150	-40~125	•	•	•
74LVTH125	quad buffer/line driver with bus hold	2.7 - 3.6	-32 / +64	2,9	150	-40~125	•	•	•
74VHC125	quad buffer/line driver	2.0 - 5.5	+/- 8	3	60	-40~125	•	•	•
74VHC126	quad buffer/line driver	2.0 - 5.5	+/- 8	3,3	60	-40~125	•	•	•

Hex Buffers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1
74AHC04	hex inverter	2.0 - 5.5	+/- 8	3	60	-40~125	•	•	•
74AHC14	hex inverter; Schmitt-trigger	2.0 - 5.5	+/- 8	3,2	60	-40~125	•	•	•
74AHCU04	hex inverter; unbuffered	2.0 - 5.5	+/- 8	2,4	60	-40~125	•	•	•
74AHCV14A	hex inverter; Schmitt-trigger	1.8 - 5.5	+/- 16	3,2	60	-40~125		•	
74AHCV17A	hex buffer; Schmitt-trigger	1.8 - 5.5	+/- 16	3,2	60	-40~125		•	
74ALVC04	hex inverter	1.65 - 3.6	+/- 24	2	150	-40~85	•	•	•
74ALVC14	hex inverter; Schmitt-trigger	1.65 - 3.6	+/- 24	2,4	150	-40~85	•	•	•
74LV14A	hex inverter; Schmitt-trigger	2.0 - 5.5	+/- 12	3,4	60	-40~125		•	
74LV17A	hex inverter	2.0 - 5.5	+/- 12	5,1	60	-40~125		•	
74LVC04A	hex inverter	1.65 - 5.5	+/- 24	2	175	-40~125	•	•	•
74LVC14A	hex inverter; Schmitt-trigger	1.2 - 3.6	+/- 24	3,2	175	-40~125	•	•	•
74LVCU04A	hex inverter; unbuffered	1.2 - 3.6	+/- 24	2	175	-40~125	•	•	•
74LVT04	hex inverter	2.7 - 3.6	-20 / +32	2,6	150	-40~125	•	•	
74LVT14	hex inverter; Schmitt-trigger	2.7 - 3.6	-32/+64	3,8	150	-40~125	•	•	•
74VHC14	hex inverter; Schmitt-trigger	2.0 - 5.5	+/- 8	3,2	60	-40~125	•	•	•

Octal Buffers

Type number	Description	Features					Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1	SOT360-1	SOT764-1	SOT362-1
74AHC244	octal buffer/line driver	2.0 - 5.5	+/- 8	3,5	60	-40~125	•	•	•	
74AHC541	octal buffer/line driver	2.0 - 5.5	+/- 8	3,5	60	-40~125	•	•	•	
74AHCV244A	octal buffer/line driver; Schmitt-trigger	1.8 - 5.5	+/- 16	3	60	-40~125		•		
74AHCV541A	octal buffer/line driver; Schmitt-trigger	1.8 - 5.5	+/- 16	3	60	-40~125		•	•	
74ALVC244	octal buffer/line driver	1.65 - 3.6	+/- 24	2,9	130	-40~85	•	•	•	
74ALVC541	octal buffer/line driver	1.65 - 3.6	+/- 24	2,3	130	-40~85	•	•	•	
74LV244A	octal buffer/line driver	2.0 - 5.5	+/- 16	2,9	60	-40~125		•		
74LV540A	octal inverter/line driver	2.0 - 5.5	+/- 16	3,1	60	-40~125		•		
74LV541A	octal buffer/line driver	2.0 - 5.5	+/- 16	2,9	60	-40~125		•		
74LVC240A	octal inverter/line driver	1.2 - 3.6	+/- 24	3,5	175	-40~125	•	•	•	
74LVC541A	octal buffer/line driver	1.2 - 3.6	+/- 24	3,3	175	-40~125	•	•	•	
74LVC2244A	octal buffer/line driver	1.2 - 3.6	+/- 12	3,1	175	-40~125	•	•	•	
74LVC244A	octal buffer/line driver	1.2 - 3.6	+/- 24	2,8	175	-40~125	•	•	•	
74LVCH244A	octal buffer/line driver with bus hold	1.2 - 3.6	+/- 24	2,8	175	-40~125	•	•	•	
74LVT240	octal inverter/line driver with bus hold	2.7 - 3.6	-32 / +64	2,5	150	-40~125	•	•		
74LVT241	octal buffer/line driver with bus hold	2.7 - 3.6	-32 / +64	2,8	150	-40~125	•	•	•	
74LVT2241	octal buffer/line driver with bus hold	2.7 - 3.6	+/- 12	3,3	150	-40~125	•	•		
74LVT2244	octal buffer/line driver with bus hold	2.7 - 3.6	+/- 12	2,9	150	-40~125	•	•		
74LVT244A	octal buffer/line driver with bus hold	2.7 - 3.6	-32 / +64	2,6	150	-40~125	•	•	•	
74LVTH244A	octal buffer/line driver with bus hold	2.7 - 3.6	-32 / +64	2,6	150	-40~125	•	•	•	
74LVT244B	octal buffer/line driver with bus hold	2.7 - 3.6	-32 / +64	2	150	-40~125	•	•		
74LVTH244B	octal buffer/line driver with bus hold	2.7 - 3.6	-32 / +64	2	150	-40~125	•	•		
74LVTN16244B	16-bit buffer/line driver	2.7 - 3.6	-32 / +64	1,8	150	-40~125				•
74VHC244	octal inverter/line driver	2.0 - 5.5	+/- 8	3,5	60	-40~125	•	•	•	
74VHC541	octal buffer/line driver	2.0 - 5.5	+/- 8	3,5	60	-40~125	•	•	•	

Multibyte Buffers

Type number	Description	Features					Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT137-1	SOT355-1	SOT362-1	SOT364-1
74LVC827	10-bit buffer/line driver	1.2 - 3.6	+/- 24	4	175	-40~125	•			
74LVC827A	10-bit buffer/line driver	1.2 - 3.6	+/- 24	4	175	-40~125		•		
74ALVC16244	16-bit buffer/line driver	1.2 - 3.6	+/- 24	1,9	150	-40~85			•	
74ALVT16244	16-bit buffer/line driver with bus hold	2.3 - 3.6	-32 / +64	1,5	200	-40~85			•	
74AVC16244	16-bit buffer/line driver	0.8 - 3.6	+/- 12	2	200	-40~85			•	
74AVCH16244	16-bit buffer/line driver with bus hold	0.8 - 3.6	+/- 12	2	200	-40~85			•	
74LVC16240A	16-bit inverter/line driver	1.2 - 3.6	+/- 24	2,7	175	-40~125			•	
74LVC16241A	16-bit buffer/line driver	1.2 - 3.6	+/- 24	2,9	175	-40~125			•	
74LVC16244A	16-bit buffer/line driver	1.2 - 3.6	+/- 24	3	175	-40~125			•	
74LVCH16244A	16-bit buffer/line driver with bus hold	1.2 - 3.6	+/- 24	3	175	-40~125			•	
74LVC162244A	16-bit buffer/line driver	1.2 - 3.6	+/- 24	2,9	175	-40~125			•	
74LVCH162244A	16-bit buffer/line driver with bus hold	1.2 - 3.6	+/- 12	2,9	175	-40~125			•	
74LVCH16541A	16-bit buffer/line driver with bus hold	1.2 - 3.6	+/- 24	2,7	175	-40~125			•	
74LVT16240A	16-bit inverter/line driver with bus hold	2.7 - 3.6	-32 / +64	2	150	-40~125			•	
74LVT162240A	16-bit inverter/line driver with bus hold	2.7 - 3.6	+/- 12	2,6	150	-40~125			•	
74LVT162244B	16-bit buffer/line driver with bus hold	2.7 - 3.6	+/- 12	2,8	150	-40~125			•	
74LVT16244B	16-bit buffer/line driver with bus hold	2.7 - 3.6	-32 / +64	1,8	150	-40~125			•	
74LVTH16244B	16-bit buffer/line driver with bus hold	2.7 - 3.6	-32 / +64	1,8	150	-40~125			•	
74ALVT16827	20-bit buffer/line driver with bus hold	2.3 - 3.6	-32 / +64	1,3	200	-40~85				•
74ALVT162827	20-bit buffer/line driver with bus hold	2.3 - 3.6	+/- 12	2,2	75	-40~85				•

Multibyte Drivers

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT362-1	SOT364-1
74ALVC162334A	16-bit registered driver	1.65 - 3.6	+/- 24	6		-40~85	•	
74ALVC16834A	18-bit registered driver	1.65 - 3.6	+/- 24	4		-40~85		•
74ALVC16835A	18-bit registered driver	1.65 - 3.6	+/- 24	4		-40~85		•
74ALVC162834A	18-bit registered driver	1.65 - 3.6	+/- 24	6		-40~85		•
74ALVC162835A	18-bit registered driver	1.65 - 3.6	+/- 24	6		-40~85		•
74ALVT162823	18-bit buffer/line driver with bus hold	2.3 - 3.6	+/- 12	3	150	-40~85		•
74AVC16834A	18-bit registered driver	1.2 - 3.6	+/- 12	2		-40~85		•
74AVC16835A	18-bit registered driver	1.2 - 3.6	+/- 12	2		-40~85		•
74ALVC16836A	20-bit registered driver	1.65 - 3.6	+/- 24	4		-40~85		•
74ALVC162836A	20-bit registered driver	1.65 - 3.6	+/- 24	6		-40~85		•
74AVC16836A	20-bit registered driver	1.2 - 3.6	+/- 12	2		-40~85		•

Single Flip Flops

Type number	Description	Features					Package (suffix)							
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1	SOT1226	SOT886	SOT1202	SOT833-1	SOT765-1	SOT505-2	SOT1203
74AHC1G79	single D-type flip-flop	2.0 - 5.5	+/- 8	3,5	90	-40~125	•							
74AUP1G74	single D-type flip-flop with set and reset	1.1 - 3.6	+/- 1.9	9,2	400	-40~125					•		•	•
74AUP1G79	single D-type flip-flop	1.1 - 3.6	+/- 1.9	9,1	400	-40~125	•	•	•	•				
74AUP1G80	single D-type flip-flop	1.1 - 3.6	+/- 1.9	9,1	400	-40~125	•		•	•				
74AUP1G175	single D flip-flop with reset	1.1 - 3.6	+/- 1.9	7,4	70	-40~125			•	•				
74AUP1G374	single D-type flip-flop	1.1 - 3.6	+/- 1.9	7,9	400	-40~125			•	•				
74LVC1G74	single D-type flip-flop with set and reset	1.65 - 5.5	+/- 32	3,5	280	-40~125					•	•	•	•
74LVC1G79	single D-type flip-flop	1.65 - 5.5	+/- 32	2,2	450	-40~125	•	•	•	•				
74LVC1G80	single D-type flip-flop	1.65 - 5.5	+/- 32	2,4	450	-40~125	•	•	•	•				
74LVC1G175	single D flip-flop with reset	1.65 - 5.5	+/- 32	3,1	300	-40~125			•	•				
74LVC2G74	single D-type flip-flop with set and reset	1.65 - 5.5	+/- 32	3,5	280	-40~125					•	•	•	•

Dual Flip Flops

Type number	Description	Features					Package (suffix)					
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT765-1	SOT1203	SOT833-1	SOT108-1	SOT402-1	SOT762-1
74AHC74	dual D-type flip-flop with set and reset	2.0 - 5.5	+/- 8	3,7	170	-40~125				•	•	•
74ALVC74	dual D-type flip-flop with set and reset	1.65 - 3.6	+/- 24	2,3	425	-40~85				•	•	•
74AUP2G79	dual D-type flip-flop	1.1 - 3.6	+/- 1.9	8,5	400	-40~125	•	•	•			
74AUP2G80	dual D-type flip-flop	1.1 - 3.6	+/- 1.9	9,1	400	-40~125	•	•	•			
74LVC74A	dual D-type flip-flop with set and reset	1.2 - 3.6	+/- 24	2,5	250	-40~125				•	•	•

Octal Flip Flops

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1	SOT360-1	SOT764-1
74AHC273	octal D-type flip-flop with reset	2.0 - 5.5	+/- 8	4,2	165	-40~125	•	•	•
74AHC374	octal D-type flip-flop	2.0 - 5.5	+/- 8	4,4	185	-40~125	•	•	
74AHC377	octal D-type flip-flop with data enable	2.0 - 5.5	+/- 8	3,9	175	-40~125	•	•	
74AHC574	octal D-type flip-flop	2.0 - 5.5	+/- 8	4,4	130	-40~125	•	•	•
74ALVC374	octal D-type flip-flop	1.65 - 3.6	+/- 24	2,5	300	-40~85	•	•	•
74ALVC574	octal D-type flip-flop	1.65 - 3.6	+/- 24	2,5	300	-40~85	•	•	•
74LVC273	octal D-type flip-flop with reset	1.2 - 3.6	+/- 24	6	230	-40~125	•	•	•
74LVC374A	octal D-type flip-flop	1.2 - 3.6	+/- 24	2,7	100	-40~125	•	•	•
74LVC377	octal D-type flip-flop with data enable	1.2 - 3.6	+/- 24	6	230	-40~125	•	•	
74LVC574A	octal D-type flip-flop	1.2 - 3.6	+/- 24	3,2	150	-40~125	•	•	•

Multibyte Flip Flops

Type number	Description	Features					Package (suffix)				
		V_{cc} (V)	I_o (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT137-1	SOT355-1	SOT815-1	SOT362-1	SOT364-1
74LVC823A	9-bit D-type flip-flop	1.2 - 3.6	+/- 24	5,4	150	-40~125	•	•	•		
74AVC16374	16-bit D-type flip-flop	1.2 - 3.6	+/- 12	1,5	350	-40~85				•	
74LVC16374A	16-bit D-type flip-flop	1.2 - 3.6	+/- 24	3,8	150	-40~125				•	
74LVCH16374A	16-bit D-type flip-flop with bus hold	1.2 - 3.6	+/- 24	3,8	150	-40~125				•	
74LVCH162374A	16-bit D-type flip-flop with bus hold	1.2 - 3.6	+/- 24	3,8	150	-40~125				•	
74LVT162374	16-bit D-type flip-flop with bus hold	2.7 - 3.6	+/- 12	3	150	-40~85				•	
74LVT16374A	16-bit D-type flip-flop with bus hold	2.7 - 3.6	-32/+64	3	150	-40~85				•	
74LVTH16374A	16-bit D-type flip-flop with bus hold	2.7 - 3.6	-32/+64	3	150	-40~85				•	
74ALVT16823	18-bit D-type flip-flop with bus hold	2.3 - 3.6	-32/+64	1,9	250	-40~85					•
74ALVT16821	20-bit D-type flip-flop	2.3 - 3.6	-32/+64	1,8	150	-40~85					•
74ALVT162821	20-bit D-type flip-flop	2.3 - 3.6	+/- 12	3,2	150	-40~85					•

Single Gates

Type number	Description	Features					Package (suffix)											
		V_{cc} (V)	I_o (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1	SOT1226	SOT886	SOT1202	SOT363	SOT1255	SOT765-1	SOT505-2	SOT1203	SOT833-1	SOT1174-1	SOT108-1	SOT402-1	SOT762-1
74AHC1G00	single 2-input NAND gate	2.0 - 5.5	+/- 8	3,5	60	-40~125	•													
74AHC1G02	single 2-input NOR gate	2.0 - 5.5	+/- 8	3,2	60	-40~125	•													
74AHC1G08	single 2-input AND gate	2.0 - 5.5	+/- 8	3,2	60	-40~125	•													
74AHC1G32	single 2-input OR gate	2.0 - 5.5	+/- 8	3,2	60	-40~125	•													
74AHC1G86	2-input EXCLUSIVE-OR gate	2.0 - 5.5	+/- 8	3,4	60	-40~125	•													
74AHC30	8-input NAND gate	2.0 - 5.5	+/- 8	3,6	60	-40~125											•	•	•	•
74AUP1G00	single 2-input NAND gate	1.1 - 3.6	+/- 1.9	8,3	70	-40~125	•	•	•	•										
74AUP1G02	single 2-input NOR gate	1.1 - 3.6	+/- 1.9	8,3	70	-40~125	•	•	•	•										
74AUP1G08	single 2-input AND gate	1.1 - 3.6	+/- 1.9	8,2	70	-40~125	•	•	•	•										
74AUP1G11	single 3-input AND gate	1.1 - 3.6	+/- 1.9	6,9	70	-40~125			•	•	•									
74AUP1G32	single 2-input OR gate	1.1 - 3.6	+/- 1.9	7,9	70	-40~125	•	•	•	•										
74AUP1G57	configurable gate; Schmitt trigger	1.1 - 3.6	+/- 1.9	8,7	70	-40~125			•	•	•	•								
74AUP1G58	configurable gate; Schmitt trigger	1.1 - 3.6	+/- 1.9	8,7	70	-40~125			•	•	•	•								
74AUP1G86	single 2-input EXCLUSIVE-OR gate	1.1 - 3.6	+/- 1.9	9	70	-40~125	•	•	•	•										
74AUP1G97	configurable gate; Schmitt trigger	1.1 - 3.6	+/- 1.9	8,7	70	-40~125			•	•	•	•								
74AUP1G98	configurable gate; Schmitt trigger	1.1 - 3.6	+/- 1.9	8,9	70	-40~125			•	•	•	•								

Single Gates (continued)

Type number	Description	Features					Package (suffix)												
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1	SOT1226	SOT886	SOT1202	SOT363	SOT1255	SOT765-1	SOT505-2	SOT1203	SOT833-1	SOT1174-1	SOT108-1	SOT402-1	SOT762-1
74AUP1G132	single 2-input NAND gate Schmitt-trigger	1.1 - 3.6	+/- 1.9	10	70	-40~125	•	•	•	•										
74AUP1G332	single 3-input OR gate	1.1 - 3.6	+/- 1.9	6,8	70	-40~125			•	•	•									
74AUP1G386	single 3-input EXCLU-SIVE-OR gate	1.1 - 3.6	+/- 1.9	8,6	70	-40~125			•	•	•									
74AUP1G885	dual function gate	1.1 - 3.6	+/- 1.9	7,6	70	-40~125							•		•	•				
74AUP1G0832	single 3-input AND-OR gate	1.1 - 3.6	+/- 1.9	6,7	70	-40~125			•	•	•									
74AUP1G3208	single 3-input OR-AND gate	1.1 - 3.6	+/- 1.9	7,4	70	-40~125			•	•	•	•								
74AUP1Z04	crystal driver with enable and internal resistor	1.1 - 3.6	+/- 1.9	5,6	70	-40~125			•	•	•									
74AUP1Z125	crystal driver with enable and internal resistor	1.1 - 3.6	+/- 1.9	4,7	70	-40~125			•	•	•									
74AXP1G00	single 2-input NAND gate	0.7 - 2.75	+/- 4.5	2,7	70	-40~85		•	•	•										
74AXP1G02	single 2-input NOR gate	0.7 - 2.75	+/- 4.5	2,6	70	-40~85		•	•	•										
74AXP1G08	single 2-input AND gate	0.7 - 2.75	+/- 4.5	2,6	70	-40~85		•	•	•										
74AXP1G10	single 3-input NAND gate	0.7 - 2.75	+/- 4.5	2,6	70	-40~85			•	•										
74AXP1G11	single 3-input AND gate	0.7 - 2.75	+/- 4.5	2,6	70	-40~85			•	•										
74AXP1G32	single 2-input OR gate	0.7 - 2.75	+/- 4.5	2,5	70	-40~85		•	•	•										
74AXP1G57	configurable gate; Schmitt trigger	0.7 - 2.75	+/- 4.5	4,6	70	-40~85			•	•		•								
74AXP1G58	configurable gate; Schmitt trigger	0.7 - 2.75	+/- 4.5	4,5	70	-40~85			•	•		•								
74AXP1G86	single 2-input Exclu-sive-OR gates	0.7 - 2.75	+/- 4.5	4,5	70	-40~85		•	•	•										
74AXP1G97	configurable gate; Schmitt trigger	0.7 - 2.75	+/- 4.5	4,5	70	-40~85			•	•		•								
74AXP1G98	configurable gate; Schmitt trigger	0.7 - 2.75	+/- 4.5	4,5	70	-40~85			•	•										
74LVC1G00	single 2-input NAND gate	1.65 - 5.5	+/- 32	2,2	175	-40~125	•	•	•	•										
74LVC1G02	single 2-input NOR gate	1.65 - 5.5	+/- 32	2,1	150	-40~125	•	•	•	•										
74LVC1G08	single 2-input AND gate	1.65 - 5.5	+/- 24	2,1	150	-40~125	•	•	•	•										
74LVC1G10	single 3-input NAND gate	1.65 - 5.5	+/- 32	2,6	175	-40~125			•	•	•									
74LVC1G11	single 3-input AND gate	1.65 - 5.5	+/- 32	2,6	175	-40~125			•	•	•	•								
74LVC1G27	single 3-input NOR gate	1.65 - 5.5	+/- 32	2,6	150	-40~125			•	•	•									
74LVC1G32	single 2-input OR gate	1.65 - 5.5	+/- 32	2,1	150	-40~125	•	•	•	•										
74LVC1G57	configurable gate; Schmitt trigger	1.65 - 5.5	+/- 32	6,3	150	-40~125			•	•	•									
74LVC1G58	configurable gate; Schmitt trigger	1.65 - 5.5	+/- 32	6,3	150	-40~125			•	•	•									
74LVC1G86	single 2-input EXCLU-SIVE-OR gate	1.65 - 5.5	+/- 32	2,4	150	-40~125	•	•	•	•										
74LVC1G97	configurable gate; Schmitt trigger	1.65 - 5.5	+/- 32	6,3	150	-40~125			•	•	•	•								
74LVC1G98	configurable gate; Schmitt trigger	1.65 - 5.5	+/- 32	6,3	150	-40~125			•	•	•									
74LVC1G99	configurable gate; Schmitt trigger	1.65 - 5.5	+/- 32	8,4	150	-40~125								•	•	•				
74LVC1G332	single 3-input OR gate	1.65 - 5.5	+/- 32	2,6	150	-40~125			•	•	•	•								
74LVC1G386	single 3-Input EXCLU-SIVE-OR gate	1.65 - 5.5	+/- 32	4,5	150	-40~125					•									

Single Gates (continued)

Type number	Description	Features					Package (suffix)												
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1	SOT1226	SOT886	SOT1202	SOT363	SOT1255	SOT765-1	SOT505-2	SOT1203	SOT833-1	SOT1174-1	SOT108-1	SOT402-1	SOT762-1
74LVC1GX04	crystal driver	1.65 - 5.5	+/- 24	2,8	150	-40~125					•									
74LVC30A	8-input NAND gate	1.65 - 5.5	+/- 24	3,6	175	-40~125												•	•	•
XC7SH02	single 2-input NOR gate	2.0 - 5.5	+/- 8	3,2	60	-40~125	•													
XC7SH08	single 2-input AND gate	2.0 - 5.5	+/- 8	3,2	60	-40~125	•													
XC7SH32	single 2-input OR gate	2.0 - 5.5	+/- 8	3,2	60	-40~125	•													
XC7SH86	2-input EXCLUSIVE-OR gate	2.0 - 5.5	+/- 8	3,4	60	-40~125	•													

Dual Gates

Type number	Description	Features					Package (suffix)										
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT886	SOT1202	SOT363	SOT765-1	SOT505-2	SOT1203	SOT833-1	SOT1233	SOT552-1	SOT1081-2	SOT1160-1
74AHC2G00	dual 2-input NAND gate	2.0 - 5.5	+/- 8	3,5	60	-40~125				•	•						
74AHC2G08	dual 2-input AND gate	2.0 - 5.5	+/- 8	3,2	60	-40~125				•	•						
74AHC2G32	dual 2-input OR gate	2.0 - 5.5	+/- 8	3,2	60	-40~125				•	•						
74AUP2G00	dual 2-input NAND gate	1.1 - 3.6	+/- 1.9	8,3	70	-40~125				•		•	•	•			
74AUP2G02	dual 2-input NOR gate	1.1 - 3.6	+/- 1.9	8,3	70	-40~125				•		•	•				
74AUP2G08	dual 2-input AND gate	1.1 - 3.6	+/- 1.9	8,2	70	-40~125				•		•	•	•			
74AUP2G32	dual 2-input OR gate	1.1 - 3.6	+/- 1.9	7,9	70	-40~125				•		•	•				
74AUP2G57	configurable multiple function gate	1.1 - 3.6	+/- 1.9	8,7	70	-40~125									•	•	•
74AUP2G58	dual configurable gate; Schmitt trigger	1.1 - 3.6	+/- 1.9	8,7	70	-40~125									•	•	•
74AUP2G86	dual 2-input EXCLUSIVE-OR gate	1.1 - 3.6	+/- 1.9	9	70	-40~125				•		•	•				
74AUP2G97	dual configurable gate; Schmitt trigger	1.1 - 3.6	+/- 1.9	8,7	70	-40~125									•	•	•
74AUP2G98	dual configurable gate; Schmitt trigger	1.1 - 3.6	+/- 1.9	8,9	70	-40~125									•	•	•
74AUP2G132	dual 2-input NAND gate Schmitt-trigger	1.1 - 3.6	+/- 1.9	10	70	-40~125				•		•	•				
74AUP2G3404	buffer and inverter	1.1 - 3.6	+/- 1.9	4	70	-40~125	•	•	•								
74AUP2T1326	dual supply buffer/line driver	1.1 - 3.6	+/- 1.9	3,8	70	-40~125										•	
74LVC2G00	dual 2-input NAND gate	1.65 - 5.5	+/- 32	2,2	175	-40~125				•	•	•	•	•			
74LVC2G02	dual 2-input NOR gate	1.65 - 5.5	+/- 32	2,4	150	-40~125				•	•	•	•				
74LVC2G08	dual 2-input AND gate	1.65 - 5.5	+/- 24	2,1	150	-40~125				•	•	•	•	•			
74LVC2G32	dual 2-input OR gate	1.65 - 5.5	+/- 32	2,2	150	-40~125				•	•	•	•				
74LVC2G86	dual 2-input EXCLUSIVE-OR gate	1.65 - 5.5	+/- 32	2,3	150	-40~125				•	•	•	•				

Triple Gates

Type number	Description	Features					Package (suffix)					
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT765-1	SOT1203	SOT833-1	SOT108-1	SOT402-1	SOT762-1
74AUP3G0434	dual inverter and single buffer	1.1 - 3.6	+/- 1.9	4	70	-40~125	•	•	•			
74AUP3G3404	dual buffer and single inverter	1.1 - 3.6	+/- 1.9	4	70	-40~125	•	•	•			
74LVC10A	triple 3-input NAND gate	1.2 - 3.6	+/- 24	3,9	150	-40~125				•	•	•
74LVC11	triple 3-input AND gate	1.2 - 3.6	+/- 24	3,7	150	-40~125				•	•	•

Quad Gates

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1
74AHC00	quad 2-input NAND gate	2.0 - 5.5	+/- 8	3,2	60	-40~125	•	•	•
74AHC02	quad 2-input NOR gate	2.0 - 5.5	+/- 8	2,9	60	-40~125	•	•	•
74AHC08	quad 2-input AND gate	2.0 - 5.5	+/- 8	3,5	60	-40~125	•	•	•
74AHC32	quad 2-input OR gate	2.0 - 5.5	+/- 8	3,5	60	-40~125	•	•	•
74AHC86	quad 2-input EXCLUSIVE-OR gate	2.0 - 5.5	+/- 8	3,4	60	-40~125	•	•	•
74AHC132	quad 2-input NAND gate; Schmitt-trigger	2.0 - 5.5	+/- 8	3,3	60	-40~125	•	•	•
74ALVC00	quad 2-input NAND gate	1.65 - 3.6	+/- 24	2,1	145	-40~85	•	•	•
74ALVC02	quad 2-input NOR gate	1.65 - 3.6	+/- 24	2,2	150	-40~85	•	•	•
74ALVC08	quad 2-input AND gate	1.65 - 3.6	+/- 24	2	150	-40~85	•	•	•
74ALVC32	quad 2-input OR gate	1.65 - 3.6	+/- 24	2	150	-40~85	•	•	•
74LVC00A	quad 2-input NAND gate	1.2 - 3.6	+/- 24	2,1	150	-40~125	•	•	•
74LVC02A	quad 2-input NOR gate	1.2 - 3.6	+/- 24	2,1	150	-40~125	•	•	•
74LVC08A	quad 2-input AND gate	1.2 - 3.6	+/- 24	2,1	150	-40~125	•	•	•
74LVC32A	quad 2-input OR gate	1.2 - 3.6	+/- 24	2,1	150	-40~125	•	•	•
74LVC86A	quad 2-input EXCLUSIVE-OR gate	1.2 - 3.6	+/- 24	3	150	-40~125	•	•	•
74LVC132A	quad 2-input NAND gate; Schmitt-trigger	1.2 - 3.6	+/- 24	3,4	175	-40~125	•	•	•
74LVT02	quad 2-input NOR gate	2.7 - 3.6	-32/+64	2,8	150	-40~85	•	•	
74LVT08	quad 2-input AND gate	2.7 - 3.6	-32/+64	3,4	150	-40~85	•	•	
74VHC02	quad 2-input NOR gate	2.0 - 5.5	+/- 8	2,9	60	-40~125	•	•	•
74VHC08	quad 2-input AND gate	2.0 - 5.5	+/- 8	3,5	60	-40~125	•	•	•
74VHC32	quad 2-input OR gate	2.0 - 5.5	+/- 8	3,5	60	-40~125	•	•	•

Single Latches

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT886	SOT1202	SOT363
74AUP1G373	single D-type transparent latch	1.1 - 3.6	1.9/-1.9	8,5		-40~125	•	•	•

Octal Latches

Type number	Description	Features					Package (suffix)
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT362-1
74AVC16334A	16-bit registered driver	1.2 - 3.6	+/- 12	2		-40~85	•
74AVC16373	16-bit D-type transparent latch	1.2 - 3.6	+/- 12	2		-40~85	•
74AVC16373	16-bit D-type transparent latch	1.2 - 3.6	+/- 12	2		-40~85	•
74LVC16373A	16-bit D-type transparent latch	1.2 - 3.6	+/- 24	3		-40~125	•
74LVCH16373A	16-bit D-type transparent latch with bus hold	1.2 - 3.6	+/- 24	3		-40~125	•
74LVC162373A	16-bit D-type transparent latch	1.2 - 3.6	+/- 12	3,2		-40~125	•
74LVCH162373A	16-bit D-type transparent latch with bus hold	1.2 - 3.6	+/- 24	3,2		-40~125	•
74LVT16373A	16-bit D-type transparent latch with bus hold	2.7 - 3.6	-32/+64	1,9		-40~85	•
74LVT162373	16-bit D-type transparent latch with bus hold	2.7 - 3.6	+/- 12	2,5		-40~85	•

Octal Shift Registers

Type number	Description	Features					Package (suffix)					
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1	SOT109-1	SOT403-1	SOT763-1
74AHC164	8-bit serial-in/parallel-out shift register	2.0 - 5.5	+/- 8	4,5	115	-40~125	•	•	•			
74AHC594	8-bit serial-in/parallel-out shift register	2.0 - 5.5	+/- 8	4,1	160	-40~125				•	•	•
74AHC595	8-bit serial-in/parallel-out shift register	2.0 - 5.5	+/- 8	4	170	-40~125				•	•	•
74LVC594A	8-bit serial-in/parallel-out shift register	1.2 - 5.5	+/- 24	3,1	180	-40~125				•	•	•
74LVC595A	8-bit serial-in/parallel-out shift register	1.2 - 5.5	+/- 24	4	180	-40~125				•	•	•
74VHC595	8-bit serial-in/parallel-out shift register	2.0 - 5.5	+/- 8	4	170	-40~125				•	•	•

Octal Transceivers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1	SOT360-1	SOT764-1
74AHC245	octal transceiver	2.0 - 5.5	+/- 8	3,5	60	-40~125	•	•	•
74AHCV245A	octal transceiver; Schmitt-trigger	1.8 - 5.5	+/- 16	3,2	60	-40~125		•	
74ALVC245	octal transceiver	1.65 - 3.6	+/- 24	2,3	130	-40~85	•	•	•
74LV245A	octal transceiver	2.0 - 5.5	+/- 16	3,1	60	-40~125		•	
74LVC2245A	octal transceiver	1.2 - 3.6	+/- 12	3,3	175	-40~125	•	•	•
74LVC245A	octal transceiver	1.2 - 3.6	+/- 24	2,9	175	-40~125	•	•	•
74LVCH245A	octal transceiver with bus hold	1.2 - 3.6	+/- 24	2,9	175	-40~125	•	•	•
74LVT245B	octal transceiver	2.7 - 3.6	-32/+64	2,4	150	-40~125	•	•	•
74LVT245	octal transceiver	2.7 - 3.6	-32/+64	2,4	150	-40~125	•	•	•
74LVT640	octal transceiver with bus hold; inverting	2.7 - 3.6	-32/+64	2,4	150	-40~125	•	•	
74LVT2245	octal transceiver with bus hold	2.7 - 3.6	+/- 12	3,2	150	-40~125	•	•	
74LVTH2245	octal transceiver with bus hold	2.7 - 3.6	+/- 12	3,2	150	-40~125	•	•	
74VHC245	octal transceiver	2.0 - 5.5	+/- 8	3,5	60	-40~125	•	•	•

Multibyte Transceivers

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT362-1	SOT364-1
74ALVC16245	16-bit transceiver	1.65 - 3.6	+/- 24	1,9	150	-40~85	•	
74ALVT162245	16-bit transceiver with bus hold	2.3 - 3.6	+/- 12	2,3	75	-40~85	•	
74AVC16245	16-bit transceiver	1.2 - 3.6	+/- 12	2	200	-40~85	•	
74AVCH16245	16-bit transceiver with bus hold	1.2 - 3.6	+/- 12	2	200	-40~85	•	
74LVC16245A	16-bit transceiver	1.2 - 3.6	+/- 24	3	175	-40~125	•	
74LVCH16245A	16-bit transceiver with bus hold	1.2 - 3.6	+/- 24	3	175	-40~125	•	
74LVC162245A	16-bit transceiver	1.2 - 3.6	+/- 12	3,3	175	-40~125	•	
74LVCH162245A	16-bit transceiver with bus hold	1.2 - 3.6	+/- 12	3,3	175	-40~125	•	
74LVT16543A	16-bit registered transceiver with bus hold	2.7 - 3.6	-32/+64	2,2	150	-40~125		•
74LVT162245B	16-bit transceiver with bus hold	2.7 - 3.6	+/- 12	2,5	150	-40~125	•	
74LVT16245B	16-bit transceiver with bus hold	2.7 - 3.6	-32/+64	1,9	150	-40~125	•	
74LVTH16245B	16-bit transceiver with bus hold	2.7 - 3.6	-32/+64	1,9	150	-40~125	•	
74LVTN16245B	16-bit transceiver	2.7 - 3.6	-32/+64	1,9	150	-40~125	•	
74LVC32245A	32-bit transceiver	1.2 - 3.6	+/- 24	2,2	175	-40~125		

Hex Translators

Type number	Description	Features					Package (suffix)	
		V_{cc} (V)	I_o (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT109-1	SOT403-1
74HC4049	hex inverter with 15V tolerant inputs	2.0 - 6.0	+/- 5.2	8		-40~125	•	•
74HC4050	hex buffer with 15V tolerant inputs	2.0 - 6.0	+/- 5.2	7		-40~125	•	•

5. Dual Supply Translators

Dual Supply Single Buffers

Type number	Description	Features						Package (suffix)									
		V_{CC} (V)	V_{CC} (B)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1	SOT1226	SOT886	SOT1202	SOT363	SOT765-1	SOT1203	SOT833-1	SOT552-1	SOT1160-1
74AUP1T34	single dual supply translating buffer	1.1 - 3.6	1.1 - 3.6	+/- 1.9	15,2		-40~125	•	•	•	•						
74AVC1T1022	dual supply clock fan-out buffer	0.8 - 3.6	0.8 - 3.6	+/- 12	4		-40~125									•	•
74AXP1T34	single dual-supply translating buffer	0.7 - 2.75	1.2 - 5.5	+/- 12	4,7		-40~125	•	•	•	•						
74AXP1T125	single dual-supply translating buffer	0.7 - 2.75	1.2 - 5.5	+/- 12	4,7		-40~125			•	•	•					
74AXP2T3407	dual-supply translating buffer	0.7 - 2.75	1.2 - 5.5	+/- 12	4,6		-40~125						•	•	•		
74AXP1T14	dual-supply Schmitt-trigger inverter	0.7 - 2.75	1.2 - 5.5	+/- 12	4,9		-40~125	•	•								
74AXP1T57	single dual-supply translating configu-rable gate; Schmitt-trigger inputs	0.7 - 2.75	1.2 - 5.5	+/- 12	4,8		-40~125						•	•	•		

Dual Supply Quad Buffer

Type number	Description	Features						Package (suffix)
		V_{CC} (V)	V_{CC} (B)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT402-1
74LVC4T3144	4-bit Dual Supply Buffer/Line driver	1.2 - 5.5	1.2 - 5.5	+/- 24	6,3		-40~125	•

Dual Supply - Single Gates

Type number	Description	Features						Package (suffix)				
		V_{CC} (V)	V_{CC} (B)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT363	SOT1255	SOT552-1	SOT1081-2	SOT1337-1
74AXP1T32	single dual-supply translating 2-input OR-gate	0.7 - 2.75	1.2 - 5.5	+/- 12	4,9		-40~125	•	•			
74AXP2T08	dual-supply dual translating 2-input AND gate	0.7 - 2.75	1.2 - 5.5	+/- 12	4,9		-40~125			•	•	•

Dual Supply Octal Shift Register

Type number	Description	Features						Package (suffix)	
		V_{CC} (V)	V_{CC} (B)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT360-1	SOT764-1
74LVC8T595	Dual supply 8-bit serial-in/serial-out or paral-lel-out shift register	1.1 - 5.5	1.1 - 5.5	+/- 24	4,1		-40~125	•	•

Dual Supply Single Transceiver

Type number	Description	Features						Package (suffix)			
		V_{CC} (V)	V_{CC} (B)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT886	SOT1202	SOT363	SOT1255
74AUP1T45	single dual-supply voltage level translating transceiver	1.1 - 3.6	1.1 - 3.6	+/- 1.9	15,6		-40~125	•	•	•	
74AVC1T45	single dual-supply voltage level translating transceiver	0.8 - 3.6	0.8 - 3.6	+/- 12	2,1		-40~125	•	•	•	•
74AVCH1T45	single dual-supply voltage translating transceiver with bus hold	0.8 - 3.6	0.8 - 3.6	+/- 12	2,1		-40~125	•	•	•	
74LVC1T45	single dual-supply voltage level translating transceiver	1.2 - 5.5	1.2 - 5.5	+/- 24	2,5		-40~125	•	•	•	
74LVCH1T45	single dual-supply voltage translating transceiver with bus hold	1.2 - 5.5	1.2 - 5.5	+/- 24	2,5		-40~125	•	•	•	

Dual Supply Dual Transceiver

Type number	Description	Features						Package (suffix)				
		V_{CC} (V)	V_{CC} (B)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT765-1	SOT505-2	SOT1203	SOT833-1	SOT1160-1
74AVC2T45	dual-bit dual-supply voltage level translating transceiver	0.8 - 3.6	0.8 - 3.6	+/- 12	2,1		-40~125	•	•	•	•	
74AVC2T245	dual-bit dual-supply voltage level translating transceiver	0.8 - 3.6	0.8 - 3.6	+/- 12	2,1		-40~125					•
74AVCH2T45	dual-bit dual-supply voltage translating transceiver with bus hold	0.8 - 3.6	0.8 - 3.6	+/- 12	2,1		-40~125	•		•	•	
74LVC2T45	dual-bit dual-supply voltage level translating transceiver	1.2 - 5.5	1.2 - 5.5	+/- 24	2,5		-40~125	•		•	•	
74LVCH2T45	dual-bit dual-supply voltage level translating transceiver with bus hold	1.2 - 5.5	1.2 - 5.5	+/- 24	2,5		-40~125	•		•	•	

Dual Supply Quad Transceiver

Type number	Description	Features						Package (suffix)			
		V_{CC} (V)	V_{CC} (B)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT109-1	SOT403-1	SOT763-1	SOT1161-1
74AVC4T245	4-bit dual-supply voltage level translating transceiver	0.8 - 3.6	0.8 - 3.6	+/- 12	2,1		-40~125	•	•	•	•
74AVC4TD245	4-bit dual-supply voltage level translating transceiver	0.8 - 3.6	0.8 - 3.6	+/- 12	2,1		-40~125		•	•	•
74AVCH4T245	4-bit dual-supply voltage translating transceiver with bus hold	0.8 - 3.6	0.8 - 3.6	+/- 12	2,1		-40~125	•	•	•	•

Dual Supply Octal Transceiver

Type number	Description	Features						Package (suffix)		
		V_{CC} (V)	V_{CC} (B)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT137-1	SOT355-1	SOT815-1
74AVC8T245	8-bit dual-supply voltage level translating transceiver	0.8 - 3.6	0.8 - 3.6	+/- 12	2,1		-40~125		•	•
74AVCH8T245	8-bit dual-supply voltage translating transceiver with bus hold	0.8 - 3.6	0.8 - 3.6	+/- 12	2,1		-40~125		•	•
74LVC4245A	8-bit dual-supply voltage translating transceiver	1.2 - 5.5	1.2 - 5.5	+/- 24	3,5		-40~125	•	•	•
74LVC8T245	8-bit dual-supply voltage translating transceiver	1.2 - 5.5	1.2 - 5.5	+/- 24	3,5		-40~125		•	•
74LVCH8T245	8-bit dual-supply voltage translating transceiver with bus hold	1.2 - 5.5	1.2 - 5.5	+/- 24	3,5		-40~125		•	•

Dual Supply Multibyte Transceiver

Type number	Description	Features						Package (suffix)	
		V_{CC} (V)	V_{CC} (B)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT362-1	SOT364-1
74ALVC164245	16-bit dual-supply voltage level translating transceiver	1.5 - 5.5	1.5 - 3.6	+/- 24	2,9		-40~125	•	
74AVC16T245	16-bit dual-supply voltage level translating transceiver	0.8 - 3.6	0.8 - 3.6	+/- 12	2,1		-40~125	•	
74AVCH16T245	16-bit dual-supply voltage translating transceiver with bus hold	0.8 - 3.6	0.8 - 3.6	+/- 12	2,1		-40~125	•	
74AVC20T245	20-bit dual-supply voltage level translating transceiver	0.8 - 3.6	0.8 - 3.6	+/- 12	3,5		-40~125		•
74AVCH20T245	20-bit dual-supply voltage translating transceiver with bus hold	0.8 - 3.6	0.8 - 3.6	+/- 12	3,5		-40~125		•

Dual Supply Multibyte Translator

Type number	Description	Features						Package (suffix)
		V_{CC} (V)	V_{CC} (B)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT109-1
HEF4104B	quad low-to-high voltage translator	3.0 - 15.0	3.0 - 15.0	+/- 2.4	340		-40~85	•

6 . Low threshold over-voltage tolerant inputs

Single Buffers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1	SOT886	SOT402-1
74AHCT1G04	single inverter	4.5 - 5.5	+/- 8	4,5	60	-40~125	•	•	
74AHCT1G14	single inverter; Schmitt-trigger	4.5 - 5.5	+/- 8	4,1	60	-40~125	•		
74AHCT1G17	single buffer; Schmitt-trigger	4.5 - 5.5	+/- 8	4,1	60	-40~125	•		
74AHCT17A	single buffer Schmitt trigger	4.5 - 5.5	+/- 8	3,2	60	-40~125			•
74AHCT1G125	single buffer/line driver	4.5 - 5.5	+/- 8	3,4	60	-40~125	•	•	
74AHCT1G126	single buffer/line driver	4.5 - 5.5	+/- 8	3,4	60	-40~125	•	•	
XC7SET04	single inverter	4.5 - 5.5	+/- 8	3,5	60	-40~125	•		
XC7SET14	single inverter Schmitt-trigger	4.5 - 5.5	+/- 8	4,1	60	-40~125	•		
XC7SET125	single buffer/line driver	4.5 - 5.5	+/- 8	3,4	60	-40~125	•	•	

Dual Buffers

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT765-1	SOT505-2
74AHCT2G125	dual buffer/line driver	4.5 - 5.5	+/- 8	3,4	60	-40~125	•	•
74AHCT2G126	dual buffer/line driver	4.5 - 5.5	+/- 8	3,4	60	-40~125	•	
74AHCT2G241	dual buffer/line driver	4.5 - 5.5	+/- 8	3,4	60	-40~125	•	

Triple Buffers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT765-1	SOT505-2	SOT833-1
74AHCT3G04	triple inverter	4.5 - 5.5	+/- 8	3	60	-40~125	•		
74AHCT3G14	triple inverter; Schmitt-trigger	4.5 - 5.5	+/- 8	4,1	60	-40~125	•	•	•
XC7WT14	triple inverter; Schmitt-trigger	4.5 - 5.5	+/- 8	4,1	60	-40~125	•	•	•

Quad Buffers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1
74ABT125	quad buffer/line driver	4.5 - 5.5	-32 / +64	3,1	100	-40~85	•	•	•
74ABT126	quad buffer/line driver	4.5 - 5.5	-32 / +64	3	100	-40~85	•	•	
74AHCT125	quad buffer/line driver	4.5 - 5.5	+/- 8	3	60	-40~125	•	•	•
74AHCT126	quad buffer/line driver	4.5 - 5.5	+/- 8	3	60	-40~125	•	•	•
74VHCT125	quad buffer/line driver	4.5 - 5.5	+/- 8	3	60	-40~125	•	•	•
74VHCT126	quad buffer/line driver	4.5 - 5.5	+/- 8	3	60	-40~125	•	•	•

Hex Buffers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1
74ABT04	hex inverter	4.5 - 5.5	- 15 / 20	2,2	100	-40~85	•	•	
74AHCT04	hex inverter	4.5 - 5.5	+/- 8	3	60	-40~125	•	•	•
74AHCT14A	hex inverter; Schmitt-trigger	4.5 - 5.5	+/- 8	3,7	60	-40~125		•	
74AHCT14	hex inverter; Schmitt-trigger	4.5 - 5.5	+/- 8	4	60	-40~125	•	•	•
74AHCT04A	hex inverter	4.5 - 5.5	+/- 8	3,1	60	-40~125		•	
74LV04AT	hex inverter	4.5 - 5.5	+/- 12	5,1	30	-40~125		•	
74VHCT14	hex inverter; Schmitt-trigger	4.5 - 5.5	+/- 8	4,1	60	-40~125	•	•	•

Octal Buffers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1	SOT360-1	SOT764-1
74ABT244	octal buffer/line driver	4.5 - 5.5	-32 / +64	2,9	100	-40~85	•	•	
74AHCT244A	octal buffer/line driver	4.5 - 5.5	+/- 8	3,5	60	-40~125		•	
74AHCT244	octal buffer/line driver	4.5 - 5.5	+/- 8	3,5	60	-40~125	•	•	•
74AHCT541A	octal buffer/line driver	4.5 - 5.5	+/- 8	3,5	60	-40~125		•	•
74AHCT541	octal buffer/line driver	4.5 - 5.5	+/- 8	3,5	60	-40~125	•	•	•
74AHCT240	octal inverter/line driver	4.5 - 5.5	+/- 8	3	60	-40~125	•	•	•
74LV244AT	octal buffer/line driver	4.5 - 5.5	+/- 16	2,8	60	-40~125		•	
74LV541AT	octal buffer/line driver	4.5 - 5.5	+/- 16	2,8	60	-40~125		•	
74VHCT244	octal inverter/line driver	4.5 - 5.5	+/- 8	5	60	-40~125	•	•	•
74VHCT541	octal buffer/line driver	4.5 - 5.5	+/- 8	3,5	60	-40~125	•	•	•

Multibyte Buffers

Type number	Description	Features					Package (suffix)
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT362-1
74ABT16240A	16-bit inverter/line driver	4.5 - 5.5	-32 / +64	2	150	-40~85	•
74ABT16244A	16-bit buffer/line driver	4.5 - 5.5	-32 / +64	2,1	150	-40~85	•
74ABT162244	16-bit buffer/line driver	4.5 - 5.5	-32 / 12	3,2	100	-40~85	•
74ABTH162240	16-Bit Buffer/Line Driver	4.5 - 5.5	-32/+12	2,7	100	-40~85	•

Single and Dual Flip Flops

Type number	Description	Features					Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1	SOT108-1	SOT402-1	SOT762-1
74AHCT1G79	single D-type flip-flop	4.5 - 5.5	+/- 8	3,5	90	-40~125	•			
74ABT74	dual D-type flip-flop	4.5 - 5.5	-15/+20	3	250	-40~85		•	•	
74AHCT74	dual D-type flip-flop	4.5 - 5.5	+/- 8	3,3	160	-40~125		•	•	•

Octal Flip Flops

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1	SOT360-1	SOT764-1
74AHCT273	octal D-type flip-flop	4.5 - 5.5	+/- 8	4	120	-40~125	•	•	•
74AHCT374	octal D-type flip-flop	4.5 - 5.5	+/- 8	4,3	140	-40~125	•	•	
74AHCT377	octal D-type flip-flop	4.5 - 5.5	+/- 8	4	140	-40~125	•	•	
74AHCT574	octal D-type flip-flop	4.5 - 5.5	+/- 8	4,4	130	-40~125	•	•	•

Single Gate

Type number	Description	Features					Package (suffix)							
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1	SOT886	SOT1202	SOT363	SOT108-1	SOT402-1	SOT762-1	SOT1255
74AHCT1G00	single 2-input NAND gate	4.5 - 5.5	+/- 8	3,6	60	-40~125	•							
74AHCT1G02	single 2-input NOR gate	4.5 - 5.5	+/- 8	3,5	60	-40~125	•							
74AHCT1G08	single 2-input AND gate	4.5 - 5.5	+/- 8	3,6	60	-40~125	•							
74AHCT1G32	single 2-input OR gate	4.5 - 5.5	+/- 8	3,3	60	-40~125	•							
74AHCT1G86	2-input EXCLUSIVE-OR gate	4.5 - 5.5	+/- 8	3,5	60	-40~125	•							
74AHCT30	8-input NAND gate	4.5 - 5.5	+/- 8	3,3	60	-40~125					•	•	•	
74AUP1T57	configurable gate with voltage level translation	2.3 - 3.6	+/- 1.9	8,7	70	-40~125		•	•	•				
74AUP1T58	configurable gate with voltage level translation	2.3 - 3.6	+/- 1.9	8,7	70	-40~125		•	•	•				
74AUP1T98	configurable gate with voltage level translation	2.3 - 3.6	+/- 1.9	8,7	70	-40~125		•	•	•				
74AUP1T97	configurable gate with voltage level translation	2.3 - 3.6	+/- 1.9	8,7		-40~125		•	•	•				•
XC7SET02	single 2-input NOR gate	4.5 - 5.5	+/- 8	3,5	60	-40~125	•							
XC7SET08	single 2-input AND gate	4.5 - 5.5	+/- 8	3,6	60	-40~125	•							
XC7SET32	single 2-input OR gate	4.5 - 5.5	+/- 8	3,3	60	-40~125	•							
XC7SET86	2-input EXCLUSIVE-OR gate	4.5 - 5.5	+/- 8	3,5	60	-40~125	•							

Dual Gates

Type number	Description	Features					Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT765-1	SOT505-2	SOT108-1	SOT402-1
74ABT20	dual 4-input NAND gate	4.5 - 5.5	-15/+20	2,7	100	-40~85			•	•
74AHCT2G00	dual 2-input NAND gate	4.5 - 5.5	+/- 8	3,6	60	-40~125	•			
74AHCT2G08	dual 2-Input AND gate	4.5 - 5.5	+/- 8	3,6	60	-40~125	•	•		
74AHCT2G32	dual 2-input OR gate	4.5 - 5.5	+/- 8	3,3	60	-40~125	•	•		

Quad Gates

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1
74ABT00	quad 2-input NAND gate	4.5 - 5.5	-15/+20	2,5	100	-40~85	•	•	
74ABT08	quad 2-input AND gate	4.5 - 5.5	-15/+20	2,4	100	-40~85	•	•	
74ABT32	quad 2-input OR gate	4.5 - 5.5	-15/+20	2,3	100	-40~85	•	•	
74AHCT00	quad 2-input NAND gate;	4.5 - 5.5	+/- 8	3,3	60	-40~125	•	•	•
74AHCT02	quad 2-input NOR gate	4.5 - 5.5	+/- 8	3,8	60	-40~125	•	•	•
74AHCT08	quad 2-input AND gate	4.5 - 5.5	+/- 8	5	60	-40~125	•	•	•
74AHCT32	quad 2-input OR gate	4.5 - 5.5	+/- 8	5	60	-40~125	•	•	•
74AHCT86	quad 2-input EXCLUSIVE-OR gate	4.5 - 5.5	+/- 8	3,4	60	-40~125	•	•	•
74AHCT132	quad 2-input NAND gate; Schmitt-trigger	4.5 - 5.5	+/- 8	3,5	60	-40~125	•	•	•
74VHCT02	quad 2-input NOR gate	4.5 - 5.5	+/- 8	3,8	60	-40~125	•	•	•
74VHCT08	quad 2-input AND gate	4.5 - 5.5	+/- 8	5	60	-40~125	•	•	•
74VHCT32	quad 2-input OR gate	4.5 - 5.5	+/- 8	5	60	-40~125	•	•	•

Octal Latch

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1	SOT360-1	SOT764-1
74AHCT573	octal D-type transparent latch	4.5 - 5.5	+/- 8	3,9		-40~125	•	•	•

Octal Shift Register

Type number	Description	Features					Package (suffix)					
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1	SOT109-1	SOT403-1	SOT763-1
74AHCT164	8-bit serial-in/parallel-out shift register	4.5 - 5.5	+/- 8	3,4	115	-40~125	•	•	•			
74AHCT594	8-bit serial-in/parallel-out shift register	4.5 - 5.5	+/- 8	3,8	160	-40~125				•	•	•
74AHCT595	8-bit serial-in/parallel-out shift register	4.5 - 5.5	+/- 8	3,8	170	-40~125				•	•	•
74VHCT595	8-bit serial-in/parallel-out shift register	4.5 - 5.5	+/- 8	3,8	170	-40~125				•	•	•

Octal Transceiver

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1	SOT360-1	SOT764-1
74ABT245	octal transceiver	4.5 - 5.5	-32/+64	2,9	100	-40~85	•	•	
74AHCT245A	octal transceiver	4.5 - 5.5	+/- 8	3	60	-40~125		•	
74AHCT245	octal transceiver	4.5 - 5.5	+/- 8	5	60	-40~125	•	•	•
74LV245AT	octal transceiver	4.5 - 5.5	+/- 16	3,1	60	-40~125		•	
74VHCT245	octal transceiver	4.5 - 5.5	+/- 8	5	60	-40~125	•	•	•

Multibyte Transceiver

Type number	Description	Features					Package (suffix)
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT362-1
74ABT16245B	16-bit transceiver	4.5 - 5.5	-32/+64	2,3	150	-40~85	•
74ABT162245A	16-bit transceiver	4.5 - 5.5	-32/+12	3	100	-40~85	•
74ABTH162245A	16-bit transceiver	4.5 - 5.5	-32/+12	3	80	-40~85	•

7. Standard input with clamp diode and open-drain outputs

Triple Buffers

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT765-1	SOT505-2
74HC3G06	triple inverter	2.0 - 6.0	5,2	9	36	-40~125	•	
74HC3G07	triple buffer	2.0 - 6.0	5,2	9	36	-40~125	•	•

Hex Buffer

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1
74HC05	hex inverter	2.0 - 6.0	5,2	11	36	-40~125	•	•	•

Multibyte Buffers

Type number	Description	Features					Package (suffix)
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1
74HC9114	9-bit inverter Schmitt-trigger	2.0 - 6.0	5,2	12	36	-40~125	•
74HC9115	9-bit buffer Schmitt-trigger	2.0 - 6.0	5,2	12	36	-40~125	•

Multibyte Buffers

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1
74HC03	quad 2-input NAND gate	2.0 - 6.0	5,2	8	36	-40~125	•	•
74LV03	quad 2-input NAND gate	1.0 - 5.5	+/- 12	8	30	-40~125	•	

8 . Low threshold input with clamp diode and open-drain outputs

Triple Buffers

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT765-1	SOT505-2
74HCT3G06	triple inverter	4.5 - 5.5	4	9	36	-40~125	•	
74HCT3G07	triple buffer	4.5 - 5.5	4	9	36	-40~125	•	•

Multibyte Buffers

Type number	Description	Features					Package (suffix)
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1
74HCT9114	9-bit inverter Schmitt-trigger	4.5 - 5.5	4	13	36	-40~125	•

Quad Gate

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1
74HCT03	quad 2-input NAND gate	4.5 - 5.5	+/- 4	10	36	-40~125	•	•

9. Standard over-voltage tolerant input and open-drain outputs

Single Buffers

Type number	Description	Features					Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1	SOT1226	SOT886	SOT1202
74AHC1G07	single buffer	2.0 - 5.5	8	2,5	60	-40~125	•			
74AUP1G06	single inverter	1.1 - 3.6	1,9	4,5	70	-40~85	•	•	•	•
74AUP1G07	single buffer	1.1 - 3.6	1,9	4,4	70	-40~85	•	•	•	•
74AXP1G06	single inverter	0.7 - 2.75	4,5	3,5	70	-40~85		•	•	•
74AXP1G07	single buffer	0.7 - 2.75	4,5	2,6	70	-40~85		•	•	•
74LVC1G06	single inverter	1.65 - 5.5	32	2,3	175	-40~125	•	•	•	•
74LVC1G07	single buffer	1.65 - 5.5	32	2,2	175	-40~125	•	•	•	•

Dual Buffers

Type number	Description	Features					Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT886	SOT1202	SOT363	SOT1255
74AXP2G07	dual buffer	0.7 - 2.75	4,5	3,4	70	-40~85	•	•		•
74AUP2G06	dual inverter	1.1 - 3.6	1,9	4,5	70	-40~85	•	•	•	
74AUP2G07	dual buffer	1.1 - 3.6	1,9	4,4	70	-40~85	•	•	•	•
74LVC2G06	dual inverter	1.65 - 5.5	32	2,3	175	-40~125	•	•	•	•
74LVC2G07	dual buffer	1.65 - 5.5	32	2,6	175	-40~125	•	•	•	•

Triple Buffers

Type number	Description	Features					Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT765-1	SOT505-2	SOT1203	SOT833-1
74AUP3G07	triple buffer	0.8 - 3.6	4	2,7	70	-40~85	•		•	•
74LVC3G06	triple inverter	1.65 - 5.5	32	2	175	-40~125	•	•	•	•
74LVC3G07	triple buffer	1.65 - 5.5	32	2,1	175	-40~125	•	•	•	•

Hex Buffers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT108-1	SOT402-1	SOT762-1
74AHCV07A	hex buffer	1.8 - 5.5	16	3,8	60	-40~125		•	
74LV05A	hex buffer	2.0 - 5.5	12	2,9	60	-40~125		•	
74LV07A	hex buffer	2.0 - 5.5	16	3,6	60	-40~125		•	
74LVC06A	hex inverter	1.65 - 5.5	32	2,2	175	-40~125	•	•	•
74LVC07A	hex buffer	1.65 - 5.5	32	2,2	175	-40~125	•	•	•

Single gates

Type number	Description	Features					Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT353-1	SOT1226	SOT886	SOT1202
74AHC1G09	single 2-input AND gate	2.0 - 5.5	+/- 8	3,2	60	-40~125	•			
74AUP1G09	single 2-input AND gate	1.1 - 3.6	1,9	8,5	70	-40~125	•	•	•	•
74AUP1G38	single 2-input NAND gate	1.1 - 3.6	1,9	8,5	70	-40~125	•	•	•	•
74AXP1G09	single 2-input AND gate	0.7 - 2.75	4,5	2,6	70	-40~85		•	•	•
74LVC1G38	single 2-input NAND gate	1.65 - 5.5	32	2,3	175	-40~125	•	•	•	•

Dual Gates

Type number	Description	Features					Package (suffix)						
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT886	SOT1202	SOT363	SOT765-1	SOT505-2	SOT1203	SOT833-1
74AUP2G38	dual 2-input NAND gate	1.1 - 3.6	1,9	8,5	70	-40~125				•		•	•
74AUP2G0604	inverter and inverter with open-drain	1.1 - 3.6	+/- 1.9	4	70	-40~125	•	•	•				
74AUP2G3407	buffer and buffer with open-drain	1.1 - 3.6	+/- 1.9	4,1	70	-40~125	•	•	•				
74LVC2G38	dual 2-input NAND gate	1.65 - 5.5	32	2,1	175	-40~125				•	•	•	•

Octal Shift registers

Type number	Description	Features					Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT109-1	SOT403-1	SOT763-1
NPIC6C595	8-bit serial-in/parallel-out shift register	4.5 - 5.5	100	90	10	-40~125	•	•	•
NPIC6C596	8-bit serial-in/serial or parallel-out shift register	4.5 - 5.5	100	90	10	-40~125	•	•	•
NPIC6C596A	8-bit serial-in/serial or parallel-out shift register	2.3 - 5.5	100	90	10	-40~125	•	•	•

Multibyte Shift Registers

Type number	Description	Features					Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT163-1	SOT360-1
NPIC6C4894	12-bit shift registers	4.5 - 5.5	100	90	10	-40~125	•	•

10 . Low threshold over-voltage tolerant input and open drain outputs

Single Buffers

Type number	Description	Features					Package (suffix)
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	fmax (MHz)	T_{amb} (°C)	SOT402-1
74AHCT07A	hex buffer	4.5 - 5.5	+/- 8	4	60	-40~125	•
74LV07AT	hex buffer	4.5 - 5.5	16	3,5	60	-40~125	•

11. Bus Switches

Single switches

Type number	Description	Features						Package (suffix)		
		V_{CC} (V)	V_{PASS} (V)	R_{ON} (Ohm)	f(-3dB) (MHz)	t_{pd} (ns)	T_{amb} (°C)	SOT833-1	SOT902-2	SOT530-1
CBTD3306	bus switch level translator	4.5 - 5.5	3,3	7	300	0,25	-40~85	•	•	•

Octal switches

Type number	Description	Features						Package (suffix)	
		V_{CC} (V)	V_{PASS} (V)	R_{ON} (Ohm)	f(-3dB) (MHz)	t_{pd} (ns)	T_{amb} (°C)	SOT764-1	SOT360-1
74CBTLVD3244	bus switch level translator	3.0 - 3.6	1,8	7	400	0,2	-40~125	•	•
74CBTLVD3245	bus switch level translator	3.0 - 3.6	1,8	7	400	0,2	-40~125	•	•

Multibyte switches

Type number	Description	Features						Package (suffix)			
		V_{CC} (V)	V_{PASS} (V)	R_{ON} (Ohm)	f(-3dB) (MHz)	t_{pd} (ns)	T_{amb} (°C)	SOT815-1	SOT355-1	SOT137-1	SOT362-1
74CBTLVD3384	10-bit bus switch level translator	3.0 - 3.6	1,8	7	400	0,2	-40~125	•	•		
74CBTLVD3861	10-bit bus switch level translator	3.0 - 3.6	1,8	7	400	0,2	-40~125	•	•		
CBTD3384	10-bit bus switch level translator	4.5 - 5.5	3,3	7	300	0,25	-40~85		•	•	
CBTD3861	10-bit bus switch level translator	4.5 - 5.5	3,3	7	300	0,25	-40~85	•	•		
CBTD16210	20-bit bus switch level translator	4.5 - 5.5	3,3	7	300	0,25	-40~85				•

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