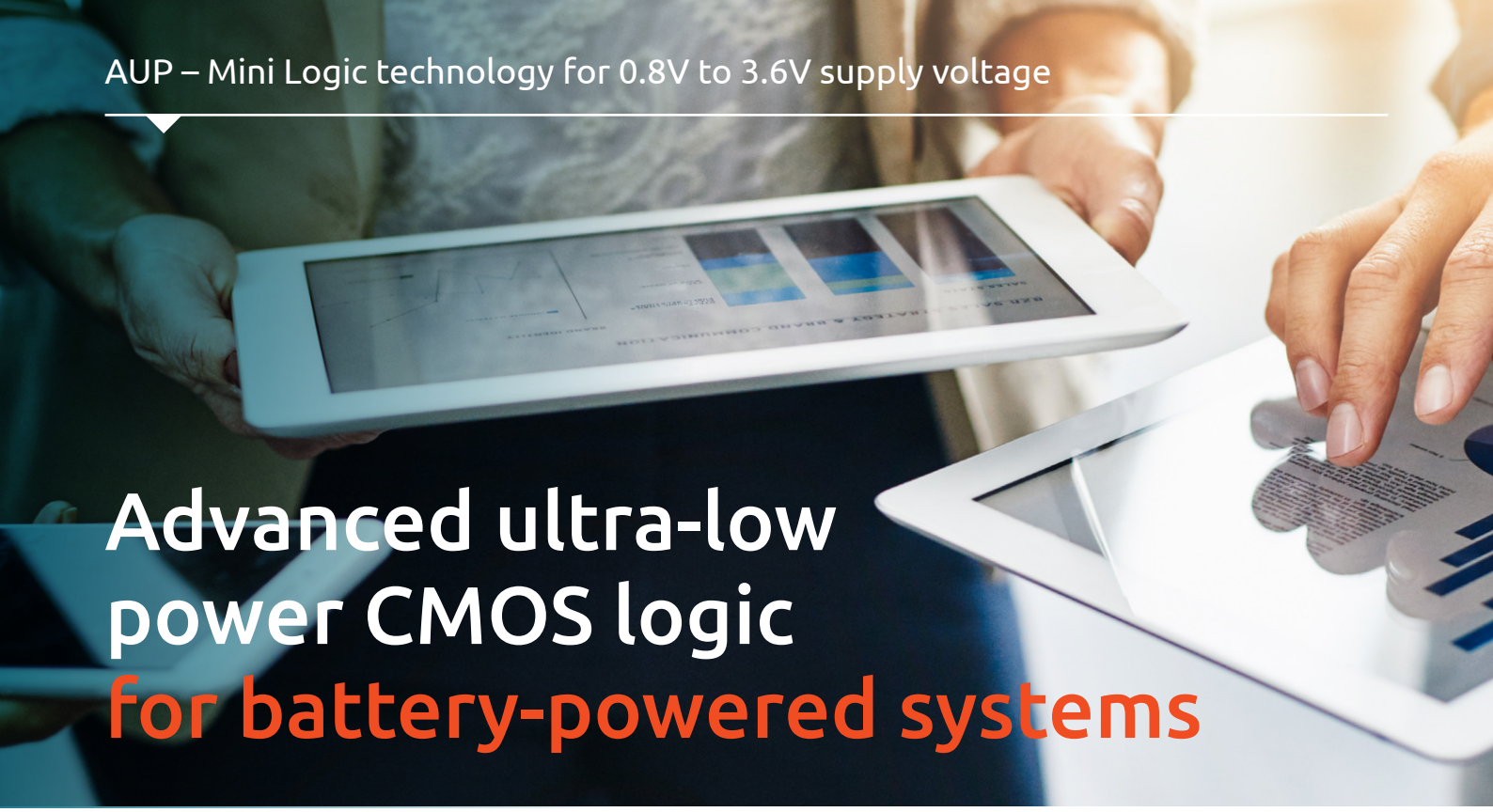

Advanced ultra-low power CMOS logic for battery-powered systems

AUP is a low-voltage high-performance logic technology that enables low static and dynamic power dissipation. AUP is Nexperia's logic technology with the lowest output drive and is characterized by ultra-low power consumption -an ideal combination for portable systems that rely on batteries.

AUP devices are ideally suited for use in mixed-voltage applications because of their wide supply voltage range. AUP technology allows a device supplied at 1.8 V to interface between 3.3 V and 1.8 V systems, helping interface various generations of MCUs. AUP technology's input hysteresis also smoothens signal transitions to preserve signal integrity. Our AUP portfolio is composed of single, dual and triple gate functions, including voltage translators and innovative solutions such as configurable and combination logic types.

Key features

- Low power dissipation and propagation delay (3.4ns typ)
- Wide supply voltage range, from 0.8V to 3.6V
- Input hysteresis, with Schmitt-action on all inputs
- Low-threshold input & over-voltage tolerant I/O options
- 1.9mA balanced output drive current
- Automotive options (-Q100 portfolio)

Key benefits

- Superior speed-power combination
- Full range of logic functions & packages
- Suitable for mixed low-voltage applications
- Extended battery life for portable devices
- Simplified board layout & mechanical stability
- Strong signal integrity and high noise immunity

AUP characteristics

Supply voltage (V)	Propagation delay, typ (ns)	Output drive (mA)	Standby current (µA)	Temperature range (°C)
0.8 to 3.6	3.4	±1.9	0.9	-40 to +125

At 3.3V, AUP delivers a superior speed-power combination by offering significant power saving and optimized propagation delay. AUP outperforms both AUC and LVC technology on energy consumption, positioning it among our lowest power logic families.

nexperia

EFFICIENCY WINS.

Available types

Nexperia's AUP portfolio consists of buffers/inverters/drivers, gates (AND, NAND, XOR, OR, NOR), combination logic, configurable logic, D-type flip-flops, level-shifters/translators, Schmitt-triggers, digital multiplexers and latches/registered drivers.
Types released in AUP technology may support overvoltage-tolerant inputs, Schmitt-trigger inputs, low-threshold inputs, partial power-down circuitry and open-drain outputs.

Applications

- Smartphones & tablets
- Consumer electronics
- Portable computing
- Wearables
- Automotive (ADAS, BMS & infotainment)

1G Single-gates functions	Description	SOT1269-2 (GX4)	SOT753 (GV)	SOT353-1 (GW)	SOT1226 (GX)	SOT363 (GW)	SOT1115 (GN)	SOT1202 (GS)	SOT1255 (GX)	SOT886 (GM)	SOT891 (GF)	SOT765-1 (DC)	SOT1089 (GF)	SOT1116 (GN)	SOT1203 (GS)	SOT1233 (GX)	SOT833-1 (GT)	SOT902-2 (GM)
74AUP1G00	Single 2-input NAND gate			•	•		•	•		•	•							
74AUP1G02	Single 2-input NOR gate			•	•		•	•		•	•							
74AUP1G04	Single inverter	•	•	•	•		•	•		•	•							
74AUP1G06	Single inverter; open-drain			•	•		•	•		•	•							
74AUP1G07	Single buffer; open-drain	•		•	•		•	•		•	•							
74AUP1G08	Single 2-input AND gate			•	•		•	•		•	•							
74AUP1G0832	Single 3-input AND-OR gate					•	•	•		•	•							
74AUP1G09	Single 2-input AND gate; open-drain			•	•		•	•		•	•							
74AUP1G11	Single 3-input AND gate					•	•	•		•	•							
74AUP1G125	Single buffer/line driver (3-state)			•	•		•	•		•	•							
74AUP1G126	Single buffer/line driver (3-state)			•	•		•	•		•	•							
74AUP1G132	Single 2-input NAND gate Schmitt-trigger			•	•		•	•		•	•							
74AUP1G14	Single inverter; Schmitt-trigger	•	•	•	•		•	•		•	•							
74AUP1G157	Single 2-input multiplexer					•	•	•	•	•	•							
74AUP1G158	Single 2-input multiplexer; inverting					•	•	•		•	•							
74AUP1G16	Single buffer/line driver (3-state)			•						•	•							
74AUP1G17	Single buffer Schmitt-trigger	•	•	•	•		•	•		•	•							
74AUP1G175	Single D flip-flop with reset; positive-edge trigger					•	•	•		•	•							
74AUP1G18	1-to-2 demultiplexer (3-state)					•	•	•		•	•							
74AUP1G19	1-to-2 decoder/demultiplexer					•	•	•		•	•							
74AUP1G240	Single inverter/line driver (3-state)			•	•		•	•		•	•							
74AUP1G32	Single 2-input OR gate			•	•		•	•		•	•							
74AUP1G3208	Single 3-input OR-AND gate					•	•	•	•	•	•							
74AUP1G332	Single 3-input OR gate					•	•	•		•	•							
74AUP1G34	Single buffer	•		•	•		•	•		•	•							
74AUP1G373	Single D-type transparent latch (3-state)					•	•	•		•	•							
74AUP1G374	Single D-type flip-flop; positive-edge trigger (3-state)					•	•	•		•	•							
74AUP1G38	Single 2-input NAND gate; open-drain			•	•		•	•		•	•							
74AUP1G386	Single 3-input EXCLUSIVE-OR gate					•	•	•		•	•							
74AUP1G57	Configurable gate; Schmitt trigger					•	•	•	•	•	•							
74AUP1G58	Configurable gate; Schmitt trigger					•	•	•	•	•	•							
74AUP1G74	Single D-type flip-flop with set and reset; positive-edge trigger											•	•	•	•	•	•	•
74AUP1G79	Single D-type flip-flop; positive-edge trigger		•	•	•		•	•		•	•							
74AUP1G80	Single D-type flip-flop; positive-edge trigger			•	•		•	•		•	•							
74AUP1G86	Single 2-input EXCLUSIVE-OR gate			•	•		•	•		•	•							
74AUP1G885	Dual function gate											•	•	•	•		•	•
74AUP1G97	Configurable gate; Schmitt trigger					•	•	•	•	•	•							
74AUP1G98	Configurable gate; Schmitt trigger					•	•	•	•	•	•							
74AUP1GU04	Single inverter; unbuffered			•	•		•	•		•	•							
74AUP1Z04	Crystal driver with enable and internal resistor					•	•	•		•	•							
74AUP1Z125	Crystal driver with enable and internal resistor (3-state)					•	•	•		•	•							

2G Dual-gates & 3G Triple-gates functions	Description	SOT363 (GW)	SOT1115 (GN)	SOT1202 (GS)	SOT1255 (GX)	SOT886 (GM)	SOT891 (GF)	SOT765-1 (DC)	SOT1089 (GF)	SOT1116 (GN)	SOT1203 (GS)	SOT1233 (GX)	SOT833-1 (GT)	SOT902-2 (GM)	SOT552-1 (DP)	SOT1160-1 (GU)
74AUP2G00	Dual 2-input NAND gate							•	•	•	•	•	•	•		
74AUP2G02	Dual 2-input NOR gate							•	•	•	•		•	•		
74AUP2G04	Dual inverter	•	•	•	•	•	•									
74AUP2G06	Dual inverter; open-drain	•	•	•		•	•									
74AUP2G0604	Inverter with open-drain and inverter	•	•	•		•	•									
74AUP2G07	Dual buffer; open-drain	•	•	•	•	•	•									
74AUP2G08	Dual 2-input AND gate							•	•	•	•	•	•	•		
74AUP2G125	Dual buffer/line driver (3-state)							•	•	•	•	•	•	•		
74AUP2G126	Dual buffer/line driver (3-state)							•	•	•	•	•	•	•		
74AUP2G132	Dual 2-input NAND gate Schmitt-trigger							•	•	•	•	•	•	•		
74AUP2G14	Dual inverter Schmitt-trigger	•	•	•	•	•	•									
74AUP2G157	Single 2-input multiplexer							•	•	•	•		•	•		
74AUP2G16	Dual buffer	•				•	•									
74AUP2G17	Dual buffer Schmitt-trigger	•	•	•		•	•									
74AUP2G240	Dual inverter/line driver (3-state)							•	•	•	•		•	•		
74AUP2G241	Dual buffer/line driver (3-state)							•	•	•	•		•	•		
74AUP2G32	Dual 2-input OR gate							•	•	•	•	•	•	•		
74AUP2G34	Dual buffer	•	•	•	•	•	•									
74AUP2G3404	Buffer and inverter	•	•	•		•	•									
74AUP2G3407	Buffer and buffer with open-drain	•	•	•		•	•									
74AUP2G38	Dual 2-input NAND gate; open-drain							•	•	•	•		•	•		
74AUP2G57	Dual configurable gate; Schmitt trigger														•	•
74AUP2G58	Dual configurable gate; Schmitt trigger														•	•
74AUP2G79	Dual D-type flip-flop; positive-edge trigger							•	•	•	•		•	•		
74AUP2G80	Dual D-type flip-flop; positive-edge trigger							•	•	•	•		•	•		
74AUP2G86	Dual 2-input EXCLUSIVE-OR gate							•	•	•	•		•	•		
74AUP2G97	Dual configurable gate; Schmitt trigger														•	•
74AUP2G98	Dual configurable gate; Schmitt trigger														•	•
74AUP2GU04	Dual inverter; unbuffered	•	•	•		•	•									
74AUP3G04	Triple inverter							•	•	•	•		•	•		
74AUP3G0434	Dual inverter and single buffer							•	•	•	•		•	•		
74AUP3G07	Triple buffer; open-drain							•		•	•		•	•		
74AUP3G14	Triple inverter; Schmitt-trigger							•		•	•		•	•		
74AUP3G16	Triple buffer							•	•					•		
74AUP3G17	Triple buffer Schmitt-trigger							•		•	•		•	•		
74AUP3G34	Triple buffer							•	•	•	•	•	•	•		
74AUP3G3404	Dual buffer and single inverter							•	•	•	•		•	•		

1T Voltage Translators	Description	SOT353-1 (GW)	SOT1226 (GX)	SOT363 (GW)	SOT1115 (GN)	SOT1202 (GS)	SOT1255 (GX)	SOT886 (GM)	SOT891 (GF)
74AUP1T00	2-input single supply translating NAND gate	•	•						
74AUP1T02	2-input single supply translating NOR gate	•	•						
74AUP1T04	Single supply translating inverter	•	•						
74AUP1T08	2-input single supply translating AND gate	•	•						
74AUP1T14	Single supply translating Schmitt-Trigger Inverter	•	•						
74AUP1T17	Single supply translating Schmitt-Trigger Buffer	•	•						
74AUP1T32	2-input single supply translating OR gate	•	•						
74AUP1T34	Single dual supply translating buffer	•	•		•	•		•	•
74AUP1T45	Single dual-supply voltage level translating transceiver (3-state)			•	•	•		•	•
74AUP1T50	Single supply translating Schmitt-Trigger Buffer	•	•						
74AUP1T57	Configurable gate with voltage level translation			•	•	•		•	•
74AUP1T58	Configurable gate with voltage level translation			•	•	•		•	•
74AUP1T86	2-input single supply translating X-OR gate	•	•						
74AUP1T87	2-input single supply translating X-NOR gate	•	•						
74AUP1T97	Configurable gate with voltage level translation			•	•	•	•	•	•
74AUP1T98	Configurable gate with voltage level translation			•	•	•		•	•

Packages

Our AUP family of Si-gate CMOS devices uses advanced process technology and next-generation packaging. AUP devices are available in Mini Logic packages –up to 10 pins/pads. Leadless mini logic packages are known as MicroPak and leaded mini logic packages are called PicoGate. Our choice of 4, 5, 6, 8 and 10-pin packages enables customers to select the appropriate combination of features and performance in a minimal footprint.

Nearly 100 AUP functions are available from Nexperia -primarily in leadless XSON and X2SON packages & leaded TSSOP and VSSOP packages. Our AUP family operates over an extended temperature range (-40 °C to 125°C) to match many applications' requirements, from portable and consumer electronics to advanced Automotive systems.

	4-pin	5-pin			6-pin					
										
Package (suffix)	X2SON4 (GX4)	TSOP5 (GV)	TSSOP5 (GW)	X2SON5 (GX)	TSSOP6 (GW)	XSON6 (GM)	XSON6 (GF)	XSON6 (GS)	XSON6 (GN)	X2SON6 (GX)
Package number	SOT1269-2	SOT753	SOT353-1	SOT1226	SOT363	SOT886	SOT891	SOT1202	SOT1115	SOT1255
L x W x H, Pitch -in mm	0.6 x 0.6 x 0.35, 0.4	2.9 x 2.75 x 1.1, 0.95	2.1 x 2.1 x 0.95, 0.65	0.8 x 0.8 x 0.35, 0.4	2.1 x 2.1 x 0.95, 0.65	1.45 x 1.0 x 0.5 , 0.5	1 x 1 x 0.5, 0.35	1.0 x 1.0 x 0.35, 0.35	0.9 x 1.0 x 0.35, 0.3	1.0 x 0.8 x 0.35, 0.4

	8-pin							10-pin	
									
Package (suffix)	VSSOP8 (DC)	XQFN8 (GM)	XSON8 (GT)	XSON8 (GF)	XSON8 (GS)	XSON8 (GN)	X2SON8 (GX)	TSSOP10 (DP)	XQFN10 (GU)
Package number	SOT765-1	SOT902-2	SOT833-1	SOT1089	SOT1203	SOT1116	SOT1233	SOT552-1	SOT1160-1
L x W x H, Pitch -in mm	2.0 x 3.1 x 1.0, 0.5	1.6 x 1.6 x 0.5, 0.5	1.95 x 1.0 x 0.5, 0.5	1.35 x 1 x 0.5, 0.55	1.35 x 1.0 x 0.35, 0.35	1,2 x 1 x 0.35, 0.3	1.35 x 0.8 x 0.35, 0.4	3.0 x 4.9 x 1.1, 0.5	1.4 x1.8 x 0.5, 0.4

To learn more about AUP technology, visit:
nexperia.com/products/logic/family/AXP/

To discover our full Mini Logic portfolio, visit:
nexperia.com/products/logic/family/MINI-LOGIC/

Date of release:
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