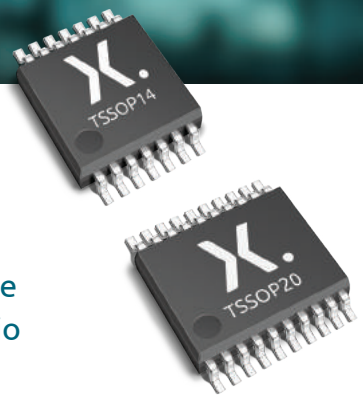
LV-A(T) logic
with partial power-down feature



LV-A(T) solutions from Nexperia offer low leakage when powered down, for modular standby applications. LV-A types feature CMOS input levels, while LV-AT types include low-input thresholds for TTL interfacing –enabling voltage translation. LV-A(T) products are suitable for computing, printer and smart TV applications. Our LV-A(T) portfolio is comprised of more than 15 Standard Logic types, all with partial power down support.

Our LV-A(T) portfolio consists of LV-A and LV-AT. LV-A comprises standard logic 2-input gates as well as buffers, inverters and transceivers with overvoltage tolerant Schmitt-trigger action inputs designed for CMOS interfaces.

LV-AT comprises standard logic inverters, buffers & transceivers with low-input threshold overvoltage tolerant Schmitt-trigger action inputs designed for TTL interfaces. LV-AT includes types with additional features such as open-drain outputs.

Nexperia's LV-A(T) family offers a typical 4.5ns propagation delay, 20µA standby current and operates with low noise ($V_{OL(p)}$ < 0.8 V).

All our LV-A(T) products are available in industry-standard 14-pin or 20-pin leaded TSSOP packages, specified from -40 °C to +125 °C. These can be released in our Automotive (-Q100) portfolio to address specific requirements.

Key Features & benefits

- Wide supply voltage range
  - from 2.0V to 5.5V for LV-A
  - from 4.5V to 5.5V for LV-AT
- Partial power down support (I_{OFF} circuitry)
- Low noise operation ($V_{OL(p)}$ < 0.8 V)
- Full range of gates, buffers, inverters & transceivers
- Overvoltage tolerant inputs
- CMOS- or TTL-input variants & Schmitt-trigger options
- Standard TSSOP14 and TSSOP20 packages

Applications

- Medium and low speed applications
- Standby & power-down applications
- Computing peripherals incl. printers
- Home entertainment incl. TV & STB

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EFFICIENCY WINS.

I_{OFF} circuitry

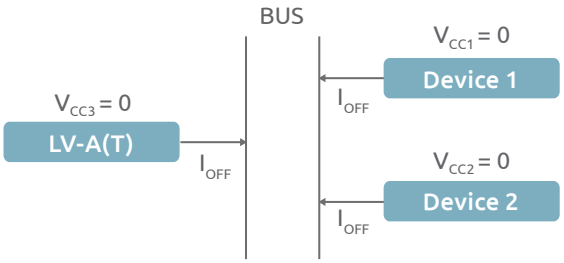
This feature disables outputs, preventing any damaging backflow current through the device when powered down. I_{OFF} circuitry enables partial power-down mode operation, ideal for modular standby applications. LV-A(T) solutions are the only Standard Logic 5V family with I_{OFF} circuitry from Nexperia.

Over-voltage tolerant inputs

The maximum voltage applied to an input may exceed the supply voltage. For LV-A(T), 5.5V may be applied to the inputs irrespective of the supply voltage. Thanks to this feature, LV-AT solutions are suitable for HIGH to LOW level translation (e.g. when supplied at 3.3V, 5.0V may be applied to the input to achieve 5.0V to 3.3V voltage translation).

Open-drain outputs

Open-drain outputs have an NMOS transistor to ground. To achieve a logical high on the output when the product is in the high impedance state (3-state), a pull-up resistor can be used to reach the desired output voltage level. The pull-up resistor can be used with a pull-up voltage higher or lower than the supply voltage. LV-A(T) can be used with a pull-up voltage 5.5V or less and allows for voltage translation.



Disabling power using I_{OFF} feature

Parametrics

	Supply Voltage (V_{CC})	Output Drive (V_O)	Prop Delay (t_{PD})	Temperature Range (T_{amb})	Static Current (I_{CC})
LV-A	2.0 – 5.5 V	+/- 16 mA	4.9 ns at 2.5 V 3.7 ns at 3.3 V 2.9 ns at 5.0 V	−40 °C to +125 °C	0.1 µA (typ.)
LV-AT	4.5 – 5.5 V	+/- 16 mA	2.9 ns at 5.0 V	−40 °C to +125 °C	0.1 µA (typ.)

Packages

Suffix	Name	Package family	Dimensions (L x W x H, pitch - in mm)	
PW	SOT402-1	TSSOP14	6.4 x 5 x 1.1, 0.65	
PW	SOT360-1	TSSOP20	6.5 x 6.4 x 1.1, 0.65	

Browse our entire LV-A(T) range and learn about the technology:
nexperia.com/products/logic/family/LV-A/

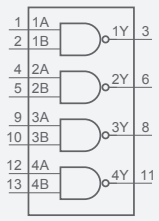
Available types

Gates	
74LV00A	Quad 2-input NAND
74LV02A	Quad 2-input NOR
74LV08A	Quad 2-input AND
74LV32A	Quad 2-input OR
74LV7032A	Quad 2-input OR; Schmitt-trigger
Buffers, Inverters & Transceivers	
74LV04AT	Hex inverter; TTL-enabled
74LV05A	Hex inverter with open-drain
74LV07A	Hex buffer with open-drain
74LV07AT	Hex buffer with open drain; TTL-enabled
74LV14A	Hex inverter; Schmitt-trigger
74LV17A	Hex buffer; Schmitt-trigger
74LV244A	Octal buffer/line-driver (3-state)
74LV244AT	Octal buffer/line-driver (3-state); TTL-enabled
74LV245A	Octal bus transceiver (3-state)
74LV245AT	Octal bus transceiver (3-state); TTL-enabled
74LV540A	Inverting octal buffer/line-driver (3-state)
74LV541A	Octal buffer/line-driver (3-state)
74LV541AT	Octal buffer/line-driver (3-state); TTL-enabled

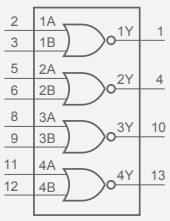
Functional diagrams

LV-A Control Logic: Gates

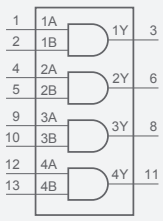
74LV00A



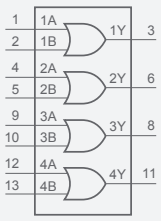
74LV02A



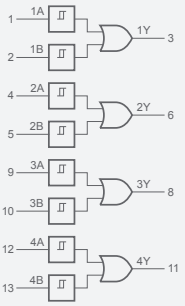
74LV08A



74LV32A

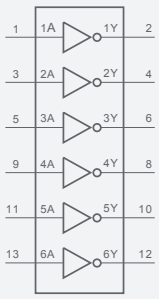


74LV7032A

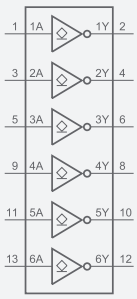


LV-A(T) Asynchronous Interface Logic: Buffers, Inverters & Transceivers

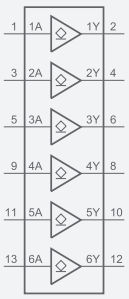
74LV04AT



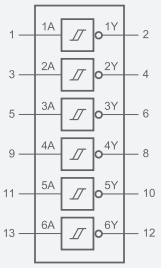
74LV05A



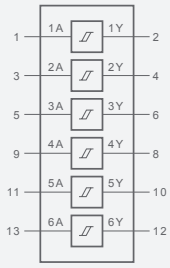
74LV07A(T)



74LV14A



74LV17A



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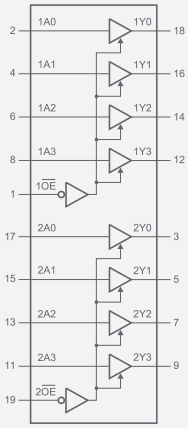
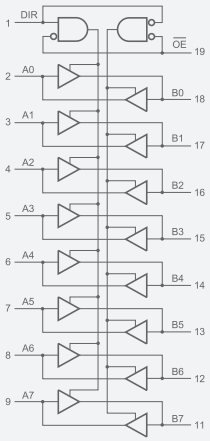
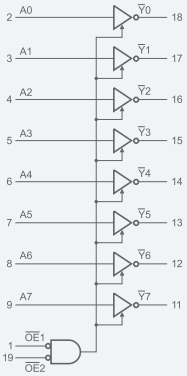


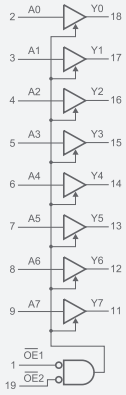
74LV245A(T)



74LV540A



74LV541A(T)

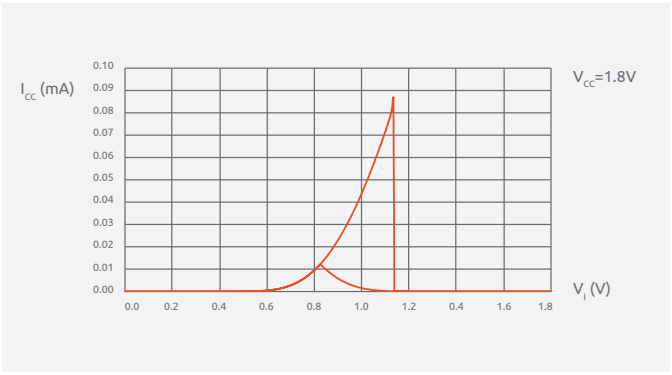


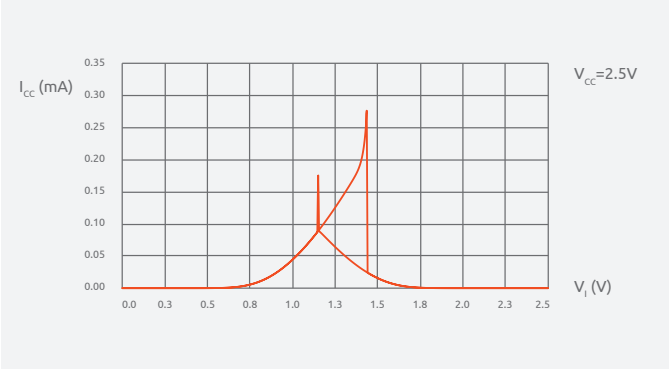
74LV-AT types are TTL-enabled, allowing for 3.3V to 5V voltage translation thanks to transistor-to-transistor logic

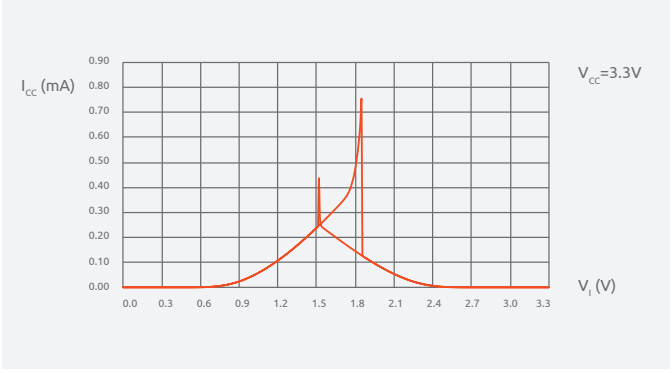
Input characteristics of LV-A

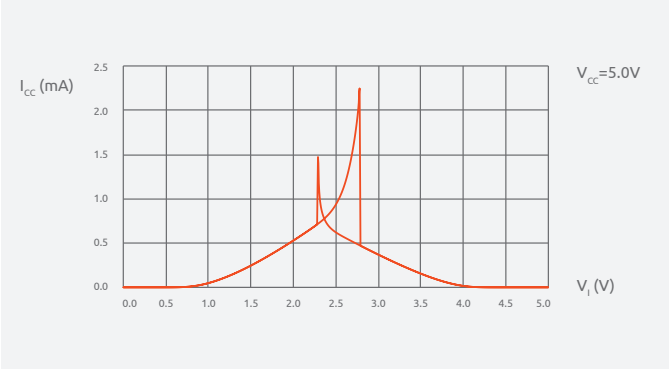
CMOS inputs with Schmitt-trigger action

LV-A products have CMOS inputs with Schmitt-trigger action which produces a small input switching hysteresis (~100mV) that improves noise immunity.
LV-A solutions operate with defined input levels $V_{IL} \leq 0.3xV_{CC}$ and $V_{IH} \geq 0.7xV_{CC}$ for supply range V_{CC} 2.0 to 5.5V.



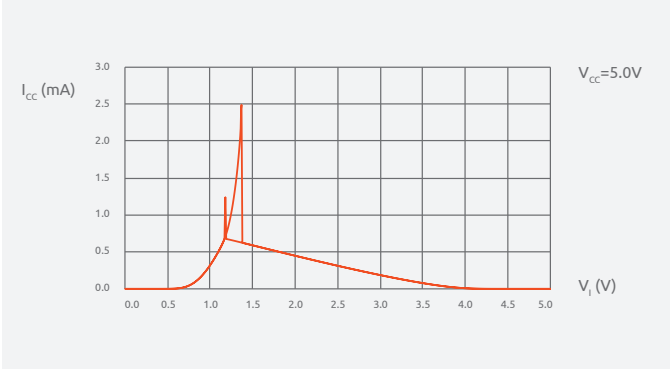






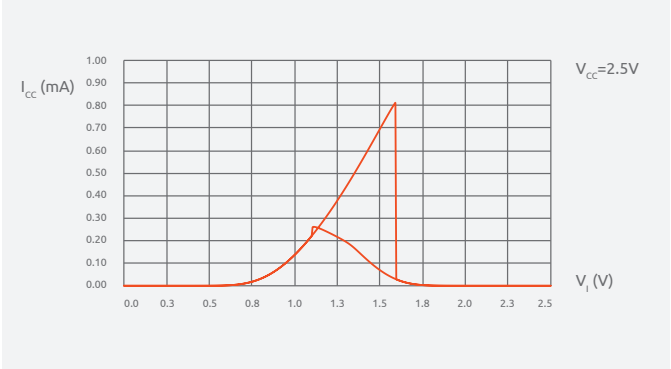
TTL inputs with Schmitt-trigger action

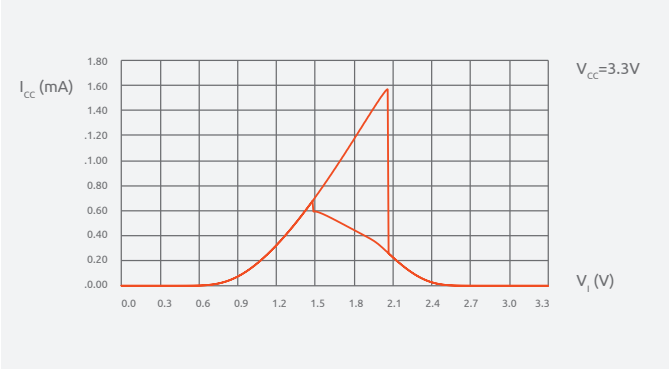
LV-AT products have low-threshold TTL inputs with Schmitt-trigger action which produces a small input switching hysteresis (~100mV) that improves noise immunity.
LV-AT solutions operate with defined input levels $V_{IL} \leq 0.8V$ and $V_{IH} \geq 2.0V$ for supply range V_{CC} 4.5 to 5.5V.

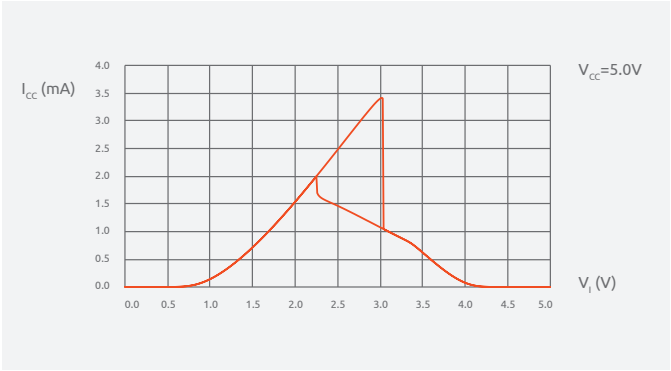


Schmitt-trigger inputs

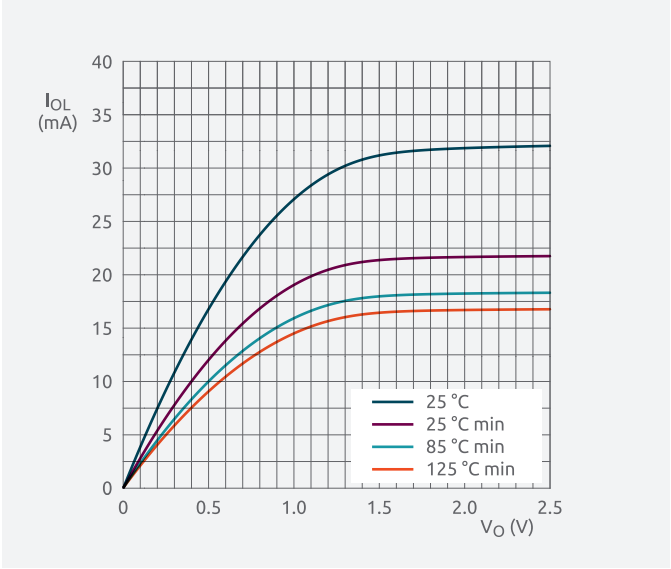
74LV14A and 74LV17A products have true Schmitt-trigger inputs that specify input hysteresis for interfacing slower input rise and fall times. The switching threshold is adjusted for rising edge (Vt+) and falling edge (Vt–). The difference between the switching points is called hysteresis (ΔVt).



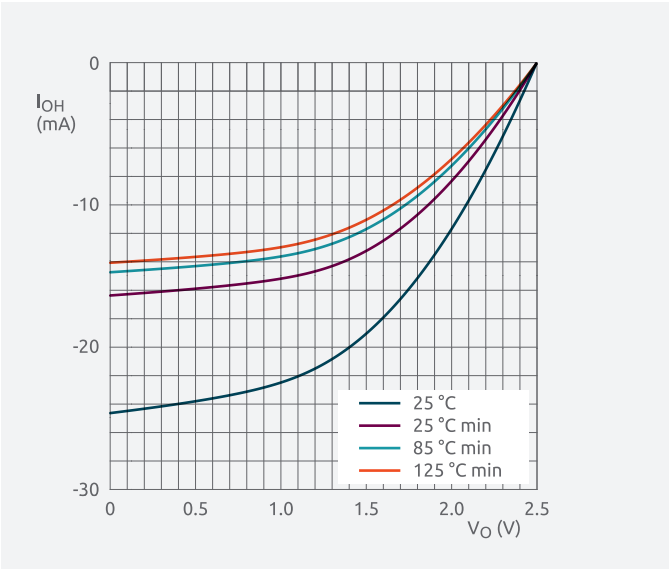




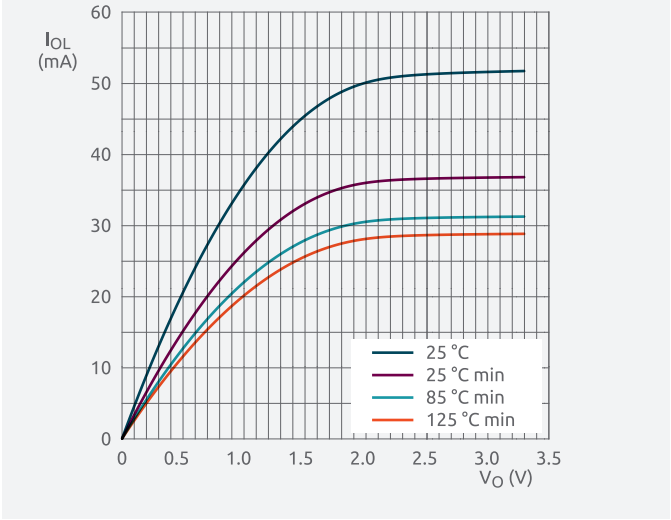
Output characteristics



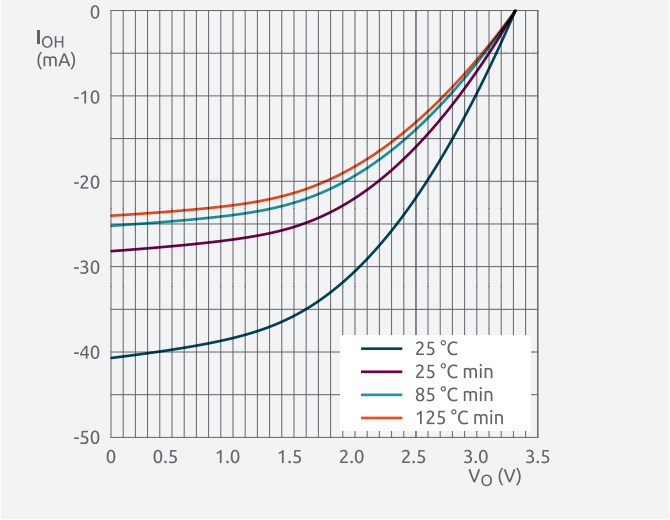
V_{cc} = 2.5V, output driving LOW



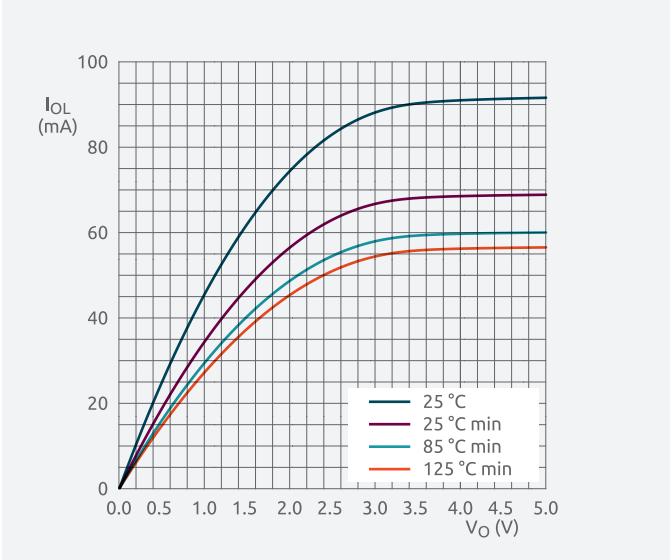
V_{cc} = 2.5V, output driving HIGH



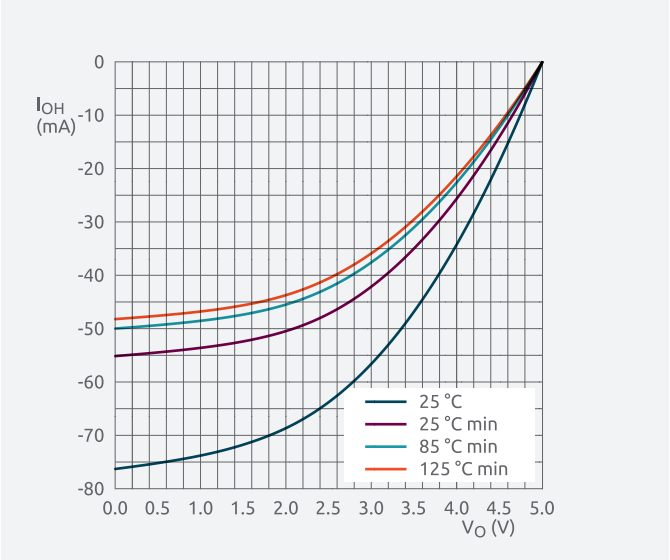
V_{cc} = 3.3V, output driving LOW



V_{cc} = 3.3V, output driving HIGH



V_{cc} = 5.0V, output driving LOW



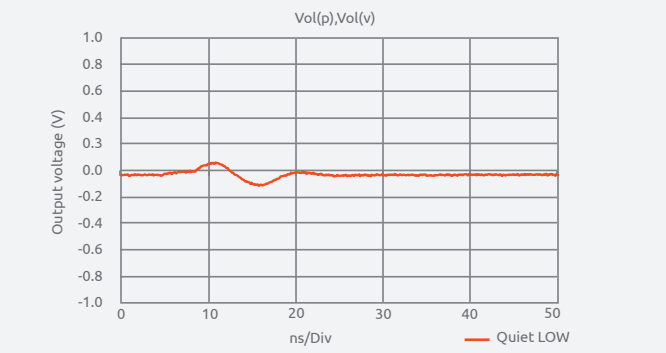
V_{cc} = 5.0V, output driving HIGH

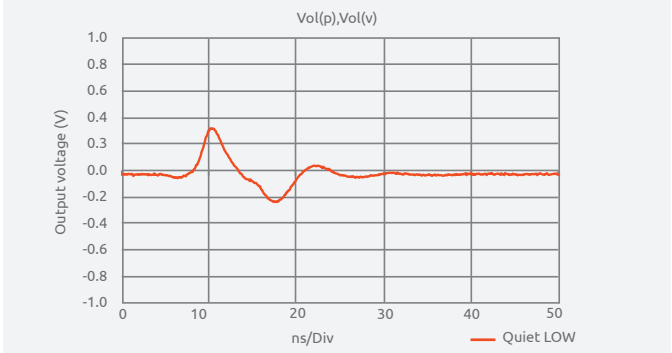
Noise characteristics

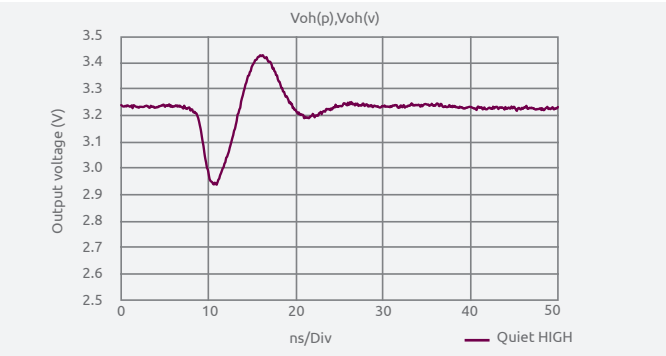
Simultaneous-switching noise can generate glitches in electronic systems.
Performance for LV-A(T) is measured as follows in the below graphs: (T_{amb}=25°C; C_L=50pF)

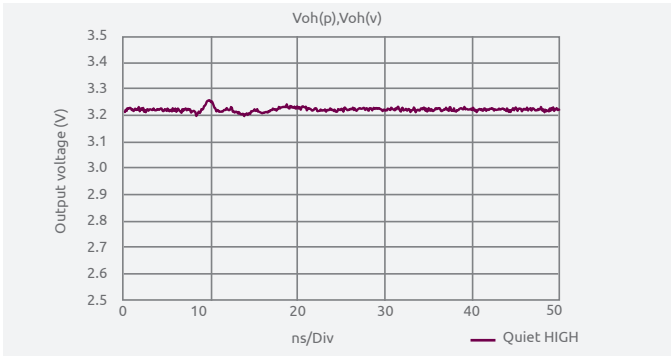
- $V_{OL(p)}$, $V_{OL(v)}$ when one output is driven low while other outputs simultaneously transition HIGH to LOW.
- $V_{OH(v)}$, $V_{OH(p)}$ when one output is driven high while other outputs simultaneously transition LOW to HIGH.

LV-A at V_{cc} = 3.3V

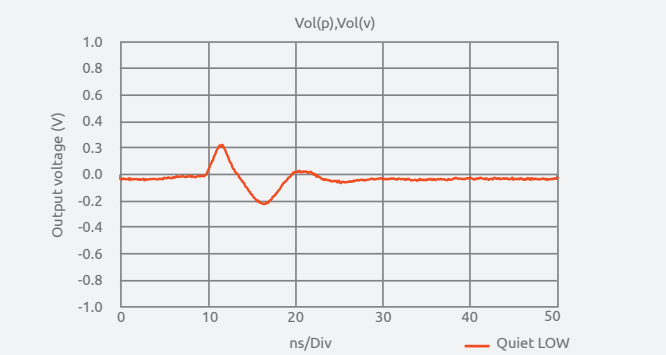


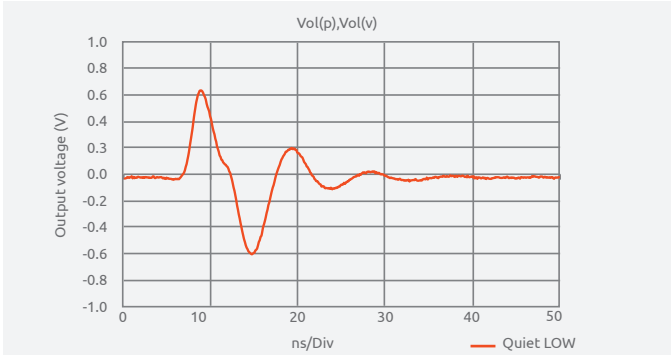


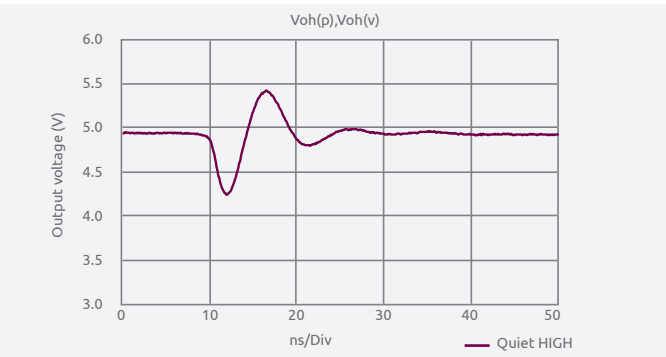


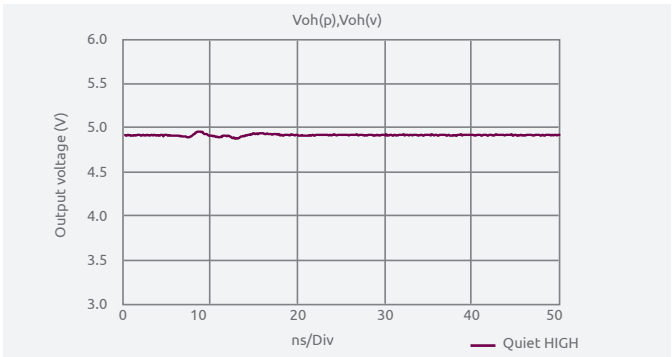


LV-A at V_{cc} = 5V









Date of release:
March 2019