Reliability Monitoring Results

Quarters: Q1/2021 to Q4/2021
Based on structural similarity

Supplier	**User Part Number**
Nexperia B.V.	74LVCH16374ADGG

Part Description: 16-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)

Function Family: LVC
Process family: Sub micron
Package family: TSSOP

JESD47 Test		Test Conditions	Duration	# Lots	# Quantity	# Rejects
# 1	**TEST** Pre- and Post-Stress Electrical Test	Tamb = 25 °C	N/A	see below	all parts	see below
# 2	**PC** Preconditioning	JESD22-A113 MSL 1	N/A	863	73980	0
# 5a	**HTOL EFR** High Temperature Operating Life Extrinsic	JESD22-A108 Tj = 150°C $V_{CCMAX} \leq V \leq 1.2*V_{CCMAX}$	48 hours or 168 hours	356	51713	0
# 5b	**HTOL IFR** High Temperature Operating Life Intrinsic	JESD22-A108 Tj = 150°C $V_{CCMAX} \leq V \leq 1.2*V_{CCMAX}$	≥500 hours	134	9791	0
# 7	**TC** Temperature Cycling	JESD22-A104 -65 °C to 150°C	≥500 cycles	478	37734	0
# 9	**uHAST / HAST** unbiased or biased High Accelerated Stress Test	JESD22-A101 Tamb = 130 °C, RH = 85%, V = V_{CCMAX}	96 hours	462	36246	0

Calculation of PPM, FIT and MTTF

Test considered for PPM calculation: High Temperature Operating LifeTest Extrinsic (HTOL EFR, Test # 5a above)
Test considered for FIT and MTTF calculations: High Temperature Operating LifeTest Intrinsic(HTOL IFR, Test # 5b above)
Confidence level 60%, derated to 55 °C, activation energy 0.7 eV, test time 168 to 1000 hours

Product Family	Package Family	Quantity	Rejects	Extrinsic Failure Rate (PPM)	Intrinsic Failure Rate (FIT)	MTTF (hrs)
LVC	TSSOP	9791	0	18	0.5	2.22 E+09