Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.philips.com/ or http://www.semiconductors.philips.com/, use **http://www.nexperia.com**

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:
- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved
Should be replaced with:
- **© Nexperia B.V. (year). All rights reserved**.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

R_10001

Guideline for the laser marking layout of WLCSP devices

Rev. 01 — 10 February 2010 **Report**

Document information

Info	Content
Title	R_10001
Short title (1 line)	R_10001
Subtitle	Guideline for the laser marking layout of WLCSP devices
Short subtitle (1 line)	WLCSP marking guideline
Document ID	R_10001_1
Document type	Report
Revision number	01
Keywords	product name, lot ID, pin A1 location, bump-to-bump pitch, standard or high performance solder ball
Abstract	This document presents the NXP laser marking guideline for the delivery of Wafer-Level Chip-Scale Package (WLCSP) devices of the product line Integrated Discretes (IDs).

Revision history

Rev	Date	Description
01	20100210	initial version

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

1. Introduction

The laser marking on the back side of the device supports the process of identification as well as internal and external traceability. To encode all relevant information into the device marking the following parameters are used:

- Orientation of pin A1 marker
- Orientation of lot ID with respect to the pin A1 marker
- Lot ID and product name characters

2. Layout rules for laser marking

2.1 Lot ID and product name marking

The standard marking consists of three lines. Figure 1 shows the outline of the marking. The first line consists of the pin A1 marker. The second line (placeholder <product name>) indicates the product name. If there is enough space all 4 product name numbers are marked.

The third line (placeholder <lot ID>) denotes the lot ID. If possible all 5 characters of the lot ID are marked.

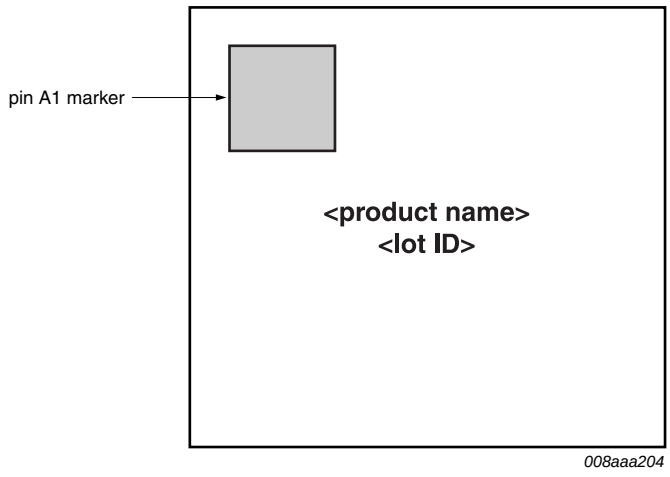


Fig 1. Outline of the marking

Figure 2 shows an example of IP4035CX24/LF. The 'YYYY' is the placeholder for the lot ID. This is a standard solder ball device with 500 μm bump-to-bump pitch.

Special rules apply if there are space constraints:

- If there is not enough space for three lines the lot ID line has precedence. In this case, only the lot ID and the pin A1 indicator are marked
- The leading numbers are omitted if there is not enough space for all characters of the lot ID or product name. This is true in the example in Figure 2 where the leading two product name numbers are left out

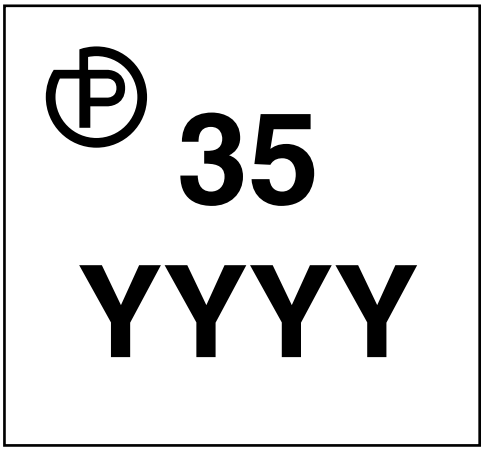


Fig 2. Marking example of IP4035CX24/LF

2.2 Pin A1 marking

The location of the pin A1 is indicated by a ‘P’ encompassed by a ¾ circle with a diameter of 300 μm (typical). This marker will be referred to as ‘P’ in the following text.

The design of the pin A1 marker is shown in Figure 3. The ‘P’ can be freely rotated. The ‘P’ can also be mirrored with regards to the circle as shown in Figure 4.

Notice: There is no special meaning associated with the mirrored ‘P’. The mirroring enables the marking of vertical or horizontal lines on the die.

Fig 3. Pin A1 marker design

Fig 4. Mirrored pin A1 marker design

Two rules allow a differentiation between the used ball material and between the bumping pitch.

Rule 1a: If a standard solder ball is used the corner of the pin A1 circle is located near to the edge of the die as shown in Figure 5.

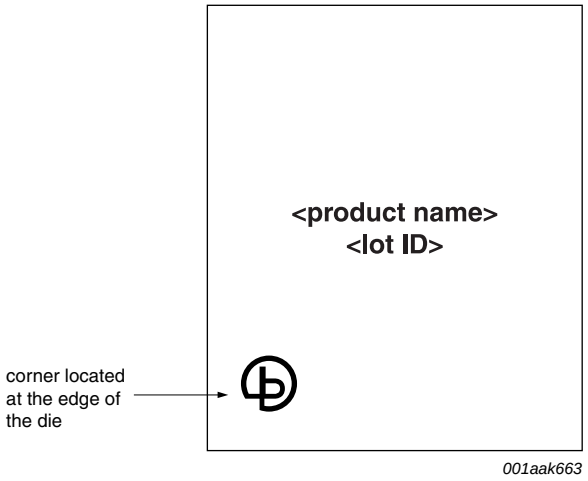


Fig 5. Pin A1 orientation of a standard solder ball

Rule 1b: If a high performance solder ball is used the corner of the pin A1 circle is pointing into the opposite direction, i.e. inside the die. This is depicted in Figure 6.

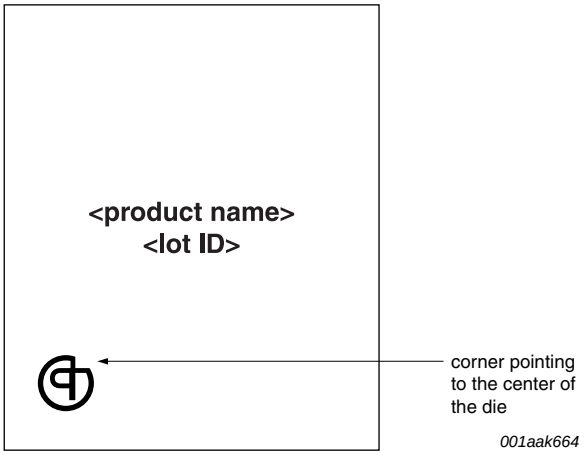


Fig 6. Pin A1 orientation of a high performance solder ball

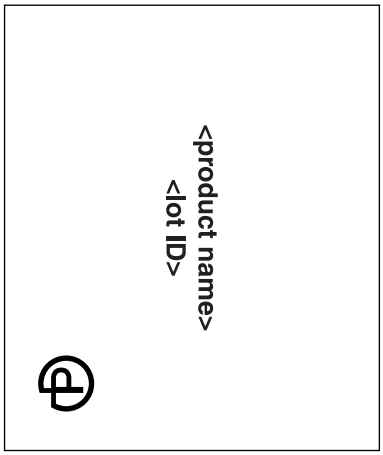
The differentiation between a 500 μm and a 400 μm solder ball pitch is possible by looking at the orientation of the 'P' and the product name or lot ID characters. The following two rules govern this relationship.

Rule 2a: If it is a 500 μm pitch product, the 'P' character and the product name or lot ID lines have the same orientation. An example is shown in Figure 7.

001aak665

Fig 7. 500 μm pitch device with a standard solder ball

Rule 2b: If it is a 400 μm pitch product, the 'P' character and the product name or lot ID lines have the opposite orientation. An example is shown in Figure 8.



001aak666

Fig 8. 400 μm pitch device with a standard solder ball

The following figure shows several examples in order to clarify the marking rules.

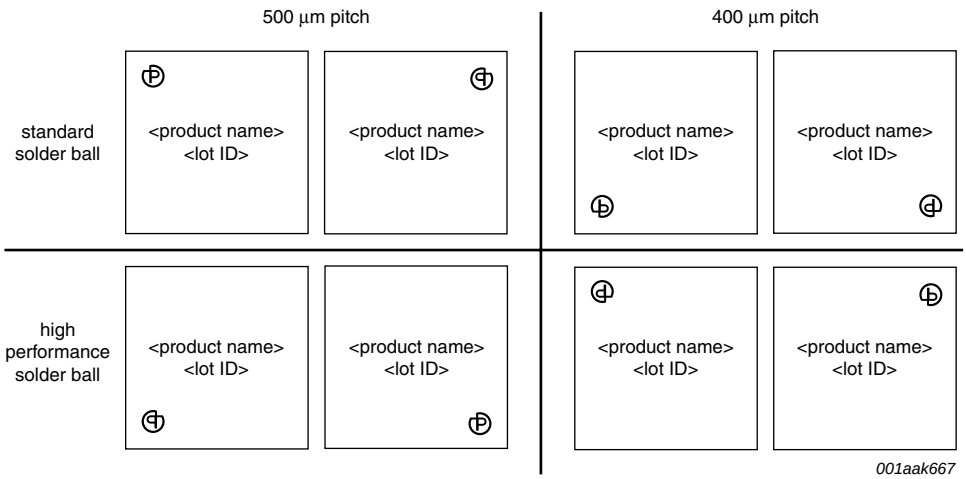


Fig 9. Examples for pin A1 markings to differentiate the solder ball material and pitch

3. Legal information

3.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

3.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on a weakness or default in the customer application/use or the application/use of customer's third party customer(s) (hereinafter both referred to as "Application"). It is customer's sole responsibility to check whether the NXP Semiconductors product is suitable and fit for the Application planned. Customer has to do all necessary testing for the Application in order to avoid a default of the Application and the product. NXP Semiconductors does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

3.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

4. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 10 February 2010
Document identifier: R_10001_1