PESD1V0Y1BBSF

Extremely low clamping bidirectional ESD protection diode

1 April 2022 **Short data sheet**

1. General description

Extremely low clamping, extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, part of the TrEOS protection family. This device is housed in a DSN0603-2 (SOD962-2) leadless, ultra-small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of one line
- ESD protection up to ±14 kV contact discharge according to IEC 61000-4-2
- Extremely low diode capacitance: C_d = 0.16 pF at 1 MHz
- Extremely low insertion loss: -0.29 dB at 10 GHz
- Extremely low return loss: -20.6 dB at 10 GHz
- RF performance does not degrade over the operation voltage range
- Extremely low leakage current: < 1 nA at 1 V
- Extremely low inductance protection path to ground
- Very high surge robustness: 5.5 A for a 8/20 µs pulse
- IEC 61000-4-4 robust up to level 3 on I/O ports (corresponds to 40 A into a 50 Ohm termination)
- Ultra-small SMD package

3. Applications

- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals
- USB4, USB3.2 and Thunderbolt 3 and 4 data lines. Please refer to chapter "7. Application information", for details.

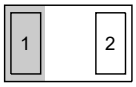
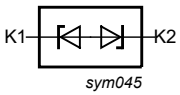
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage			-1	-	1	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	0.16	-	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 Transparent top view **DSN0603-2 (SOD962-2)**	
2	K2	cathode (diode 2)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD1V0Y1BBSF	DSN0603-2	silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body	SOD962-2

7. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

Due to the very low trigger voltage V_{t1}, it needs to be ensured that V_{RWM} is not exceeded under normal application conditions. If the device is used in an USB 3.2 environment, place the device between the AC coupling capacitor and the transceiver. Refer to the USB 3.2 specification for maximum working voltages.

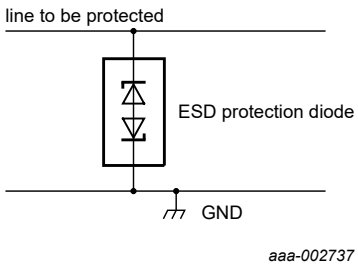


Fig. 1. Application diagram

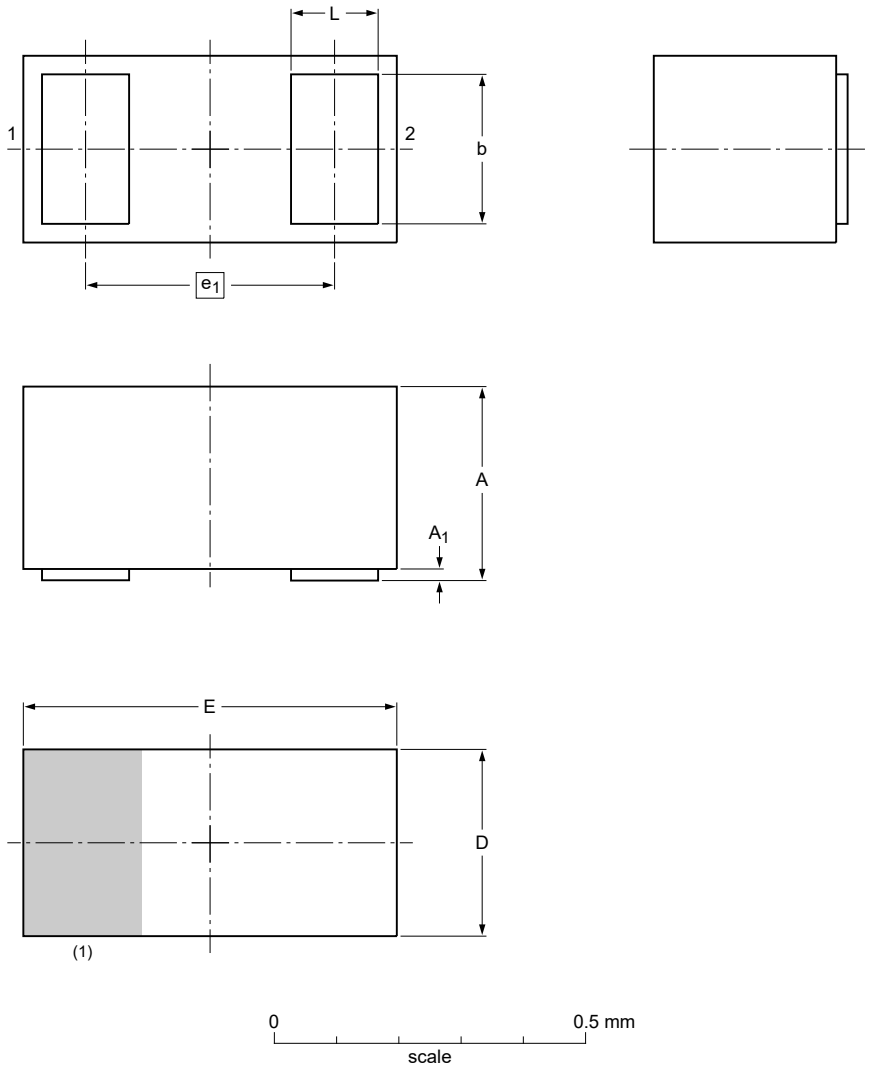
Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

8. Package outline

Leadless ultra small package; 2 terminals; body 0.6 x 0.3 x 0.3 mm **SOD962-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	D	E	e_1	L
mm	max	0.32	0.03	0.25	0.325	0.625		0.15
	nom						0.4	
	min	0.28		0.23	0.275	0.575		0.13

Note
1. The marking bar indicates the cathode.

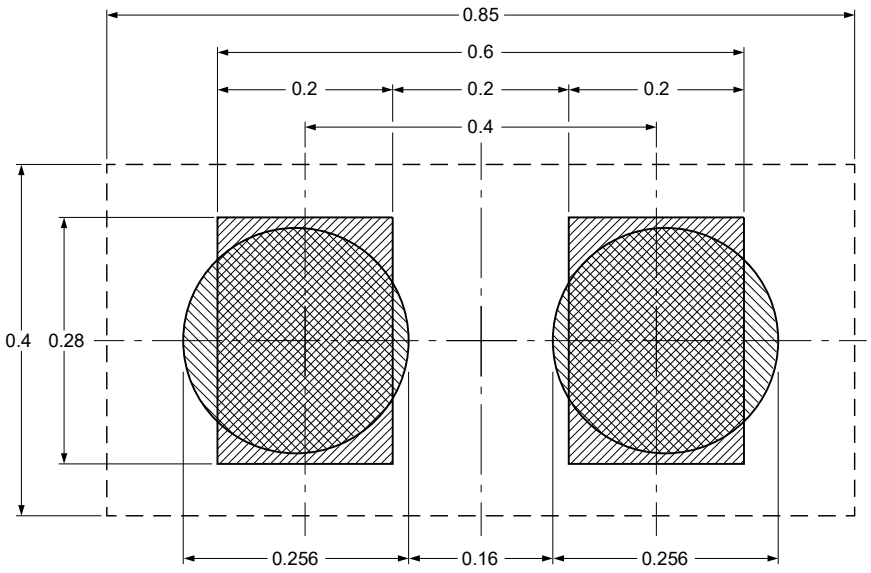
sod962-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOD962-2						~~13-07-12~~ 13-07-17

Fig. 2. Package outline DSN0603-2 (SOD962-2)

9. Soldering

Footprint information for reflow soldering of leadless ultra small package; 2 terminals **SOD962-2**



recommended stencil thickness: 0.1 mm

occupied area

solder paste

solder lands

Dimensions in mm

Issue date ~~16-02-01~~ 20-09-15

sod962-2_fr

Fig. 3. Reflow soldering footprint for DSN0603-2 (SOD962-2)

10. Revision history

Table 4. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD1V0Y1BBSF_SDS v.1	20220401	Product data sheet	-	-

11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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