UM90006

MiniLab II

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Document information

Information	Content
Keywords	MiniLab II
Abstract	MiniLab II is an evaluation platform to measure specially designed DC-to-DC-converters.This user manual describes MiniLab II and details its use in the design and evaluation of a synchronous DC-to-DC buck converter.

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1. Introduction

The need for ‘on the fly testing’ or quick evaluation of parts without setting up complicated and expensive measurement instruments is high in the semiconductor business. The main requirement is to evaluate component performance, preferably in a representative application. Making results immediately visible after starting the experiment is very useful. Since measurement instruments are often quite heavy and immobile, a light portable solution would be a nice bonus. Nexperia has managed to combine all of the above mentioned properties in MiniLab II.

MiniLab II features side-by-side comparison of two devices under test (DUT) with in-line efficiency measurements. The results are displayed straightaway on two dedicated OLED displays. Each side has separate terminals for connecting a load, however if necessary both DUTs can be daisy-chained into one combined system, while still being monitored separately. In this case, the load of the first DUT will be shut off by a load switch using a P-channel MOSFET.

The MiniLab II is an easy to use evaluation platform to measure specially designed fully operational 30 W DC-to-DC-converters with integrated control features. Both asynchronous and synchronous operation at various load conditions can be shown. Test points at all relevant circuit points make it very easy to monitor the states of the converter operation as well as the used semiconductor technology. Furthermore, the modular-based approach of the MiniLab II allows the DC-to-DC converter components such as the utilized semiconductors to easily be changed. Hence, MiniLab II is an evaluation board to benchmark technology and simultaneously a learning platform.

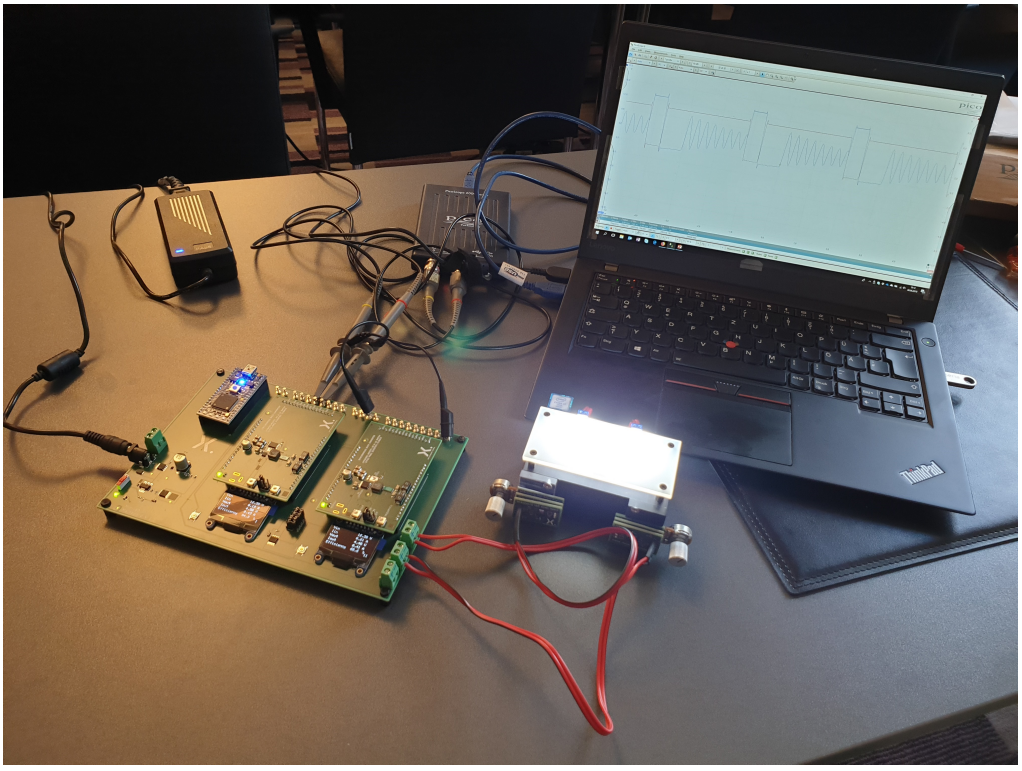


Fig. 1. MiniLab II

In this user manual the basic theory of asynchronous and synchronous DC-to-DC step-down converter is explained. At the end a synchronous DC-to-DC converter is dimensioned with Nexperia small signal MOSFET and power Schottky rectifiers. This specially designed converter is evaluated using the MiniLab II platform.

Functional block diagram

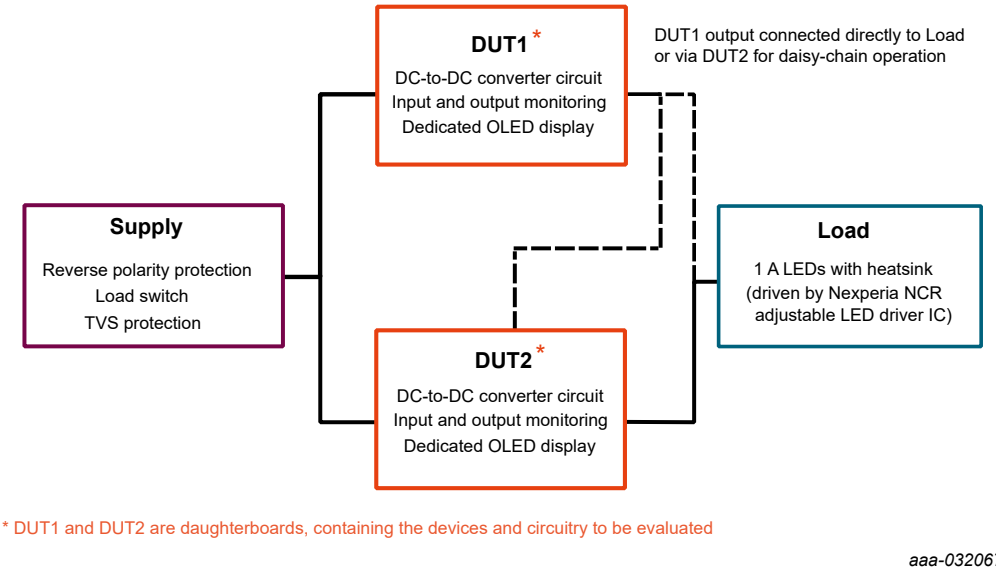


Fig. 2. Block diagram MiniLab II - DC-to-DC step-down converter

2. Quick start

Fig. 3 shows the MiniLab II mainboard PCB, with key components identified with Markers.

1. For a functional test please insert the LPC1768 in the micro controller socket (**Marker 10**). Pin 1 of the microcontroller must be inserted in the upper left corner.
2. Insert the desired DUT in corresponding socket (**Markers 6** and **7**). The analogous load interface is marked with **4** and **5** respectively.
3. Use the screw terminals to ensure proper connection from the load to the MiniLab II and watch out carefully for the polarity.
4. To run the MiniLab II in normal mode (each DUT separately) place all jumpers at **Marker 8** to the right hand side.
5. Supply the MiniLab II with power by using either the barrel jack or the screw terminal at **Marker 1**. At this point power is supplied to the micro controller and the OLED displays (Nexperia graphic identifier on both displays should been seen). For switching on the DUTs please move the main switch down (**Marker 2**). When the DUTs are active the indicator LED in left corner of the mainboard is on.
6. Use the tactile switches (**Marker 3**) to change the OLED screens. By default you can choose between input voltage and current, output voltage and current, efficiency or a summarizing screen with all of the information.
7. Once running the waveforms can monitored using an oscilloscope connected to respective turret terminals at **Marker 9**.

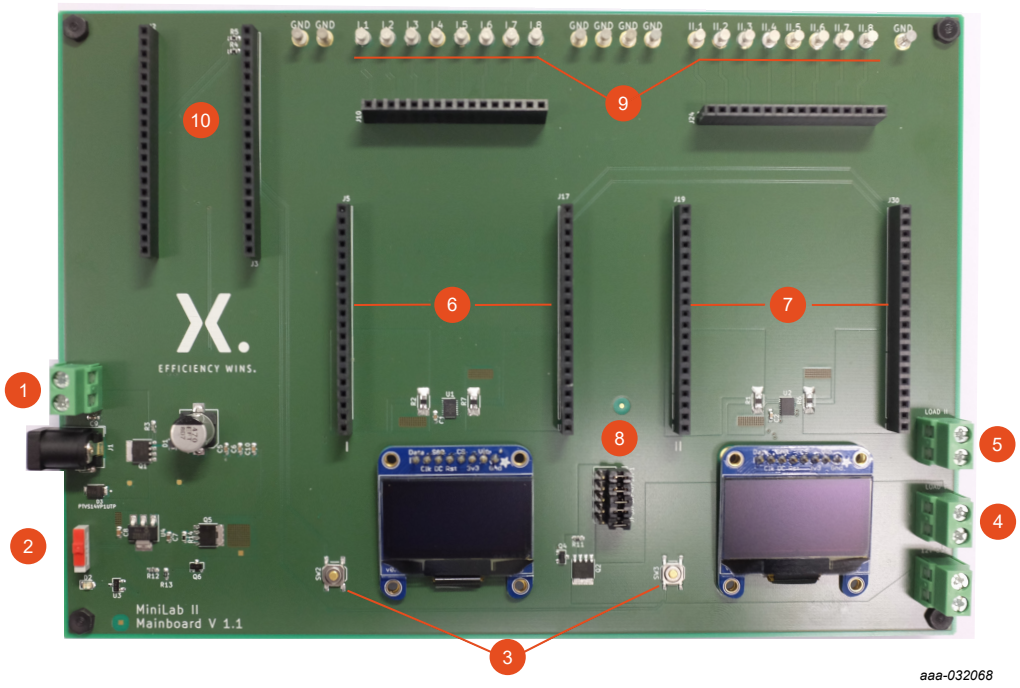


Fig. 3. MiniLab II mainboard v1.1

Table 1. Mainboard markers

Marker	Name	Function
1	DC input terminal or barrel jack	DC supply
2	DC input ON/OFF switch	Down = ON, Up = OFF
3	Switch OLEDs	Change OLED display
4	Output 1	Connect load 1
5	Output 2	Connect load 2
6	DUT1	Insert daughterboard DUT 1
7	DUT2	Insert daughterboard DUT 2
8	Output jumpers	All on LHS for daisy-chain, DUT1 to DUT2, operation. All on RHS for standalone operation
9	Test points (waveforms)	Left = DUT 1, Right = DUT 2
10	Microcontroller	Insert µC

3. Mainboard technical description

Fig. 4 shows the MiniLab II mainboard schematic diagram. The DC input of the mainboard is protected against voltage spikes through a transient voltage suppressor diode (D3) from Nexperia's PTVS14VP1UP. In addition, reverse polarity protection (RPP) is implemented to avoid damage in case of reverse connection of the power supply (Q1). There are many ways to achieve such kind of RPP. Starting with a simple diode over a bipolar transistor. For high efficiency a MOSFET is the preferred solution. This is due to the low R_{DSon} and hence the smallest voltage drop. A P-channel MOSFET is preferred because there is no need for an additional gate drive circuit. The gate is just pulled to ground. To ensure that the voltage rating between source and gate are not exceeded an additional 16 V Zener diode from the BZX series is implemented to clamp the voltage. The MOSFET (Q5) is a BUK6Y14-40P which is an automotive-qualified type.

The microcontroller (LPC1768) and power monitor ICs (U1 and U2) are supplied by a separate 5 V line, provided by a low-dropout regulator (U4). The supply line is connected to a high-side load switch which is realized with the same MOSFET as used for reverse polarity protection. The gate of the p-channel MOSFET is pulled down to ground with one of Nexperia's small signal MOSFETs which is connected to the main switch of the mainboard. This switch enables the DUTs.

Input and output of each DUT is monitored via a power monitor IC (LTC2992) and a 10 mΩ sense resistor. The power monitoring IC communicates over I^2C with the microcontroller. This microcontroller then again communicates over SPI with two monochrome OLED displays to show the measurement results. Two tactile switches are by default programmed to switch between the OLEDs displays.

DUT 1 is connected to another load switch to enable a disconnection of the load 1 in case of daisy-chain operation which is realized with the parallel jumpers (J2 - J5).

3.1. Mainboard schematic

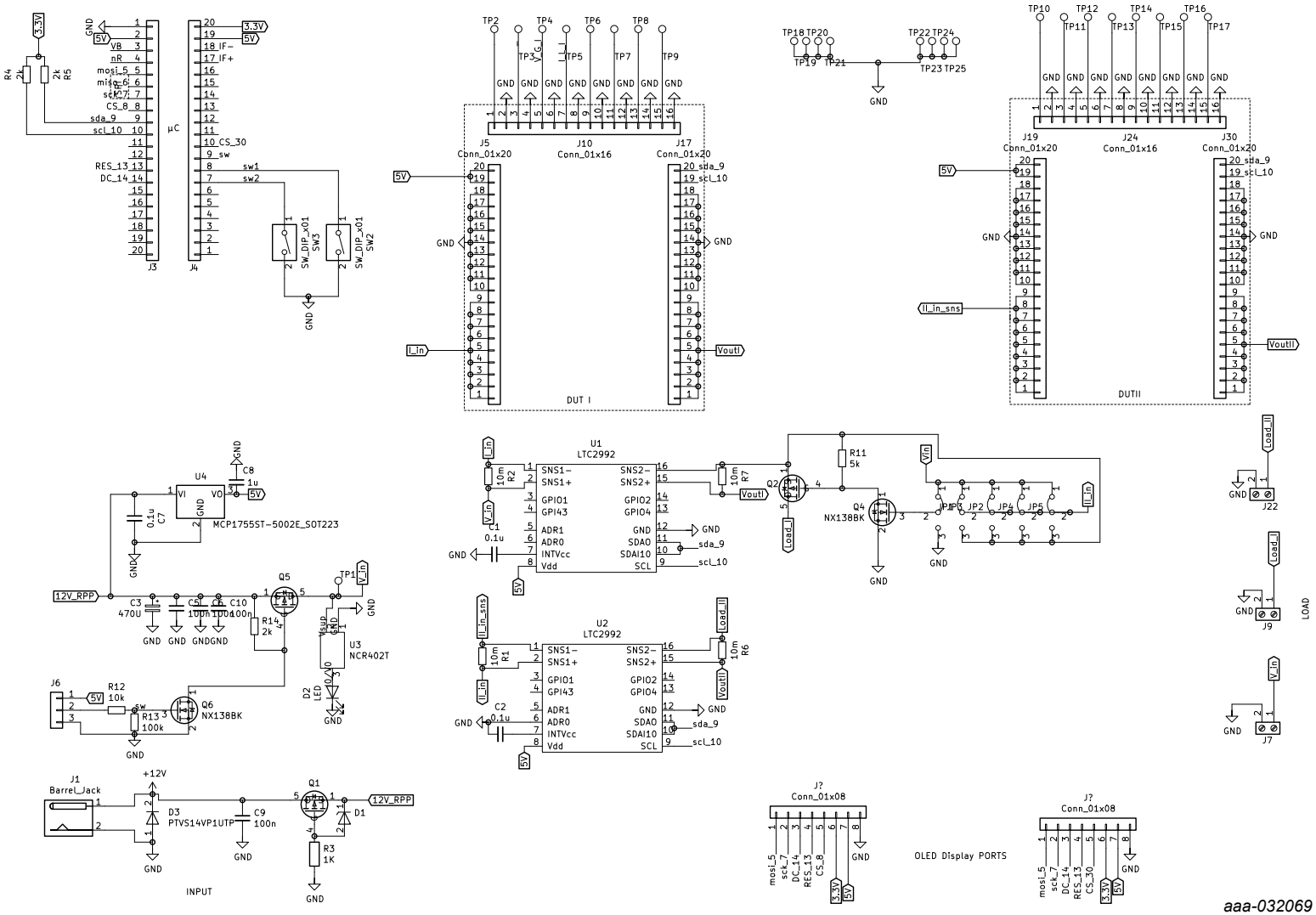


Fig. 4. MiniLab II mainboard schematic diagram

4. DC-To-DC step-down conversion (buck converter)

Theory

In application areas, where high output power and highly efficient power conversion is required, step-down converters are the preferred solution. Compared to linear regulators the cost is higher due to higher component count and additional control circuitry. Additionally, great care must be taken within the design process with respect to EMI (small input and output loops, multilayer PCB, dedicated ground plane etc.). Looking at cases where the V_{in}-to-V_{out} ratio is high. The linear regulator gets more and more inefficient because the power loss over the transistor increases proportionally with the difference between V_{in} and V_{out}. Many applications use both converters in series to provide a robust solution.

A simple step-down converter could be realized using a resistor divider consisting of a variable resistor and a load resistor. In this way the output voltage over the load resistor depends on the ratio of the resistor divider. Again, the efficiency is directly linked to the V_{out}-to-V_{in} ratio. As an improvement of this simple circuit the next step would be to replace the variable resistor with an ideal switch (SW1). Assuming continuous pulse operation of the switch the result would be a pulsed voltage at the load resistance. However, the average of this rectangular-shaped output voltage is the desired output voltage which is equal to the product of duty cycle and input voltage. A lossless filter is needed to extract the output voltage. Usually, a 2nd order LC filter is used to suppress the unwanted AC components of the chopped output voltage at the resistive output load.

A second switch needs to be added in the freewheeling path of the inductance, otherwise the coil will be destroyed. The stored magnetic energy in the inductor L is directly proportional to the current flowing through it. Without a freewheeling path and when the switch SW1 is opened, the current of the inductance has to rapidly change and thus its stored magnetic energy has to be dissipated in the switch. Usually this leads to the destruction of the switch. The resulting converter is depicted in Fig. 5a).

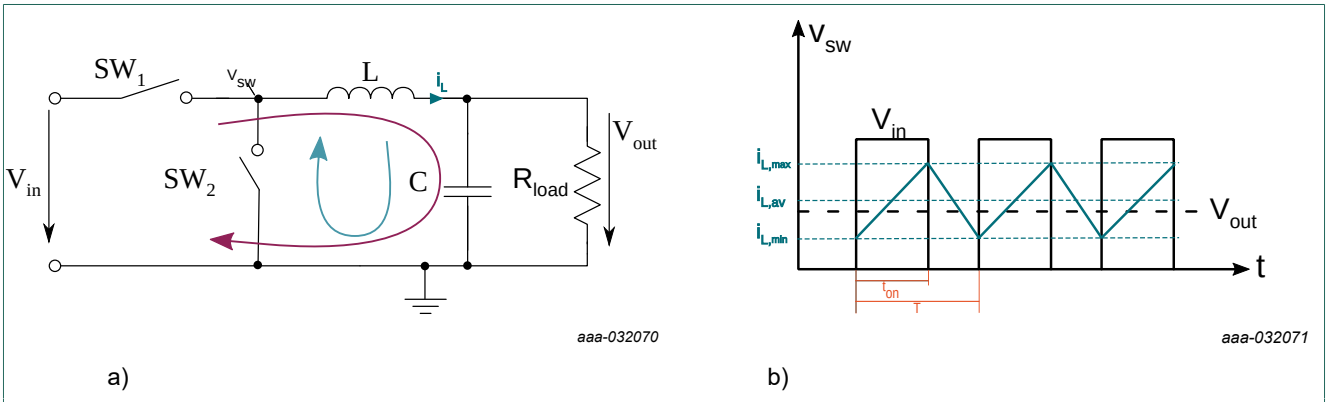


Fig. 5. Ideal step-down converter a) simplified schematic and b) CCM waveforms

The step-down converter operates in two states. The first one is the on-state (SW1 closed SW2 open). During the on-state the load is supplied by the input voltage and at the same time energy is transferred and stored in the magnetic field of the inductor (rise of load current). Applying Kirchhoff's second law the inductor voltage V_L results in Eq (1) - shown as the violet loop in Fig. 5 a).

$$V_{L(on)} = V_{in} - V_{out} \quad (1)$$

The time of the on-state is defined as t_{on}. In graph in Fig. 5 b) it is can be seen that the inductor current rises during t_{on}. The second state is the off-state and the switch positions are reversed (SW1 open SW2 closed). During the off-state the energy of the coil is transferred to the load. Again applying Kirchhoff's second law the inductor voltage results in Eq (2) - shown as the blue loop in Fig. 5 a).

$$V_{L(off)} = -V_{out} \quad (2)$$

The time t_{off} can be obtained by subtracting t_{on} from the period. During this time the inductor current is decreasing. The waveform of the inductor current is called sawtooth function.

$$\Delta I_{L(off)} = I_{L(max)} - I_{L(min)} \quad (3)$$

The ripple of this function, (see Eq 3), has an important role for the selection process of the inductor which will be discussed later in this section. Assuming energy conversion in steady state and that the inductor current is not falling below zero (Continuous Conduction Mode) it follows that the sum of on-state and off-state inductor voltage is equal to zero. It furthermore follows, that the sum of on- and off-state energy is equal to zero. Subsequently that the rising ripple current is equal to falling ripple. This can be expresses as on-state and off-state voltage:

$$(V_{in} - V_{out}) \cdot t_{on} - V_{out} \cdot (T - t_{on}) = 0 \quad (4)$$

$$V_{out} = \frac{t_{on}}{T} \cdot V_{in} = D \cdot V_{in} \quad (5)$$

The term $\frac{t_{on}}{T}$ is called duty cycle D and from now on will be referred to as that. In summary it can be stated that for an ideal step-down converter, operating in CCM, the output to input voltage ratio is determined by the duty cycle.

4.1. Part selection

Since in practice there are no ideal switches, the efficiency of the step-down converter depends on the selection of the right discrete parts and right dimensioning of the passive components.

Passive components

There are three important parameters which need to be determined before calculating values for your passive components. The first one is the output power which is needed by the load. The output power determines the input power. A good converter achieves between 88% - 95% efficiency. With that in mind the capability of the power supply should be at least 20% higher. The second one is the switching frequency f_{sw}, this determines the size of the inductance and capacitance. There is tradeoff between increasing the switching frequency and EMI (electromagnetic interference). Increasing the switching frequency can lead to increased EMI. This tradeoff must always be tailored to the application. The third parameter is the maximum allowable inductor ripple current. A good starting point in practice is $\Delta I_L = 0.2 \ldots 0.3 \times I_{out}$.

If these three parameters are determined, the inductance can be derived by integration of $V_{L(on)}$ (1) or $V_{L(off)}$ (2):

$$V_{L(on)} = L \cdot \frac{di}{dt} \quad (6)$$

$$di = \frac{(V_{in} - V_{out})}{L} dt \quad (7)$$

$$\Delta I_L = \frac{(V_{in} - V_{out})}{L} t_{on} \quad (8)$$

$$L = V_{out} \cdot \frac{(1 - D)}{\Delta I_L \cdot f_{sw}} \quad (9)$$

The boundary condition in which the step-down converter runs at the limit of the continuous mode (current goes down exactly to zero before it increases again) can be calculated by inserting $\Delta I_L = 2\ I_{av}$ in Eq 9. The ripple of the output voltage depends not only on the chosen inductor it also depends on the capacitance of the output capacitor. The voltage ripple decreases for increasing capacitance. To determine the minimum capacitance for a given voltage ripple it must be considered that the capacitor needs to be charged as much during t_{on} ($\Delta I_C = \Delta I_L/t_{on} \times t$) and discharged during t_{off} ($\Delta I_C = \Delta I_L/t_{off} \times t$). Otherwise the output voltage would change as well as the average current. Starting with:

$$i_c = C \frac{dV_c}{dt} \quad (10)$$

$$\Delta V = \frac{\Delta I_L}{C} \cdot \left[\int_0^{t_{on/2}} \frac{1}{t_{on}} \cdot t\, dt + \int_0^{t_{off/2}} \frac{1}{t_{off}} \cdot t\, dt \right] \quad (11)$$

$$\Delta V_C = \frac{\Delta I_L}{8 \cdot C \cdot f_{sw}} \quad (12)$$

For real capacitors the Equivalent Series Resistance (ESR) needs to be taken into account.

$$\Delta V_C = \Delta I_L \cdot \left(ESR + \frac{1}{8 \cdot C \cdot f_{sw}} \right) \quad (13)$$

Semiconductor components

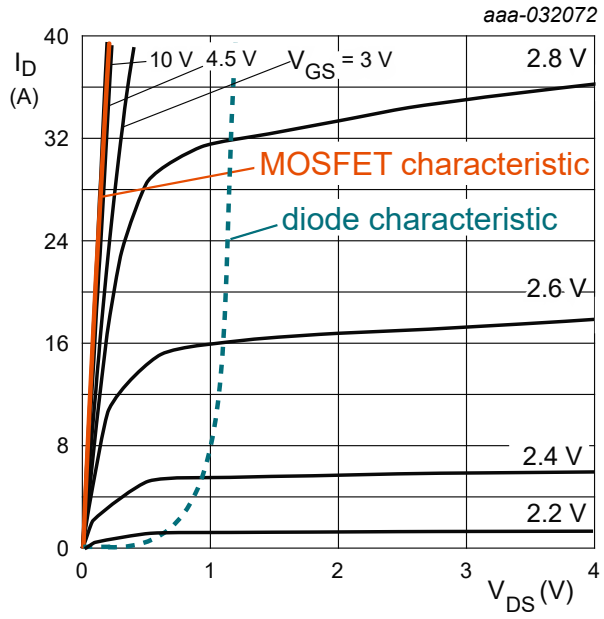
After dimensioning of the passive components the semiconductor components need to be chosen. For an asynchronous converter besides the MOSFET for SW1, a Schottky diode needs to be selected in the freewheeling path (SW2). A diode with an average forward current with sufficient safety margin should be selected. We assume that the main loss mechanism is the conduction loss of the diode. Using the forward voltage V_F of the diode, the conduction loss can be defined as:

$$P_{cond} = V_F \cdot I_{out} \cdot (1 - D) \quad (14)$$

To ensure full operation of the duty cycle the reverse recovery time of the diode needs to be significantly lower than the on time. Otherwise part of the duty cycle can't be operated

Nexperia offers a broad portfolio of power Schottky diodes in various packages. For best thermal performance diodes in CFP (Clip Flat Power) packages should be selected. These packages use clip bonding technology which allows a higher power density on occupied PCB area compared to same class wire-bonded Schottky diodes.

For synchronous conversion SW2 is replaced by a second MOSFET. There is no generally right choice between synchronous and asynchronous conversion. It always depend on the application requirements. A big advantage of the asynchronous converter is that it only needs one gate driving stage. This makes it more cost effective and reduces the driver losses which in low to medium power segment have a big impact big impact on the overall efficiency. On the other hand the forward voltage drop of a low-side MOSFET with sufficiently low R_{DSon} is much smaller compared to Schottky rectifiers of the same power class, which can be seen in Fig. 6.



T_j = 25 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

This difference in forward voltage drop means that the conduction losses of a low-side switch would be reduced by a great amount. This is especially important if the application is in the medium to high power segment.

Whenever switching takes place, charge needs to be transferred within the MOSFET or diode. In a synchronous converter there is a short time when both switches are open, this is the so-called dead-time. During this time the body diode of the low-side MOSFET is conducting which is highly undesirable since it has a high forward voltage. To improve the dead-time behavior, a medium power Schottky diode can be added in parallel to the low-side switch. This Schottky diode will also conduct during the dead-time and therefore keep the losses to minimum. It will also improve the thermal behavior due to heat spreading through both devices.

With that in mind MOSFETs can be selected. Nexperia offers a wide range of automotive qualified power MOSFETs from small leadless DFN packages for medium power applications to clip bonded LFPAK packages for higher powers.

The voltage class of the MOSFETs to be selected is determined by the maximum input voltage of the DC-to-DC converter. A sufficient safety margin should be considered. The switch has three types of losses which has to be considered when selecting a MOSFET for a switching application. Conduction losses (also referred to as I^2R losses), switching losses (mainly determined by total rise- and fall-times and switching frequency) and driver losses (which depend on total gate charge and switching frequency).

As the name of the first loss mechanism states the conduction losses of the MOSFETs can be defined as:

$$P_{cond(HS)} = I_{out}^2 \cdot R_{DSon} \cdot D \quad (15)$$

$$P_{cond(LS)} = I_{out}^2 \cdot R_{DSon} \cdot (1 - D) \quad (16)$$

As can be seen a small R_{DSon} minimizes the conduction losses of the MOSFET. The faster the MOSFET is able to switch in terms of rise and fall times the smaller the switching loss are. The switching losses can be described as:

$$P_{SW(HS)} = V_{in} \cdot I_{out} \cdot 0.5 \cdot (t_r + t_f) \cdot f_{sw} \quad (17)$$

$$P_{SW(LS)} = V_{SD} \cdot I_{out} \cdot 0.5 \cdot (t_r + t_f) \cdot f_{sw} \quad (18)$$

In Eq 18 V_{SD} is the forward voltage of the source drain diode of the MOSFET (body diode). Before the driver losses are explained, the definition of the gate charge is discussed. Fig. 7 shows the gate charge definitions which can be found in all Nexperia MOSFET data sheets.

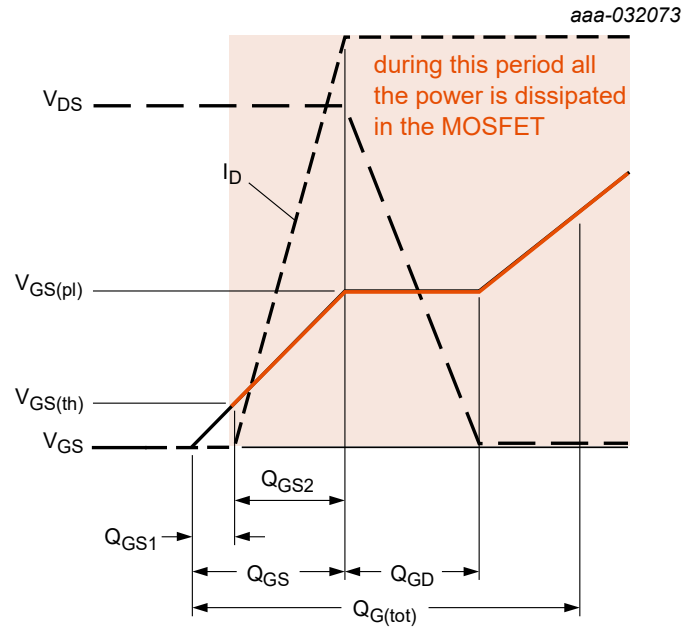


Fig. 7. Gate charge definitions waveform

Fig. 7 shows the gate to source voltage over time. The dashed lines show in parallel the development of drain current and drain to source voltage. Additionally, the distribution of the total date charge can be seen. At the point where the gate to source voltage reaches the threshold voltage the drain current starts to build up, but the drain to source voltage stays at the same potential. In other words, the MOSFET dissipates power. This process continues until the V_{GS} reaches the plateau voltage (Miller plateau). At this time the V_{DS} starts to decrease and the drain current has reached its maximum.

It is evident that the smaller the difference between plateau and threshold voltage the faster the MOSFET switches between on- and off-state and the less switching losses occur. At the point where V_{DS} has reached its minimum value the MOSFET has reached its R_{DSon}.

When turning the MOSFET off the gate drain capacitance has to be discharged. If the driver's input impedance is too high significant portion of the resulting displacement current unintentionally charges the gate source capacitance which leads to an unintended lift of the gate to source voltage.

This phenomenon is called parasitic turn on or Miller induced turn on. MOSFETs where the ratio of Q_{GD} / Q_{GS} is < 1 are immune to this effect.

The driver losses are defined as:

$$P_{driver} = \left(V_{Gate\ (HS)} \cdot Q_{G\ (HS)} + V_{Gate\ (LS)}\right) \cdot f_{sw} \quad (19)$$

Again, the switching frequency is a key parameter. To keep the driver losses small, it is advisable to use a MOSFET with a small $Q_{G(tot)}$. Since the gate charge is inversely proportional to the R_{DSon} there will always be a trade-off between these two technologies. When comparing different technologies it can be of advantage to introduce a FOM (figure of merit) which is the product of these two parameters. This FOM can be used to find the best MOSFET for the given application. For the low-side switch dead-time loss is another factor which needs to be considered. It can be calculated by:

$$P_{dead\ time\ (LS)} = V_{SD} \cdot I_{out} \cdot 2 \cdot t_{dead} \cdot f_{sw} \quad (20)$$

This loss can be improved by the factor V_{SD} / V_F when using a parallel Schottky diode to low-side switch. This is of course assuming that the during the dead-time only the Schottky diode is conducting. In reality the body diode of the low-side switch will conduct too. Regardless of that, the thermal performance of the low-side will be improved due to heat spreading between the two devices.

In summary there are two basic types of step-down conversion asynchronous and synchronous. The trade-off between those is given by comparing the loss in Eq 14 to the losses in Eq 16, Eq 17 and Eq 18. Generally, it depends strongly on the power rating and cost of the application to know which is the most suitable solution.

In the following section a synchronous step-down converter with parallel Schottky diode is designed and tested using the mainboard described in the beginning of this user manual.

4.2. Buck converter design example

The following buck converter is designed according to the guidance given in the previous chapter. The design parameters are given in table Table 2:

Table 2. Design parameters for a step-down converter

Parameter	Value	Description
V_{in}	12 V	Input voltage
V_{out}	3.3 V	Output voltage
I_{out}	4 A	Maximum output current
ΔI	0.3 A	Inductor current ripple @ duty cycle = 50%
f_{sw}	300 kHz - 1 MHz	Switching frequency

This design enables the evaluation of low switching frequencies as well as high switching frequencies. This means for inductor selection the lowest frequency is the most critical one and for switching losses calculation later on the highest switching frequency. For duty cycle and inductance we get the following results using Eq 5 and Eq 9:

$$D = \frac{3.3\ V}{12\ V} = 0.275 \tag{21}$$

$$L = \frac{3.3\ V \cdot (1 - 0.275)}{0.3 \cdot 4\ A \cdot 3 \cdot 10^5 Hz} \approx 6.8\ \mu H \tag{22}$$

Assuming that the AC portion of the RMS current is negligible. If this not the case the RMS current can be calculate the following way:

$$I_{RMS}^2 = I_{DC}^2 + \frac{\Delta I^2}{12} \tag{23}$$

MOSFETs

For the high-side and low-side switches we chose PMPB20EN, a medium power MOSFET which is suitable for 12 V automotive applications. PMPB20EN is housed in a DFN2020MD-6 package. This is a 2 x 2 mm leadless package with an exposed drain pad for optimized thermal conduction and high robustness. Additionally, it features tin-plated solderable side pads for optical solder inspection and has the following characteristics:

Table 3. PMPB20EN quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	30	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	V_{GS} = 10 V; T_{amb} = 25 °C; t ≤ 5 s	[1]	-	-	10.4	A
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 7 A; T_j = 25 °C		-	16.5	19.5	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

Table 4. PMPB20EN characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = 15 V; I_D = 5 A; V_{GS} = 10 V; T_j = 25 °C		-	7.2	10.8	nC
Q_{GS}	gate-source charge			-	1	-	nC
Q_{GD}	gate-drain charge			-	0.67	-	nC
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; I_D = 5 A; V_{GS} = 4.5 V; $R_{G(ext)}$ = 1.7 Ω; T_j = 25 °C		-	9	-	ns
t_r	rise time			-	17	-	ns
$t_{d(off)}$	turn-off delay time			-	9	-	ns
t_f	fall time			-	8	-	ns

With a voltage rating of 30 V there is enough safety margin for possible voltage spikes. This transistor is also immune against Miller induced turn on since Q_{GD} / Q_{GS} < 1. Conduction and switching losses for the high-side are:

$$P_{cond(HS)} = 4A^2 \cdot 16.5\ m\Omega \cdot 0.275\ m\Omega = 76\ mW \quad (24)$$

$$P_{sw(HS)} = 12\ V \cdot 4A \cdot 0.5 \cdot (17ns + 8\ ns) \cdot 1\ MHz = 600\ mW \quad (25)$$

For the low-side the losses are:

$$P_{cond(LS)} = 4A^2 \cdot 16\ m\Omega \cdot (1 - 0.275) = 191\ mW \quad (26)$$

$$P_{sw(LS)} = 0.8V \cdot 4A \cdot 0.5 \cdot (17ns + 8\ ns) \cdot 1\ MHz = 40\ mW \quad (27)$$

$$P_{dead\text{-}time(LS)} = 0.8V \cdot 4A \cdot 2 \cdot 20ns \cdot 1\ MHz = 128\ mW \quad (28)$$

The driver losses are then:

$$P_{driver} = 2 \cdot 5V \cdot 7.2\ nC \cdot 1\ MHz = 72\ mW \quad (29)$$

Summing up to total power loss:

$$P_{loss(tot)} = 72.6 + 191 + 600 + 40 + 128 + 72 = 1{,}103.6\ mW\ (1.1\ W) \quad (30)$$

Calculating the efficiency with:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} = 92\ \% \quad (31)$$

Schottky diode

The power loss during the dead-time can be decreased by adding a 3 A low V_F Schottky diode in parallel to the low side switch. This will also improve the switching loss of the low side switch by a factor of V_F / V_{SD}. Of course it also possible to reduce the switching frequency to reduce dead-time

and switching loss. However, this again results in larger inductors. This design covers low switching frequencies as well as high switching frequencies.

For the Schottky diode we use PMEG40T30ER in CFP3 package. The CFP package line contains clip bond technology for high thermal robustness and reliability. PMEG40T30ER has the following characteristics:

Table 5. PMEG40T30ER quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{F(AV)}$	average forward current	δ = 0.5; square wave; f = 20 kHz; T_{sp} ≤ 150 °C		-	-	3	A
V_R	reverse voltage	T_j = 25 °C		-	-	40	V
V_F	forward voltage	I_F = 3 A; T_j = 25 °C; pulsed	[1]	-	460	525	mV
I_R	reverse current	V_R = 10 V; T_j = 25 °C; pulsed	[1]	-	5	16	µA
		V_R = 40 V; T_j = 25 °C; pulsed	[1]	-	8	28	µA

[1] Very short pulse, in order to maintain a stable junction temperature.

Table 6. PMEG40T30ER characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_d	diode capacitance	V_R = 1 V; f = 1 MHz; T_j = 25 °C		-	560	-	pF
		V_R = 10 V; f = 1 MHz; T_j = 25 °C		-	240	-	pF
t_{rr}	reverse recovery time step recovery	I_F = 0.5 A; I_R = 0.5 A; $I_{R(meas)}$ = 0.1 A; T_j = 25 °C		-	18	-	ns
	reverse recovery time ramp recovery	dI_F/dt = 200 A/µs; I_F = 6 A; T_j = 25 °C		-	12	-	ns

The low-side losses will change accordingly to:

$$P_{SW(LS)} = 0.46\,V \cdot 4\,A \cdot 0.5 \cdot (17\,ns + 8\,ns) \cdot 1\,MHz = 0.7\,mW \quad (32)$$

$$P_{dead\text{-}time} = 0.46\,V \cdot 4\,A \cdot 2 \cdot 20\ ns \cdot 1\,MHz = 22.1\,mW \quad (33)$$

And there for the total losses to:

$$P_{loss(tot)} = 72.6 + 191 + 600 + 73 + 23 + 72 = 1{,}031.6\,mW\,(1.03\,W) \quad (34)$$

The overall efficiency increases by approximately 1% to 93%.

4.3. Buck converter schematic

Fig. 8 shows the schematic diagram of the synchronous buck converter designed in the previous section.

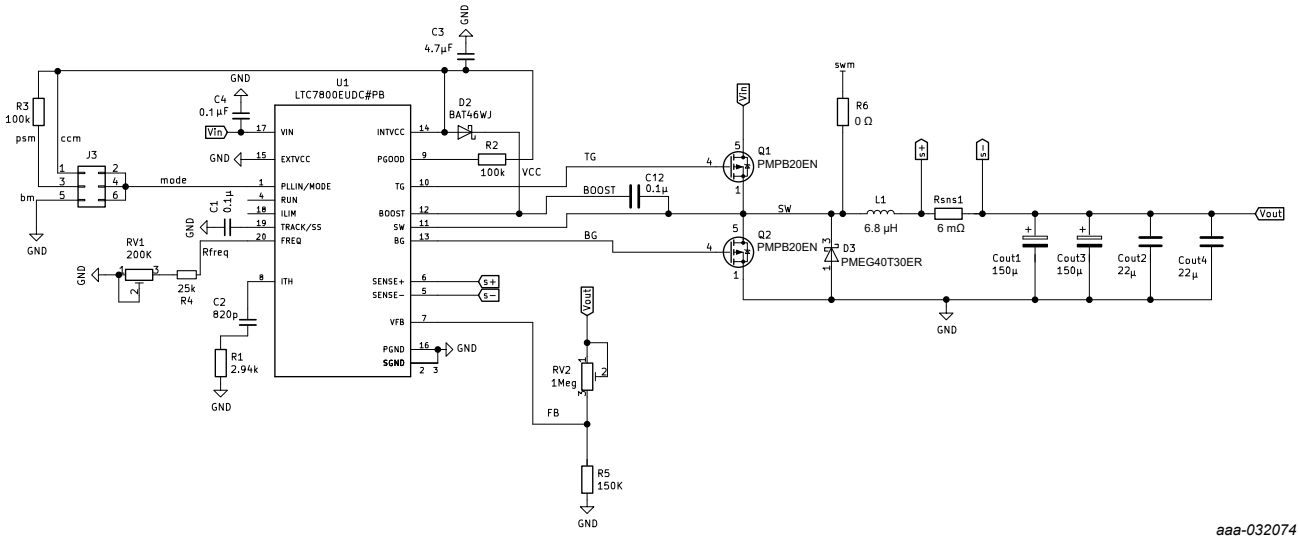


Fig. 8. Synchronous buck converter schematic diagram

The controller IC is the LTC7800 from Analog Devices. It contains the gate drivers as well as feedback control and inductor sensing circuits. For proper gate driving a bootstrap circuit is implemented with D2 (BAT46) and C12. The feedback pin contains a 0.8 V precision voltage. Using RV2 the duty cycle of the controller can be changed and thus the output voltage. The frequency can be adjusted via a fixed resistor between 300 kHz and 2.2 MHz. Via RV1 it is possible to change the frequency in that range.

It is possible to vary the operation mode between forced continuous conduction mode, pulse skipping mode and burst mode using J3. The burst mode is the most efficient operation mode for low load conditions since the controller switches only if a output voltage threshold is detected.

4.4. PCB layout

For the design a 4 layer FR4 PCB is chosen. The second layer is a ground plane and connected to enough VIAs to the other layers. This is done to improve the EMI behavior. The third layer is used to route the measurements leads to the mainboard. The controller and his peripheral circuitry is placed on the bottom side as can be seen in Fig. 11. The controller is placed directly under the switching MOSFETs to keep the traces as short as possible to avoid stray inductances. The actual buck converter is placed on the top side. For a good EMI the input and output loops need to be kept as small as possible. In other words the input capacitor needs to be placed as close to the high-side switch as possible (Fig. 10). Same is valid for the output capacitor. The most critical point is the switching node. Here it is advised to keep commutation loop between the high-side switch, low-side switch, inductor and output capacitor as small as possible. Also the trace width of the high power traces should be appropriate for conducting high currents. The Schottky diode is placed very closely to low-side switch to keep stray inductance to a minimum and conserve the efficiency benefit with which the Schottky diode comes with. The resulting layout is shown in Fig. 9, Fig. 10, Fig. 11 and Fig. 12.

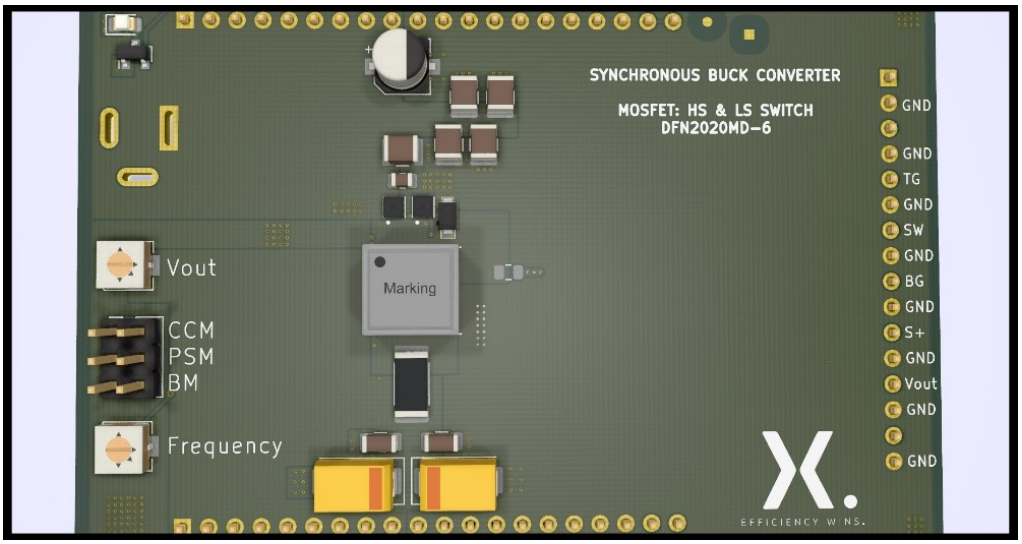


Fig. 9. Buck converter PCB layout: top side

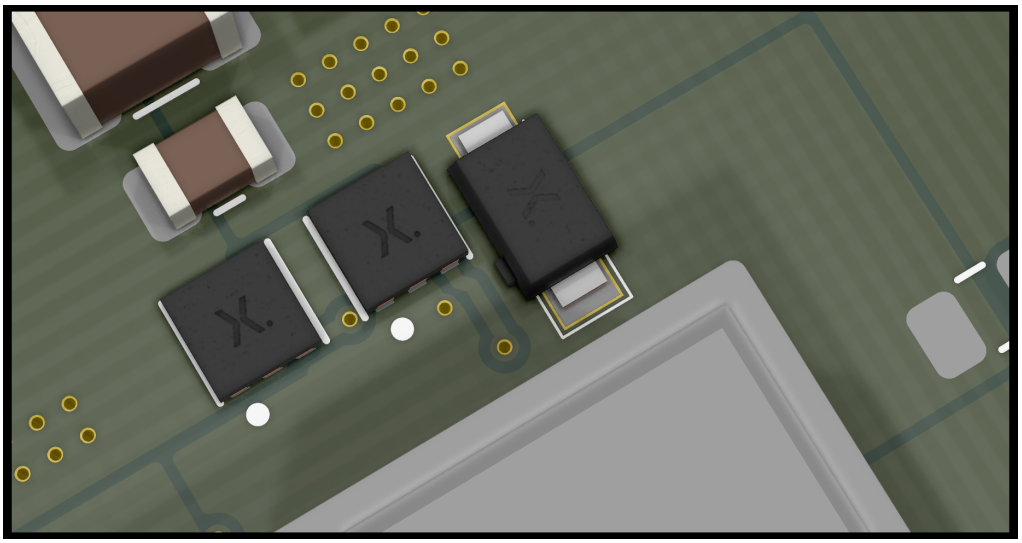


Fig. 10. Buck converter PCB layout: top side detail showing MOSFETs and Schottky diode

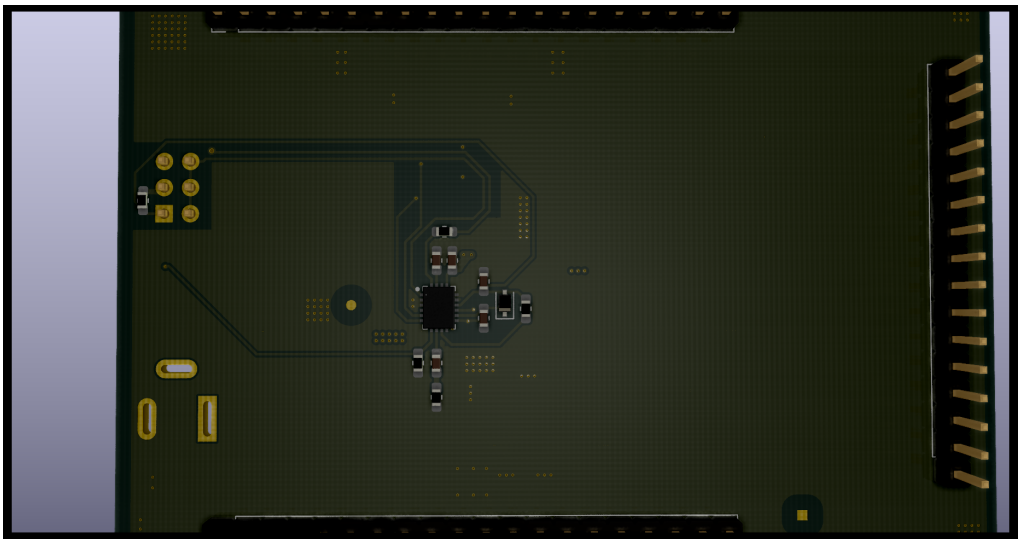


Fig. 11. Buck converter PCB layout: bottom side

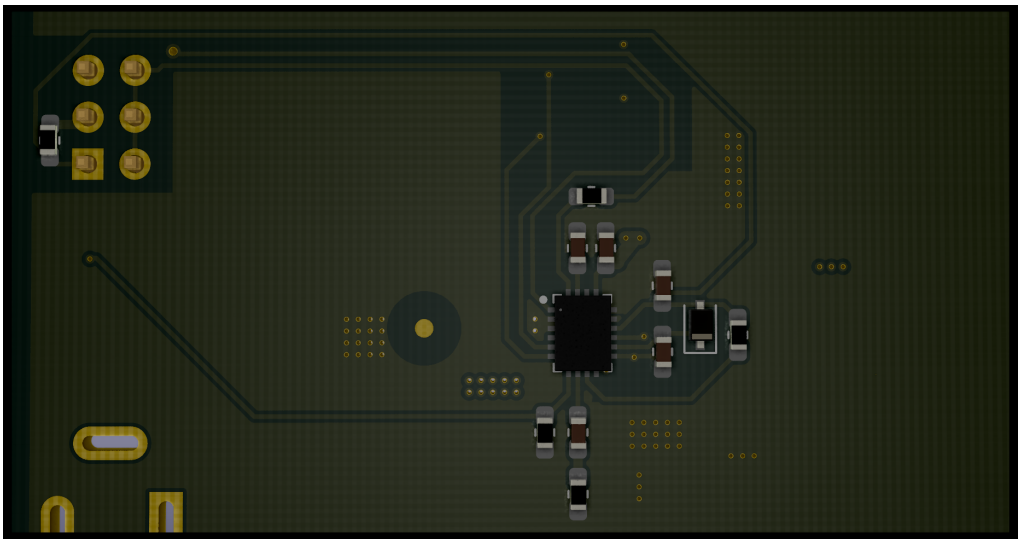


Fig. 12. Buck converter PCB layout: bottom side detail showing controller IC

5. Measurement results

The synchronous buck converter described in the previous sections is inserted in the first test socket of the MiniLab II mainboard (DUT1 socket).

Mainboard power is supplied by a 12 V, 3 A DC power supply. Oscilloscope probes are connected to the top and bottom gate test points on the mainboard (I.3 and I.5). Using the potentiometers on the buck converter board, the output voltage is set to 3.3 V and the frequency to 750 kHz.

The operation is set to forced continuous mode.

No load

The recorded waveforms for the no load case can be seen in Fig. 13. The high-side gate is represented by the yellow trace and the low-side gate by the pink trace (measured against ground). Because the source potential of the low-side is ground the actual 5 V gate drive waveform is recorded and it can be seen that the turn on ringing is very small.

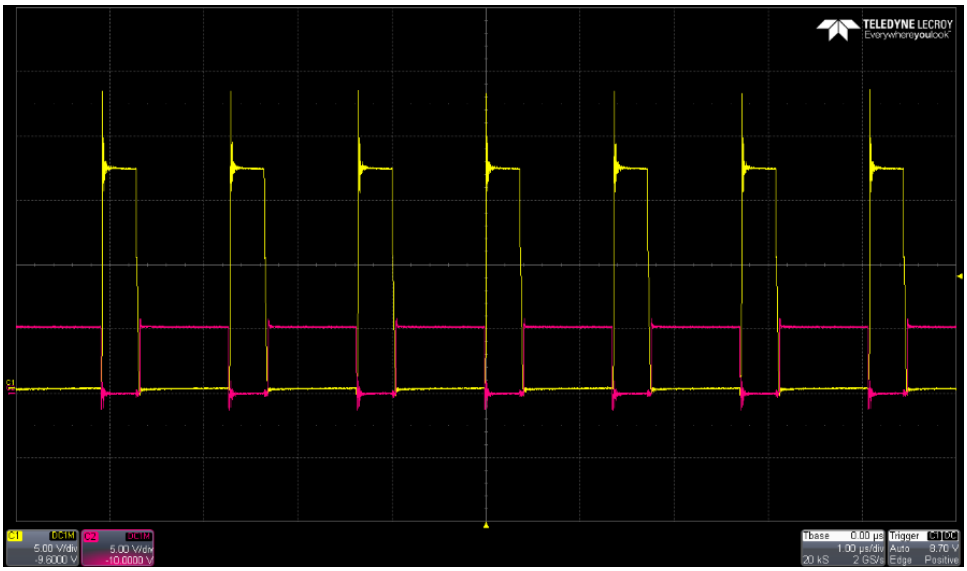
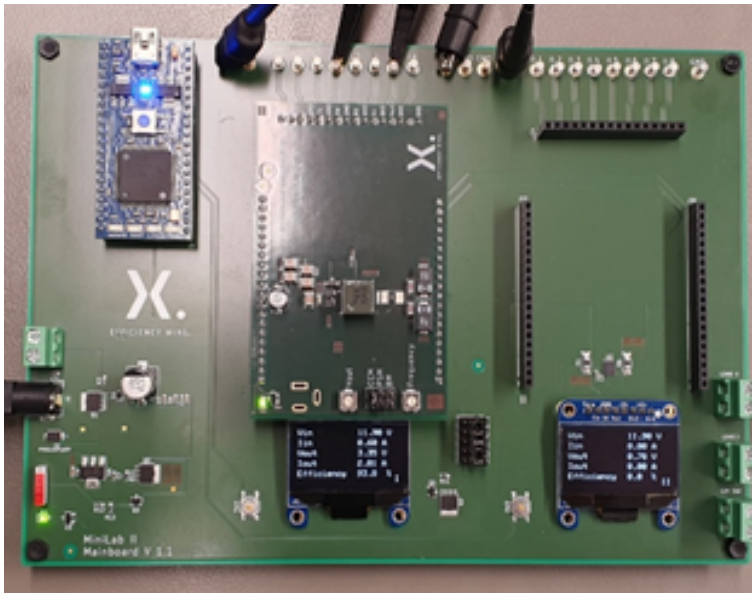


Fig. 13. Continuous mode gate waveforms: high-side (yellow), low-side (pink)

2 A load

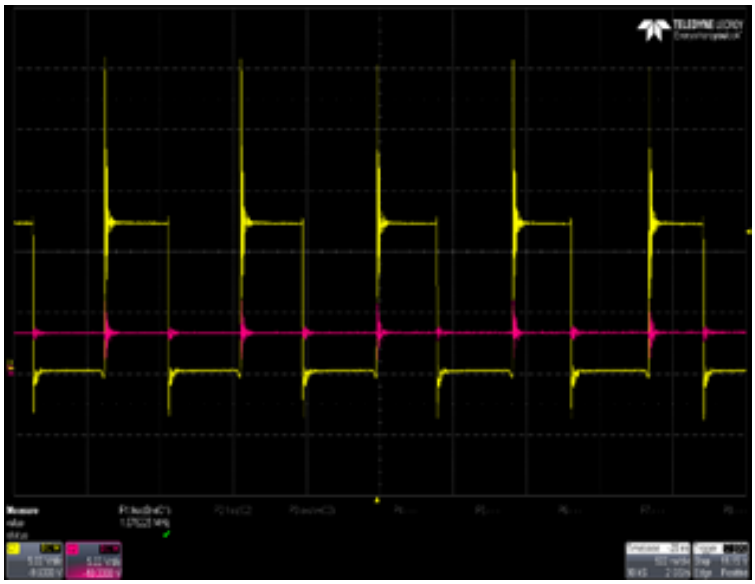
In the next measurement a DC electronic load is connected to the load I interface. The DC load is set to 2 A. The frequency is increased to 1 MHz. The oscilloscope probes are connected to I.4 and I.7 which represent the switching node and the output voltage respectively; see Fig. 14 and Fig. 15.

The efficiency of the buck converter is 93.8%.



I_I = 2 A; V_{out} = 3.3 V; f = 1 MHz

Fig. 14. MiniLab II set up with step-down converter board

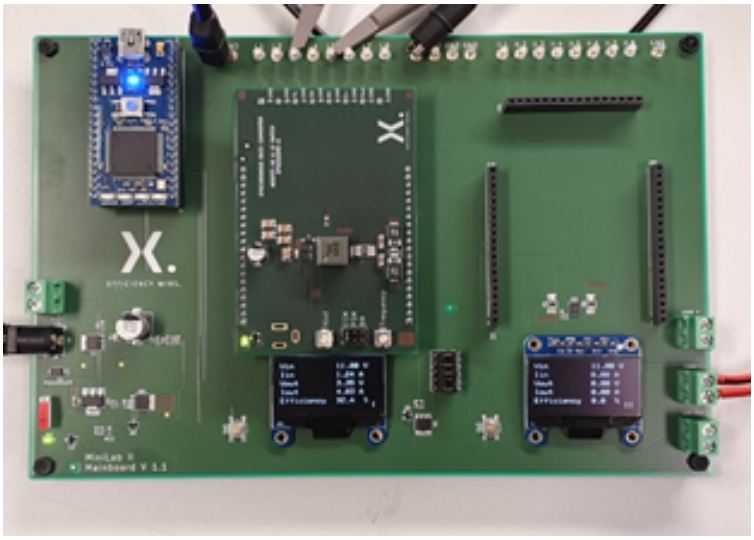


I_I = 2 A; V_{out} = 3.3 V; f = 1 MHz

Fig. 15. Switching node (yellow) and output voltage (pink) waveforms

4 A load

The experiment is repeated with a 4 A load current. The frequency is set to 750 kHz. See Fig. 16 and Fig. 17.



I_l = 4 A; V_{out} = 3.3 V; f = 750 kHz

Fig. 16. MiniLab II set up with step-down converter board

I_l = 4 A; V_{out} = 3.3 V; f = 750 kHz

Fig. 17. Switching node voltage waveform

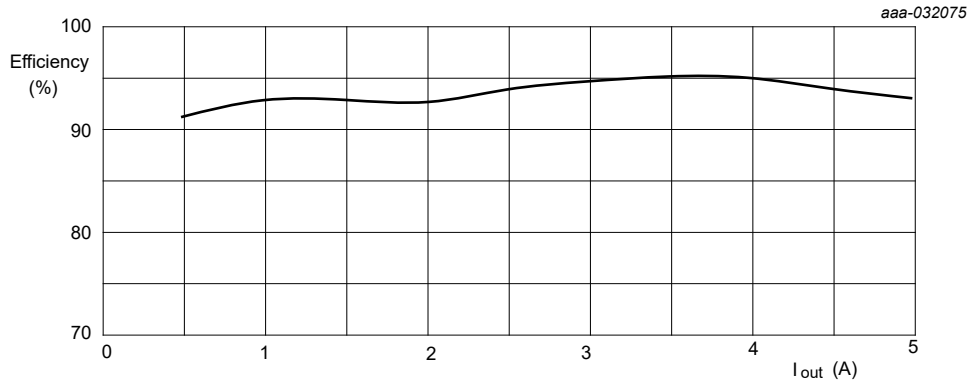
The resulting efficiency of the converter at this operation point is 92.4%, which corresponds very well with the calculated efficiency. Although input and output capacitance losses as well as inductor losses were neglected.

Efficiency as a function of output current

As a last experiment the buck converter output voltage is set to 4.7 V and the frequency to 1 MHz.

The load current is than stepped from 0.5 to 5 A Fig. 18 At 5 A the temperature of the high-side switch was 48 °C, the temperature of low-side switch 45.5 °C and the temperature of the Schottky diode was 35.5 °C.

The efficiency of the buck converter is always over 90% and has its maximum efficiency at 4 A with 95%.



V_{out} = 4.7 V; f = 1 MHz; PMPB20EN with PMEG40T30ER

Fig. 18. Efficiency as a function of output current

6. Summary

This document describes the principles for DC-to-DC conversion step down conversion.

A reference design for a synchronous DC-to-DC converter was presented with the most important design aspects, such as power dissipation in the switching stage. Highly efficient medium power DC-to-DC converters can be designed with Nexperia small-signal MOSFETs. For optimized efficiency, synchronous DC-to-DC converters with parallel Schottky diodes to the low-side switch are recommended. Also for this topology, Nexperia can offer suitable power Schottky diodes in various packages.

7. Revision history

Table 7. Revision history

Revision number	Date	Description
1.1	20200918	Initial version

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