**Important notice**

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.philips.com/ or http://www.semiconductors.philips.com/, use **http://www.nexperia.com**

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:
- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved
Should be replaced with:
- **© Nexperia B.V. (year). All rights reserved**.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

# NXP's AXP translators

## Introduction

In order to reduce power dissipation in electronic applications there is a trend toward lower supply voltages. A consequence of this trend is a necessity to interface in modular designs between applications at different supply voltages.

NXP has added innovative voltage level translating devices to its existing Advanced eXtremely low Power (AXP) logic family to further improve its portfolio of translator products. These translating gates ensure interface compatibility of new lower voltage designs to existing products without serious power dissipation penalties.

## Requirements of low power logic families

As general-purpose components, logic devices are used at different frequencies and power supply voltages in a multitude of applications. This large diversity has produced the need to express a single parameter that can be used in determining the power dissipation of a device in a given application. Looking at the components of power dissipation, we can better understand the evolution that has occurred within discrete logic to reduce it.

### 1. Quiescent power dissipation

Theoretically, when a CMOS device is not switching and the input levels are GND or $V_{CC}$, no direct MOS transistor current path exists between $V_{CC}$ and GND. In practice, however, thermally generated minority carriers allow a very small leakage current to flow between $V_{CC}$ and GND. This leakage current is typically a few nano-ampere, and produces the quiescent supply current $I_{CC}$, as it is represented in device datasheets. To calculate maximum quiescent power dissipation use:

$$PD_Q = V_{CC} \times I_{CC} \qquad (1)$$

### 2. Static power dissipation

In the case where full swing input levels (GND or $V_{CC}$) cannot be applied, a direct MOS transistor current path can exist between $V_{CC}$ and GND, which leads to additional supply current through the input buffer and results in additional power dissipation. $\Delta I_{CC}$ represents this additional current due to an input level of $V_{CC}$ – 0.6 V. To calculate the static power dissipation use:

$$PD_{STAT} = V_{CC} \times (I_{CC} + n\Delta I_{CC}) \qquad (2)$$

Where n represents the number of inputs held at $V_{CC}$ – 0.6 V.

**3. Dynamic power dissipation**

When clocking a CMOS device, the charging and discharging of on-chip parasitic and load capacitance dissipates power. Further power dissipation occurs at the point the output switches, when both the p-channel and the n-channel transistors are partially conducting. This transient energy loss is typically only 10% of that due to parasitic capacitance. Due to the linear relationship between power dissipation and frequency in CMOS devices, the model of the device for power dissipation calculations is a capacitance ($C_{PD}$)

The total dynamic power dissipation per device is:

$$PD_{DYN} = \sum(C_{PD} V_{CC}^2 f_I) + \sum(C_L V_{CC}^2 f_O) \qquad (3)$$

where:

- $C_{PD}$ is the power dissipation capacitance per buffer
- $f_I$ is the input frequency
- $f_O$ is the output frequency
- $C_L$ is the total external load capacitance per output.

**4. Total power dissipation**

Combining the components of static and dynamic power dissipation results in an equation for the total power dissipation:

$$PD = V_{CC} \times (I_{CC} + n\Delta I_{CC}) + \sum(C_{PD} V_{CC}^2 f_I) + \sum(C_L V_{CC}^2 f_O) \qquad (4)$$

Assuming that the frequency of an application is constant, it becomes clear from equation four that to reduce total system power dissipation, system designers need to lower the supply voltage $V_{CC}$ as much as they can, and where possible drive all digital inputs with $V_{CC}$ or GND.

The discrete logic supplier must offer logic families that provide the required speed performance at the lower voltages, have the lowest power dissipation capacitance ($C_{PD}$) possible and have inputs that present the lowest possible capacitive load ($C_L$).

In 2005, NXP released the Advanced Ultra-low Power CMOS (AUP) logic family. AUP is the lowest power logic family suitable for 3.3 V applications; it is fully specified for applications from 1.1–3.6 V, allowing the migration of many applications from the 3.3V node to 1.8V and beyond.

In 2012 NXP logic released the Advanced eXtremely low Power CMOS (AXP) logic family. AXP is the lowest power logic family suitable for 2.5 V applications; it is fully specified for applications from 0.75–2.75 V, allowing the migration of many applications from the 1.8V node to 1.2V and beyond. It provides the lowest propagation delay of all low power families, and critically, it provides system designers with the lowest $C_{PD}$, typically just 2.9 pF, which is more than a 50% reduction when compared to competing low voltage / low power families.

Another power saving feature is the low capacitance of AXP inputs. The capacitive load seen by any device driving an AXP input is up to 40% less than when driving other low voltage families, leading to a dynamic power dissipation savings at the system level. Recognizing that it is not always possible to drive inputs at $V_{CC}$ and GND, NXP has also designed the AXP inputs to have very low $\Delta I_{CC}$.

When driving a push-pull logic input, a long output transition will lead to higher cross bar current through the input, and thus increased system power dissipation. To avoid this situation, the output transition time must be reduced. However, doing so in an uncontrolled manner can lead to high dV/dt events that result in reflections, signal integrity issues and in some cases EMC issues. Unlike other low voltage families that utilize low current drive outputs, AUP and AXP outputs incorporate edge rate feedback to ensure minimal power dissipation through the driven input buffer without jeopardizing signal integrity.

### AXP translators—supporting modular designs

From a time-to-market perspective, it is often necessary to re-use previously tested and qualified circuits instead of completely redeveloping them. In modular designs, this may limit the supply voltage options available to the designer. Although it is possible to develop a newer circuit at 1.8 V, a requirement may be to interface to existing solutions at 3.3 V or 5.0 V. A result of this situation could be decisions to:

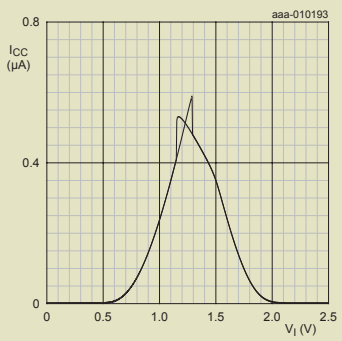
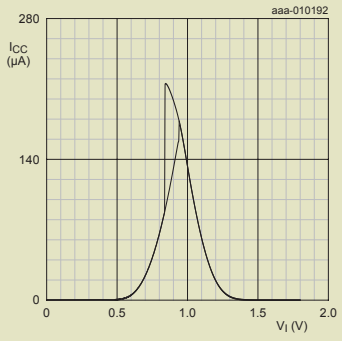
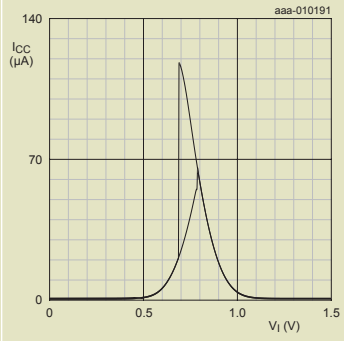
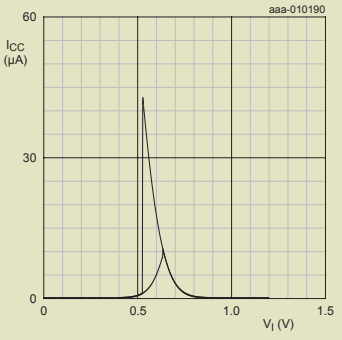
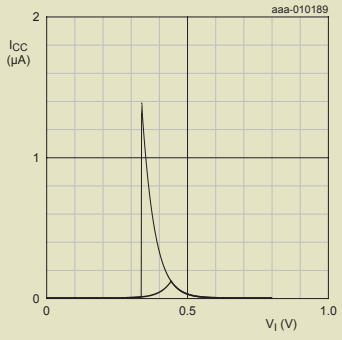
- continue to use the higher voltage with its 83% (3.3 V) or 178% (5.0 V) higher power dissipation penalty
- use a supply voltage level compatible with the switching levels of the 3.3 V existing solution and accept a higher dissipation due to $\Delta I_{CC}$.

Neither of these approaches are attractive from a power dissipation standpoint. To enable low power designs that are compatible with existing modular solutions, NXP has introduced its portfolio of AXP translating gates and buffers. These low power dual supply devices combine the 0.7 – 2.75 V AXP input stage with a higher voltage, low noise 1.2 – 5.5 V output stage.

### Inputs

The AXP translators use the existing AXP inputs. These are fully specified for supply voltage ranges of 2.3 – 2.7 V, 1.65 – 1.95 V, 1.4 – 1.6 V, 1.1 – 1.3 V and 0.75 – 0.85 V. The ESD protection circuit used results in the input being over voltage tolerant to 2.75 V. This tolerance permits the application of input signals that exceed the supply voltage. The input options include Schmitt-trigger inputs and Schmitt-trigger action inputs. Schmitt-trigger action makes the input tolerant of slower input transition rates. Hysteresis is not specified, but the input can tolerate input transition rise and fall rates of 200 ns/V. Schmitt-trigger inputs include an input hysteresis specification and have no restriction on input transition rates. Table 1 shows the typical characteristics of the Schmitt-trigger action input; Table 2 shows the typical characteristics of the Schmitt-trigger input.

## Table 1. Typical Schmitt-trigger action input characteristics of AXP Translators

| $V_{CC}$ = 2.5 V | $V_{CC}$ = 1.8 V | $V_{CC}$ = 1.5 V |
|---|---|---|
|  |  |  |
| **$V_{CC}$ = 1.2 V** | **$V_{CC}$ = 0.8 V** | |
|  |  | |



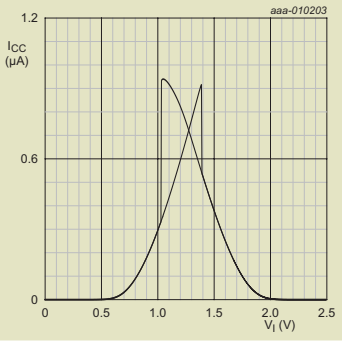
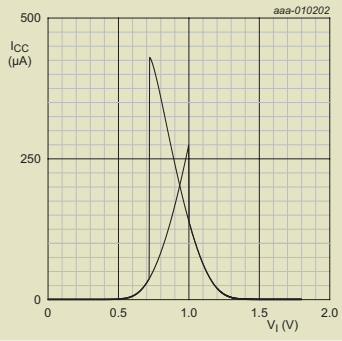
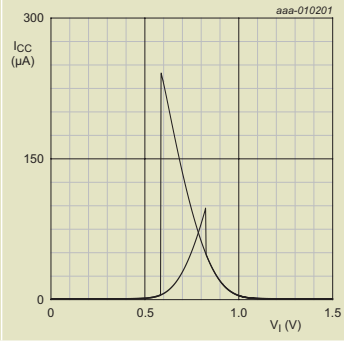
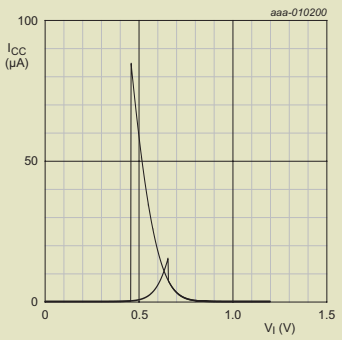
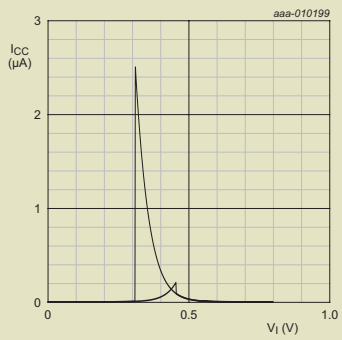








## Table 2. Typical Schmitt-trigger input characteristics of AXP Translators

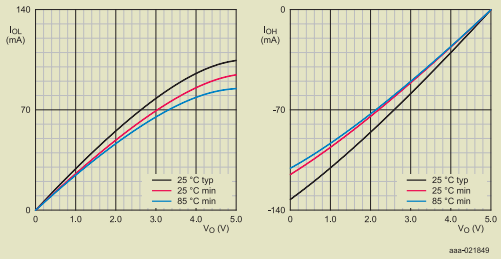
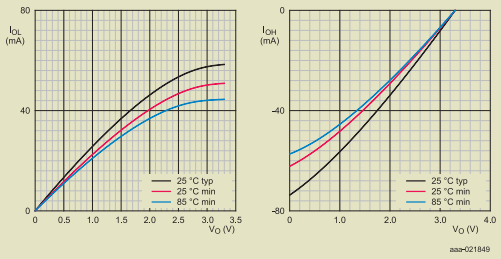
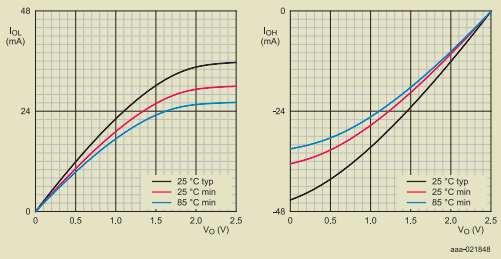
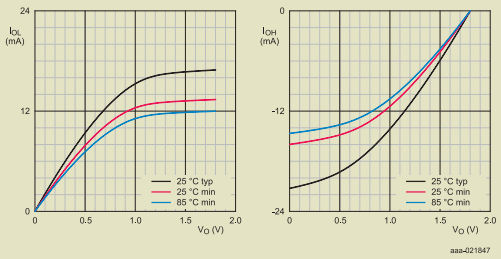
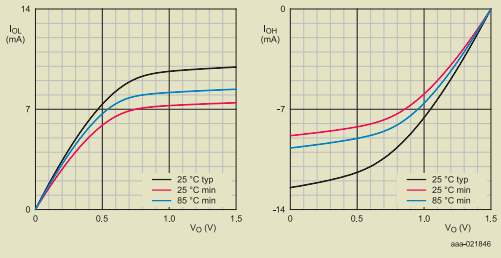
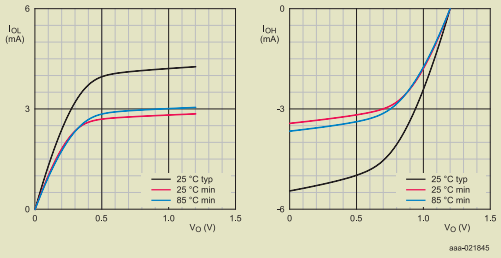
| $V_{CC}$ = 2.5 V | $V_{CC}$ = 1.8 V | $V_{CC}$ = 1.5 V |
|---|---|---|
|  |  |  |
| **$V_{CC}$ = 1.2 V** | **$V_{CC}$ = 0.8 V** | |
|  |  | |

The use of AXP inputs facilitates interfacing to lower voltage outputs without the excessive $\Delta I_{CC}$ due to mismatch between the input HIGH logic level and supply voltage.

### Outputs

AXP translators incorporate a newly developed output structure to enable interfacing to higher voltage inputs. The output is fully specified for supply voltage ranges of 4.5–5.5 V, 3.0–3.6 V, 2.3–2.7 V, 1.65–1.95 V and 1.4–1.6 V. To support partial power down mode, the output features $I_{OFF}$, which ensures there is no current leakage path through the outputs when the device supply voltage is set to 0 V. Table 3 shows the output characteristics of AXP translators.

**Table 3. Typical output characteristics of AXP Translators**

| $V_{CC}$ = 5.0 V | $V_{CC}$ = 3.3 V |
|---|---|
|  |  |
| **$V_{CC}$ = 2.5 V** | **$V_{CC}$ = 1.8 V** |
|  |  |
| **$V_{CC}$ = 1.5 V** | **$V_{CC}$ = 1.2 V** |
|  |  |

### Low power dissipation and input capacitance

The use of NXP's state-of-the-art C050 process ensures that AXP translators have the lowest parasitic capacitance possible. This approach results in a typical input capacitance of 0.5 pF, or 50% of that of leading AVC 3 V translator solutions, and 25% of leading LVC 5 V translator solutions. The effect on the power dissipation capacitance is equally as impressive. AXP translators are modelled as a 0.8 pF capacitance on the input supply ($C_{PDI}$) and a 7.6 pF capacitance on the output supply ($C_{PDO}$). By comparison, existing leading 3 V solutions have $C_{PDI}$ and $C_{PDO}$ of 2 pF and 17 pF, respectively; existing leading 5 V solutions have $C_{PDI}$ and $C_{PDO}$ of 4 pF and 18 pF, respectively. These values are used with equation 5 to estimate power dissipation.

$$PD_{DYN} = \sum(C_{PDI} V_{CCI}^2 f_I) + \sum((C_L + C_{PDO}) V_{CCO}^2 f_O) \qquad (5)$$

Table 4 shows a comparison of dynamic power dissipation of leading translator families.

**Table 4. Comparison of power dissipation capacitance of leading translator families**

| | LVC | | AVC | | AXP | |
|---|---|---|---|---|---|---|
| $V_{CC}$ | $C_{PDI}$ | $C_{PDO}$ | $C_{PDI}$ | $C_{PDO}$ | $C_{PDI}$ | $C_{PDO}$ |
| 0.8 V | — | — | 1 | 9 | 0.5 | — |
| 1.2 V | — | — | 2 | 11 | 0.6 | 6.9 |
| 1.5 V | — | — | 2 | 11 | 0.7 | 6.9 |
| 1.8 V | 2 | 15 | 2 | 12 | 0.8 | 6.9 |
| 2.5 V | 3 | 16 | 2 | 14 | 1.0 | 7.0 |
| 3.3 V | 3 | 16 | 2 | 17 | — | 7.2 |
| 5.0 V | 4 | 18 | — | — | — | 7.6 |

### Low noise characteristics

Typically, at a supply voltage of 0.7 V, the input switching threshold will be 350 mV. As a result, when translating between high and low voltage domains, it is important to consider the effect of high voltage output noise on switching of the low voltage input. Figure 1 shows the noise on an output set LOW when another output transitions LOW to HIGH and HIGH to LOW.

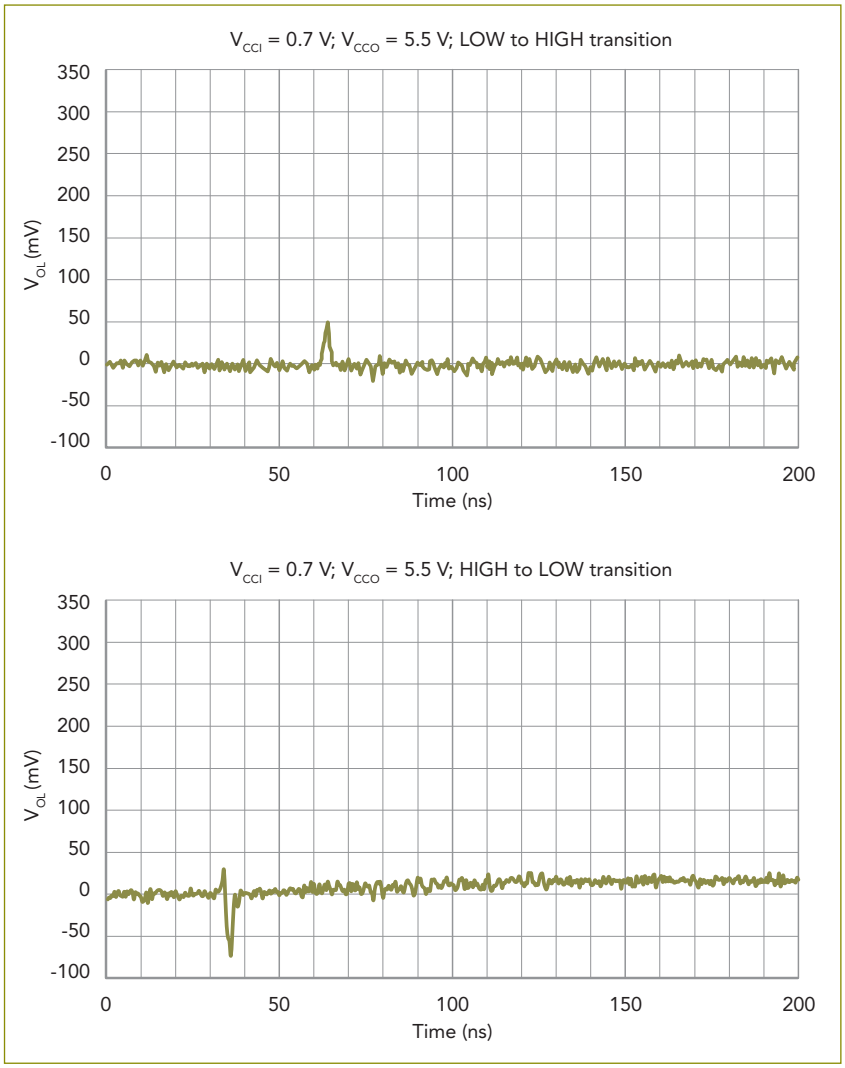



Figure 1 Noise characteristics of AXP Translators

$V_{OL(p)}$ is the maximum value of $V_{OL}$. It represents the change in the GND level due to the output switching. It is important to minimize this value, as the GND level is the reference point for the input switching level. It can be seen that the worst case $V_{OL(p)}$ for AXP translators is 50 mV, much less than the > 350 mV required to switch the input.

### Reduced power and footprint

AXP translators are available in industry standard leaded PicoGate and leadless MicroPak packages, making them suitable for volume constrained (area and height) portable applications such as smart phones and tablet PCs.

The lower gate count Mini logic products reduce time-to-market by making it easy to implement last-minute changes. They also improve the cost-effectiveness of crowded layouts, by simplifying routing and eliminating dependencies in intricate line-layout patterns. Table 2 shows the AXP translator packages currently available.

## Table 5. Package options for AXP translating gates

| Package suffix | GW | GX | GW | GM | GN | GS | DC |
|---|---|---|---|---|---|---|---|
| | 5-pin | 5-pin | 6-pin | 6-pin | 6-pin | 6-pin | 8-pin |
| |  |  |  |  |  |  |  |
| Package | SOT353 | SOT1226 | SOT363 | SOT886 | SOT1115 | SOT1202 | SOT765-1 |
| Width (mm) | 2.10 | 0.80 | 2.10 | 1.00 | 1.00 | 1.00 | 3.10 |
| Length (mm) | 2.00 | 0.80 | 2.00 | 1.45 | 0.90 | 1.00 | 2.00 |
| Height (mm) | 1.00 | 0.35 | 1.00 | 0.50 | 0.35 | 0.35 | 1.00 |
| Pitch (mm) | 0.65 | 0.50 | 0.65 | 0.50 | 0.30 | 0.35 | 0.50 |

| Package suffix | GT | GN | GS | DP | GU | GF |
|---|---|---|---|---|---|---|
| | 8-pin | 8-pin | 8-pin | 10-pin | 10-pin | 10-pin |
| |  |  |  |  |  |  |
| Package | SOT833 | SOT1116 | SOT1203 | SOT552-1 | SOT1160-1 | SOT1081-2 |
| Width (mm) | 1.00 | 1.00 | 1.00 | 3.00 | 1.40 | 1.00 |
| Length (mm) | 1.95 | 1.20 | 1.35 | 3.00 | 1.80 | 1.70 |
| Height (mm) | 0.50 | 0.35 | 0.35 | 1.10 | 0.50 | 0.50 |
| Pitch (mm) | 0.50 | 0.30 | 0.35 | 0.50 | 0.40 | 0.35 |

## Summary

By providing low-power voltage level translator products, NXP Semiconductors continues to support the migration of applications to lower voltages, resulting in power savings. In modular designs, newer applications can take advantage of the lower power provided by reducing the supply voltage without having to redesign existing higher voltage applications. AXP translators provide the interface: they are the lowest dynamic and static power translators in the industry. Inputs and outputs support partial power-down applications by not presenting a current leakage path when the device is powered down. Low noise outputs ensure signal integrity. AXP translators enable voltage level translation between an input range of 0.7 V to 2.75 V and an output supply range of 1.2 V to 5.5 V. They are available in leading industry packages.

For more information about AXP and other translators see:
**www.nxp.com/products/discretes-and-logic/logic/level-shifters-translators:MC_29482**



© 2016 NXP B.V.
All rights reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights.

Date of release: February 2016
Published in the USA