

Efficient prediction of ESD discharge current according to OPEN Alliance 100BASE-T1 specification using SEED

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Abstract – In this paper the “ESD Discharge Current Measurement” recommended in [1] is modelled using SEED methodology and compared with measurement. The characterisation and implementation of SEED model blocks (see Fig. 1) are discussed. Special attention is given to modelling of the common mode choke and external ESD protection device because they are important factors determining the system-level ESD robustness of the overall system. The transient system-level response on ESD pulses as well as the residual currents into IC are evaluated using TLP and ESD generator models.

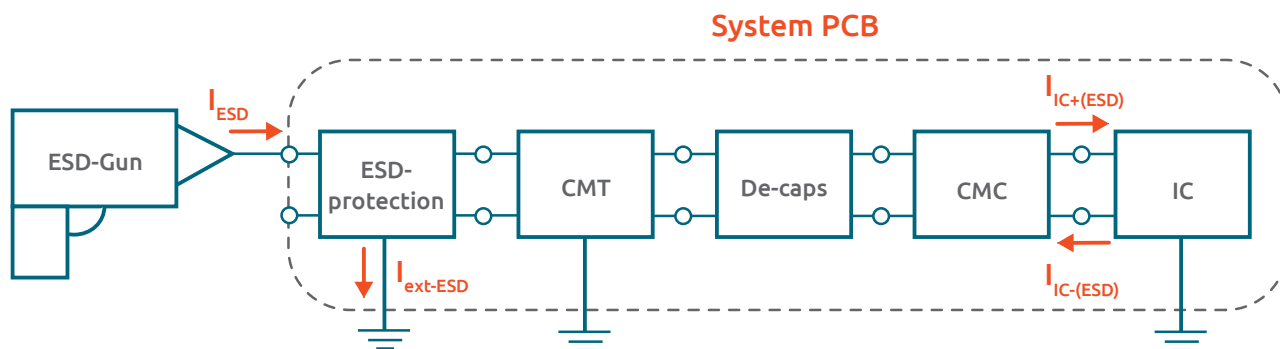


Figure 1 - Equivalent circuit block diagram of SEED model for the ESD Discharge Current Measurement reference circuit. A detailed description of each system model block will be given in Section II.

Introduction

Automotive Ethernet in the form of 100BASE-T1 according to OPEN Alliance is getting more and more popular and will be used by various car OEMs all around the world. In the document [1] OPEN Alliance is proposing a measurement called “ESD Discharge Current Measurement” which gives an estimation of the overall system-level ESD robustness of the system. This test determines the residual current into the PHY¹, identifying the ESD robustness class according to human body model requirements [2].

System efficient ESD design (SEED) is a modelling methodology aiming to predict the ESD robustness of a system, evaluating transient currents and voltages during an ESD event [3-6]. It is based on equivalent circuit and behavioural models. Transmission Line Pulse (TLP) [7] and Network Analyser measurements are typically used as input for characterisation of an individual element or system part. Together with an appropriate model for the ESD generator, the methodology has been used to study ESD events on system-level for high-speed data transfer applications such as USB3 [8].

In this paper, we are applying the SEED methodology to replicate the ESD Discharge Current Measurement Test recommended for 100BASE-T1 application. This analysis allows to draw conclusions on how different parameters like parasitic inductance of the external ESD protection device, its trigger and snap-back behaviour influence the system level ESD robustness. Furthermore, it allows to predict the electromagnetic stress other passive devices in the application are exposed to during an ESD event.

The paper is structured as follows: Section II describes the used test setup. Section III introduces the SEED model derived from the measurement setup and show characterisation and simulation results of each model block. The outcome of the system model verification with ESD generator is analysed in Section IV.

¹ PHY stands for physical layer interface and refers to the transceiver.

ESD Discharge Current Measurement According to OPEN Alliance

To measure the current which flows into a PHY during an ESD event, a special PCB is recommended by the OPEN Alliance [1]. This test network resembles the Medium Dependent Interface (MDI) where the PHY is replaced with a resistor network. The block diagram in Fig. 1 shows the different blocks of the MDI. It consists of an external ESD device, the common mode termination (CMT) elements, a decoupling network, a common mode choke (CMC) and a 100BASE-T1 PHY (IC). A photograph of the used PCB is depicted in Fig. 2.

Whereas the CMC is a single device with an inductance of $200\mu\text{H}$, the ESD device can be a single device which integrates matched ESD protection for both data lines (used in this paper) or two separate devices each connected between GND and one of the data lines. The PHY is replaced by the "Transceiver Emulation Network" retaining the electrical behavior during the ESD test. In contrast to [1], here, a $2\ \Omega$ and a $50\ \Omega$ resistors are used. The $2\ \Omega$ resistor emulates the typical behavior of the IC internal protection in a simplified way, meanwhile the $50\ \Omega$ resistor minimizes the measurement effort of the IC current. The CMT network, located between the CMC and external ESD protection devices, consists of four discrete elements: two $1\ \text{k}\Omega$ resistors are connected together between the data lines. The middle contact between those resistors and GND is accomplished via a capacitor of $4.7\ \text{nF}$ and a resistor of $100\ \text{k}\Omega$ in parallel. The CMT network is followed by two $100\ \text{nF}$ capacitances used for decoupling. The input of the test board is directly connected to the ESD device. The output connectors behind the "Transceiver Emulation Network"

To measure the ESD Discharge current according to [1] the MDI ground is connected to a ground plane with a minimum size of $0.5\ \text{m}$ by $0.5\ \text{m}$. The outputs are connected via a $50\ \Omega$ RF attenuator to an oscilloscope. The ESD pulse will be generated by an ESD generator (ESD gun) whose tip is in direct contact to one of the input pins. Following the IEC61000-4-2 [9] the setup of the ESD is $C = 150\ \text{pF}$ and $R = 330\ \Omega$. For $4\ \text{kV}$ and $6\ \text{kV}$ the discharge current is measured and for passing the specification the limits according to [1] need to be fulfilled.

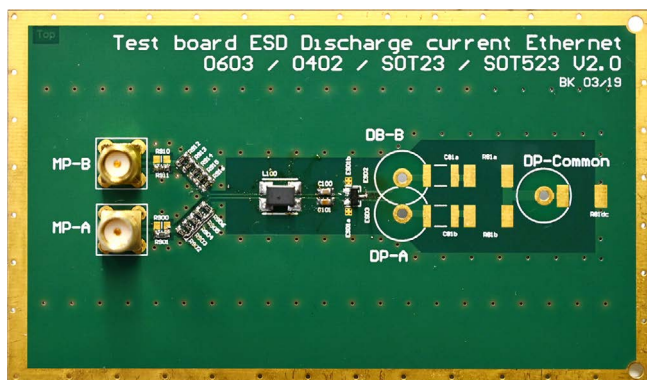


Figure 2 - Photo of reference PCB, in the size of $10.25\ \text{cm}$ by $5.95\ \text{cm}$, for ESD Discharge Current Measurements.

SEED Simulation

SEED is developed to perform system-level ESD analysis using transient simulations. To do so, it is essential to have an appropriate model for each part of the target system. Figure 1 shows schematically all necessary SEED model parts implemented here.

To reduce the modelling effort and accelerate the simulation process, a behavioural modelling approach is used. The model is tuned on the device typical static and dynamic characteristics. The model is implemented in form of an equivalent circuit consisting of lumped elements, controlled sources and feedback loops, and S-Parameters blocks.

The Advanced Design System (ADS) from Keysight is used here to perform system-level transient analysis.

Characterisation and Modelling of the ESD Generator

To perform system-level simulations and achieve good agreement with measurements a model of the ESD generator has to be configured and tuned. The model used here is based on proposals discussed in [10]. The parameters of this model are tuned to fit the simulated current waveform on the measured waveform of the ESD generator. Here, a NoiseKen ESD generator was used. The calibration is done according to IEC61000-4-2 [9]. The reference waveform for the tuning of the model of the ESD generator is obtained from a $2\ \text{kV}$ discharge into a $2\ \Omega$ Pellegrini target fixed on the large coupling plane. The resulting current waveform was captured at the gun tip with a F-65 current probe.

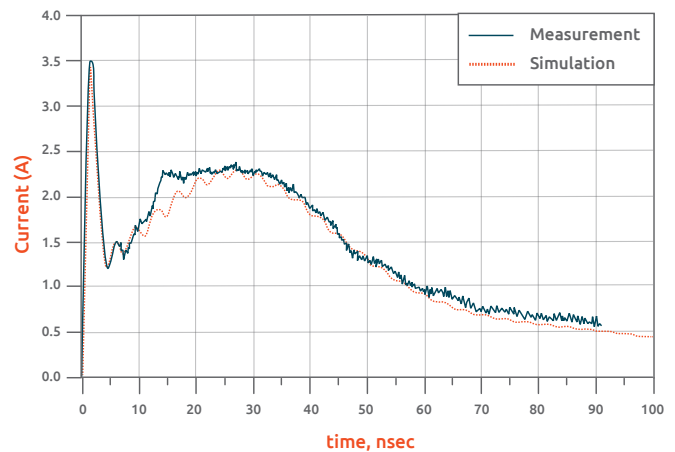


Figure 3 - Model and measurement of ESD generator waveform at $2\ \text{kV}$ on a $2\ \Omega$ reference target.

Figure 3 shows a comparison between simulated and measured time domain current curves in both first and second peak regions for a $2\ \text{kV}$ discharge. A good agreement with measurement can be observed.

Characterisation and Modelling of the Decoupling and Termination Network

The common-mode termination network and decoupling capacitors are represented in the simulation using lumped elements. The decoupling capacitors of 100nF separate the IC and the connector pins galvanically. Furthermore, they protect against slow pulses, e.g. Surge [11], but not against fast ESD pulses.

Characterisation and Modelling of CMC

A CMC of 200 μ H is recommended to be used in the IC protection circuitry according to the specification [1]. The model for the CMC is divided into a small-signal and a large-signal part. The small-signal model can be derived from a S-parameters measurement of the CMC. A fitted lumped circuit model could also be used in order to speed up the simulation time [12]. Here, the measured S-Parameters are imported directly into the simulation tool. Since S-Parameters only enclose the small-signal behaviour, partly including dynamic response and completely ignoring the saturation effect, an extended model is developed to improve dynamic and include saturation behaviour as well. As already shown in [13], the dynamic behaviour of the external ESD protection as well as the impact of the inductance, here the CMC, are crucial for the accurate prediction of the current waveforms at the IC.

For characterisation of the CMC the TLP test method [7] was applied. The time domain IV-curves depicted in Figures 4 and 5 show the typical response of the CMC at different TLP voltages. Here, we can clearly identify three regions of response: dynamic (I), static or small-signal (II) and saturation (III) region.

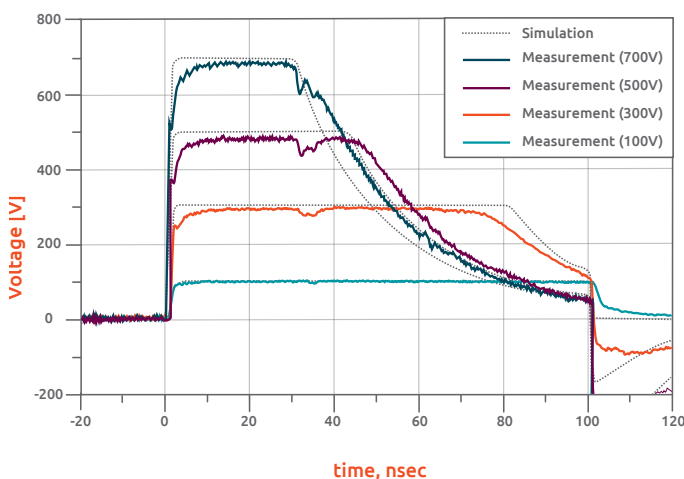


Figure 4 - Voltage response of CMC on TLP pulses with 600ps rise and 100ns duration time at different voltage levels with dynamic (I), static or small-signal (II) and saturation (III) region.

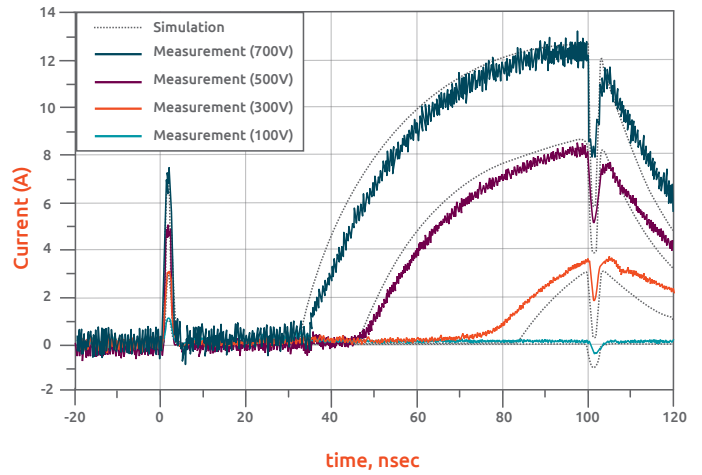


Figure 5 - Current response of CMC on TLP pulses with 600ps rise and 100ns duration time at different voltage levels with dynamic (I), static or small-signal (II) and saturation (III) region.

Figure 6 summarizes the static and saturation regions for different TLP voltages. Each point of the depicted IV curve represents an averaged value of corresponding current and voltage time domain curves as shown exemplary in Figures 4 and 5, evaluated in a window from 70 to 90 ns.

For better protection of the IC against high ESD currents, it is important that the external protection triggers before the CMC goes into saturation mode. The high voltage drop over the CMC allows the external protection device to trigger.

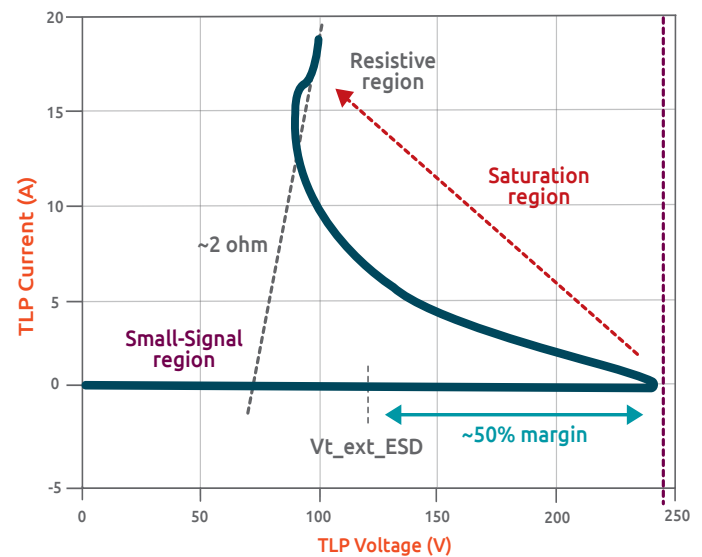


Figure 6 - TLP graph for CMC, voltage and current are averaged between 70 and 90 ns. At 240 V the CMC goes into saturation. In an effective ESD protection concept, the external ESD protection should trigger before the CMC goes into saturation.

Therefore, it must be made sure that the ESD protection device triggers first. This CMC brings a reasonable safety margin between the trigger point of the external ESD protection used here at 120 V and the 240 V where the CMC starts to saturate. However, it is not sufficient to consider only the static part of the CMC IV-curve for prediction of the overall system robustness.

The dynamic response of the choke itself, see Figure 4, plays a crucial role in the validation of the peak currents flowing into the IC during the first peak of the ESD event. Figure 7 illustrates this dynamic behaviour of the choke by showing the maximum current vs the peak voltage.

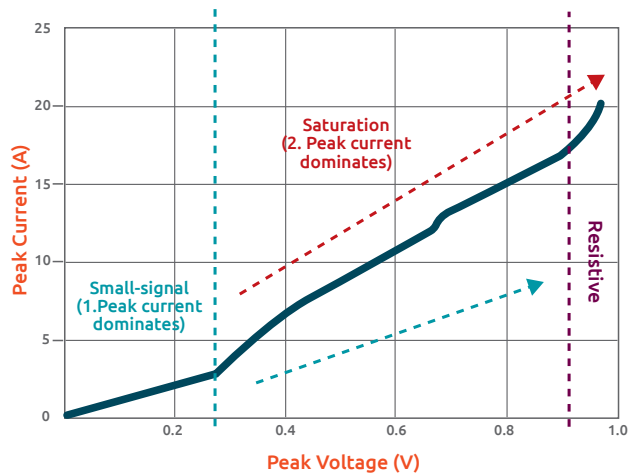


Figure 7 - TLP graph for CMC based on peak voltage and current.

In contrast to Figure 6, current and voltage are not averaged, but peak values are taken. For the correct evaluation of the system behaviour during the first peak of ESD pulse, the green trend line related to the development of the current overshoot produced by CMC should be modelled accurately.

For modelling of the full CMC behaviour the S-Parameters based CMC model (small-signal model) is extended with two additional model blocks. The first block is responsible for transition from static into saturation region, whereby the resistance change of the CMC signal through path is modelled. To realize this, a voltage controlled changeable resistor (voltage controlled switch) is added in parallel to the main model. For determination of the onset time of the saturation effect a RC network is used to control the state of the switch in dependence of the input voltage level and rise time.

A feedback loop keeps the switch control circuit in a defined condition during the whole ESD event duration. To control the increase time and decay time of the voltage and current pulse of the CMC, an inductor is connected in series with the switch. The second block added to the small-signal CMC model improves the representation of the dynamic behaviour, which mainly governs the voltage overshoot generated by the CMC. This is implemented by adding of a rise time filter into the signal path of the full CMC model. The overall model is fitted by variation of the parameters related to each model block.

Figures 4 and 5 show how the simulated voltage and current time domain curves are matching very well the corresponding measurements of the CMC. The resulting IV-curve of the tuned model is depicted in Figure 8.

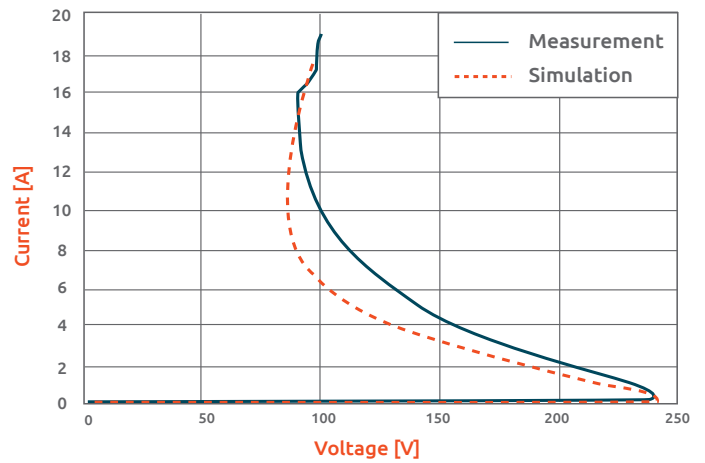


Figure 8 - Measured and simulated graph for CMC, voltage and current are averaged between 70 and 90 ns of 100ns TLP pulses.

Characterisation and Modelling of External ESD Protection

According to the specification [1], the external ESD protection is placed near the system board connector. In this position, it can guarantee a certain robustness level of the overall system, protecting not only the IC but all discrete components located in the signal path e.g. capacitors and the CMC. In order to predict the behaviour of the system and its robustness at different ESD levels, a precise model of the external ESD protection is needed. Here, a silicon based ESD protection² with a trigger voltage of $V_t = 120$ V, a snap-back voltage of $V_h = 32$ V and a dynamic resistance of $R_{dyn} = 0.1$ Ω is used.

For the implementation, the static as well as the dynamic behaviour of the chosen ESD protection device are characterized and modelled. For this purpose, an improved dynamic model based on the approach described in [6] is used.

The static behaviour of the ESD protection device, consisting of leakage, snapback (turn-on), linear and non-linear (thermal unstable) regions, is modelled with help of voltage controlled switches and a diode SPICE model. The RC network and feedback loop are responsible for the state of the switches during a second peak of the ESD pulse. The dynamic behaviour of the model is implemented via two RC integration networks combined in a way to control the voltage drop over ESD protection as well as its decay time during the first peak of the applied ESD pulse.

The main advantages of the extended dynamic model are correct representation of the thermal behaviour of the ESD protection device and a more accurate description of both the effect of conductivity modulation and inductive overshoot. In this paper, the conductivity modulation effect is of highest importance for the representation of the voltage overshoot which occurs on the external protection side and will be translated over the CMC to the IC I/O pin in form of peak current.

By following the procedure described in [6], the improved dynamic model is fitted to TLP measurement data as shown in Figure 9.

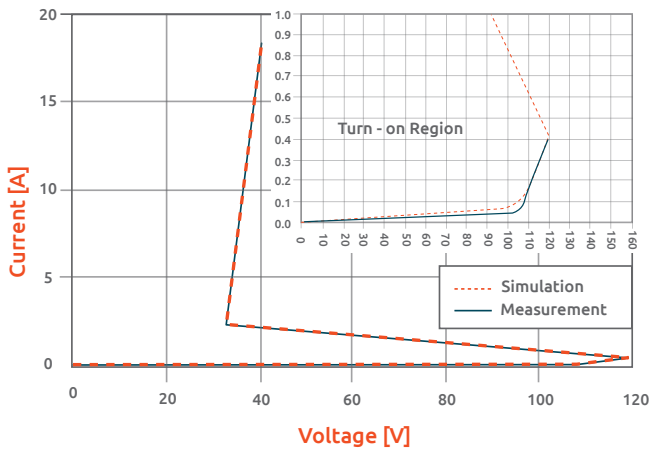


Figure 9 - Measured and simulated graph for external silicon-based ESD protection, voltage and current are averaged between 70 and 90 ns.

In order to evaluate the dynamic characteristics of the ESD device like conductivity modulation and inductive overshoot, special attention has to be given to the voltage and current peaks which occur during the first nanoseconds of the applied ESD pulse. In Figure 10, the peak voltage vs. TLP current is shown. A strong conductivity modulation effect can be observed. The improved dynamic model is capturing this effect very well.

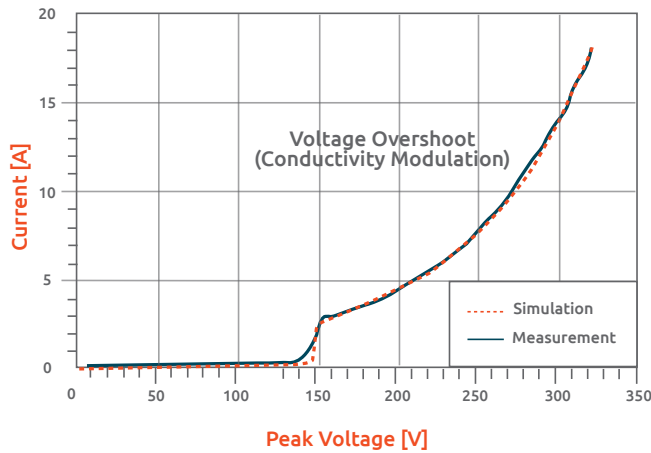


Figure 10 - Measured and simulated graph for external silicon-based ESD protection lean on peak voltage and current of 1ns rise time TLP pulses.

Verification of System Model

After introducing the parts of the SEED model, the complete system model, see Figure 1, is validated against measurements of a reference board with and without external ESD protection using TLP.

Reference Board without External ESD Protection

Figure 11 shows TLP measurements of the reference system, see Figure 2, including CMT, decoupling capacitors, CMC and IC network, excluding external ESD protection and compares them with simulation results achieved using all the corresponding parts of described SEED model. Here, the ESD generator model and the model of the external ESD protection are not used. The TLP pulse is modelled with an ideal pulse source and 200ps rise time filter, whereby the modelled pulse form is optimised on the captured pulse of the target system at 100V TLP. The simulation resamples the measurements to a high degree.

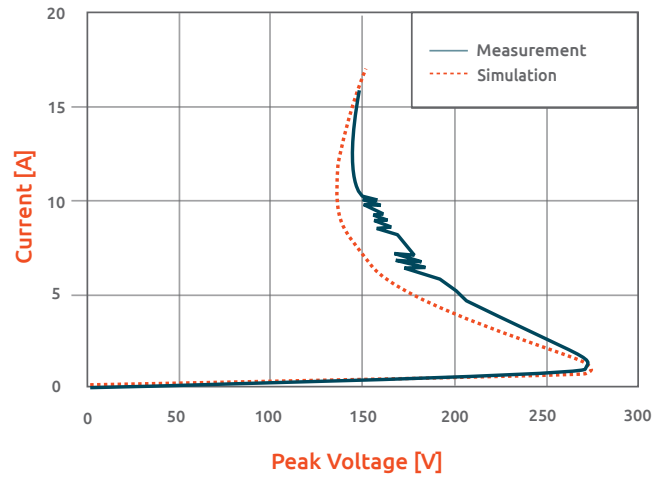


Figure 11 - Measured and simulated graph for unprotected reference board, voltage and current are averaged between 70 and 90 ns of 100ns TLP pulses.

Reference Board with External ESD Protection

In Figure 12, the TLP graph of a reference board with external ESD protection is shown in comparison with simulation results using SEED. The simulation reproduces the measurement data to an extraordinary degree.

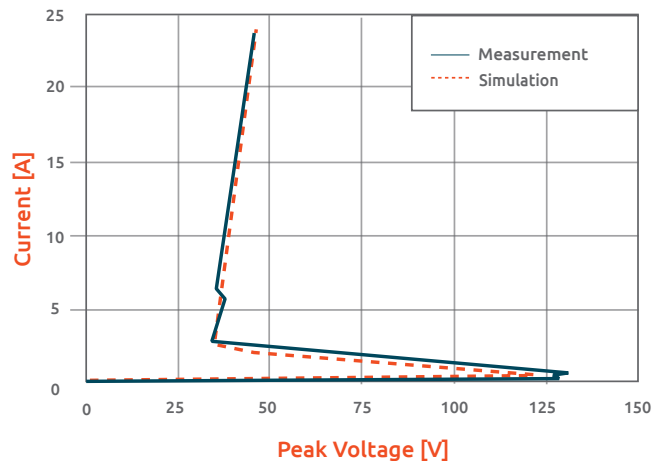


Figure 12 - Measured and simulated TLP graph for the reference board with external ESD protection device, voltage and current are averaged between 70 and 90 ns of 100ns TLP pulses.

Based on the results we can conclude that the implemented SEED model is fully suitable not only for qualitative but also quantitative prediction of the overall system-level robustness. Moreover, it can be used for preliminary tests using different system blocks and components. Therefore, in the next Section, this system model will be tested using ESD Gun model, whereby the transient residual current flowing into the IC will be evaluated.

Application

In real environment an ESD event may occur during human being touches the GND or I/O pin(s) of the system board connector. In this case, IEC61000-4-2 ESD pulses [9] will be injected into the system and generate transient currents which may destroy the system IC. Therefore, the ESD generator model will be applied to demonstrate the ability of the proposed SEED model, which was discussed and verified in Section III, to replicate the real ESD scenario emulated with help of ESD generator.

Figures 13 and 14 show results for positive ESD gun discharge of 4 kV level. In this case ESD generator model and external ESD protection model are used within the SEED model.

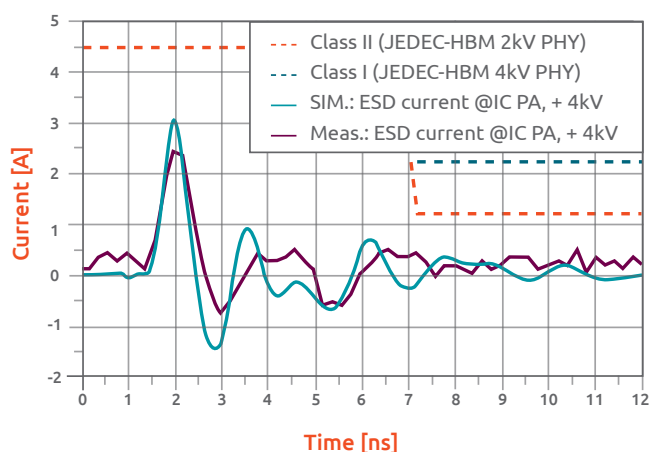


Figure 13 - Zoom in dynamic overshoot region of measured and simulated graph for the reference board with external ESD protection device for ESD gun discharge of +4kV.

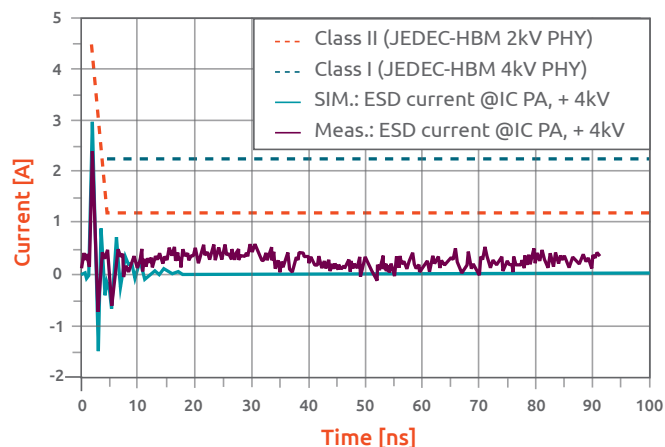


Figure 14 - Measured and simulated graph for the reference board with external ESD protection device for ESD gun discharge of +4kV.

Both graphics demonstrate the resulting simulated current curves in time domain concurrently showing the measured current at IC I/O pin. The yellow and red dashed lines show the limits of the I and II Class of the JEDEC-HBM standard [2] accordingly. The used SEED model provides an estimation of the tested system predicting ca. 20% higher maximal current peak. For the static part of the curve however, the simulation rather underestimates the measurement. Despite this deviations, the proposed SEED model shows to be applicable for the modelling of this measurement setup.

The observed deviations between the simulated and measured results can be explained by electromagnetic coupling effects, which are not encountered in the actual SEED model, i.e. effects related to crosstalk or electromagnetic radiation of ESD generator relay. In such case, the maximal current measured at the IC I/O pin(s) may be destructively attenuated by virtue of coupling effects between the ESD gun and the test board components like board traces, CMT network or CMC.

To minimize these effects an additional effort could be spend to improve the shielding of the board from the direct impact of the relay, here the ESD generator has not been shielded against the DUT. Also, to improve the modelled behaviour of the system an S-Parameters model of PCB may be added to the SEED model.

Conclusion

The application of SEED methodology on a such complex circuit like 100BASE-T1, which consists of diverse components modelled using sophisticated approaches aiming to replicate both static and especially dynamic behaviour of the whole system, has proven to be a good solution for estimation of the overall system transient response under ESD conditions. Furthermore, it can be used for the prediction of the system-level ESD robustness according to IEC61000-4-2 [9] and evaluation of the IC robustness according to JEDEC-HBM [2] requirements.

The SEED model developed and verified in this paper may be used to study the impact of variation of system and external ESD protection device parameters to achieve the optimal protection of the system IC in order to minimize the engineering and verification time.

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