

# Can DFNs be successfully wave soldered?

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The wave soldering evaluation for DFN (Dual or Discrete Flat No lead) had been executed to determine whether, beside reflow soldering, a wave soldering process could be used to solder DFN components. The first step was a feasibility study. This was followed by the determination and improvement of critical parameters for minimizing solder defects. DoE (Design of Experiment) was used to vary SMD (Surface Mount Device) adhesive bonding, positioning, pad layout and transport direction in a systematic way while soldering in two different inert atmosphere wave solder systems. Surprisingly good soldering results were found and quantified using AOI (Automated Optical Inspection) and AXI (Automated X-ray Inspection). A solder gap of 20 µm was easily filled, showing only low voiding.

### Leadless SMDs

DFN is a package of the BTC (Bottom Termination Component) type. This type has its contact pads on the bottom of the component. These components are designed for surface mounting on printed circuit boards (PCB). They are typically placed in solder paste and soldered using the reflow process. In this special case, we wanted to determine if transistors in a DFN housing could be soldered together with THT (Through-Hole Technology) components using the wave soldering process.

It should be stated here that, when SMT (Surface Mount Technology) was first introduced about 40-50 years ago, it was quite normal to solder SMDs together with through-hole components in one step using wave soldering [1]. For this assembly technology, there were sophisticated design suggestions under the keyword DFM (Design for Manufacturing) with pad dimensions matched to each SMD package. Glue dots to fix the component location on PCB are part of the design rules. The components must be placed for wave soldering on the solder side. At the moment of soldering, the solder must touch and flow around them. In addition, pad lengths must protrude relatively far beyond the end of the leads to ensure contact and wetting with the liquid solder [2].

BTC packages were introduced at the beginning of the new millennium as the technology trend moved away from the wave process toward smaller and smaller SMD packages for the reflow process. The advantage of the BTC package – besides the main motivation of saving space by eliminating leads – are short routes and good dissipation of heat losses into the PCB by way of the soldered thermal pad. In the meantime, DFM and manufacturing parameters for a safe BTC assembly by reflow soldering have become well documented [3].

### Visual acceptance criteria for DFN

The acceptance criteria of the globally recognized guideline IPC-A-610 is used widely for checking the assembly and soldering success [4]. Of course, the problem with BTC is that the solderable lead surfaces are on the underside of the component for the most part. That means most of the solder connections are hidden or only partially visible. Correspondingly, for example, the side length of the solder joint does not offer a feature that can be visually checked.

To allow the visual inspection of solder connections and the position using AOI, many component manufacturers offer versions with side wettable flanks (SWF). This means that the exterior cut faces of the component leads at the edge of the components are plated so that they can be soldered. Otherwise, only the solder wetting recognizable on the pad protrusions, the component position and the absence of excess solder, such as solder bridges and solder balls, remain for visual inspection.

### Design variants

In the evaluation tests three types of transistor packages have been used (Figure 1):



Figure 1: DFN components for this investigation

The types b) and c) have SWT while type a) does not. Figure 1 shows that types a) and b) have only three pads on the bottom. The two small pads (the two corner pins) are independent from the heatsink.

For type c), the pads 1, 2, 5 and 6 are internally connected to the heatsink. Because of this the pads 2 and 5 do not need to be joined during the wave soldering process. The electrical function is assured anyway.

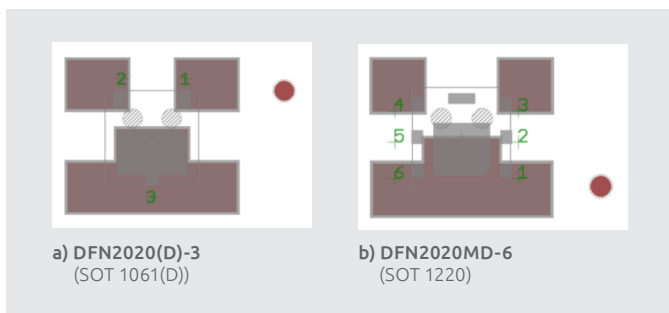


Figure 2: Pad suggestions at the start of the investigation

Figure 2 depicts pad design suggestions from Nexperia for the wave soldering process. In the figure, the copper layer is shown in red and includes the pin 1 marking on the PCB. The hatched circle areas show the positions and sizes of the glue dots. The gray rectangles are the wettable contact surfaces on the bottom of the corresponding component. The pin numbers are shown in green color and the component outline is drawn as a thin gray line. In addition, a cross marks the center of gravity of the component. This cross also marks the desired component position relative to the copper layer.

The manufacturing tests were performed in two campaigns named in the following as Phase I and Phase II. For type c), it was feared that short circuits by solder bridging might form on the sides, due to the SWT and three pins along the sides.

Several pad design variants were created to prevent solder bridges. These included pads with a wide and a narrow thermal pad beneath the component package, pads with clipped corners on the exterior pad areas and glue dots on the edge of the component package in comparison to glue dots beneath the component (Figure 3).

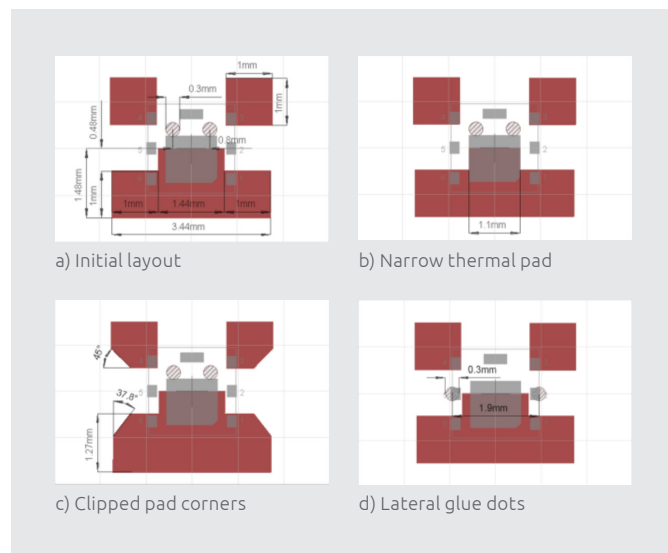


Figure 3: Pad layout variants, Phase I

No specific differences in the pad geometries were made between types a), b) and c). Merely the pin 1 marking on the component type was changed for differentiation and the defined assembly position.

In Phase I, the soldering method was found to be quite successful. There were virtually no short circuits. The main defect feature was found to be dewetting. For this reason, variants with greater pad protrusions were fabricated and the angle of rotation was systematically varied relative to the transport direction (Figure 4).

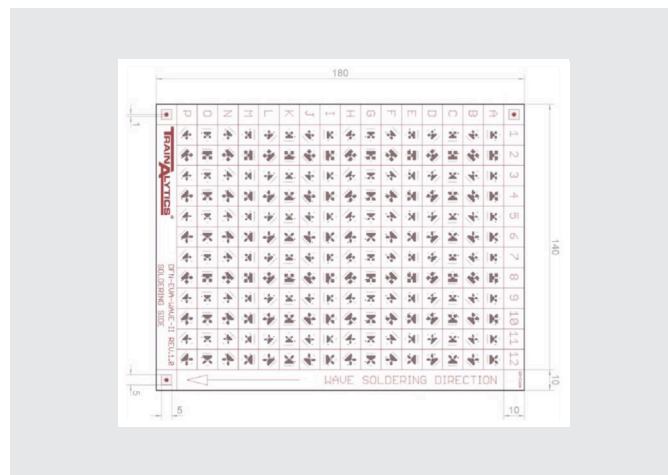


Figure 4: Phase II test board with pad and direction variants

On the test board for Phase II, the pads were configured for the two packages in 12 columns and 16 rows. In this way, every package is offset in 8 angles of rotation of 45° with respect to each other and the design variants are distributed across the 12 columns.

### Process variants

The soldering tests were performed on two different wave-soldering systems, both equipped with an inert gas tunnel. A target of 500 ppm of residual oxygen content is used for soldering in the nitrogen atmosphere in the tunnel.

The soldering systems differed in the nozzle structure and the soldering alloy. SAC303 was used to solder in the dual-wave system. The Powerflow system uses a perforated nozzle (Wörthmann wave) with SN100C.

The exact specifications and additional parameters are listed in the following:

- SMD adhesive: red, viscous
- Adhesive stencil: stainless steel, 200 µm and 250 µm
- Adhesive pressure: automatic system
- Component placement: automatic, zero vertical offset
- Adhesive curing: reflow system, 2 minutes, 160°C
- Wave soldering: The transport direction is indicated in the test board layout (Fig. 4) using an arrow.
  - (a) Dual wave with a bath temperature of 260°C; transport speed: 1 m/min; preheating temperature (bottom): 120-130°C; contact time in the first wave (chip wave): 0.6 seconds; time in the main wave (laminar wave): 2.4 seconds
  - (b) Powerflow: first wave switched off, main wave is the Wörthmann type with 5 rows of perforations; bath temperature: 260°C; transport speed: 1 m/min; contact time in the Wörthmann wave: 1.8 seconds
- Soldering alloy (composition in percent by weight)
  - (a) Dual wave: SAC303 (Sn-3.4Ag-0.3Cu)
  - (b) Wörthmann wave: SN100C (Sn-0.75Cu-0.05Ni)
- Flux in both systems: ORL0 as per J-STD-004; alcohol based, low-solid (resin-free), halide-free, developed for wave soldering with lead-free solder
- AOI in offline operation
- AXI, in this case as computer tomography in offline operation

### DoE Phase II

Components in this project were placed on the PCBs according to the Test Plan 6528. A total of 30 PCBs were completely populated with both component types having wettable edges. Another 12 PCBs were populated with type a (SOT1061) without wettable edges on the half intended for this type.

The factors for the statistical design of the experiment are listed below.

- A: 2 adhesive point locations GP1 & GP2
- B: 6 pad design variants F1-F6
- C: 8 angles of rotation (from 0°–315° in 45° steps)
- D: 2 wave soldering systems; for the solder and flux, see section “Process variants”

To evaluate the soldering results, AOI was used based on the exterior defect features of position, dewetting and solder bridges. As the PCBs were delivered with a QR code, the evaluation using AXI could be repeated for a direct comparison. Manual inspection of random samples resulted in agreement with the test results. The DoE test planning and evaluation were performed using a statistics program and based on the AOI results.

### The best result

As an example, Figure 5 depicts the difference in the reflection behavior between components with and without side wettable flanks. However, the detectable reflection at the wettable flank was not used in this case as a special AOI criterion. It can be seen that complete pad wetting is sufficient as an indication for gap filling. The photographs of Figure 5c) and d) show examples of dewetting on one pad in each case. The solder gap is also not filled on these pads. Compare the examples from the AXI tests in Figure 11.

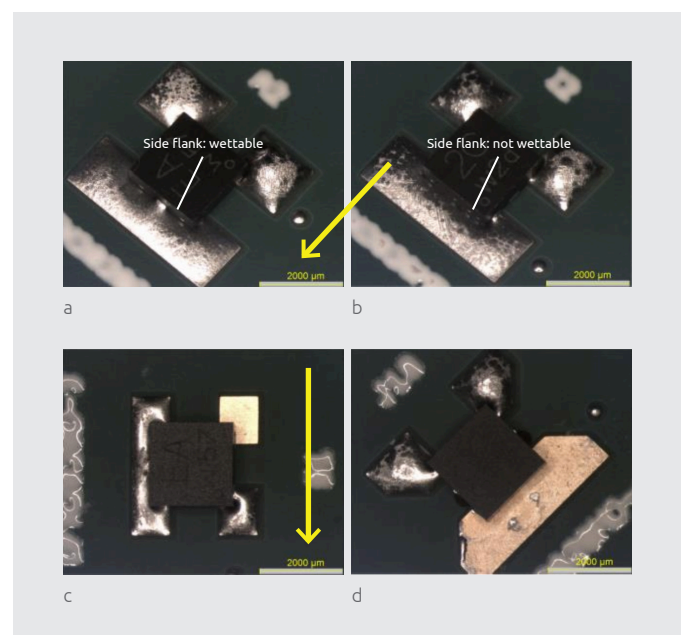


Figure 5: Wetting detectable during inspection (arrows = transport direction)

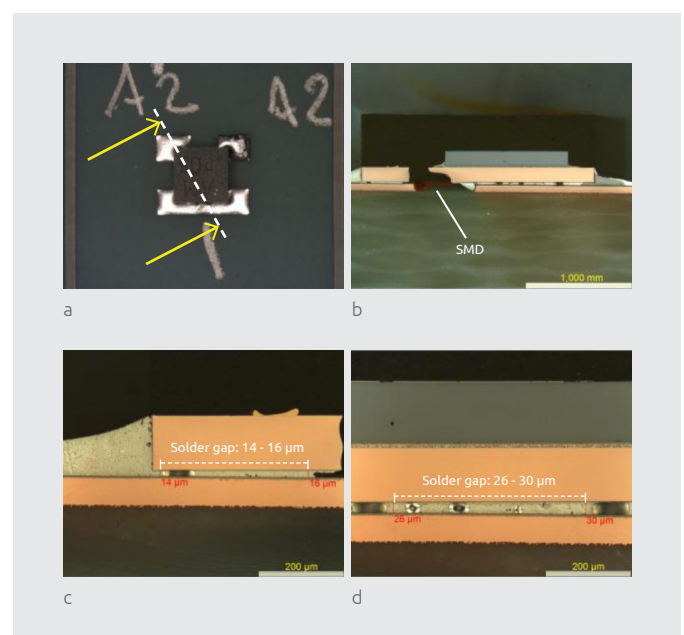


Figure 6: Micrograph planes, micrographs and solder gap thickness

The micrographs show a comparably small voids content in the solder gap (Figure 6b, 6c and 6d). The height and diameter of the glue dots did not have a significant effect on the thickness of the solder gap. Under the given manufacturing conditions, the result was that the glue dots beneath the component led to a more uniform solder gap thickness. See Fig. 6 a-d and Table 1. This variation did not have a noticeable effect on the defect rate.

Sample no.	Glue dot			Solder gap thickness	
	Location	Diameter	Screen thickness	Corner pin	Thermal pad
A2	On the side	300 µm	200 µm	15 µm	28 µm
B2	Beneath the component	300 µm	200 µm	15 µm	20 µm
G2	On the side	400 µm	250 µm	19 µm	28 µm
H2	Beneath the component	400 µm	250 µm	19 µm	20 µm

Table 1: Effect of the SMD adhesive on the solder gap

The DoE evaluation showed that the pad size and orientation relative to the transport direction were crucial for soldering success with the dual wave. See Figure 7 to Figure 10 beneath. The large pads (pad variants F2, F4, F6) led to considerably fewer wetting defects than the small pads (variants F1, F3, F5). The clipping of the corners (F3-F6) was more of a disadvantage. See Figure 8, Factor B. The orientation of the thermal pad protrusion trailing in the

wake of the transport direction led to success when soldering with the dual wave (Figure 7). For the components with 6 leads, only sporadic defects occurred with the dual wave for these variants, too (Figure 8). The tests using the Wörthmann wave provided the best result in terms of low defect counts. In this case, the defect count was so low that the evaluation program could not supply a correlation, see Figure 9 and Figure 10.

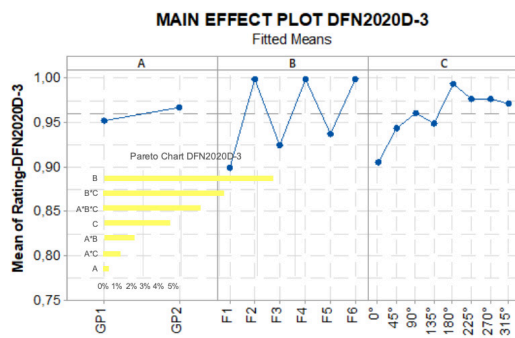


Figure 7: Dual wave D-3

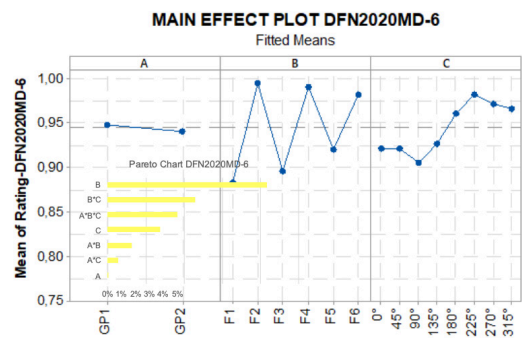


Figure 8: Dual wave MD-6

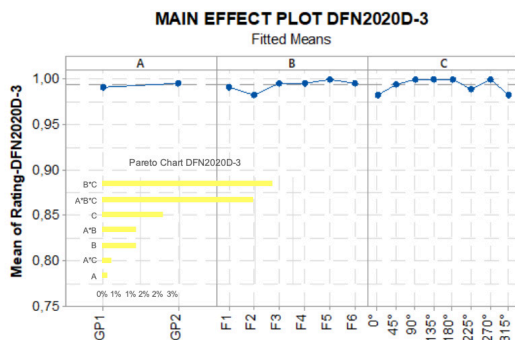


Figure 9: Wörthmann wave D-3

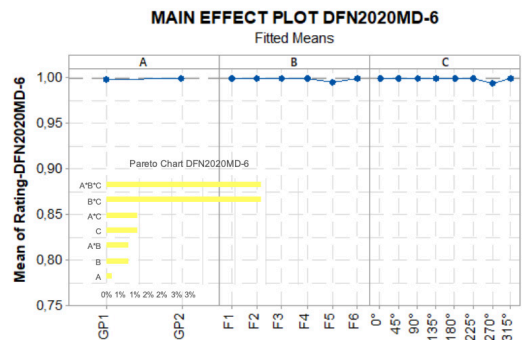


Figure 10: Wörthmann wave MD-6

The AXI photographic examples show the greater difficulty in creating an evaluation algorithm in this case. In the tomosynthesis layer image (Figure 11) in the solder gap plane, the soldered area appears bright. See the defect-free example b) If, however, the solder gap filling is missing as marked in example a) at pin 3, example d) at pin 2 and example e) at pin 1, the component lead appears as a bright rectangle. Incomplete solder coverage on the pad protrusion is still reliably detected. See example c) at pin 1 (on the thermal path in this case).

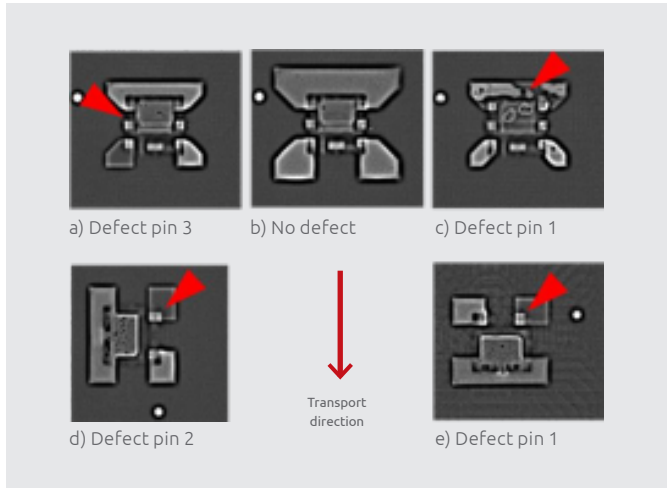


Figure 11: Tomosynthesis layer evaluation

This investigation did not continue to determine if the void content on the thermal pad can be quantified using AXI.

## Conclusions

- These DFN components can be safely wave soldered.
- Better wetting on larger pad areas – in this case, the space required for the component on the PCB increases by a factor of 4 compared to a reflow layout.
- Surprisingly good gap filling in the adhesive-defined solder gap thickness of 15 – 30  $\mu\text{m}$ .
- Advantage of the Wörthmann over the dual wave; in Phase II, too few defects occurred regardless of the pad size or orientation, so that no statistical correlation was possible.
- Component orientation:  
DFN2020-3 and DFN2020D-3 (3 leads) at 180° with respect to the transport direction, i. e., the thermal area faces backward with respect to the transport direction (trailing);  
DFN2020MD-6 (6 leads) at 225° with respect to the transport direction, i. e. rotated another 45°.

It is important to note that the parameters were successfully optimized using the DoE method with manageable test effort that could be estimated in advance.

Postface: These results should not be interpreted as a recommendation to attach BTC preferably by wave soldering in order to reduce solder joint voiding.

## Acknowledgement

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## References

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- [2] R. J. Klein Wassink, M. M. F. Verguld, Manufacturing Techniques for Surface Mounted Assemblies, Electrochemical Publications, 1995.
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