Addressing floating inputs
in digital systems

In the normal operations of a digital system, the input to any digital device within is clearly defined - it is either one or zero. There are however interface cases where outputs may be disabled that can result in floating inputs.

Consider a situation of 8, 16, 32 or 64 CMOS inputs, arranged in a bus. Typically, any of a number of drivers may control this input bus. But in some cases, such as low power modes, none of the active drivers are engaged by the overall system. Uncontrolled, the voltage present at an input is determined by random, unpredictable factors, not defined by the design of the overall system. That uncontrolled input is said to float.

Random events may unpredictably bring the floating input voltage up to a point that the device will interpret as a one, or down to the point that the device will interpret as a zero. This will cause output switching, a high current event that may cause supply or ground bounce. As input thresholds are dependent upon supply the floating input may cause the output to switch back to its previous state. In the worst case the floating input may cause output oscillation, which will effect correct operation and cause excessive power dissipation.

Bus-hold circuitry eliminates floating inputs

Figure 1 is a representation of the input to a CMOS digital component. If V_I is solidly one, the NMOS transistor on the bottom switches on, and the PMOS transistor on the top switches off. This switches the output to ground, or an output of digital zero. If V_I is solidly zero, the opposite happens, and the output is switched to V_{CC}, or digital one.
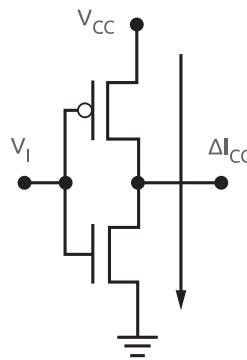

Figure 1 - CMOS input buffer

When V_I floats — it isn't one or zero - both the NMOS and PMOS transistors may operate in their linear ranges, allowing current I_{CC} to flow through both transistors. When the input floats above or below the input threshold the switching and possible oscillation described previously may occur.

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A solution to prevent this is to employ a bus hold circuit that can latch in the last input state presented at the device's input pin. Thus, even if the input would otherwise float, that input is held to its previous value. Figure 2 shows a CMOS input with bus hold cell.
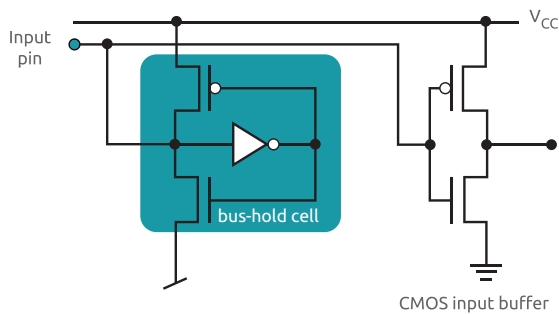

Figure 2 - CMOS input with bus hold cell

The bus hold circuitry is a latch which requires a minimum current to switch states, so floating inputs will not cause switching or excessive power dissipation. Only a solid one or zero will cause it to switch. Thus, even when the input floats, the overall output stays at the value mandated by the previously defined input of one or zero.

Pull-up or pull-down resistors for a solid start up

The bus hold input is a solution to ensuring defined inputs at all times. At power-up the bus hold cell (latch) may contain either a one or a zero. When a system first powers on, the system may require that the input of a device must start off with a one or alternatively start off with a zero. The solution might either be a pull-up resistor from V_{CC} to enforce an input of one, or a pull-down resistor to enforce an input of zero.

Calculating resistor values

Let's take the case of a pull-up resistor. The formula used to calculate its value is:

$$R_{PULL-UP} = (V_{CC} - V_{TH}) / I_{BHLO}$$

V_{CC} is the value of the device's power supply. We will assume, for this example that the device is supplied at 3.0 V.

V_{TH} is a function of V_{IH}, the input voltage that the device will always recognize as a one, and V_{IL}, the voltage that the device will always recognize as zero:

$$V_{TH} = (V_{IH} + V_{IL}) / 2$$

If V_{IH} is 2.0 V and V_{IL} is 0.8 V
$$V_{TH} = (2.0 + 0.8) / 2$$
$$V_{TH} = 1.4V$$

I_{BHLO} is the bus hold LOW overdrive current. It can be found in the Nexperia datasheet for the device (e.g. 500 μA).

So, substituting values:
$$R_{PULL-UP} = (V_{CC} - V_{TH}) / I_{BHLO}$$
$$R_{PULL-UP} = (3.0 - 1.4) / 500 \times 10^{-6}$$
$$R_{PULL-UP} = 3200 \ \Omega$$

Pull-down resistor

For a pull-down resistor, the formula is:
$$R_{PULL-DOWN} = (V_{TH}) / I_{BHHO})$$

A similar calculation yields 2800 Ω

Figure 3 shows a typical bus-hold characteristic and load lines of different pull-up resistor values.

For values less than 8k Ω there is no intersection of the load line with bus-hold line, so no issue in pulling up an initial low state input to high state. For larger resistor values the load line intersects the bus-hold line and this intersection point becomes the maximum voltage level to which the bus-hold is pulled from low, the input is never switching to high beyond this point.
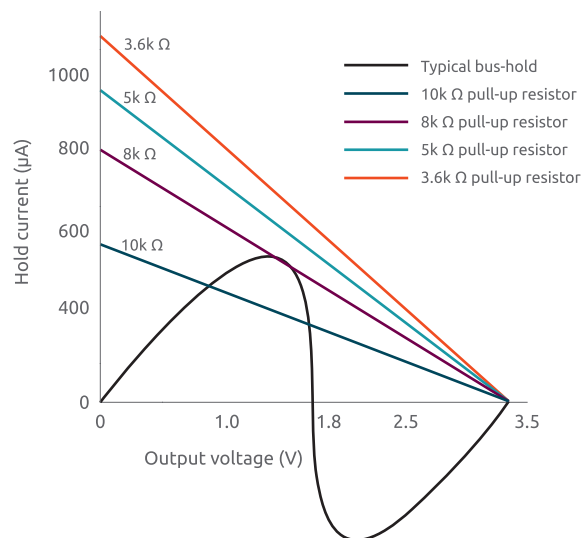

Figure 3 - Typical bus hold characteristic and resistor load lines

Availability of the bus-hold feature

The bus-hold feature is standard on all of Nexperia's LVT (Low Voltage Technology) and ALVT (Advanced Low-Voltage BiCMOS Technology) bus-interface products. This includes all 8- and 16-bit buffers, inverters, drivers, flip-flops, latches/registered drivers, level shifters/translators, and transceivers.

On other Nexperia families, the bus-hold feature is indicated by the addition of an "H" in the product number. Examples are 74LVCH245 instead of 74LVC245 and 74AVCH2T45 instead of 74AVC2T45).