MC9S12KG128

SoC Guide

V01.01

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Revision History

Version Number	Revision Date	Author	Description of Changes
01.00	16.JUL.02	Roberto Frontera	Original Version
01,01	22 NOV 02	Daniel Yu	Change load cap value on VDD and VDDPLL. Correct expanded bus timing from 20MHz to 25 MHz

Section 1 Introduction

Section 2 Signal Description

Appendix B Package Information

Preface

The SoC Guide provides information about the MC9S12KG128 device made up of standard HCS12 blocks and the HCS12 processor core. This document is part of the customer documentation. A complete set of device manuals also includes the HCS12 Core Guide and all the individual Block Guides of the implemented modules. In a effort to reduce redundancy all module specific information is located only in the respective Block Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

Document References

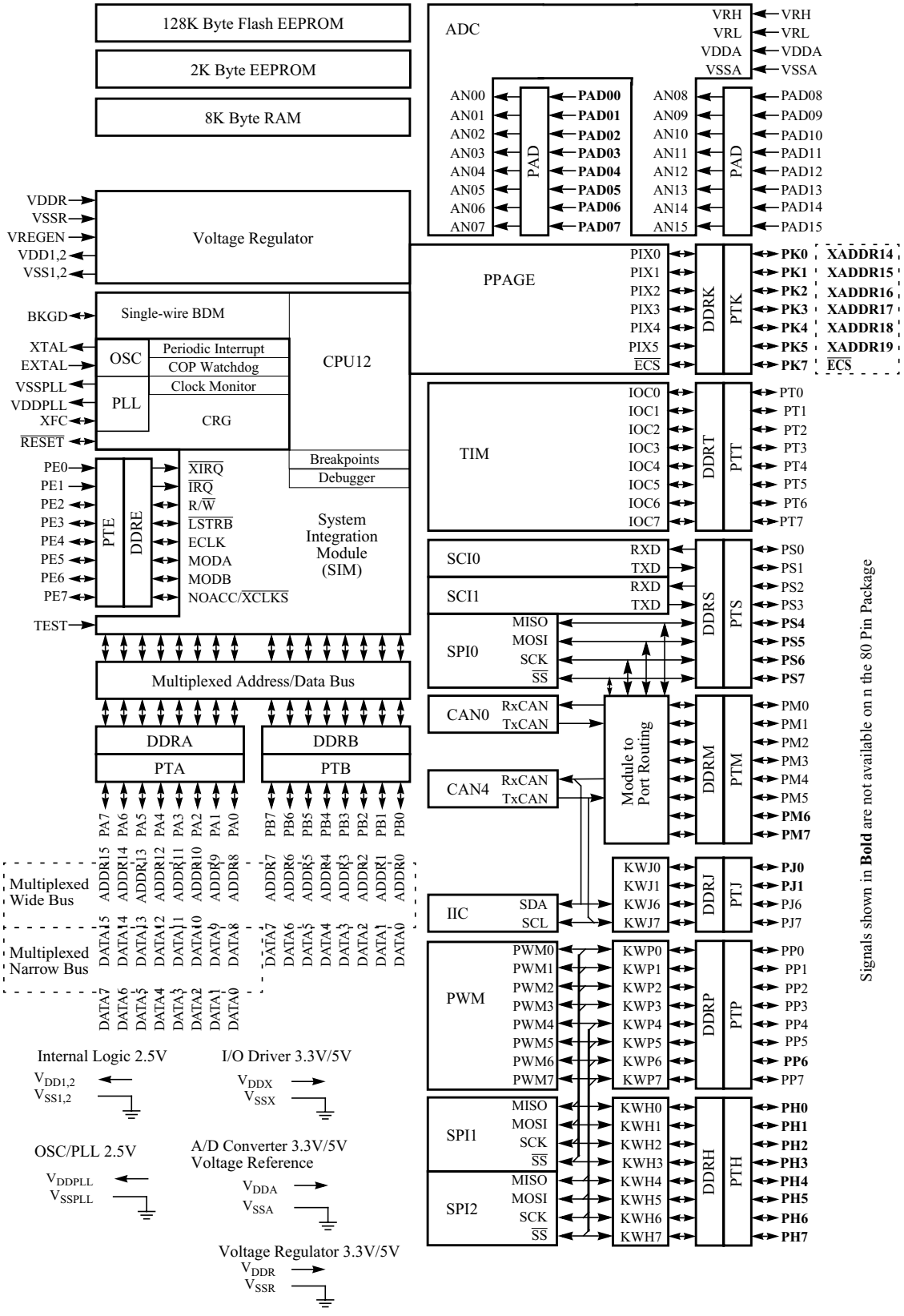
User Guide	Version	Document Order Number
HCS12 V1.5 Core Guide	1.2	HCS12COREUG
Analog to Digital Converter 10 Bit 16 Channel (ATD_10B16C) Block Guide	V03	S12ATD10B16CV3/D
Clock and Reset Generator (CRG) Block Guide	V04	S12CRGV4/D
2K Byte EEPROM (EETS2K) Block Guide	V01	S12EETS2KV1/D
128K Byte Flash with Error Code Correction (FTS128K1ECC) Block Guide	V01	S12FTS128K1ECCV1/D
Inter IC Bus (IIC) Block Guide	V02	S12IICV2/D
Freescale Scalable CAN (FSCAN) Block Guide	V02	S12MSCANV2/D
Oscillator Loop Control Pierce (OSC_LCP) Block Guide	V01	S12OSCLCPV1/D
Port Integration Module (PIM_9KG128) Block Guide	V01	S12PIM9KG128V1/D
Pulse Width Modulator 8 Bit 8 Channel (PWM_8B8C) Block Guide	V01	S12PWM8B8CV1/D
Serial Communication Interface (SCI) Block Guide	V03	S12SCIV3/D
Serial Peripheral Interface (SPI) Block Guide	V03	S12SPIV3/D
Timer 16 Bit 8 Channel (TIM_16B8C) Block Guide	V01	S12TIM16B8CV1/D
Voltage Regulator (VREG_3V3) Block Guide	V01	S12VREG3V3V1/D

Section 1 Introduction

1.1 Overview

The MC9S12KG128 is composed of standard on-chip peripherals including a 16-bit central processing unit (CPU12), 128K bytes of Flash EEPROM, 2K bytes of EEPROM, 8K bytes of RAM, two asynchronous serial communications interface (SCI), three serial peripheral interface (SPI), IIC-bus, an 8-channel IC/OC timer, 16-channel 10-bit analog-to-digital converter (ADC), an 8-channel pulse-width modulator (PWM), two CAN 2.0 A, B software compatible modules, 29 discrete digital I/O channels (Port A, Port B, PortE and Port K), and 20 discrete digital I/O lines with interrupt and wakeup capability. The MC9S12KG128 has full 16-bit data paths throughout, however, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements.

Figure 1-1 MC9S12KG128 Block Diagram



1.2 Features

- HCS12 Core
  - 16-bit HCS12 CPU
    i. Upward compatible with M68HC11 instruction set
    ii. Interrupt stacking and programmer's model identical to M68HC11
    iii. Instruction queue
    iv. Enhanced indexed addressing
- System Integration Module (SIM)
  - MEBI (Multiplexed External Bus Interface)
  - MMC (Memory Map and Interface)
  - INT (Interrupt Controller)
  - DBG (Debugger)
  - BDM (Background Debug Mode)
- Oscillator
  - 4Mhz to 16Mhz frequency range
  - Pierce with amplitude loop control
  - Clock monitor
- Clock and Reset Generator (CRG)
  - Phase-locked loop clock frequency multiplier
  - Self Clock mode in absence of external clock
  - COP watchdog
  - Real Time interrupt (RTI)
- Memory
  - 128K Byte Flash EEPROM
    i. Internal program/erase voltage generation
    ii. Security and Block Protect bits
    iii. Hamming Error Correction Coding (ECC)
  - 2K Byte EEPROM
  - 8K Byte static RAM

    Single-cycle misaligned word accesses without wait states
- Analog-to-Digital Converter (ADC)
  - 16-channel module with 10-bit resolution

  - External conversion trigger capability
- 8-channel Timer (TIM)
  - Programmable input capture or output compare channels
  - Simple PWM mode
  - Counter Modulo Reset
  - External Event Counting
  - Gated Time Accumulation
- 8-channel Pulse Width Modulator (PWM)
  - Programmable period and duty cycle per channel
  - 8-bit 8-channel or 16-bit 4-channel
  - Edge and and center aligned PWM signals
  - Emergency shutdown input
- Two 1M bit per second, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Serial interfaces
  - Two asynchronous serial communication interface (SCI)
    Infrared capability
  - Three synchronous serial peripheral interface (SPI)
  - Inter-IC Bus (IIC)
- Internal 2.5V Regulator
  - Input voltage range from 3.15V to 5.5V
  - Low power mode capability
  - Low Voltage Reset (LVR) and Low Voltage Interrupt (LVI)
- 20 key wake up inputs
  - Rising or falling edge triggered interrupt capability
  - Digital filter to prevent short pulses from triggering interrupts
  - Programmable pull ups and pull downs
- Operating frequency for ambient temperatures (T_A -40°C to 125°C)

  - 50MHz equivalent to 25MHz Bus Speed
- 112-Pin LQFP or 80-Pin QFP package
  - I/O lines with 3.3V/5V input and drive capability
  - 3.3V/5V A/D converter inputs

1.3 Modes of Operation

- Normal modes
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode[1]
  - Normal Expanded Narrow Mode[1]
  - Emulation Expanded Wide Mode[1]
  - Emulation Expanded Narrow Mode[1]
- Special Operating Modes
  - Special Single-Chip Mode with active Background Debug Mode
  - Special Test Mode[1] (Freescale use only)
  - Special Peripheral Mode[1] (Freescale use only)
- Each of the above modes of operation can be configured for three Low power submodes
  - Stop Mode
  - Pseudo Stop Mode
  - Wait Mode
- Secure operation, preventing the unauthorized read and write of the memory contents.

1.4 System Memory Map

Shows the device memory map of the MC9S12KG128 after reset

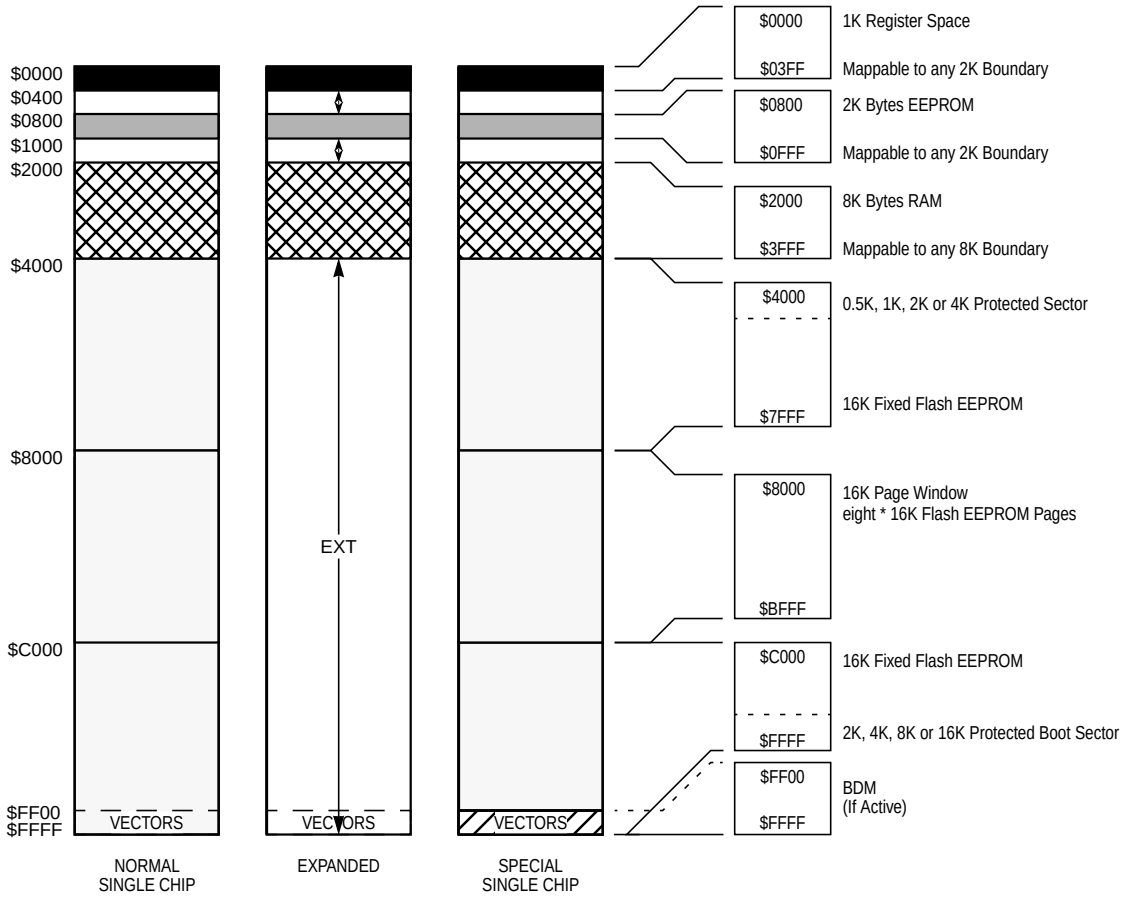
Table 1-1 Device Memory Map

Address	Module	Size
$000 - $017	CORE (Ports A, B, E, Modes, Inits, Test)	24
$018	Reserved	1
$019	Voltage Regulator (VREG)	1
$01A - $01B	Device ID register (PARTID)	2
$01C - $01F	CORE (MEMSIZ, IRQ, HPRIO)	4

NOTES:
1. Expanded modes are only available in the 112 pin package version.

$020 - $02F	CORE (DBG)	16
$030 - $033	CORE (PPAGE, Port K)	4
$034 - $03F	Clock and Reset Generator (PLL, RTI, COP)	12
$040 - $06F	Standard Timer 16-bit 8 channels (TIM)	48
$070 - $07F	Reserved	16
$080 - $0AF	Analog to Digital Converter 10-bit 16 channels (ATD)	48
$0B0 - $0C7	Reserved	24
$0C8 - $0CF	Serial Communications Interface 0 (SCI0)	8
$0D0 - $0D7	Serial Communications Interface 1 (SCI1)	8
$0D8 - $0DF	Serial Peripheral Interface 0 (SPI0)	8
$0E0 - $0E7	Inter Integrated Circuit Bus (IIC)	8
$0E8 - $0EF	Reserved	8
$0F0 - $0F7	Serial Peripheral Interface 1 (SPI1)	8
$0F8 - $0FF	Serial Peripheral Interface 2 (SPI2)	8
$100- $10F	Flash Control Register	16
$110- $11B	EEPROM Control Register	12
$11C - $13F	Reserved	36
$140 - $17F	Freescale Scalable Controller Area Network 0 (CAN0)	64
$180 - $23F	Reserved	192
$240 - $27F	Port Integration Module (PIM)	64
$280 - $2BF	Freescale Scalable Controller Area Network 4 (CAN4)	64
$2C0 - $2E7	Pulse Width Modulator 8-bit 8 channels (PWM)	40
$2E8 - $3FF	Reserved	280
$0000 - $07FF	2K EEPROM array	2048
$0000 - $1FFF	8K RAM array	8192
$4000 - $7FFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at start	16384
$8000 - $BFFF	Flash EEPROM Page Window (eight 16k windows)	16384
$C000 - $FFFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at end and 256 bytes of Vector Space at $FF80 - $FFFF	16384

Figure 1-2 MC9S12KG128 Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0000 - $1FFF: 8K RAM (1K RAM hidden behind Register Space)
$0000 - $07FF: 2K EEPROM (not visible)

1.5 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses $001A and $001B after reset. The read-only value is a unique part ID for each revision of the chip. **Table 1-2 Assigned Part ID Numbers** shows the assigned part ID number.

Table 1-2 Assigned Part ID Numbers

Device	Mask Set Number	Part ID[1]
MC9S12KG128	**0L74N**	$7100

NOTES:
1. The coding is as follows:
Bit 15-12: Major family identifier
Bit 11-8: Minor family identifier
Bit 7-4: Major mask set revision number including FAB transfers
Bit 3-0: Minor - non full - mask set revision

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMSIZ1 (addresses $001C and $001D after reset). **Table 1-3** shows the read-only values of these registers. Refer to section Module Mapping and Control (MMC) of HCS12 Core User Guide for further details.

Table 1-3 Memory size registers

Register name	Value
MEMSIZ0	$13
MEMSIZ1	$80

Section 2 Signal Description

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals.

2.1 Device Pinout

The MC9S12KG128 and its derivatives are available in a 112-pin low profile quad flat pack (LQFP) and in a 80-pin quad flat pack (QFP). Most pins perform two or more functions, as described in the Signal Descriptions. **Figure 2-1** and **Figure 2-2** show the pin assignments for different packages.

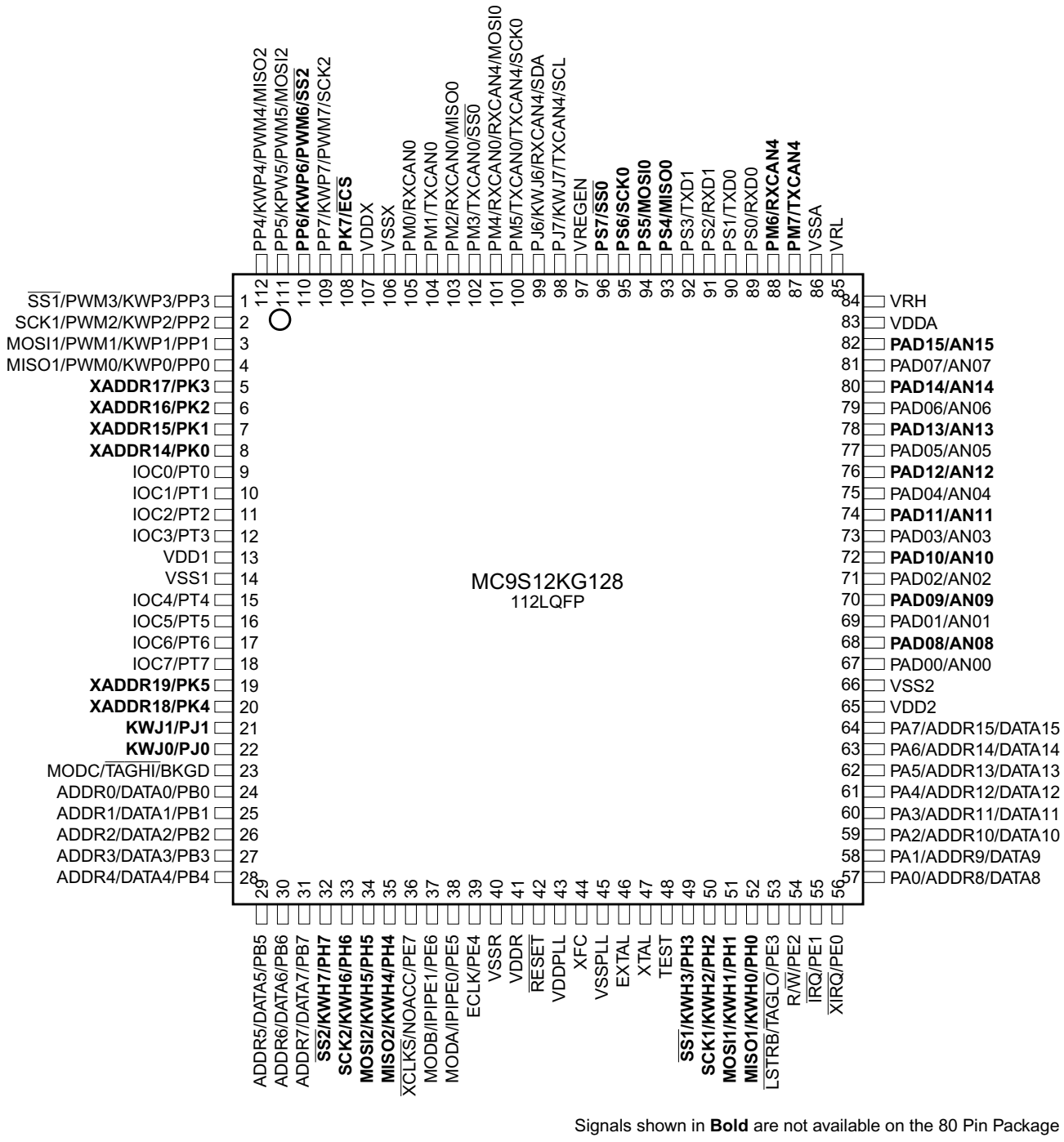


Figure 2-1 Pin assignments 112 LQFP for MC9S12KG128

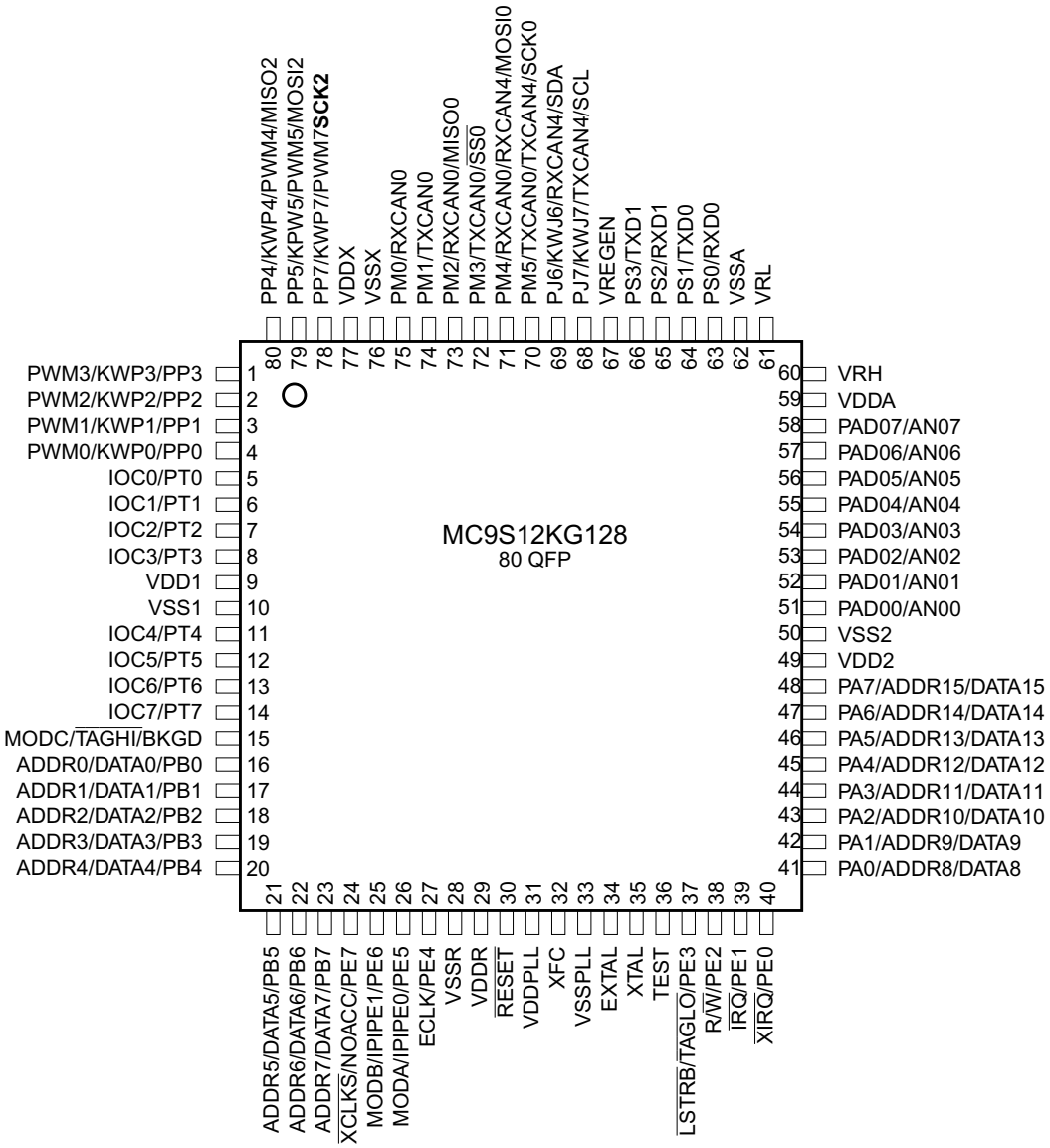


Figure 2-2 Pin assignments in 80 QFP for MC9S12KG128

2.2 Signal Properties Summary

Table 2-1 summarizes the pin functionality. Signals shown in **bold** are not available in the 80 pin package. **Table 2-2** summarizes the power and ground pins.

Table 2-1 Signal Properties

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Powered by	Internal Pull Resistor		Description
					Type	Reset State	
EXTAL	—	—	—	VDDPLL	None	None	Oscillator Pins
XTAL	—	—	—				
$\overline{\text{RESET}}$	—	—	—	VDDR			External Reset
TEST	—	—	—	N.A.			Test Input
VREGEN	—	—	—	VDDX			Voltage Regulator Enable Input
XFC	—	—	—	VDDPLL			PLL Loop Filter
BKGD	$\overline{\text{TAGHI}}$	MODC	—	VDDR	Up	Up	Background Debug, Tag High, Mode Input
PAD[15:8]	**AN[15:8]**	**—**	**—**	VDDA	None	None	**Port AD Input, Analog Inputs of ATD**
PAD[7:0]	AN[7:0]	—	—				Port AD Input, Analog Inputs of ATD
PA[7:0]	ADDR[15:8]/ DATA[15:8]	—	—	VDDR	Up	Disabled	Port A I/O, Multiplexed Address/Data
PB[7:0]	ADDR[7:0]/ DATA[7:0]	—	—				Port B I/O, Multiplexed Address/Data
PE7	NOACC	$\overline{\text{XCLKS}}$	—		Up	Up	Port E I/O, Access, Clock Select
PE6	IPIPE1	MODB	—				Port E I/O, Pipe Status, Mode Input
PE5	IPIPE0	MODA	—				Port E I/O, Pipe Status, Mode Input
PE4	ECLK	—	—		Up	Up	Port E I/O, Bus Clock Output
PE3	$\overline{\text{LSTRB}}$	$\overline{\text{TAGLO}}$	—				Port E I/O, Byte Strobe, Tag Low
PE2	R/$\overline{\text{W}}$	—	—				Port E I/O, R/$\overline{\text{W}}$ in expanded modes
PE1	$\overline{\text{IRQ}}$	—	—				Port E Input, Maskable Interrupt
PE0	$\overline{\text{XIRQ}}$	—	—				Port E Input, Non Maskable Interrupt
PH7	**KWH7**	**$\overline{\text{SS2}}$**	**—**		Up or Down	Disabled	**Port H I/O, Interrupt, $\overline{\text{SS}}$ of SPI2**
PH6	**KWH6**	**SCK2**	**—**				**Port H I/O, Interrupt, SCK of SPI2**
PH5	**KWH5**	**MOSI2**	**—**				**Port H I/O, Interrupt, MOSI of SPI2**
PH4	**KWH4**	**MISO2**	**—**				**Port H I/O, Interrupt, MISO of SPI2**
PH3	**KWH3**	**$\overline{\text{SS1}}$**	**—**				**Port H I/O, Interrupt, $\overline{\text{SS}}$ of SPI1**
PH2	**KWH2**	**SCK1**	**—**				**Port H I/O, Interrupt, SCK of SPI1**
PH1	**KWH1**	**MOSI1**	**—**				**Port H I/O, Interrupt, MOSI of SPI1**
PH0	**KWH0**	**MISO1**	**—**				**Port H I/O, Interrupt, MISO of SPI1**

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Powered by	Internal Pull Resistor		Description
					Type	Reset State	
PJ7	KWJ7	TXCAN4	SCL	VDDX	Up or Down	Up	Port J I/O, Interrupt, TX of CAN4, SCL of IIC
PJ6	KWJ6	RXCAN4	SDA				Port J I/O, Interrupt, RX of CAN4, SDA of IIC
PJ[1:0]	**KWJ[1:0]**	**—**	**—**				**Port J I/O, Interrupts**
PK7	**$\overline{\text{ECS}}$**	**ROMONE**	**—**		Up	Up	**Port K I/O, Emulation Chip Select, ROM On Enable**
PK[5:0]	**XADDR[19:14]**		**—**				**Port K I/O, Extended Addresses**
PM7	**TXCAN4**	**—**	**—**		Up or Down	Disabled	**Port M I/O, CAN4 TX**
PM6	**RXCAN4**	**—**	**—**				**Port M I/O, CAN4 RX**
PM5	TXCAN0	TXCAN4	SCK0				Port M I/O, CAN0 TX, CAN4 TX, SPI0 SCK
PM4	RXCAN0	RXCAN4	MOSI0				Port M I/O, CAN0 RX, CAN4 RX, SPI0 MOSI
PM3	TXCAN0	$\overline{\text{SS0}}$	—				Port M I/O, CAN0 TX, SPI0 $\overline{\text{SS}}$
PM2	RXCAN0	MISO0	—				Port M I/O, CAN0 RX, SPI0 MISO
PM1	TXCAN0	—	—				Port M I/O, CAN0 TX
PM0	RXCAN0	—	—				Port M I/O, CAN0 RX
PP7	KWP7	PWM7	SCK2				Port P I/O, Interrupt, PWM Channel 7, SCK of SPI2
PP6	**KWP6**	**PWM6**	**$\overline{\text{SS2}}$**				**Port P I/O, Interrupt, PWM Channel 6, SPI2 $\overline{\text{SS}}$**
PP5	KWP5	PWM5	MOSI2				Port P I/O, Interrupt, PWM Channel 5, SPI2 MOSI
PP4	KWP4	PWM4	MISO2				Port P I/O, Interrupt, PWM Channel 4, SPI2 MISO
PP3	KWP3	PWM3	$\overline{\text{SS1}}$				Port P I/O, Interrupt, PWM Channel 3, SPI1 $\overline{\text{SS}}$
PP2	KWP2	PWM2	SCK1				Port P I/O, Interrupt, PWM Channel 2, SPI1 SCK
PP1	KWP1	PWM1	MOSI1				Port P I/O, Interrupt, PWM Channel 1, SPI1 MOSI
PP0	KWP0	PWM0	MISO1				Port P I/O, Interrupt, PWM Channel 0, SPI1 MISO
PS7	**$\overline{\text{SS0}}$**	**—**	**—**		Up or Down	Up	**Port S I/O, SPI0 $\overline{\text{SS}}$**
PS6	**SCK0**	**—**	**—**				**Port S I/O, SPI0 SCK**
PS5	**MOSI0**	**—**	**—**				**Port S I/O, SPI0 MOSI**
PS4	**MISO0**	**—**	**—**				**Port S I/O, SPI0 MISO**
PS3	TXD1	—	—				Port S I/O, SCI1TXD
PS2	RXD1	—	—				Port S I/O, SCI1RXD
PS1	TXD0	—	—				Port S I/O, SCI0 TXD
PS0	RXD0	—	—				Port S I/O, SCI0 RXD
PT[7:0]	IOC[7:0]	—	—		Up or Down	Disabled	Port T I/O, Timer channels

Table 2-2 Power and Ground

Mnemonic	Nominal Voltage	Description
VDD1 VDD2	2.5 V	Internal power and ground generated by internal regulator. These also allow an external source to supply the core VDD/VSS voltages and bypass the internal voltage regulator.
VSS1 VSS2	0V	
VDDR	3.3/5.0 V	External power and ground, supply to pin drivers and internal voltage regulator.
VSSR	0 V	
VDDX	3.3/5.0 V	External power and ground, supply to pin drivers.
VSSX	0 V	
VDDA	3.3/5.0 V	Operating voltage and ground for the analog-to-digital converter and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently.
VSSA	0 V	
VRH	3.3/5.0 V	Reference voltage high for the ATD converter.
VRL	0 V	Reference voltage low for the ATD converter.
VDDPLL	2.5 V	Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
VSSPLL	0 V	

NOTE: *All VSS pins must be connected together in the application. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on MCU pin load.*

2.3 Detailed Signal Descriptions

2.3.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

2.3.2 $\overline{\text{RESET}}$ — External Reset Pin

An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.

2.3.3 TEST — Test Pin

This input only pin is reserved for test.

NOTE: *The TEST pin must be tied to VSS in all applications.*

2.3.4 VREGEN — Voltage Regulator Enable Pin

This input only pin enables or disables the on-chip voltage regulator.

2.3.5 XFC — PLL Loop Filter Pin

PLL loop filter. Please ask your Freescale representative for the interactive application note to compute PLL loop filter elements. Any current leakage on this pin must be avoided.

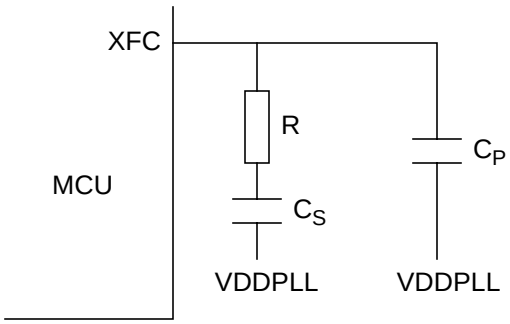


Figure 2-3 PLL Loop Filter Connections

2.3.6 BKGD / $\overline{\text{TAGHI}}$ / MODC — Background Debug, Tag High, and Mode Pin

The BKGD/$\overline{\text{TAGHI}}$/MODC pin is used as a pseudo-open-drain pin for the background debug communication. In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the instruction queue. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$.

2.3.7 PAD[15:0] / AN[15:0] — Port AD Input Pins [15:0]

PAD15 - PAD0 are general purpose input pins and analog inputs of the analog to digital converter ATD.

2.3.8 PA[7:0] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

PA7-PA0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.3.9 PB[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB7-PB0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.3.10 PE7 / NOACC / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7

PE7 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or “free” cycle. This signal will assert when the CPU is not using the bus.

The $\overline{\text{XCLKS}}$ is an input signal which controls whether a crystal in combination with the internal Loop Controlled Pierce (low power) oscillator is used or whether Full Swing Pierce oscillator/external clock circuitry is used. The state of this pin is latched at the rising edge of $\overline{\text{RESET}}$. If the input is a logic low the EXTAL pin is configured for an external clock drive or Full Swing Pierce Oscillator. If input is a logic high a Loop Controlled Pierce oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-up device during reset, if the pin is left floating, the default configuration is a Loop Controlled Pierce oscillator circuit on EXTAL and XTAL.

Table 2-3 Clock selection based on $\overline{\text{XCLKS}}$ during reset

$\overline{\text{XCLKS}}$	Description
1	Loop Controlled Pierce Oscillator selected
0	Full Swing Pierce Oscillator or external clock selected

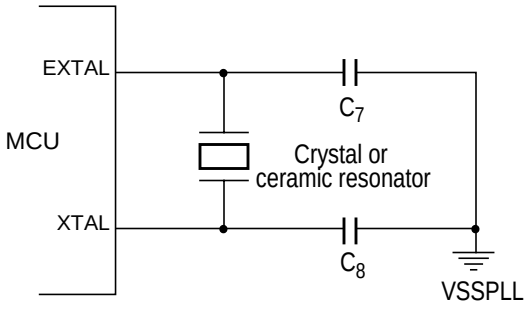
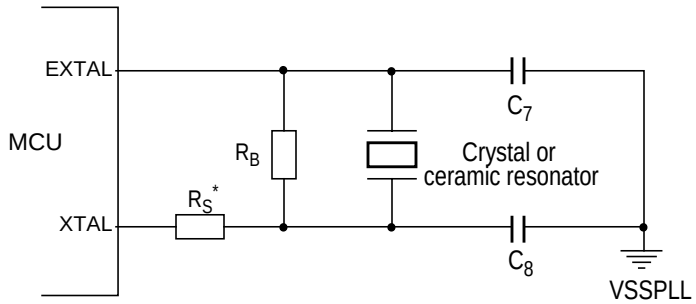


Figure 2-4 Loop Controlled Pierce Oscillator Connections ($\overline{\text{XCLKS}}$=1)



* Rs can be zero (shorted) when use with higher frequency crystals.
Refer to manufacturer’s data.

Figure 2-5 Full Swing Pierce Oscillator Connections ($\overline{\text{XCLKS}}$=0)

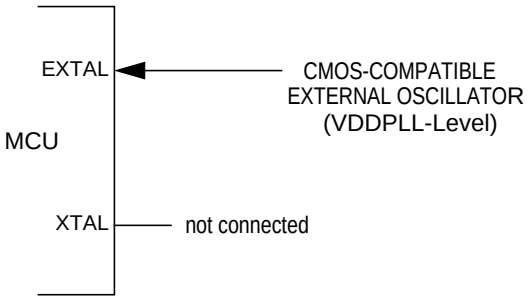


Figure 2-6 External Clock Connections ($\overline{\text{XCLKS}}$=0)

2.3.11 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE1.

2.3.12 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE0.

2.3.13 PE4 / ECLK — Port E I/O Pin 4

PE4 is a general purpose input or output pin. It can be configured to drive the internal bus clock ECLK. ECLK can be used as a timing reference.

2.3.14 PE3 / $\overline{\text{LSTRB}}$ / $\overline{\text{TAGLO}}$ — Port E I/O Pin 3

PE3 is a general purpose input or output pin. In MCU expanded modes of operation, $\overline{\text{LSTRB}}$ can be used for the low-byte strobe function to indicate the type of bus access and when instruction tagging is on, $\overline{\text{TAGLO}}$ is used to tag the low half of the instruction word being read into the instruction queue.

2.3.15 PE2 / R/$\overline{\text{W}}$ — Port E I/O Pin 2

PE2 is a general purpose input or output pin. In MCU expanded modes of operations, this pin drives the read/write output signal for the external bus. It indicates the direction of data on the external bus.

2.3.16 PE1 / $\overline{\text{IRQ}}$ — Port E Input Pin 1

PE1 is a general purpose input pin and the maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.3.17 PE0 / $\overline{\text{XIRQ}}$ — Port E Input Pin 0

PE0 is a general purpose input pin and the non-maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.3.18 PH7 / KWH7 / $\overline{\text{SS2}}$ — Port H I/O Pin 7

PH7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as slave select pin $\overline{\text{SS}}$ of the Serial Peripheral Interface 2 (SPI2).

2.3.19 PH6 / KWH6 / SCK2 — Port H I/O Pin 6

PH6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 2 (SPI2).

2.3.20 PH5 / KWH5 / MOSI2 — Port H I/O Pin 5

PH5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 2 (SPI2).

2.3.21 PH4 / KWH4 / MISO2 — Port H I/O Pin 2

PH4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 2 (SPI2).

2.3.22 PH3 / KWH3 / $\overline{\text{SS1}}$ — Port H I/O Pin 3

PH3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as slave select pin $\overline{\text{SS}}$ of the Serial Peripheral Interface 1 (SPI1).

2.3.23 PH2 / KWH2 / SCK1 — Port H I/O Pin 2

PH2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 1 (SPI1).

2.3.24 PH1 / KWH1 / MOSI1 — Port H I/O Pin 1

PH1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 1 (SPI1).

2.3.25 PH0 / KWH0 / MISO1 — Port H I/O Pin 0

PH0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 1 (SPI1).

2.3.26 PJ7 / KWJ7 / TXCAN4 / SCL — PORT J I/O Pin 7

PJ7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the transmit pin TXCAN for the Freescale Scalable Controller Area Network controller 4 (CAN4) or the serial clock pin SCL of the IIC module.

2.3.27 PJ6 / KWJ6 / RXCAN4 / SDA — PORT J I/O Pin 6

PJ6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the receive pin RXCAN for the Freescale Scalable Controller Area Network controller 4 (CAN4) or the serial data pin SDA of the IIC module.

2.3.28 PJ[1:0] / KWJ[1:0] — Port J I/O Pins [1:0]

PJ1 and PJ0 are general purpose input or output pins. They can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.3.29 PK7 / $\overline{\text{ECS}}$ / ROMONE — Port K I/O Pin 7

PK7 is a general purpose input or output pin. During MCU expanded modes of operation, this pin is used as the emulation chip select output ($\overline{\text{ECS}}$). During MCU expanded modes of operation, this pin is used to enable the Flash EEPROM memory in the memory map (ROMONE). At the rising edge of $\overline{\text{RESET}}$, the state of this pin is latched to the ROMON bit.For all other modes the reset state of the ROMON bit is as follows:

special single : ROMONE = 1

normal single : ROMONE = 1

emulation expanded wide : ROMONE = 0

emulation expanded narrow : ROMONE = 0

special test : ROMONE = 0

peripheral test : ROMONE = 1

2.3.30 PK[5:0] / XADDR[19:14] — Port K I/O Pins [5:0]

PK5-PK0 are general purpose input or output pins. In MCU expanded modes of operation, these pins provide the expanded address XADDR[19:14] for the external bus.

2.3.31 PM7 / TXCAN4 — Port M I/O Pin 7

PM7 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Freescale Scalable Controller Area Network controllers 4 (CAN4).

2.3.32 PM6 / RXCAN4 — Port M I/O Pin 6

PM6 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Freescale Scalable Controller Area Network controllers 4 (CAN4).

2.3.33 PM5 / TXCAN0 / TXCAN4 / SCK0 — Port M I/O Pin 5

PM5 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Freescale Scalable Controller Area Network controllers 0 or 4 (CAN0 or CAN4). It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

2.3.34 PM4 / RXCAN0 / RXCAN4/ MOSI0 — Port M I/O Pin 4

PM4 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Freescale Scalable Controller Area Network controllers 0 or 4 (CAN0 or CAN4). It can be configured as the master output (during master mode) or slave input pin (during slave mode) MOSI for the Serial Peripheral Interface 0 (SPI0).

2.3.35 PM3 / TXCAN0 / $\overline{SS0}$ — Port M I/O Pin 3

PM3 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0). It can be configured as the slave select pin $\overline{SS}$ of the Serial Peripheral Interface 0 (SPI0).

2.3.36 PM2 / RXCAN0 / MISO0 — Port M I/O Pin 2

PM2 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0). It can be configured as the master input (during master mode) or slave output pin (during slave mode) MISO for the Serial Peripheral Interface 0 (SPI0).

2.3.37 PM1 / TXCAN0 — Port M I/O Pin 1

PM1 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0).

2.3.38 PM0 / RXCAN0 — Port M I/O Pin 0

PM0 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0).

2.3.39 PP7 / KWP7 / PWM7 / SCK2 — Port P I/O Pin 7

PP7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 7 output. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 2 (SPI2).

2.3.40 PP6 / KWP6 / PWM6 / $\overline{SS2}$ — Port P I/O Pin 6

PP6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 6 output. It can be configured as slave select pin $\overline{SS}$ of the Serial Peripheral Interface 2 (SPI2).

2.3.41 PP5 / KWP5 / PWM5 / MOSI2 — Port P I/O Pin 5

PP5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 5 output. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 2 (SPI2).

2.3.42 PP4 / KWP4 / PWM4 / MISO2 — Port P I/O Pin 4

PP4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 4 output. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 2 (SPI2).

2.3.43 PP3 / KWP3 / PWM3 / $\overline{SS1}$ — Port P I/O Pin 3

PP3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 3 output. It can be configured as slave select pin $\overline{SS}$ of the Serial Peripheral Interface 1 (SPI1).

2.3.44 PP2 / KWP2 / PWM2 / SCK1 — Port P I/O Pin 2

PP2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 2 output. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 1 (SPI1).

2.3.45 PP1 / KWP1 / PWM1 / MOSI1 — Port P I/O Pin 1

PP1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 1 output. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 1 (SPI1).

2.3.46 PP0 / KWP0 / PWM0 / MISO1 — Port P I/O Pin 0

PP0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 0 output. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 1 (SPI1).

2.3.47 PS7 / $\overline{SS0}$ — Port S I/O Pin 7

PS6 is a general purpose input or output pin. It can be configured as the slave select pin $\overline{SS}$ of the Serial Peripheral Interface 0 (SPI0).

2.3.48 PS6 / SCK0 — Port S I/O Pin 6

PS6 is a general purpose input or output pin. It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

2.3.49 PS5 / MOSI0 — Port S I/O Pin 5

PS5 is a general purpose input or output pin. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.3.50 PS4 / MISO0 — Port S I/O Pin 4

PS4 is a general purpose input or output pin. It can be configured as master input (during master mode) or slave output pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.3.51 PS3 / TXD1 — Port S I/O Pin 3

PS3 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 1 (SCI1).

2.3.52 PS2 / RXD1 — Port S I/O Pin 2

PS2 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 1 (SCI1).

2.3.53 PS1 / TXD0 — Port S I/O Pin 1

PS1 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 0 (SCI0).

2.3.54 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 0 (SCI0).

2.3.55 PT[7:0] / IOC[7:0] — Port T I/O Pins [7:0]

PT7-PT0 are general purpose input or output pins. They can be configured as input capture or output compare pins IOC7-IOC0 of the Timer (TIM).

2.4 Power Supply Pins

MC9S12KG128 power and ground pins are described below.

NOTE: *All VSS pins must be connected together in the application.*

2.4.1 VDDX,VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.2 VDDR, VSSR — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.3 VDD1, VDD2, VSS1, VSS2 — Core Power Pins

Power is supplied to the MCU through VDD and VSS. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VREGEN is tied to ground.

NOTE: *No load allowed except for bypass capacitors.*

2.4.4 VDDA, VSSA — Power Supply Pins for ATD and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator and the analog to digital converter. It also provides the reference for the internal voltage regulator. This allows the supply voltage to the ATD and the reference voltage to be bypassed independently.

2.4.5 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

2.4.6 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently. This 2.5V voltage is generated by the internal voltage regulator.

NOTE: *No load allowed except for bypass capacitors.*

Section 3 System Clock Description

The Clock and Reset Generator provides the internal clock signals for the core and all peripheral modules. **Figure 3-1** shows the clock connections from the CRG to all modules. Consult the CRG Block Guide for details on clock generation.

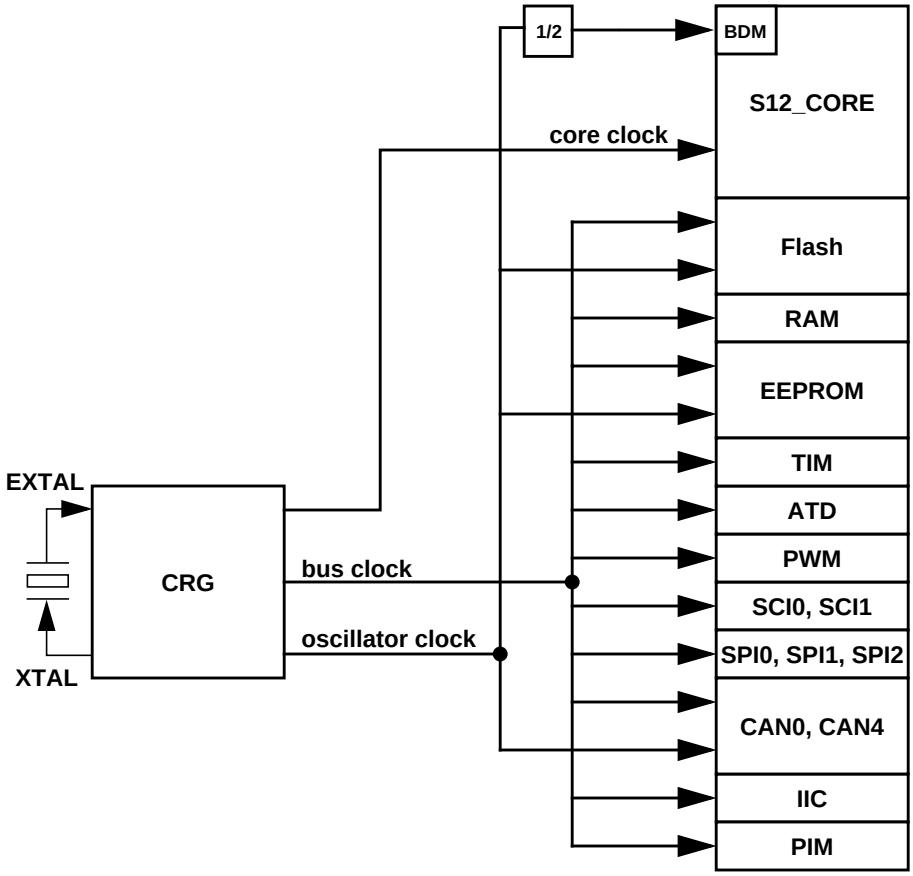


Figure 3-1 Clock Connections

Section 4 Modes of Operation

4.1 Overview

Eight possible modes determine the operating configuration of the MC9S12KG128. Each mode has an associated default memory map and external bus configuration.. In addition each operating mode, with the exception of Special Peripheral Mode(SPM), can be configured for low power operation by entering one of three low power sub-modes. The device is also equipped with security features which restrict certain modes of operation and limit access to internal memory. More detailed information on the various operating modes, and their configurations can be found in the HCS12 Core User Guide.

4.2 Modes of Operation

There are two basic categories of operating modes:

1. Normal modes: Some registers and bits are protected against accidental changes.
2. Special modes: Allow greater access to protected control registers and bits for special purposes such as testing.

In all Normal and Special modes a system development and debug feature, background debug mode (BDM), is available. In special single-chip mode, BDM is active immediately after reset.

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset (**Table 4-1**). The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal. The MODA and MODB pins are not available in the 80 pin package versions and are pulled down internally, restricting the mode selection out of reset to Single Chip Modes. When reseting into all modes except SPM, the ESTR bit in the EBICTL register is set to one, configuring the ECLK as a bus control signal, to assure that the reset vector can be fetched even if it located in an external slow memory device.

Table 4-1 Mode Selection

MODC	MODB	MODA	Mode Description	Notes
0	0	0	Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active.	Available in all package versions
0	0	1	Emulation Expanded Narrow, BDM allowed	Only available in 112 LQFP
0	1	0	Special Test (Expanded Wide), BDM allowed	Only available in 112 LQFP
0	1	1	Emulation Expanded Wide, BDM allowed	Only available in 112 LQFP
1	0	0	Normal Single Chip, BDM allowed	Available in all package versions
1	0	1	Normal Expanded Narrow, BDM allowed	Only available in 112 LQFP

Table 4-1 Mode Selection

MODC	MODB	MODA	Mode Description	Notes
1	1	0	Special Peripheral; BDM allowed but bus operations would cause bus conflicts (must not be used)	Only available in 112 LQFP
1	1	1	Normal Expanded Wide, BDM allowed	Only available in 112 LQFP

The following sections discuss the default bus setup and describe which aspects of the bus can be changed after reset on a per mode basis.

4.2.1 Normal Operating Modes

These modes provide three operating configurations: Normal Single-Chip Mode, Normal Expanded Wide Mode, and Normal Expanded Narrow Mode. Background debug (BDM) is available in all three normal modes, but must first be enabled for some operations by means of a BDM background command, then activated.

4.2.1.1 Normal Single-Chip Mode

There is no external expansion bus in this mode. Ports A and B are general purpose I/O pins, initially configured as high-impedance inputs with their internal pull-ups disabled. Port pins PE[7:2] are general purpose I/O pins, and port pins PE[1:0] are available as general purpose input only pins. All of Port E pins are initially configured as high-impedance inputs with internal pull-ups enabled.

The pins associated with Port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0, $\overline{\text{LSTRB}}$, and R/$\overline{\text{W}}$ while the MCU is in normal single chip mode.. In normal single chip mode, the associated control bits PIPOE, LSTRE, and RDWE are reset to zero, and writing a one to them in this mode does not change the operation of the associated Port E pins.

In normal single chip mode, the MODE register is writable one time. This allows a user program to change the bus mode to special single chip or normal expanded wide or normal expanded narrow modes and/or turn on visibility of internal accesses.

Port E, bit 4 can be configured for a free-running ECLK output by clearing NECLK=0. Typically the only use for an ECLK output while the MCU is in normal single chip mode would be to get a constant speed clock for use in the external application system.

4.2.1.2 Normal Expanded Wide Mode

In normal expanded wide mode, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port PE4 is configured as the ECLK output signal. These signals allow external memory and peripheral devices to be interfaced to the MCU.

Port E pins other than PE4/ECLK are configured as general purpose I/O pins (initially high-impedance inputs with internal pull-up resistors enabled). Control bits PIPOE, NECLK, LSTRE, and RDWE in the PEAR register can be used to configure Port E pins to act as bus control outputs instead of general purpose I/O pins.

It is possible to enable the pipe status signals on Port E bits 6 and 5 by setting the PIPOE bit in the PEAR register, but it would be unusual to do so in this mode. Development systems where pipe status signals are monitored would typically use the special variation of this mode.

The Port E bit 2 pin can be reconfigured as the R/$\overline{W}$ bus control signal by writing “1” to the RDWE bit in the PEAR register. If the expanded system includes external devices that can be written, such as RAM, the RDWE bit would need to be set before any attempt to write to an external location. If there are no writable resources in the external system, PE2 can be left as a general purpose I/O pin.

The Port E bit 3 pin can be reconfigured as the $\overline{LSTRB}$ bus control signal by writing “1” to the LSTRE bit in the PEAR register. The default condition of this pin is a general purpose input because the $\overline{LSTRB}$ function is not needed in all expanded wide applications.

The Port E bit 4 pin is initially configured as ECLK output with stretch. The ECLK output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. The ECLK is available for use in external select decode logic or as a constant speed clock for use in the external application system.

4.2.1.3 Normal Expanded Narrow Mode

The normal expanded narrow mode is used for lower cost production systems that use 8-bit wide external EPROMs or RAMs. Such systems take extra bus cycles to access 16-bit locations but this may be preferred over the extra cost of additional external memory devices.

Ports A and B are configured as a 16-bit address bus and Port A is multiplexed with data. Internal visibility is not available in this mode because the internal cycles would need to be split into two 8-bit cycles.

Since the PEAR register can only be written one time in this mode, use care to set all bits to the desired states during the single allowed write.

The PE3/$\overline{LSTRB}$ pin is always a general purpose I/O pin in normal expanded narrow mode. Although it is possible to write the LSTRE bit in the PEAR register to “1” in this mode, the state of LSTRE is overridden and Port E bit 3 cannot be reconfigured as the $\overline{LSTRB}$ output.

It is possible to enable the pipe status signals on Port E bits 6 and 5 by setting the PIPOE bit in the PEAR register, but it would be unusual to do so in this mode. LSTRB would also be needed to fully understand system activity. Development systems where pipe status signals are monitored would typically use special expanded wide mode or occasionally special expanded narrow mode.

The PE4/ECLK pin is initially configured as ECLK output with stretch. The ECLK output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. In normal expanded narrow mode, the ECLK is available for use in external select decode logic or as a constant speed clock for use in the external application system.

The PE2/R/W pin is initially configured as a general purpose input with a pull-up but this pin can be reconfigured as the R/$\overline{W}$ bus control signal by writing “1” to the RDWE bit in the PEAR register. If the expanded narrow system includes external devices that can be written such as RAM, the RDWE bit would need to be set before any attempt to write to an external location. If there are no writable resources in the external system, PE2 can be left as a general purpose I/O pin.

4.2.1.4 Emulation Expanded Wide Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. These signals allow external memory and peripheral devices to be interfaced to the MCU. These signals can also be used by a logic analyzer to monitor the progress of application programs.

The bus control related pins in Port E (PE7/NOACC, PE6/MODB/IPIPE1, PE5/MODA/IPIPE0, PE4/ECLK, PE3/$\overline{\text{LSTRB}}$/$\overline{\text{TAGLO}}$, and PE2/R/$\overline{\text{W}}$) are all configured to serve their bus control output functions rather than general purpose I/O. Writes to the bus control enable bits in the PEAR register in special mode are restricted.

4.2.1.5 Emulation Expanded Narrow Mode

Expanded narrow modes are intended to allow connection of single 8-bit external memory devices for lower cost systems that do not need the performance of a full 16-bit external data bus. Accesses to internal resources that have been mapped external (i.e. PORTA, PORTB, DDRA, DDRB, PORTE, DDRE, PEAR, PUCR, RDRIV) will be accessed with a 16-bit data bus on Ports A and B. Accesses of 16-bit external words to addresses which are normally mapped external will be broken into two separate 8-bit accesses using Port A as an 8-bit data bus. Internal operations continue to use full 16-bit data paths. They are only visible externally as 16-bit information if the IVIS bit is set to one in the MODE register.

Ports A and B are configured as multiplexed address and data output ports. During external accesses, address A15, data D15 and D7 are associated with PA7, address A0 is associated with PB0 and data D8 and D0 are associated with PA0. During internal visible accesses and accesses to internal resources that have been mapped external, address A15 and data D15 is associated with PA7 and address A0 and data D0 is associated with PB0.

The bus control related pins in Port E (PE7/NOACC, PE6/MODB/IPIPE1, PE5/MODA/IPIPE0, PE4/ECLK, PE3/$\overline{\text{LSTRB}}$/$\overline{\text{TAGLO}}$, and PE2/R/$\overline{\text{W}}$) are all configured to serve their bus control output functions rather than general purpose I/O. Notice that writes to the bus control enable bits in the PEAR register in special mode are restricted.

The main difference between special modes and normal modes is that some of the bus control and system control signals cannot be written in special modes.

4.2.2 Special Operating Modes

There are a total of three special operating modes: Special Single-Chip, Special Test, and Special Peripheral modes. These operating modes are commonly used in factory testing and system development.. Two of the special operating modes correspond to normal operating modes.

4.2.2.1 Special Single-Chip Mode

When the MCU is reset in this mode, the background debug mode is enabled and active. The MCU does not fetch the reset vector and execute application code as it would in other modes. Instead, the active background mode is in control of CPU execution and BDM firmware is waiting for additional serial commands through the BKGD pin. When a serial command instructs the MCU to return to normal

execution, the system will be configured as described below unless the reset states of internal control registers have been changed through background commands after the MCU was reset.

There is no external expansion bus after reset in this mode. Ports A and B are initially simple bidirectional I/O pins that are configured as high-impedance inputs with internal pull-ups disabled; however, writing to the mode select bits in the MODE register (which is allowed in special modes) can change this after reset. All of the Port E pins (except PE4/ECLK) are initially configured as general purpose high-impedance inputs with pull-ups enabled. PE4/ECLK is configured as the ECLK output in this mode.

The pins associated with Port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0, $\overline{\text{LSTRB}}$, and R/$\overline{\text{W}}$ while the MCU is in single chip modes In single chip modes, the associated control bits PIPOE, LSTRE and RDWE are reset to zero. Writing the opposite value into these bits in single chip mode does not change the operation of the associated Port E pins.

Port E, bit 4 can be configured for a free-running ECLK output by clearing NECLK=0. Typically the only use for an ECLK output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

4.2.2.2 Special Test Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. In special test mode, the write protection of many control bits is lifted so that they can be thoroughly tested without needing to go through reset.

4.2.2.3 Special Peripheral Mode

This mode is intended for Freescale factory testing of the MCU. In this mode, the CPU is inactive and an external (tester) bus master drives address, data and bus control signals in through Ports A, B and E. In effect, the whole MCU acts as if it was a peripheral under control of an external CPU. This allows faster testing of on-chip memory and peripherals than previous testing methods. Since the mode control register is not accessible in peripheral mode, the only way to change to another mode is to reset the MCU into a different mode. Background debugging should not be used while the MCU is in special peripheral mode as internal bus conflicts between BDM and the external master can cause improper operation of both functions.

4.3 Internal Visibility

Internal visibility is available when the MCU is operating in expanded wide modes or special test modes. It is not available in single-chip, peripheral or normal expanded narrow modes. Internal visibility is enabled by setting the IVIS bit in the MODE register.

If an internal access is made while the ECLK, R/$\overline{\text{W}}$, and $\overline{\text{LSTRB}}$ are configured as bus control outputs and internal visibility is off (IVIS=0), ECLK will remain low for the cycle, R/$\overline{\text{W}}$ will remain high, and address, data and the $\overline{\text{LSTRB}}$ pins will remain at their previous state.

When internal visibility is enabled (IVIS=1), certain internal cycles will be blocked from going external. During cycles when the BDM is selected, R/$\overline{\text{W}}$ will remain high, data will maintain its previous state, and address and $\overline{\text{LSTRB}}$ pins will be updated with the internal value. During CPU no access cycles when the

BDM is not driving, R/$\overline{W}$ will remain high, and address, data and the $\overline{LSTRB}$ pins will remain at their previous state.

4.4 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,
- Operation in single-chip mode,
- Operation from external memory with internal FLASH disabled.

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters stored in FLASH. Please refer to the HCS12 Core User Guide for more information about security.

4.4.1 Securing the Microcontroller

Once the user has programmed the FLASH, the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the Flash Block Guide for more details on the security configuration.

4.4.2 Operation of the Secured Microcontroller

4.4.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

4.4.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH will be disabled. BDM operations will be blocked.

4.4.3 Unsecuring the Microcontroller

There are two methods for unsecuring the Microcontroller. If the contents of the flash are known then the microcontroller can be unsecured using the backdoor key access feature. The other unsecuring method is to fully erase the FLASH.

4.4.3.1 Unsecuring the Microcontroller (backdoor key access)

In normal modes, either SINGLE CHIP or EXPANDED, the microcontroller may only be unsecured by using the backdoor key access feature. This requires knowledge of the contents of the backdoor keys, which must be written to the Flash memory space at the appropriate addresses, in the correct order. In addition, in SINGLE CHIP mode the user code stored in the Flash must have a method of receiving the backdoor key from an external stimulus. This external stimulus would typically be through one of the on-chip serial ports. After the backdoor sequence has been correctly matched, the microcontroller will be unsecured, and all Flash commands will be enabled and the Flash security byte can be programmed to the unsecure state, if desired.

Please note that if the system goes through a reset condition prior to successful configuration of unsecured mode the system will reset back into secured mode operation.

4.4.3.2 Unsecuring the Microcontroller (full FLASH erase)

In order to unsecure the microcontroller, the internal FLASH must be erased. This can be done through an external program in expanded mode.

Once the user has erased the FLASH, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH. Once this program completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

4.5 Low Power Modes

There are three low power modes available on the MC9S12KG128:

1. Stop
2. Pseudo Stop
3. Wait

Please see **Table A-8** for device operating characteristics in Stop, Pseudo Stop, and Wait modes. Consult the CRG Block Guide and the respective Block Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode.

Section 5 Resets and Interrupts

5.1 Overview

Consult the Exception Processing section of the HCS12 Core User Guide for information on resets and interrupts. Both local masking and CCR masking are included as listed in **Table 5-1**. System resets can be generated through external control of the $\overline{\text{RESET}}$ pin, through the clock and reset generator module CRG or through the low voltage reset (LVR) generator of the voltage regulator module. Refer to the CRG and VREG User Guides for detailed information on reset generation.

5.2 Vectors

5.2.1 Vector Table

Table 5-1 lists interrupt sources and vectors in default order of priority.

Table 5-1 Interrupt Vector Locations

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
$FFFE, $FFFF	External Reset, Power On Reset or Low Voltage Reset (see CRG Flags Register to determine reset source)	None	None	–
$FFFC, $FFFD	Clock Monitor fail reset	None	PLLCTL (CME, FCME)	–
$FFFA, $FFFB	COP failure reset	None	COP rate select	–
$FFF8, $FFF9	Unimplemented instruction trap	None	None	–
$FFF6, $FFF7	SWI	None	None	–
$FFF4, $FFF5	XIRQ	X-Bit	None	–
$FFF2, $FFF3	IRQ	I-Bit	IRQCR (IRQEN)	$F2
$FFF0, $FFF1	Real Time Interrupt	I-Bit	CRGINT (RTIE)	$F0
$FFEE, $FFEF	Standard Timer channel 0	I-Bit	TIE (C0I)	$EE
$FFEC, $FFED	Standard Timer channel 1	I-Bit	TIE (C1I)	$EC
$FFEA, $FFEB	Standard Timer channel 2	I-Bit	TIE (C2I)	$EA
$FFE8, $FFE9	Standard Timer channel 3	I-Bit	TIE (C3I)	$E8
$FFE6, $FFE7	Standard Timer channel 4	I-Bit	TIE (C4I)	$E6
$FFE4, $FFE5	Standard Timer channel 5	I-Bit	TIE (C5I)	$E4
$FFE2, $FFE3	Standard Timer channel 6	I-Bit	TIE (C6I)	$E2
$FFE0, $FFE1	Standard Timer channel 7	I-Bit	TIE (C7I)	$E0
$FFDE, $FFDF	Standard Timer overflow	I-Bit	TSCR2 (TOI)	$DE
$FFDC, $FFDD	Pulse accumulator overflow	I-Bit	PACTL (PAOVI)	$DC
$FFDA, $FFDB	Pulse accumulator input edge	I-Bit	PACTL (PAI)	$DA
$FFD8, $FFD9	SPI0	I-Bit	SPICR1 (SPIE, SPTIE)	$D8
$FFD6, $FFD7	SCI0	I-Bit	SCICR2 (TIE, TCIE, RIE, ILIE)	$D6
$FFD4, $FFD5	SCI1	I-Bit	SCICR2 (TIE, TCIE, RIE, ILIE)	$D4
$FFD2, $FFD3	ATD	I-Bit	ATDCTL2 (ASCIE)	$D2

$FFD0, $FFD1	Reserved	I-Bit	Reserved	$D0
$FFCE, $FFCF	Port J	I-Bit	PIEJ (PIEJ7, PIEJ6, PIEJ1, PIEJ0)	$CE
$FFCC, $FFCD	Port H	I-Bit	PIEH (PIEH7-0)	$CC
$FFCA, $FFCB	Reserved	I-Bit	Reserved	$CA
$FFC8, $FFC9		I-Bit		$C8
$FFC6, $FFC7	CRG PLL lock	I-Bit	CRGINT (LOCKIE)	$C6
$FFC4, $FFC5	CRG Self Clock Mode	I-Bit	CRGINT (SCMIE)	$C4
$FFC2, $FFC3	FLASH Double Fault Detect	I-Bit	FCNFG (DFDIE)	$C2
$FFC0, $FFC1	IIC Bus	I-Bit	IBCR (IBIE)	$C0
$FFBE, $FFBF	SPI1	I-Bit	SPICR1 (SPIE, SPTIE)	$BE
$FFBC, $FFBD	SPI2	I-Bit	SPICR1 (SPIE, SPTIE)	$BC
$FFBA, $FFBB	EEPROM coomand	I-Bit	ECNFG (CCIE, CBEIE)	$BA
$FFB8, $FFB9	FLASH command	I-Bit	FCNFG (CCIE, CBEIE)	$B8
$FFB6, $FFB7	CAN0 wake-up	I-Bit	CANRIER (WUPIE)	$B6
$FFB4, $FFB5	CAN0 errors	I-Bit	CANRIER (CSCIE, OVRIE)	$B4
$FFB2, $FFB3	CAN0 receive	I-Bit	CANRIER (RXFIE)	$B2
$FFB0, $FFB1	CAN0 transmit	I-Bit	CANTIER (TXEIE2 - TXEIE0)	$B0
$FFAE, $FFAF	Reserved	I-Bit	Reserved	$AE
$FFAC, $FFAD		I-Bit		$AC
$FFAA, $FFAB		I-Bit		$AA
$FFA8, $FFA9		I-Bit		$A8
$FFA6, $FFA7		I-Bit		$A6
$FFA4, $FFA5		I-Bit		$A4
$FFA2, $FFA3		I-Bit		$A2
$FFA0, $FFA1		I-Bit		$A0
$FF9E, $FF9F		I-Bit		$9E
$FF9C, $FF9D		I-Bit		$9C
$FF9A, $FF9B		I-Bit		$9A
$FF98, $FF99		I-Bit		$98
$FF96, $FF97	CAN4 wake-up	I-Bit	CANRIER (WUPIE)	$96
$FF94, $FF95	CAN4 errors	I-Bit	CANRIER (CSCIE, OVRIE)	$94
$FF92, $FF93	CAN4 receive	I-Bit	CANRIER (RXFIE)	$92
$FF90, $FF91	CAN4 transmit	I-Bit	CANTIER (TXEIE2 - TXEIE0)	$90
$FF8E, $FF8F	Port P	I-Bit	PIEP (PIEP7-0)	$8E
$FF8C, $FF8D	PWM Emergency Shutdown	I-Bit	PWMSDN (PWMIE)	$8C
$FF80 to $FF8B	Reserved			

5.3 Resets

Resets are a subset of the interrupts featured in**Table 5-1**. The different sources capable of generating a system reset are summarized in **Table 5-2**.

Table 5-2 Reset Summary

Reset	Priority	Source	Vector
Power-on Reset	1	CRG Module	$FFFE, $FFFF
External Reset	1	RESET pin	$FFFE, $FFFF
Low Voltage Reset	1	VREG Module	$FFFE, $FFFF
Clock Monitor Reset	2	CRG Module	$FFFC, $FFFD
COP Watchdog Reset	3	CRG Module	$FFFA, $FFFB

5.3.1 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block Guides for register reset states. Refer to the HCS12 Core User Guides for mode dependent pin configuration of port A, B and E out of reset.

Refer to the PIM Block Guide for reset configurations of all peripheral module ports.

Refer to **Table 1-1** for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

Section 6 HCS12 Core Block Description

Consult the HCS12 Core User Guide for information about the HCS12 core modules, i.e. central processing unit (CPU), interrupt module (INT), module mapping control module (MMC), multiplexed external bus interface (MEBI), the Debug module (DBG), and background debug mode module (BDM).

Section 7 Analog to Digital Converter (ATD) Block Description

Consult the ATD_10B16C Block Guide for further information about the A/D Converter module. When the ATD_10B16C Block Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 8 Clock Reset Generator (CRG) Block Description

Consult the CRG Block Guide for information about the Clock and Reset Generator module.

Section 9 EEPROM Block Description

Consult the EETS2K Block User Guide for information about the EEPROM module.

Section 10 Flash EEPROM Block Description

Consult the FTS128K1ECC Block Guide for information about the flash module.

Section 11 IIC Block Description

Consult the IIC Block User Guide for information about the Inter-IC Bus module.

Section 12 MSCAN Block Description

There are two MSCAN modules (CAN4 and CAN0). Consult the MSCAN Block User Guide for information about the Freescale Scalable CAN Module.

Section 13 OSC Block Description

Consult the OSC_LCP Block User Guide for information about the Oscillator module.

Section 14 Port Integration Module (PIM) Block Description

Consult the PIM_9KG128 Block Guide for information about the Port Integration Module.

Section 15 Pulse Width Modulator (PWM) Block Description

Consult the PWM_8B8C Block Guide for information about the Pulse Width Modulator Module. When the PWM_8B8C Block Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 16 Serial Communications Interface (SCI) Block Description

There are two Serial Communications Interface modules (SCI1 and SCI0). Consult the SCI Block Guide for information about the Serial Communications Interface module.

Section 17 Serial Peripheral Interface (SPI) Block Description

There are three Serial Peripheral Interfaces (SPI2, SPI1 and SPI0) implemented on MC9S12KG128. Consult the SPI Block User Guide for information about each Serial Peripheral Interface module.

Section 18 Timer (TIM) Block Description

Consult the TIM_16B8C Block Guide for information about the Timer module. When the TIM_16B8C Block Guide refers to *freeze mode* this is equivalent to *active BDM mode.*

Section 19 Voltage Regulator (VREG) Block Description

Consult the VREG_3V3 Block Guide for information about the dual output linear voltage regulator.

19.1 Device-specific information

19.1.1 VDD1, VDD2, VSS1, VSS2

In both the 112 pin LQFP and the 80 pin QFP package versions, both internal VDD and VSS of the 2.5V domain are bonded out on 2 sides of the device as two pin pairs (VDD1, VSS1 & VDD2, VSS2). VDD1

and VDD2 are connected together internally. VSS1 and VSS2 are connected together internally. This allows systems to employ better supply routing and further decoupling.

19.1.2 Recommended PCB Layout

The PCB must be carefully laid out to ensure proper operation of the voltage regulator as well as of the MCU itself. The following rules must be observed:

- Every supply pair must be decoupled by a ceramic capacitor connected as near as possible to the corresponding pins (C1 - C6).
- Central point of the ground star should be the VSSR pin.
- Use low ohmic low inductance connections between VSS1, VSS2 and VSSR.
- VSSPLL must be directly connected to VSSR.
- Keep traces of VSSPLL, EXTAL and XTAL as short as possible and occupied board area for C7, C8 and Q1 as small as possible.
- Do not place other signals or supplies underneath area occupied by C7, C8 and Q1 and the connection area to the MCU.
- Central power input should be fed in at the VDDA/VSSA pins.

Table 19-1 Recommended decoupling capacitor choice

Component	Purpose	Type	Value
C1	VDD1 filter cap	ceramic X7R	400nF
C2	VDD2 filter cap (80 QFP only)	ceramic X7R	400nF
C3	VDDA filter cap	ceramic X7R	100nF
C4	VDDR filter cap	X7R/tantalum	>=100nF
C5	VDDPLL filter cap	ceramic X7R	200nF
C6	VDDX filter cap	X7R/tantalum	>=100nF
C7	OSC load cap		
C8	OSC load cap		
C9	PLL loop filter cap	See PLL specification chapter	
C10	PLL loop filter cap		
R1	PLL loop filter res		
Q1	Quartz		

Figure 19-1 Recommended PCB Layout for 112LQFP

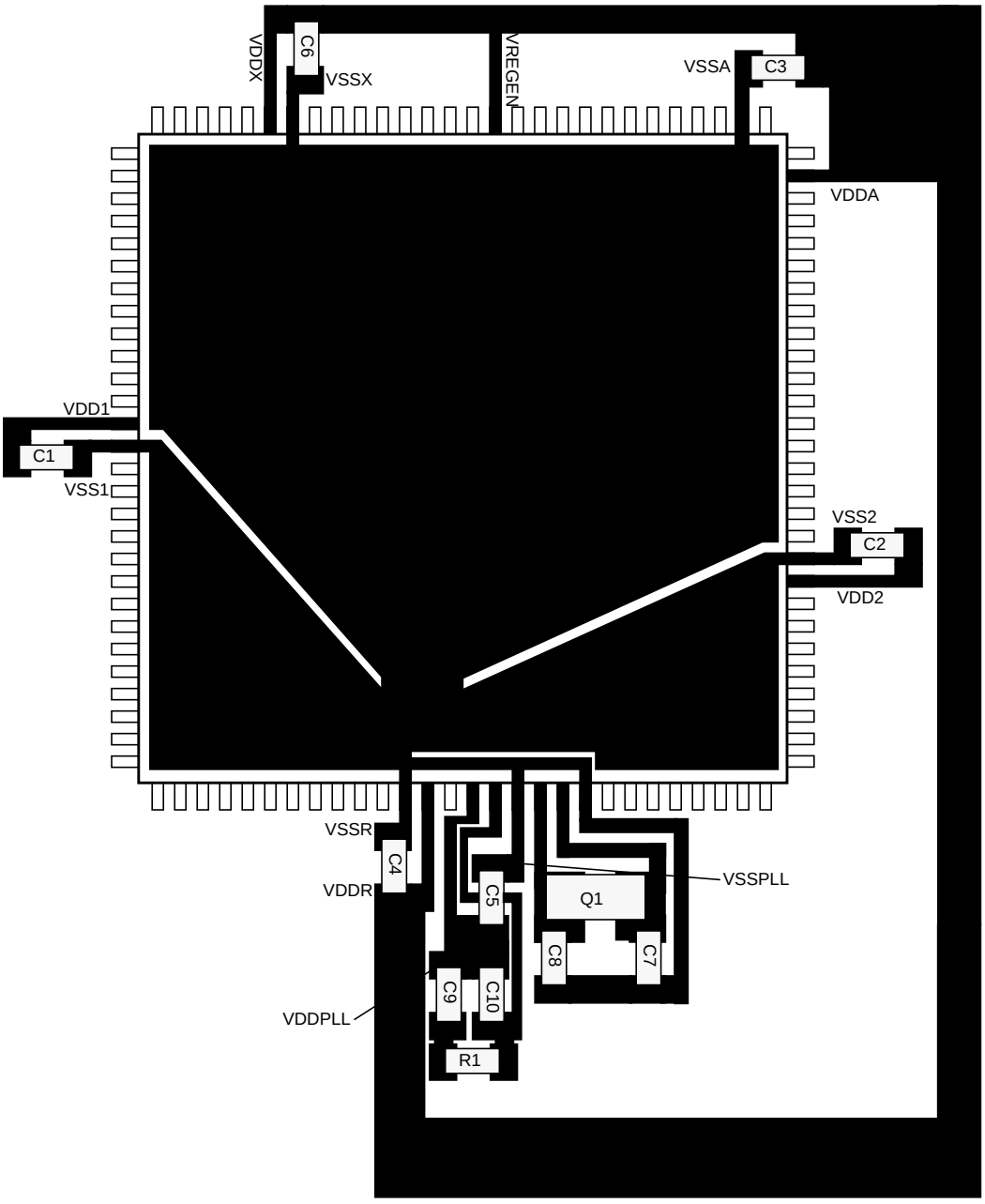
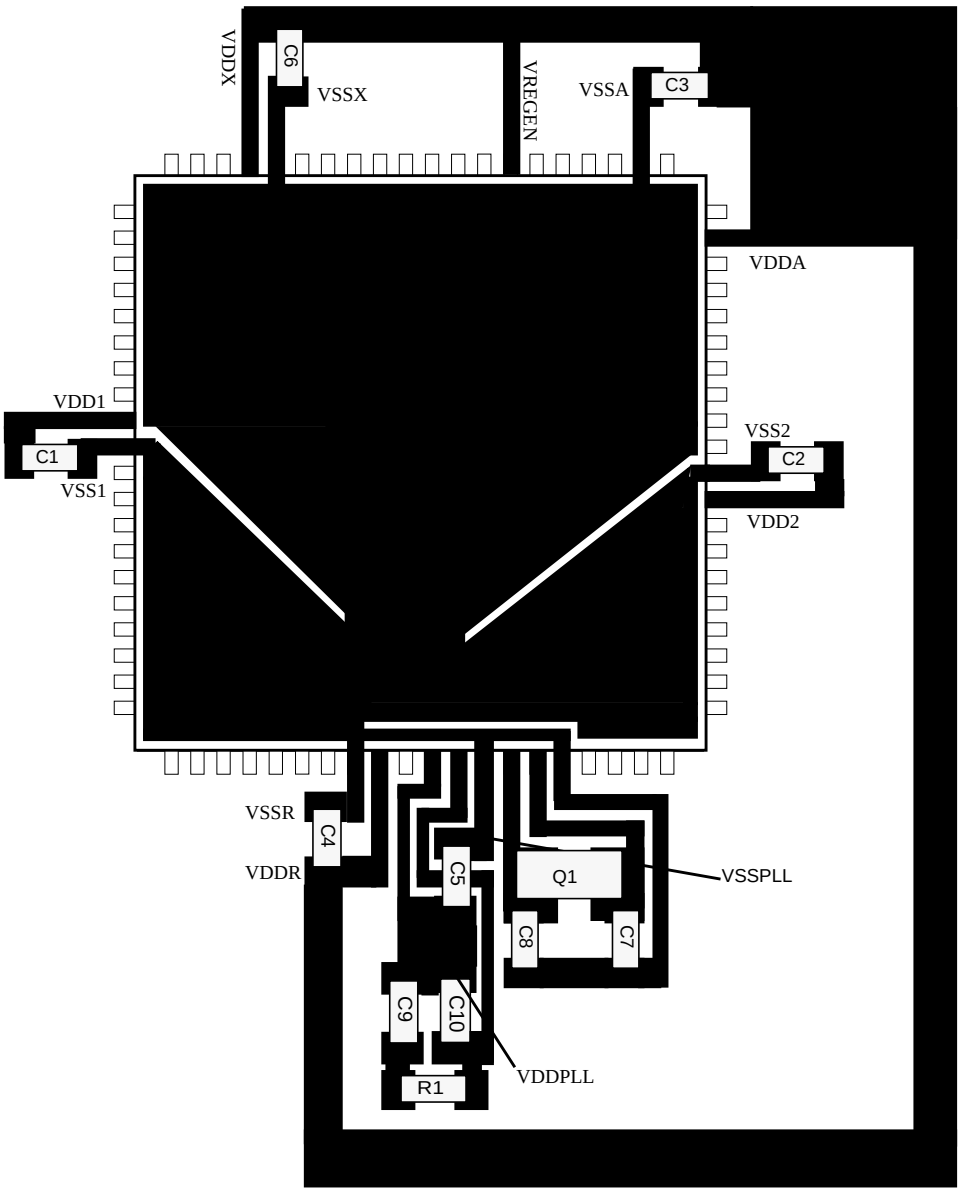


Figure 19-2 Recommended PCB Layout for 80QFP



Appendix A Electrical Characteristics

A.1 General

NOTE: *The electrical characteristics given in this section are preliminary and should be used as a guide only. Values cannot be guaranteed by Freescale and are subject to change without notice.*

This supplement contains the most accurate electrical information for the MC9S12KG128 microcontroller available at the time of publication. The information should be considered **PRELIMINARY** and is subject to change.

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

NOTE: *This classification is shown in the column labeled "C" in the parameter tables where appropriate.*

P:

Those parameters are guaranteed during production testing on each individual device.

C:

Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. They are regularly verified by production monitors.

T:

Those parameters are achieved by design characterization on a small sample size from typical devices. All values shown in the typical column are within this category.

D:

Those parameters are derived mainly from simulations.

A.1.2 Power Supply

The MC9S12KG128 utilizes several pins to supply power to the I/O ports, A/D converter, oscillator and PLL as well as the digital core.

The VDDA, VSSA pair supplies the A/D converter.
The VDDX, VSSX pair supplies the I/O pins

The VDDR, VSSR pair supplies the internal voltage regulator.
VDD1, VSS1, VDD2 and VSS2 are the supply pins for the digital logic.
VDDPLL, VSSPLL supply the oscillator and the PLL.
VSS1 and VSS2 are internally connected by metal.
VDD1 and VDD2 are internally connected by metal.
VDDA, VDDX, VDDR as well as VSSA, VSSX, VSSR are connected by anti-parallel diodes for ESD protection.

NOTE: *In the following context VDD5 is used for either VDDA, VDDR and VDDX; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted. IDD5 denotes the sum of the currents flowing into the VDDA, VDDX and VDDR pins. VDD is used for VDD1, VDD2 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL. IDD is used for the sum of the currents flowing into VDD1 and VDD2.*

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 3.3V/5V I/O pins

Those I/O pins have a nominal level of 3.3V or 5V depending on the application operating point. This group of pins is comprised of all port I/O pins, the analog inputs, BKGD pin and the RESET inputs.The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

A.1.3.2 Analog Reference

This group of pins is comprised of the VRH and VRL pins.

A.1.3.3 Oscillator

The pins EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 PLL

The pin XFC dedicated to the oscillator have a nominal 2.5V level. It is supplied by VDDPLL.

A.1.3.5 TEST

This pin is used for production testing only.

A.1.4 Current Injection

Power supply must maintain regulation within operating V_{DD5} or V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD5}$) is greater than I_{DD5}, the injection current may flow out of VDD5 and could result in external power supply going out of regulation.

Insure external VDD5 load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g. if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

A.1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS5} or V_{DD5}).

Table A-1 Absolute Maximum Ratings

Num	Rating	Symbol	Min	Max	Unit
1	I/O, Regulator and Analog Supply Voltage	V_{DD5}	-0.3	6.5	V
2	Digital Logic Supply Voltage[1]	V_{DD}	-0.3	3.0	V
3	PLL Supply Voltage (1)	V_{DDPLL}	-0.3	3.0	V
4	Voltage difference VDDX to VDDR and VDDA	Δ_{VDDX}	-0.3	0.3	V
5	Voltage difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.3	0.3	V
6	Digital I/O Input Voltage	V_{IN}	-0.3	6.5	V
7	Analog Reference	$V_{RH,}$ V_{RL}	-0.3	6.5	V
8	XFC, EXTAL, XTAL inputs	V_{ILV}	-0.3	3.0	V
9	TEST input	V_{TEST}	-0.3	10.0	V
10	Instantaneous Maximum Current Single pin limit for all digital I/O pins [2]	I_D	-25	+25	mA
11	Instantaneous Maximum Current Single pin limit for XFC, EXTAL, XTAL[3]	I_{DL}	-25	+25	mA
12	Instantaneous Maximum Current Single pin limit for TEST[4]	I_{DT}	-0.25	0	mA
13	Operating Temperature Range (packaged)	T_A	– 40	125	°C
14	Operating Temperature Range (junction)	T_J	– 40	140	°C
15	Storage Temperature Range	T_{stg}	– 65	155	°C

NOTES:
1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
2. All digital I/O pins are internally clamped to V_{SSX} and V_{DDX}, V_{SSR} and V_{DDR} or V_{SSA} and V_{DDA}.
3. These pins are internally clamped to V_{SSPLL} and V_{DDPLL}
4. This pin is clamped low to V_{SSPLL}, but not clamped high. This pin must be tied low in applications.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Latch-up	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

Table A-3 ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	2000	-	V
2	C	Machine Model (MM)	V_{MM}	200	-	V
3	C	Charge Device Model (CDM)	V_{CDM}	500	-	V
4	C	Latch-up Current at 125°C positive negative	I_{LAT}	+100 -100	-	mA
5	C	Latch-up Current at 27°C positive negative	I_{LAT}	+200 -200	-	mA

A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

NOTE: *Instead of specifying ambient temperature all parameters are specified for the more meaningful silicon junction temperature. For power dissipation calculations refer to* ***Section A.1.8 Power Dissipation and Thermal Characteristics****.*

Table A-4 Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
I/O, Regulator and Analog Supply Voltage	V_{DD5}	3.15	3.3/5	5.5	V
Digital Logic Supply Voltage[1]	V_{DD}	2.35	2.5	2.75	V
PLL Supply Voltage (1)	V_{DDPLL}	2.35	2.5	2.75	V
Voltage Difference VDDX to VDDA	Δ_{VDDX}	-0.1	0	0.1	V
Voltage Difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.1	0	0.1	V
Oscillator	f_{osc}	0.5	-	16	MHz
Bus Frequency	f_{bus}	0.5	-	25	MHz
MC9S12KG128**C** Operating Junction Temperature Range	T_J	-40	-	100	°C
Operating Ambient Temperature Range [2]	T_A	-40	27	85	°C
MC9S12KG128**V** Operating Junction Temperature Range	T_J	-40	-	120	°C
Operating Ambient Temperature Range (2)	T_A	-40	27	105	°C
MC9S12KG128**M** Operating Junction Temperature Range	T_J	-40	-	140	°C
Operating Ambient Temperature Range (2)	T_A	-40	27	125	°C

NOTES:
1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when this regulator is disabled and the device is powered from an external source.
2. Please refer to **Section A.1.8 Power Dissipation and Thermal Characteristics** for more details about the relation between ambient temperature T_A and device junction temperature T_J.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

For R_{DSON} is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in **Table A-8** and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

Table A-5 Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB[2]	θ_{JA}	-	-	54	^{o}C/W
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes[3]	θ_{JA}	-	-	41	^{o}C/W
3	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	-	-	51	^{o}C/W
4	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	-	-	41	^{o}C/W

NOTES:
1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-2
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 3.3V/5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

Table A-6 5V I/O Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input High Voltage	V_{IH}	0.65*V_{DD5}	-	V_{DD5} + 0.3	V
2	P	Input Low Voltage	V_{IL}	V_{SS5} - 0.3	-	0.35*V_{DD5}	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current (pins in high ohmic input mode)[1] V_{in} = V_{DD5} or V_{SS5}	I_{in}	–2.5	-	2.5	µA
5	P	Output High Voltage (pins in output mode) Partial Drive I_{OH} = –2.0mA Full Drive I_{OH} = –10.0mA	V_{OH}	V_{DD5} – 0.8	-	-	V
6	P	Output Low Voltage (pins in output mode) Partial Drive I_{OL} = +2.0mA Full Drive I_{OL} = +10.0mA	V_{OL}	-	-	0.8	V
7	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	-	-	–130	µA
8	P	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	-10	-	-	µA
9	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	-	-	130	µA
10	P	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	10	-	-	µA
11	D	Input Capacitance	C_{in}		6	-	pF
12	T	Injection current[2] Single Pin limit Total Device Limit. Sum of all injected currents	I_{ICS} I_{ICP}	-2.5 -25	-	2.5 25	mA
13	P	Port H, J, P Interrupt Input Pulse filtered[3]	t_{pign}			3	µs
14	P	Port H, J, P Interrupt Input Pulse passed(3)	t_{pval}	10			µs

NOTES:
1. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 C to 12 C in the temperature range from 50 C to 125 C.
2. Refer to **Section A.1.4 Current Injection**, for more details
3. Parameter only applies in STOP or Pseudo STOP mode.

Table A-7 Preliminary 3.3V I/O Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input High Voltage	V_{IH}	0.65*V_{DD5}	-	V_{DD5} + 0.3	V
2	P	Input Low Voltage	V_{IL}	V_{SS5} - 0.3	-	0.35*V_{DD5}	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current (pins in high ohmic input mode)[1] V_{in} = V_{DD5} or V_{SS5}	I_{in}	–2.5	-	2.5	µA
5	P	Output High Voltage (pins in output mode) Partial Drive I_{OH} = –2.0mA Full Drive I_{OH} = –10.0mA	V_{OH}	V_{DD5} – 0.8	-	-	V
6	P	Output Low Voltage (pins in output mode) Partial Drive I_{OL} = +2.0mA Full Drive I_{OL} = +10.0mA	V_{OL}	-	-	0.8	V
7	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	-	-	–130	µA
8	P	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	-10	-	-	µA
9	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	-	-	130	µA
10	P	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	10	-	-	µA
11	D	Input Capacitance	C_{in}		6	-	pF
12	T	Injection current[2] Single Pin limit Total Device Limit. Sum of all injected currents	I_{ICS} I_{ICP}	-2.5 -25	-	2.5 25	mA
13	P	Port P, J Interrupt Input Pulse filtered[3]	t_{PULSE}			3	µs
14	P	Port P, J Interrupt Input Pulse passed(3)	t_{PULSE}	10			µs

NOTES:
1. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 C to 12 C in the temperature range from 50 C to 125 C.
2. Refer to **Section A.1.4 Current Injection**, for more details
3. Parameter only applies in STOP or Pseudo STOP mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 25MHz bus frequency using a 4MHz oscillator.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-8 Supply Current Characteristics

Conditions are shown in **Table A-4** unless otherwise noted						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Run supply currents Single Chip, Internal regulator enabled	I_{DD5}			65	mA
2	Wait Supply current All modules enabled only RTI enabled	I_{DDW}			40 5	mA
3	Pseudo Stop Current (RTI and COP enabled) -40°C 27°C 70°C 85°C 105°C 125°C 135° C	I_{DDPS}		 TBD 600 TBD TBD TBD TBD 1000	 750 5000	µA
4	Pseudo Stop Current (RTI and COP disabled) -40°C 27°C 70°C 85°C 105°C 125°C 135°C	I_{DDPS}		 TBD 160 TBD TBD TBD TBD 700	 400 5000	µA
5	Stop Current -40°C 27°C 70°C 85°C 105°C 125°C 135°C	I_{DDS}		 TBD 30 TBD 200 TBD TBD 500	 100 5000	µA

A.2 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

A.2.1 ATD Operating Characteristics

The **Table A-9** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
VSSA ≤ VRL ≤ VIN ≤ VRH ≤ VDDA. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-9 5V ATD Operating Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 VRL VRH	 VSSA VDDA/2		 VDDA/2 VDDA	 V V
2	C	Differential Reference Voltage[1]	VRH-VRL	4.75	5.0	5.25	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK} Conv, Time at 4.0MHz[3] ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10} T_{CONV10}	 14 7 3.5		 28 14 7	 Cycles µs µs
5	D	ATD 8-Bit Conversion Period Clock Cycles(1) Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6		 26 13	 Cycles µs
6	D	Stop Recovery Time (V_{DDA}=5.0 Volts)	t_{SR}			20	µs
7	P	Reference Supply current	I_{REF}			0.375	mA

NOTES:
1. Full accuracy is not guaranteed when differential voltage is less than 4.75V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.
3. Reduced accuracy see **Table A-12** and **Table A-13**.

Table A-10 3.3V ATD Operating Characteristics

Conditions are shown in **Table A-4** unless otherwise noted; Supply Voltage 3.3V-10% <= V_{DDA} <= 3.3V+10%							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$		 $V_{DDA}/2$ V_{DDA}	 V V
2	C	Differential Reference Voltage	V_{RH}-V_{RL}	3.0	3.3	3.6	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[1] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK} Conv, Time at 4.0MHz[2] ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10} T_{CONV10}	 14 7 3.5		 28 14 7	 Cycles µs µs
5	D	ATD 8-Bit Conversion Period Clock Cycles(1) Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6		 26 13	 Cycles µs
6	D	Recovery Time (V_{DDA}=3.3 Volts)	t_{REC}			20	µs
7	P	Reference Supply current	I_{REF}			0.250	mA

NOTES:
1. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.
2. Reduced accuracy see **Table A-12** and **Table A-13**.

A.2.2 Factors influencing accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

A.2.2.1 Source Resistance:

Due to the input pin leakage current as specified in **Table A-6** and **Table A-7**in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance are allowed.

A.2.2.2 Source capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB, then the external filter capacitor, $C_f \geq 1024 * (C_{INS} - C_{INN})$.

A.2.2.3 Current injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion

values of $3FF ($FF in 8-bit mode) for analog inputs greater than VRH and $000 for values less than VRL unless the current is higher than specified as disruptive conditions.

2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.
The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K * R_S * I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table A-11 ATD Electrical Characteristics

Conditions are shown in **Table A-4** unless otherwise noted						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Max input Source Resistance	R_S	-	-	1	KΩ
2	Total Input Capacitance Non Sampling Sampling	 C_{INN} C_{INS}			 10 22	pF
3	Disruptive Analog Input Current	I_{NA}	-2.5		2.5	mA
4	Coupling Ratio positive current injection	K_p			10^{-4}	A/A
5	Coupling Ratio negative current injection	K_n			10^{-2}	A/A

A.2.3 ATD accuracy

Table A-12 and **Table A-13** specify the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-12 5V ATD Conversion Performance

Conditions are shown in **Table A-4** unless otherwise noted $V_{REF} = V_{RH} - V_{RL}$ = 5.12V. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV f_{ATDCLK} = 2.0MHz							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	10-Bit Resolution	LSB		5		mV
2	P	10-Bit Differential Nonlinearity	DNL	–1		1	Counts
3	P	10-Bit Integral Nonlinearity	INL	–2.5	±1.5	2.5	Counts
4	P	10-Bit Absolute Error[1]	AE	-3	±2.0	3	Counts
5	C	10-Bit Absolute Error at f_{ATDCLK}= 4MHz	AE		±7.0		Counts
6	P	8-Bit Resolution	LSB		20		mV
7	P	8-Bit Differential Nonlinearity	DNL	–0.5		0.5	Counts
8	P	8-Bit Integral Nonlinearity	INL	–1.0	±0.5	1.0	Counts
9	P	8-Bit Absolute Error(1)	AE	-1.5	±1.0	1.5	Counts

NOTES:
1. These values include quantization error which is inherently 1/2 count for any A/D converter.

Table A-13 3.3V ATD Conversion Performance

Conditions are shown in **Table A-4** unless otherwise noted $V_{REF} = V_{RH} - V_{RL}$ = 3.328V. Resulting to one 8 bit count = 13mV and one 10 bit count = 3.25mV f_{ATDCLK} = 2.0MHz							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	10-Bit Resolution	LSB		3.25		mV
2	P	10-Bit Differential Nonlinearity	DNL	–1.5		1.5	Counts
3	P	10-Bit Integral Nonlinearity	INL	–3.5	±1.5	3.5	Counts
4	P	10-Bit Absolute Error[1]	AE	-5	±2.5	5	Counts
5	C	10-Bit Absolute Error at f_{ATDCLK}= 4MHz	AE		±7.0		Counts
6	P	8-Bit Resolution	LSB		13		mV
7	P	8-Bit Differential Nonlinearity	DNL	–0.5		0.5	Counts
8	P	8-Bit Integral Nonlinearity	INL	–1.5	±0.1	1.5	Counts
9	P	8-Bit Absolute Error(1)	AE	-2.0	±1.5	2.0	Counts

NOTES:
1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also **Figure A-1**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

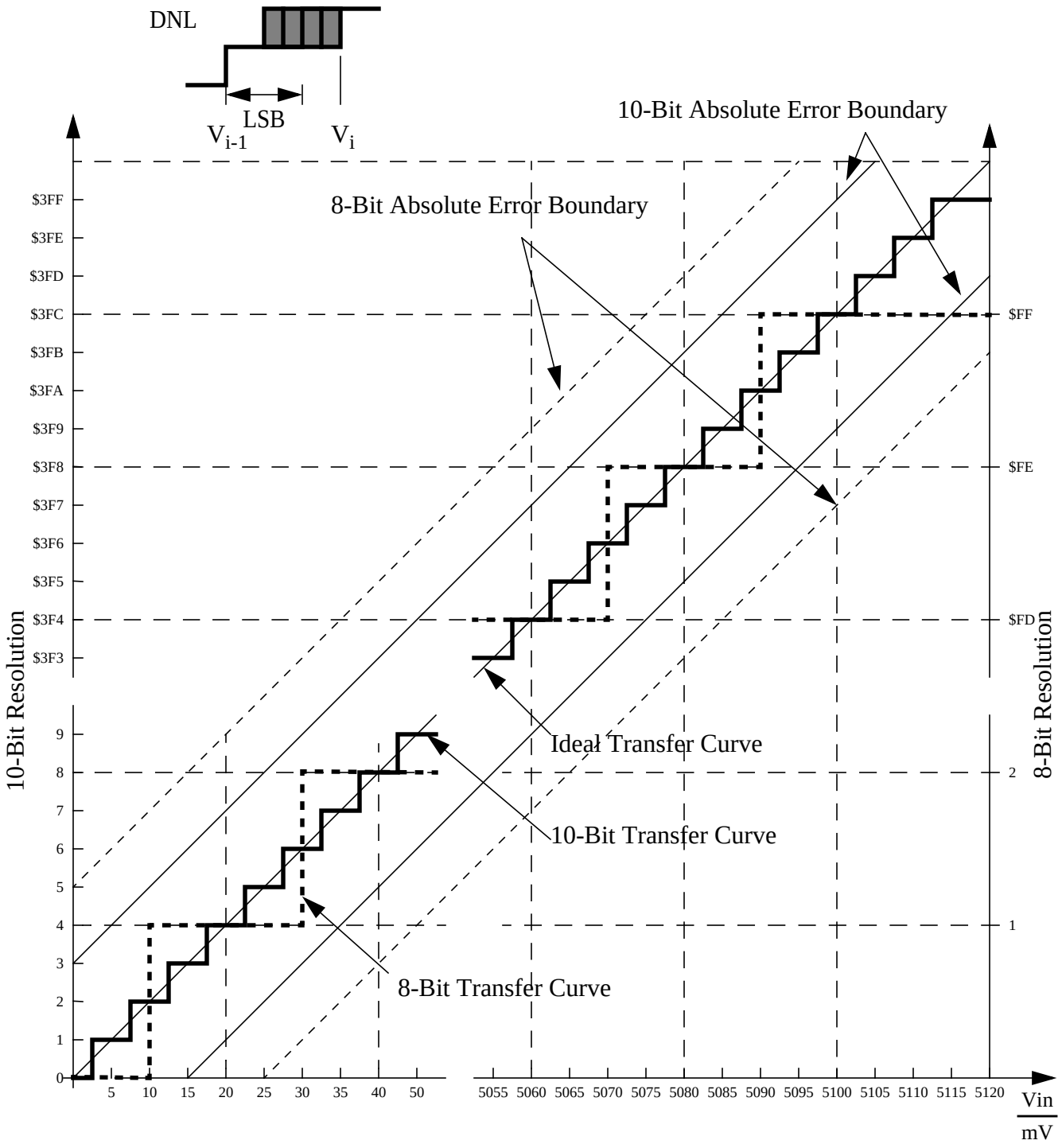


Figure A-1 ATD Accuracy Definitions

NOTE:Figure A-1 *shows only definitions, for specification values refer to* ***Table A-12*** *and* ***Table A-13*** .

A.3 NVM, Flash and EEPROM

NOTE: *Unless otherwise noted the abbreviation NVM (Non Volatile Memory) is used for both Flash and EEPROM.*

A.3.1 NVM timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash and EEPROM program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV and ECLKDIV registers respectively. The frequency of this clock must be set within the limits specified as f_{NVMOP}.

The minimum program and erase times shown in **Table A-14** are calculated for maximum f_{NVMOP} and maximum f_{bus}. The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

A.3.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{swpgm} = 9 \cdot \frac{1}{f_{NVMOP}} + 25 \cdot \frac{1}{f_{bus}}$$

A.3.1.2 Burst Programming

This applies only to the Flash where up to 32 words in a row can be programmed consecutively using burst programming by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{bwpgm} = 4 \cdot \frac{1}{f_{NVMOP}} + 9 \cdot \frac{1}{f_{bus}}$$

The time to program a whole row is:

$$t_{brpgm} = t_{swpgm} + 31 \cdot t_{bwpgm}$$

Burst programming is more than 2 times faster than single word programming.

A.3.1.3 Sector Erase

Erasing a 512 byte Flash sector or a 4 byte EEPROM sector takes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.5 Blank Check

The time it takes to perform a blank check on the Flash or EEPROM is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \approx location \cdot t_{cyc} + 10 \cdot t_{cyc}$$

Table A-14 NVM Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External Oscillator Clock	f_{NVMOSC}	0.5		50 [1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1			MHz
3	D	Operating Frequency	f_{NVMOP}	150		200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46 [2]		74.5 [3]	µs
5	D	Flash Burst Programming consecutive word [4]	t_{bwpgm}	20.4 (2)		31 (3)	µs
6	D	Flash Burst Programming Time for 32 Words (4)	t_{brpgm}	678.4 (2)		1035.5 (3)	µs
7	P	Sector Erase Time	t_{era}	20 [5]		26.7 (3)	ms
8	P	Mass Erase Time	t_{mass}	100 (5)		133 (3)	ms
9	D	Blank Check Time Flash per block	t_{check}	11 [6]		32778 [7]	t_{cyc}
10	D	Blank Check Time EEPROM per block	t_{check}	11 (6)		2058 (7)	t_{cyc}

NOTES:
1. Restrictions for oscillator in crystal mode apply!
2. Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.

3. Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus}. Refer to formulae in Sections **Section A.3.1.1 Single Word Programming- Section A.3.1.4 Mass Erase**for guidance.
4. urst Programming operations are not applicable to EEPROM
5. Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP}.
6. Minimum time, if first word in the array is not blank
7. Maximum time to complete check on an erased block

A.3.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The failure rates for data retention and program/erase cycling are specified at the operating conditions noted.

The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

NOTE: *All values shown in **Table A-15** are target values and subject to further extensive characterization.*

Table A-15 NVM Reliability Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	Data Retention at an average junction temperature of T_{Javg} = 70°C	t_{NVMRET}	15			Years
2	C	Flash number of Program/Erase cycles	n_{FLPE}	1000	10,000		Cycles
3	C	EEPROM number of Program/Erase cycles ($-40°C \leq T_J \leq 0°C$)	n_{EEPE}	10,000			Cycles
4	C	EEPROM number of Program/Erase cycles ($0°C < T_J \leq 140°C$)	n_{EEPE}	100,000			Cycles

A.4 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

A.4.1 Startup

Table A-16 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block User Guide.

Table A-16 Startup Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	T	POR release level	V_{PORR}			2.07	V
2	T	POR assert level	V_{PORA}	0.97			V
3	D	Reset input pulse width, minimum input time	PW_{RSTL}	2			t_{osc}
4	D	Startup from Reset	n_{RST}	192		196	n_{osc}
5	D	Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	20			ns
6	D	Wait recovery startup time	t_{WRS}			14	t_{cyc}

A.4.1.1 POR

The release level V_{PORR} and the assert level V_{PORA} are derived from the V_{DD} Supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

A.4.1.2 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when VDD5 is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

A.4.1.3 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

A.4.1.4 Stop Recovery

Out of STOP the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

A.4.1.5 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After t_{wrs} the CPU starts fetching the interrupt vector.

A.4.2 Oscillator

The device features an internal low-power loop controlled Pierce oscillator and a full swing Pierce oscillator/external clock mode. The selection of loop controlled Pierce oscillator or full swing Pierce oscillator/external clock depends on the $\overline{\text{XCLKS}}$ signal which is sampled during reset. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time t_{UPOSC}. The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Assert Frequency f_{CMFA}.

Table A-17 Oscillator Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1a	C	Crystal oscillator range (loop controlled Pierce)	f_{OSC}	4.0		16	MHz
1b	C	Crystal oscillator range (full swing Pierce) [1,2]	f_{OSC}	0.5		40	MHz
2	P	Startup Current	i_{OSC}	100			µA
3	C	Oscillator start-up time (loop controlled Pierce)	t_{UPOSC}		TBD[3]	50[4]	ms
4	D	Clock Quality check time-out	t_{CQOUT}	0.45		2.5	s
5	P	Clock Monitor Failure Assert Frequency	f_{CMFA}	50	100	200	KHz
6	P	External square wave input frequency	f_{EXT}	0.5		50	MHz
7	D	External square wave pulse width low	t_{EXTL}	9.5			ns
8	D	External square wave pulse width high	t_{EXTH}	9.5			ns
9	D	External square wave rise time	t_{EXTR}			1	ns
10	D	External square wave fall time	t_{EXTF}			1	ns
11	D	Input Capacitance (EXTAL, XTAL inputs)	C_{IN}		7		pF

NOTES:
1. Depending on the crystal a damping series resistor might be necessary
2. $\overline{\text{XCLKS}}$ =0 during reset
3. f_{osc} = 4MHz, C = 22pF.
4. Maximum value is for extreme cases using high Q, low frequency crystals

A.4.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL´s Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

A.4.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.

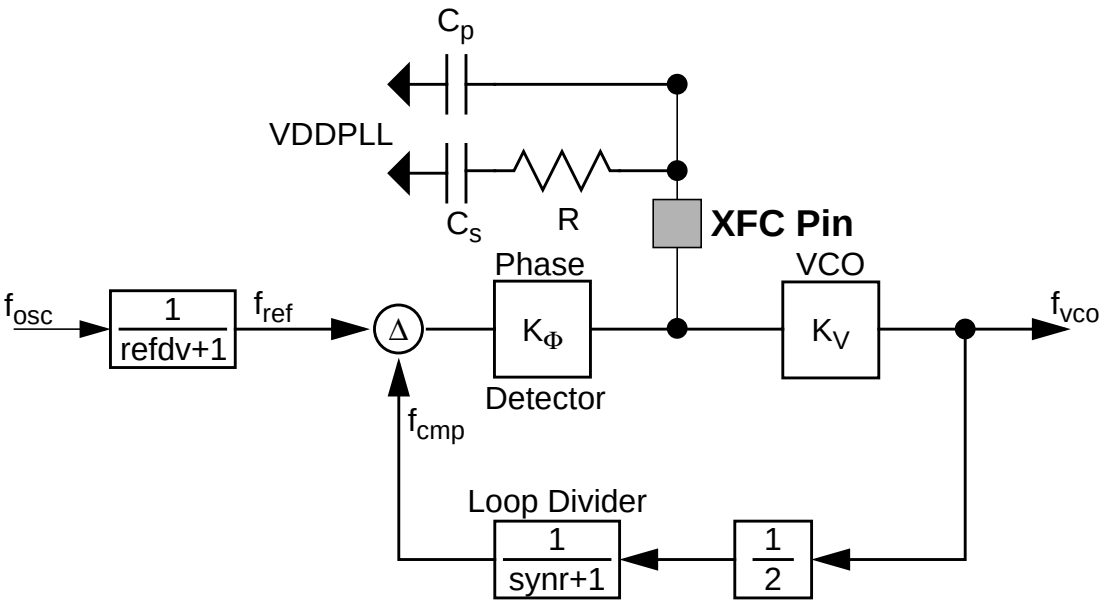


Figure A-2 Basic PLL functional diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from **Table A-18**.

The grey boxes show the calculation for f_{VCO} = 50MHz and f_{ref} = 1MHz. E.g., these frequencies are used for f_{OSC} = 4MHz and a 25MHz bus clock.

The VCO Gain at the desired VCO frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{vco})}{K_1 \cdot 1V}} = -100 \cdot e^{\frac{(60-50)}{-100}} = -90.48\text{MHz/V}$$

The phase detector relationship is given by:

$$K_\Phi = -|i_{ch}| \cdot K_V = 316.7\text{Hz}/\Omega$$

i_{ch} is the current in tracking mode.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot \left(\zeta + \sqrt{1 + \zeta^2}\right)} \cdot \frac{1}{10} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 10}; (\zeta = 0.9) \qquad f_C < 25kHz$$

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (synr + 1) \qquad = 50$$

With the above values the resistance can be calculated. The example is shown for a loop bandwidth f_C=10kHz:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi} \qquad = 2*\pi*50*10kHz/(316.7Hz/\Omega)=9.9k\Omega=\sim 10k\Omega$$

The capacitance C_s can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9) \qquad = 5.19nF =\sim 4.7nF$$

The capacitance C_p should be chosen in the range of:

$$C_s/20 \leq C_p \leq C_s/10 \qquad C_p = 470pF$$

A.4.3.2 Jitter Information

NOTE: *This section is under construction*

The basic functionality of the PLL is shown in **Figure A-2**. With each transition of the clock f_{cmp}, the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly.The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure A-3**.

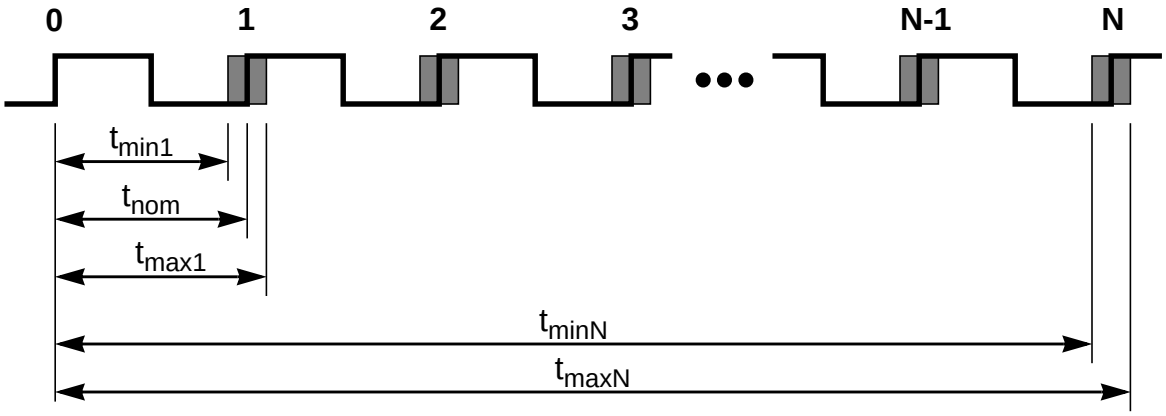


Figure A-3 Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

NOTE: *From the evaluation data a formula for t_{max}= f(N), resp. t_{min} = f(N) should be derived.*

Assuming no long term drift of the reference clock, the following will hold

$$\lim_{N \to \infty} J(N) = 0$$

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table A-18 PLL Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Self Clock Mode frequency	f_{SCM}	1		5.5	MHz
2	D	VCO locking range	f_{VCO}	8		50	MHz
3	D	Lock Detector transition from Acquisition to Tracking mode	Δ_{trk}	3%		4%[1]	—
4	D	Lock Detection	Δ_{Lock}	0%		1.5%(1)	—
5	D	Un-Lock Detection	Δ_{unl}	0.5%		2.5%(1)	—
6	D	Lock Detector transition from Tracking to Acquisition mode	Δ_{unt}	6%		8%(1)	—
7	C	PLLON Total Stabilization delay[2]	t_{stab}		0.5		ms
8	D	PLLON Acquisition mode stabilization delay(2)	t_{acq}		0.3		ms
9	D	PLLON Tracking mode stabilization delay(2)	t_{al}		0.2		ms
10	D	Fitting parameter VCO loop gain	K_1		-100		MHz/V
11	D	Fitting parameter VCO loop frequency	f_1		60		MHz
12	D	Charge pump current acquisition mode	i_{ch}		-38.5		µA
13	D	Charge pump current tracking mode	i_{ch}		-3.5		µA
14	C	Jitter fit parameter 1(2)	j_1			1.1	%
15	C	Jitter fit parameter 2(2)	j_2			0.13	%

NOTES:
1. % deviation from target frequency
2. f_{REF} = 4MHz, f_{BUS} = 25MHz equivalent f_{VCO} = 50MHz: REFDV = #$03, SYNR = #$018, Cs = 4.7nF, Cp = 470pF, Rs = 10KΩ.

A.5 MSCAN

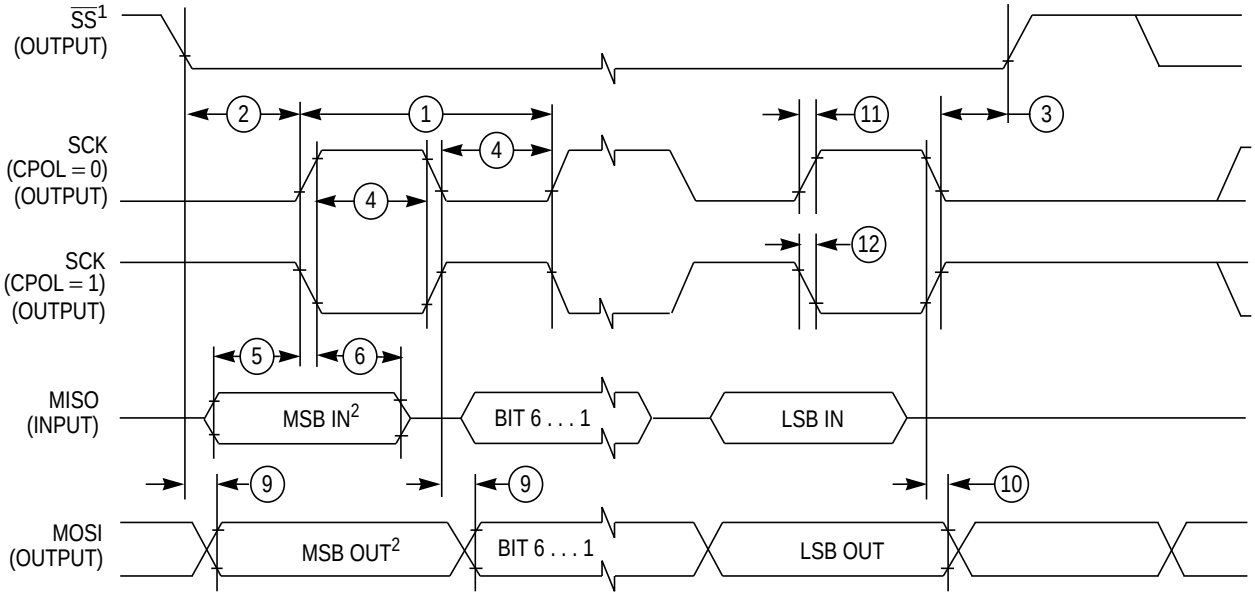
Table A-19 MSCAN Wake-up Pulse Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	MSCAN Wake-up dominant pulse filtered	t_{WUP}			2	µs
2	P	MSCAN Wake-up dominant pulse pass	t_{WUP}	5			µs

A.6 SPI

A.6.1 Master Mode

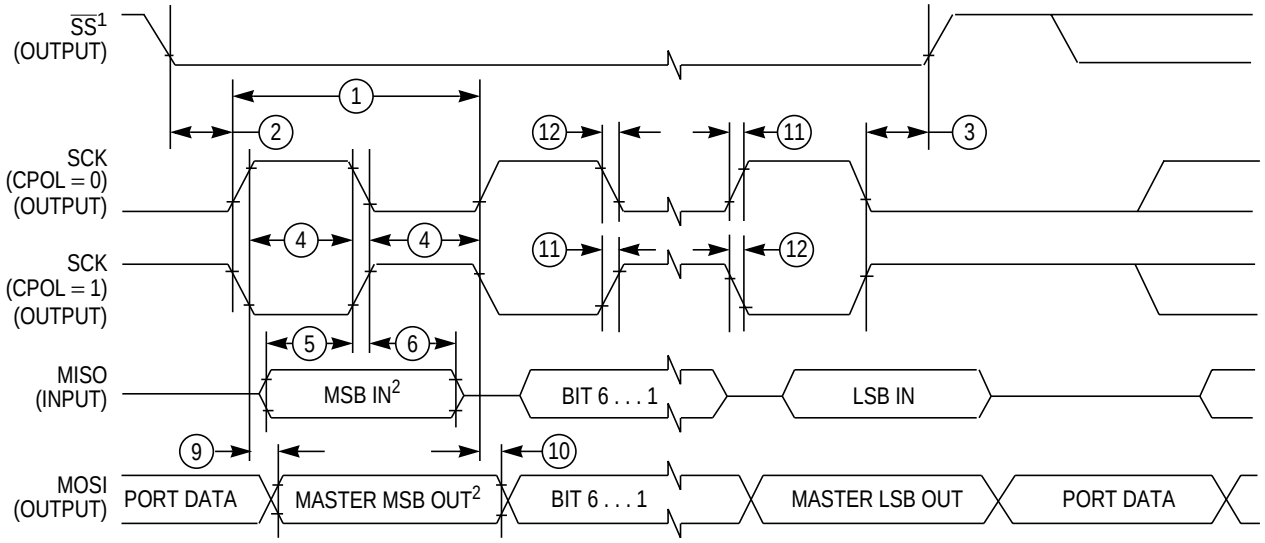
Figure A-4 and **Figure A-5** illustrate the master mode timing. Timing values are shown in **Table A-20**.



1.if configured as an output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-4 SPI Master Timing (CPHA = 0)



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

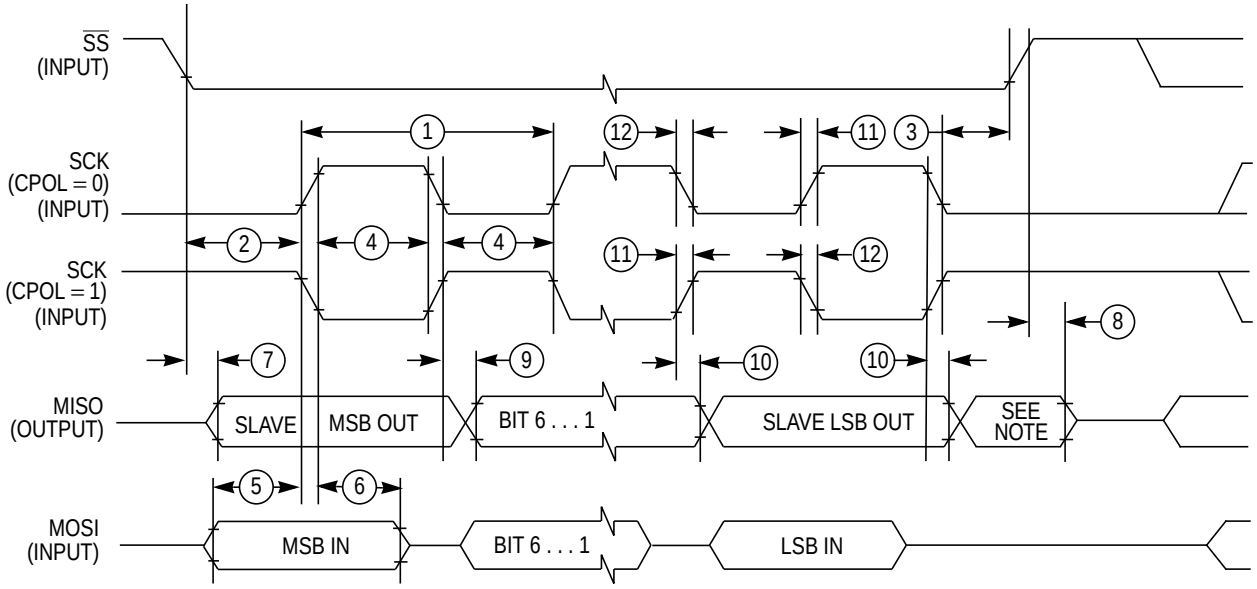
Figure A-5 SPI Master Timing (CPHA =1)

Table A-20 SPI Master Mode Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted, CLOAD = 200pF on all outputs							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Operating Frequency	f_{op}	DC		1/4	f_{bus}
1	P	SCK Period	t_{sck}	4		2048	t_{bus}
2	D	Enable Lead Time	t_{lead}	1/2		—	t_{sck}
3	D	Enable Lag Time	t_{lag}	1/2			t_{sck}
4	D	Clock (SCK) High or Low Time	t_{wsck}	t_{bus} – 30		1024 t_{bus}	ns
5	D	Data Setup Time (Inputs)	t_{su}	25			ns
6	D	Data Hold Time (Inputs)	t_{hi}	0			ns
9	D	Data Valid (after SCK Edge)	t_{v}			25	ns
10	D	Data Hold Time (Outputs)	t_{ho}	0			ns
11	D	Rise Time Inputs and Outputs	t_{r}			25	ns
12	D	Fall Time Inputs and Outputs	t_{f}			25	ns

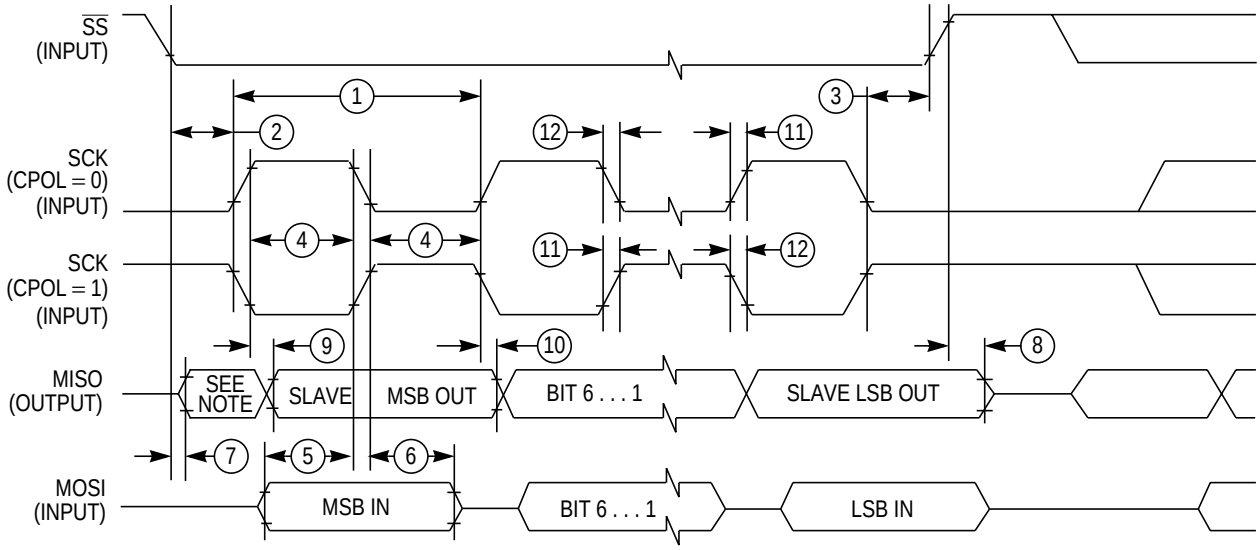
A.6.2 Slave Mode

Figure A-6 and **Figure A-7** illustrate the slave mode timing. Timing values are shown in **Table A-21**.



NOTE: Not defined but normally MSB of character just received.

Figure A-6 SPI Slave Timing (CPHA = 0)



NOTE: Not defined but normally LSB of character just received.

Figure A-7 SPI Slave Timing (CPHA =1)

Table A-21 SPI Slave Mode Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted, CLOAD = 200pF on all outputs							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Operating Frequency	f_{op}	DC		1/4	f_{bus}
1	P	SCK Period	t_{sck}	4		2048	t_{bus}
2	D	Enable Lead Time	t_{lead}	1			t_{cyc}
3	D	Enable Lag Time	t_{lag}	1			t_{cyc}
4	D	Clock (SCK) High or Low Time	t_{wsck}	t_{cyc} – 30			ns
5	D	Data Setup Time (Inputs)	t_{su}	25			ns
6	D	Data Hold Time (Inputs)	t_{hi}	25			ns
7	D	Slave Access Time	t_a			1	t_{cyc}
8	D	Slave MISO Disable Time	t_{dis}			1	t_{cyc}
9	D	Data Valid (after SCK Edge)	t_v			25	ns
10	D	Data Hold Time (Outputs)	t_{ho}	0			ns
11	D	Rise Time Inputs and Outputs	t_r			25	ns
12	D	Fall Time Inputs and Outputs	t_f			25	ns

A.7 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure A-8** with the actual timing values shown on table **Table A-22**. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

A.7.1 General Muxed Bus Timing

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.

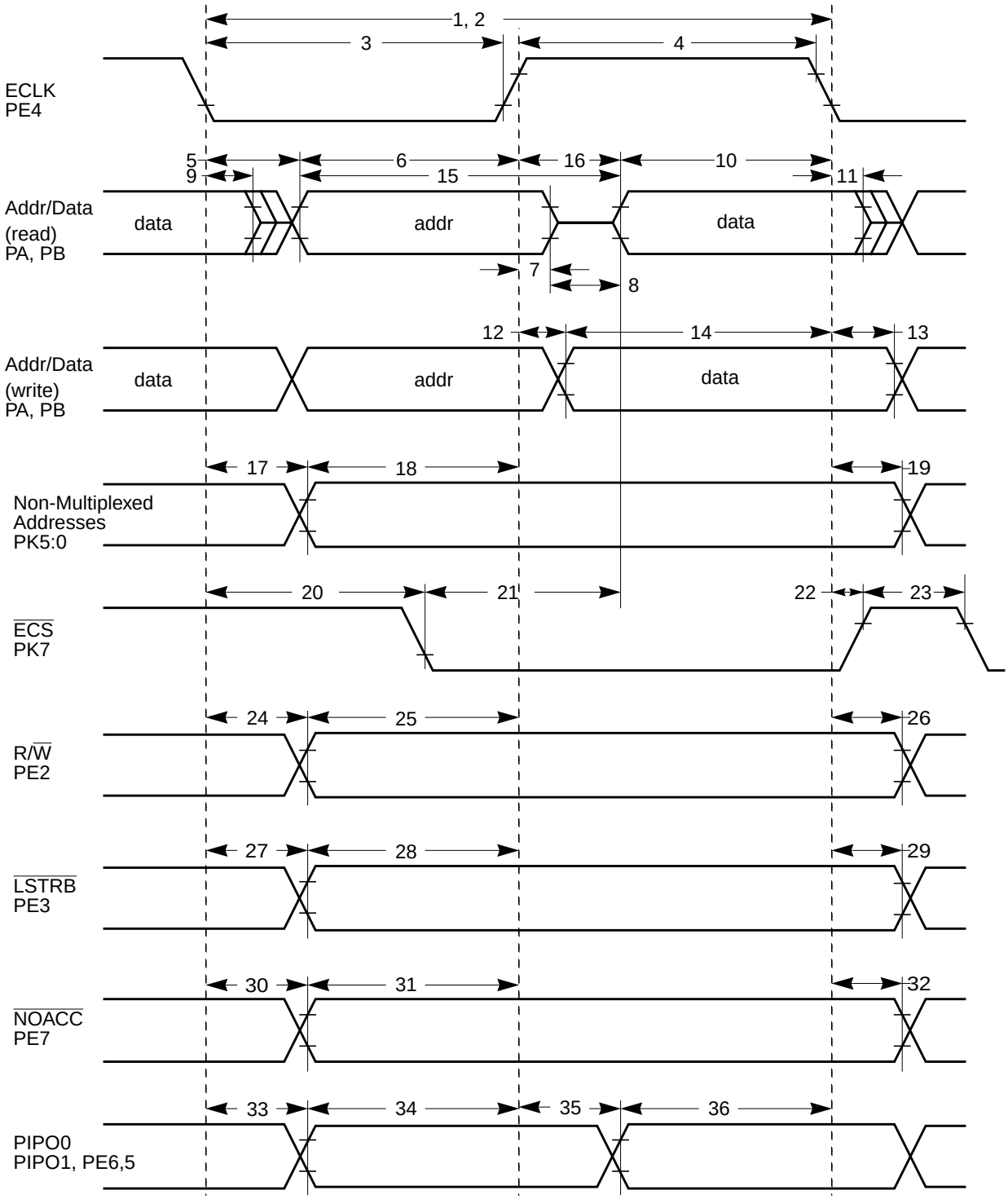


Figure A-8 General External Bus Timing

Table A-22 Expanded Bus Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 50pF							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Frequency of operation (E-clock)	f_o	0		25.0	MHz
2	P	Cycle time	t_{cyc}	40			ns
3	D	Pulse width, E low	PW_{EL}	19			ns
4	D	Pulse width, E high[1]	PW_{EH}	19			ns
5	D	Address delay time	t_{AD}			8	ns
6	D	Address valid time to E rise (PW_{EL}–t_{AD})	t_{AV}	11			ns
7	D	Muxed address hold time	t_{MAH}	2			ns
8	D	Address hold to data valid	t_{AHDS}	7			ns
9	D	Data hold to address	t_{DHA}	2			ns
10	D	Read data setup time	t_{DSR}	13			ns
11	D	Read data hold time	t_{DHR}	0			ns
12	D	Write data delay time	t_{DDW}			7	ns
13	D	Write data hold time	t_{DHW}	2			ns
14	D	Write data setup time(1) (PW_{EH}–t_{DDW})	t_{DSW}	12			ns
15	D	Address access time(1) (t_{cyc}–t_{AD}–t_{DSR})	t_{ACCA}	19			ns
16	D	E high access time(1) (PW_{EH}–t_{DSR})	t_{ACCE}	6			ns
17	D	Non-multiplexed address delay time	t_{NAD}			6	ns
18	D	Non-muxed address valid to E rise (PW_{EL}–t_{NAD})	t_{NAV}	13			ns
19	D	Non-multiplexed address hold time	t_{NAH}	2			ns
20	D	Chip select delay time	t_{CSD}			16	ns
21	D	Chip select access time(1) (t_{cyc}–t_{CSD}–t_{DSR})	t_{ACCS}	11			ns
22	D	Chip select hold time	t_{CSH}	2			ns
23	D	Chip select negated time	t_{CSN}	8			ns
24	D	Read/write delay time	t_{RWD}			7	ns
25	D	Read/write valid time to E rise (PW_{EL}–t_{RWD})	t_{RWV}	14			ns
26	D	Read/write hold time	t_{RWH}	2			ns
27	D	Low strobe delay time	t_{LSD}			7	ns
28	D	Low strobe valid time to E rise (PW_{EL}–t_{LSD})	t_{LSV}	14			ns
29	D	Low strobe hold time	t_{LSH}	2			ns
30	D	NOACC strobe delay time	t_{NOD}			7	ns
31	D	NOACC valid time to E rise (PW_{EL}–t_{LSD})	t_{NOV}	14			ns

Table A-22 Expanded Bus Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 50pF							
32	D	NOACC hold time	t_{NOH}	2			ns
33	D	PIPO0 delay time	t_{P0D}	2		7	ns
34	D	PIPO0 valid time to E rise (PW_{EL}–t_{P0D})	t_{P0V}	11			ns
35	D	PIPO1 delay time(1) (PW_{EH}-t_{P1V})	t_{P1D}	2		7	ns
36	D	PIPO1 valid time to E fall	t_{P1V}	11			ns

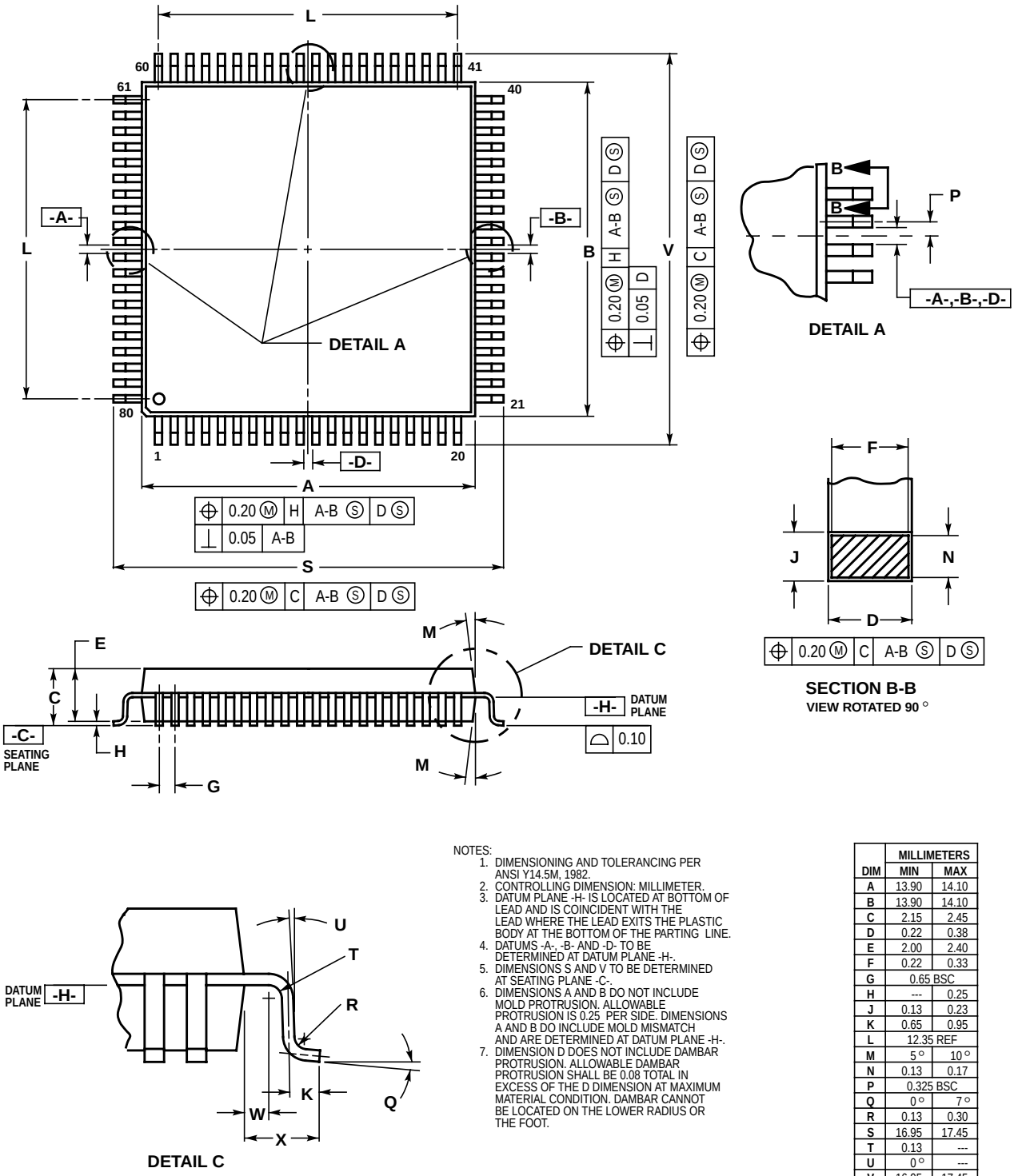
NOTES:
1. Affected by clock stretch: add N x t_{cyc} where N=0,1,2 or 3, depending on the number of clock stretches.

Appendix B Package Information

B.1 General

This section provides the physical dimensions of the MC9S12KG128 packages.

B.2 80-pin QFP package

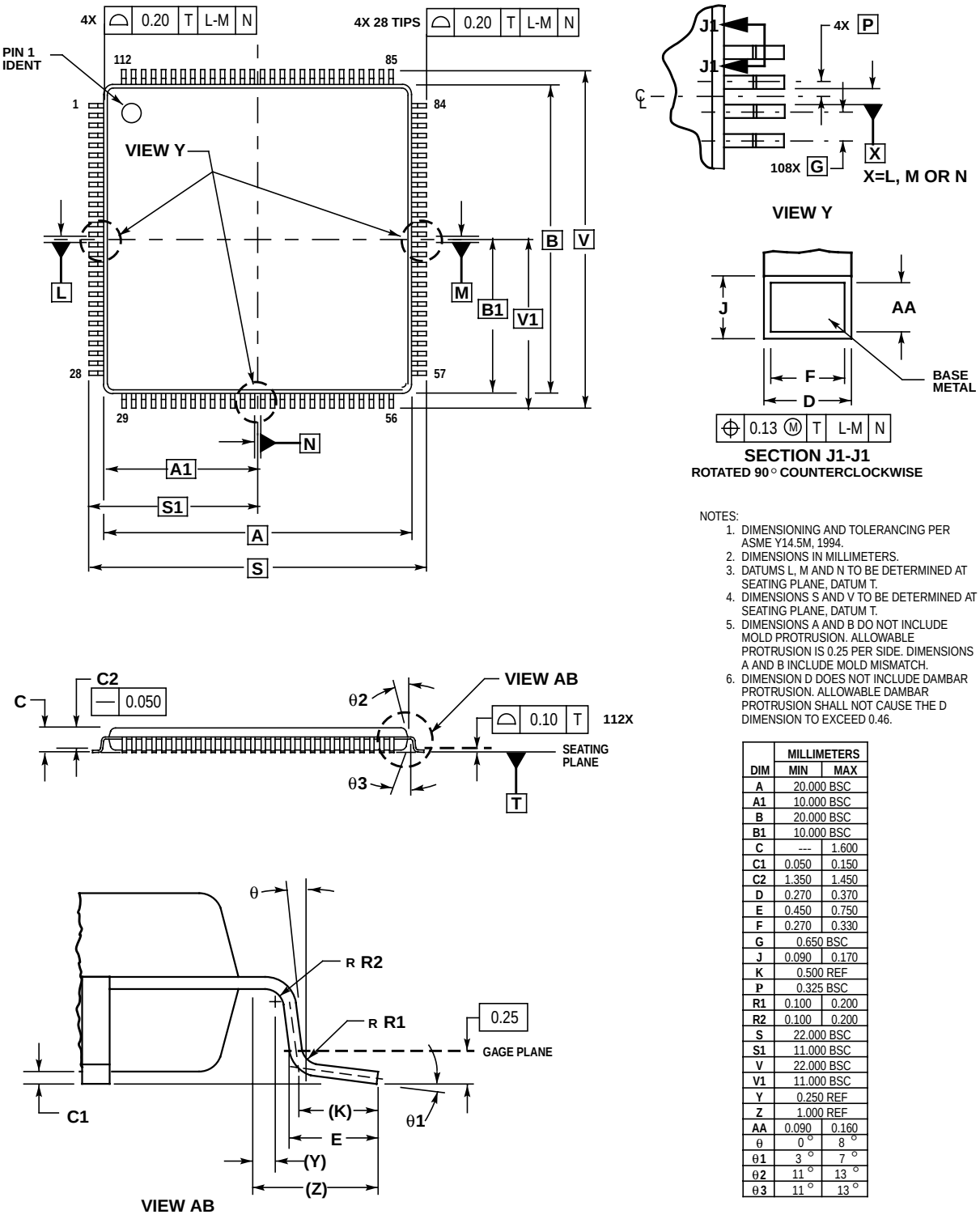


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure B-1 80-pin QFP Mechanical Dimensions (case no. 841B)

B.3 112-pin LQFP package



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.46.

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Figure B-2 112-pin LQFP Mechanical Dimensions (case no. 987)

SoC Guide End Sheet

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