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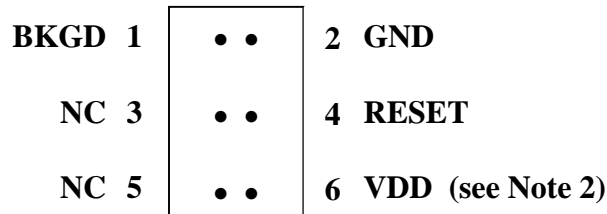
## BDM Multilink Rev B Technical Summary

Document # PE3306, Version 1.2

1. Introduction
2. Usage of BDM MULTILINK Cable
3. Startup Sequence
4. Configuration Notes

### 1.0 Introduction

P&E's BDM MULTILINK Interface Cable provides access to the Background Debug Mode (BDM) on Motorola HCS08, HC12 and HCS12 micro-controllers. It is the hardware interface between a standard IBM PC parallel port (DB25 Female Connector, see Note 1,4) and a standard 6 pin "Berg" connector. By using the BDM MULTILINK, the user can take advantage of the background debug mode to halt normal processor execution and use a PC to control the processor. The user can then directly control the target's execution, read/write registers and memory values and program internal or external FLASH memory devices. The pin outs of the connector are specified by Motorola as:



### 2.0 Usage of BDM MULTILINK Cable

BDM MULTILINK can communicate with a target whose bus frequency is between 1.6 KHz and 35 MHz.

For HCS08 devices, the P&E interface automatically adjusts to the speed of the target.

For HC12 and HCS12 processors, the P&E interface can be configured to automatically calculate the proper communications speed on reset and will use this for the entire debug session. Alternately, the user may specify the communications rate by setting the value of the IO\_DELAY\_CNT variable. The proper value is calculated by the equation:

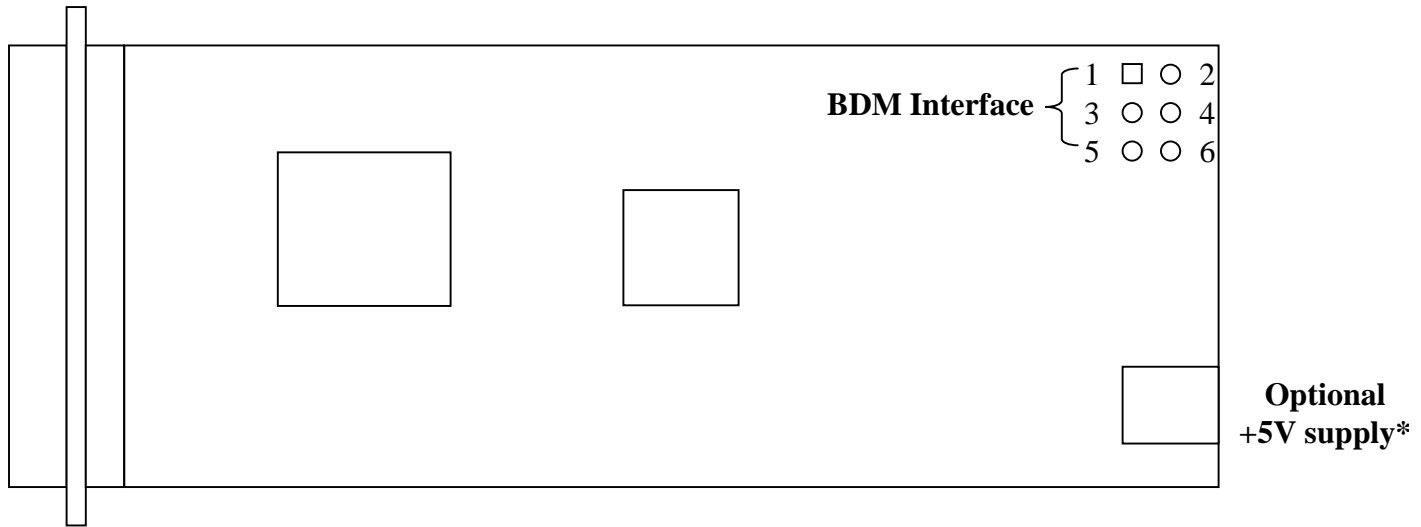
$$IO\_DELAY\_CNT = (10000000 / F_{bus}) - 1$$

Where  $F_{bus}$  is the bus frequency in hertz.

The MULTILINK cable derives its power from the target, and does not require a separate power supply. The target power supply can range from 1.8V to 5.5V. Estimates of the typical current consumption of the BDM Multilink Rev B are:

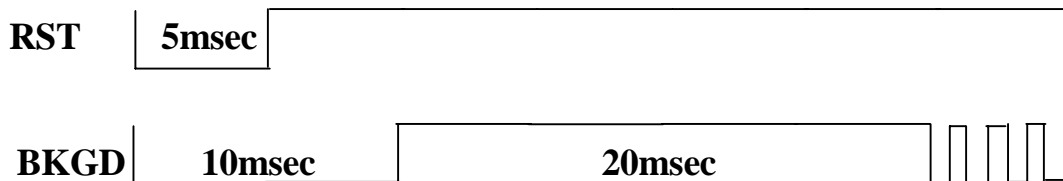
- 5V Target = 95mA
- 3V Target = 140mA
- 2V Target = 200mA

If the user does not want the cable deriving power from the target, the user can connect a 5v center negative power supply to the optional power jack (1.3mm/3.5mm). The power jack has a mechanical switch which will disconnect pin 6 (Vdd) from the internal cable power generation circuitry (although it is still used as a reference) when an external power supply plug is connected.



### 3.0 Startup Sequence

In order to use the Background Debug Mode of the microcontroller, it must be initialized coming out of reset. This is accomplished by P&E's software (In Circuit Debugger or Flash programmer) on the host PC by generating the following reset sequence.



- a) Initially the BKGD (pin-1) and Reset (pin-4) are pulled low.
- b) After 5 milliseconds, the RESET (pin-4) goes high.
- c) After 10 milliseconds, the BKGD (pin-1) goes high.
- d) Wait for 20milli second followed by activities on BKGD (pin-1).

## 4.0 Configuration Notes

**Note 1: The BIOS settings for the Parallel port should be one of the following:**

**SPP, Normal, Standard, Output Only, Unidirectional, AT.**

**Try to avoid ECP, EPP or PS/2 Bi-directional.**

**Note 2: The cable obtains power from the target through the BDM header, or optionally through an external 5v center negative power supply.**

**Note 3: The parallel cable connecting the PC parallel port and the BDM cable MUST be IEEE1284 compliant. If the cable is not marked with the IEEE1284 text, then it is not compliant.**

**Note 4: In windows XP/2000, the parallel port dialog checkbox entitled "Enable Legacy Plug and Play" should be checked. This setting is located in the Control Panel-->System-->Hardware->Device Manager->Ports->Printer Port (LPTX) dialog. You must reboot for this setting to take effect.**

**Note 5: Make sure to turn off any applications which may be trying to access the printer port (such as a Print Manager) before running P&E's software.**

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