BGS8U5

SiGe:C low-noise amplifier with bypass switch for LTE/5G NR

Rev. 5 — 1 December 2021 Product data sheet

1 General description

The BGS8U5, also known as the LTE3301U, is a Low-Noise Amplifier (LNA) with bypass switch for LTE, and 5G NR receiver applications. It is available in a small plastic 6-pin thin leadless package.

The BGS8U5 delivers system-optimized gain for LTE bands 42 and 43 where sensitivity improvement is required. Complete 5G NR bands n77, n78, and n79 are supported. When receive signal strength is sufficient, the BGS8U5 can be switched off to operate in bypass mode. Switching to bypass mode results into an increased $IP3_i$ level and supply current in bypass mode at 1 µA. The BGS8U5 requires only one external matching inductor up to 4200 MHz.

The BGS8U5 is optimized for 3300 MHz to 4200 MHz, and with one additional output matching inductor optimized for 4400-5000 MHz.

2 Features and benefits

- Operating frequency from 3300 MHz to 5000 MHz
- Noise figure 1.0 dB
- Gain 15 dB
- High input 1 dB compression point -8 dBm
- High in band $IP3_i$ 4 dBm
- Bypass switch insertion loss -3.2 dB
- Supply voltage 1.5 V to 3.1 V
- Integrated RF supply decoupling capacitor
- Optimized performance at a supply current 4.7 mA
- Bypass mode current consumption < 1 µA
- Integrated temperature stabilized bias for easy design
- Requires only one input matching inductor
- Input and output AC coupled through DC blocking capacitors
- Integrated matching for the output (LTE B42/43, 5G NR n77/n78)
- ESD protection on all pins
- Low Bill of Materials (BOM)
- 6-pins leadless package; 1.1 mm x 0.7 mm x 0.37 mm; 0.4 mm pitch
- 180 GHz transit frequency - SiGe:C technology
- Moisture sensitivity level 1

3 Applications

- LNA for LTE and 5G NR reception in smart phones
- feature phones
- tablet PCs
- RF front-end modules

4 Quick reference data

Table 1. Quick reference data

f = 3800 MHz; V_{CC} = 2.8 V; T_{amb} = 25 °C. Input matched to 50 Ω using application diagram from Figure 3 and component values as in Table 12. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	in gain mode	-	4.7	6.0	mA
		in bypass mode	-	-	1.0	µA
G_p	power gain	in gain mode	13.0	15.0	17.0	dB
		in bypass mode	-4.0	-3.2	-2.4	dB
NF	noise figure	[1] [2]	-	1.0	1.3	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	in gain mode [1]	-9.5	-8.0	-	dBm
$IP3_i$	input third-order intercept point	in gain mode; Δf = 1 MHz/10 MHz [1]	1.0	4.0	-	dBm

[1] Guaranteed by design; not tested in production
[2] PCB losses are subtracted.

5 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BGS8U5	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1.1 mm x 0.7 mm x 0.37 mm	SOT1232

6 Marking

Table 3. Marking code

Type number	Marking code
BGS8U5	T

7 Block diagram

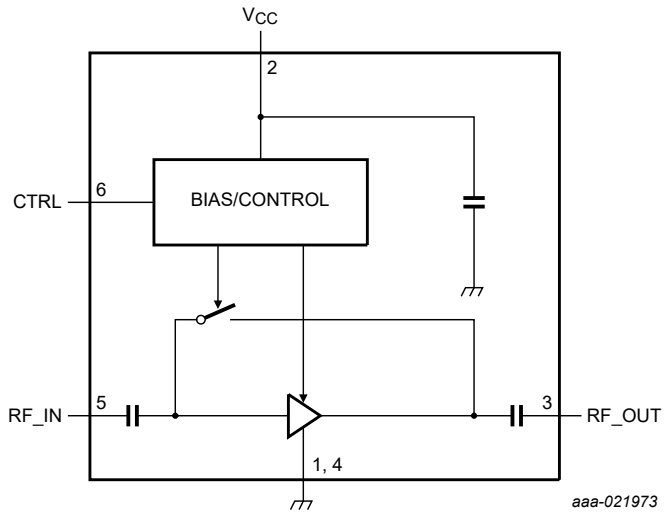


Figure 1. Block diagram

8 Pinning information

8.1 Pinning

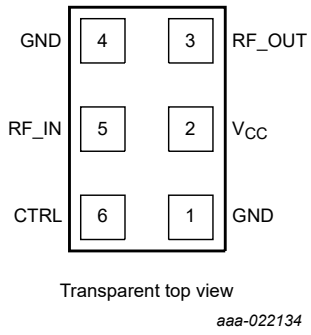


Figure 2. Pin configuration

8.2 Pin description

Table 4. Pinning

Symbol	Pin	Description
GND	1	RF ground
V_{CC}	2	supply voltage
RF_OUT	3	RF out
GND	4	RF ground
RF_IN	5	RF in
CTRL	6	gain control, switch between gain and bypass mode

9 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). See Section 18.3 "Disclaimers", paragraph 'Limiting values'.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+5.0	V
$V_{I(CTRL)}$	input voltage on pin CTRL	$V_{I(CTRL)} < V_{CC} + 0.6$ V	-0.5	+5.0	V
$V_{I(RF\_IN)}$	input voltage on pin RF_IN	DC; $V_{I(RF\_IN)} < V_{CC} + 0.6$ V [1]	-0.5	+5.0	V
$V_{I(RF\_OUT)}$	input voltage on pin RF_OUT	DC; $V_{I(RF\_OUT)} < V_{CC} + 0.6$ V [1]	-0.5	+5.0	V
$P_{i(RF)CW}$	continuous waveform RF input power	RF	-	26.0	dBm
		RF [2]	-	20.0	dBm
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	+150	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) according to ANSI/ESDA/JEDEC standard JS-001 [3]	-	±2	kV
		Charged Device Model (CDM) according to ANSI/ESDA/JEDEC standard JS-002	-	±1	kV

[1] The RF input and output are AC coupled through internal DC blocking capacitors.
[2] f = 3600 MHz, 200 hrs at T_{amb} = 100 °C
[3] HBM ESD protection level is according to JS-001 classification 2 (2000 V to < 4000 V)

10 Recommended operating conditions

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.5	-	3.1	V
T_{amb}	ambient temperature		-40	+25	+85	°C
$V_{I(CTRL)}$	input voltage on pin CTRL	bypass mode [1]	0.0	-	0.25	V
		gain mode [1]	0.8	-	V_{CC}	V

[1] $V_{I(CTRL)}$ shall be applied only after V_{cc} is applied to the device

11 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		225	K/W

12 Characteristics

Table 8. Characteristics

3400 MHz ≤ f ≤ 4200 MHz; V_{CC} = 1.8 V; T_{amb} = 25 °C; input matched 50 Ω using application diagram from Figure 3 and component values as in Table 12. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain mode						
I_{CC}	supply current	$V_{I(CTRL)}$ > 0.8 V	-	4.5	6.0	mA
G_p	power gain	f = 3400 MHz	14.0	16.0	18.0	dB
		f = 3800 MHz	12.5	14.5	16.5	dB
		f = 4200 MHz	11.0	13.0	15.0	dB
ΔG/ΔT	gain variation with temperature	[1]	-	-0.01	-	dB/°C
NF	noise figure	f = 3400 MHz [1] [2]	-	1.0	1.3	dB
		f = 3800 MHz [1] [2]	-	1.0	1.3	dB
		f = 4200 MHz [1] [2]	-	1.0	1.3	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 3400 MHz [1]	-13.0	-11.5	-	dBm
		f = 3800 MHz [1]	-11.5	-10.0	-	dBm
		f = 4200 MHz [1]	-10.5	-9.0	-	dBm
$P_{o(1dB)}$	output power at 1 dB gain compression	f = 3400 MHz [1]	-	3.5	-	dBm
		f = 3800 MHz [1]	-	3.5	-	dBm
		f = 4200 MHz [1]	-	3.5	-	dBm
$IP3_i$	input third-order intercept point	f = 3400 MHz; Δf = 1 MHz/10 MHz [1]	-2.0	1.0	-	dBm
		f = 3800 MHz; Δf = 1 MHz/10 MHz [1]	-1.0	2.0	-	dBm
		f = 4200 MHz; Δf = 1 MHz/10 MHz [1]	-1.0	2.0	-	dBm
RL_{in}	input return loss	f = 3400 MHz	9.0	12.0	-	dB
		f = 3800 MHz	9.0	12.0	-	dB
		f = 4200 MHz	-	22.0	-	dB
RL_{out}	output return loss	f = 3400 MHz	9.0	12.0	-	dB
		f = 3800 MHz	9.0	12.0	-	dB
		f = 4200 MHz	-	9.0	-	dB
ISL	isolation	f = 3400 MHz	20.0	22.0	24.0	dB
		f = 3800 MHz	20.0	22.0	24.0	dB
		f = 4200 MHz	20.0	22.0	24.0	dB
K	Rollett stability factor	f = 10 MHz - 10 GHz [1]	1	-	-	-
t_{on}	turn-on time	time from $V_{I(CTRL)}$ ON to 90 % of the gain [1]	-	0.5	1.0	µs
t_{off}	turn-off time	time from $V_{I(CTRL)}$ OFF to 10 % of the gain [1]	-	0.35	1.0	µs

Table 8. Characteristics...*continued*

3400 MHz ≤ f ≤ 4200 MHz; V_{CC} = 1.8 V; T_{amb} = 25 °C; input matched 50 Ω using application diagram from Figure 3 and component values as in Table 12. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bypass mode						
I_{CC}	supply current	$V_{I(CTRL)}$ < 0.25 V	-	-	1.0	µA
G_p	power gain	f = 3400 MHz	-4.2	-3.4	-2.6	dB
		f = 3800 MHz	-4.2	-3.4	-2.6	dB
		f = 4200 MHz	-5.0	-4.2	-3.4	dB
ISL	isolation	f = 3400 MHz	2.6	3.4	4.2	dB
		f = 3800 MHz	2.6	3.4	4.2	dB
		f = 4200 MHz	3.4	4.2	5.0	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 3400 MHz [1]	5.5	7.0	-	dBm
		f = 3800 MHz [1]	6.0	7.5	-	dBm
		f = 4200 MHz [1]	5.5	7.0	-	dBm
$IP3_i$	input third-order intercept point	f = 3400 MHz [1]	20.5	23.5	-	dBm
		f = 3800 MHz [1]	19.0	22.0	-	dBm
		f = 4200 MHz [1]	18.0	21.0	-	dBm
RL_{in}	input return loss	f = 3400 MHz	6.5	8.0	-	dB
		f = 3800 MHz	7.5	9.0	-	dB
		f = 4200 MHz	7.5	9.0	-	dB
RL_{out}	output return loss	f = 3400 MHz	5.5	7.0	-	dB
		f = 3800 MHz	6.5	8.0	-	dB
		f = 4200 MHz	6.5	8.0	-	dB
$\Delta\varphi_{S21}$	gain phase step variation	between gain mode and bypass mode				
		f = 3400 MHz [1]	-5.0	-	+5.0	deg
		f = 3800 MHz [1]	-5.0	-	+5.0	deg
		f = 4200 MHz [1]	-5.0	-	+5.0	deg

[1] Guaranteed by design; not tested in production
[2] PCB losses are subtracted.

Table 9. Characteristics

3400 MHz ≤ f ≤ 4200 MHz; V_{CC} = 2.8 V; T_{amb} = 25 °C; input matched 50 Ω using application diagram from Figure 3 and component values as in Table 12. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain mode						
I_{CC}	supply current	$V_{I(CTRL)}$ > 0.8 V	-	4.7	6.0	mA
G_p	power gain	f = 3400 MHz	14.5	16.5	18.5	dB
		f = 3800 MHz	13.0	15.0	17.0	dB
		f = 4200 MHz	11.5	13.5	15.5	dB
ΔG/ΔT	gain variation with temperature	[1]	-	-0.01	-	dB/°C
NF	noise figure	f = 3400 MHz [1] [2]	-	1.0	1.3	dB
		f = 3800 MHz [1] [2]	-	1.0	1.3	dB
		f = 4200 MHz [1] [2]	-	1.0	1.3	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 3400 MHz [1]	-11.0	-9.5	-	dBm
		f = 3800 MHz [1]	-9.5	-8.0	-	dBm
		f = 4200 MHz [1]	-7.5	-6.0	-	dBm
$P_{o(1dB)}$	output power at 1 dB gain compression	f = 3400 MHz [1]	-	6.0	-	dBm
		f = 3800 MHz [1]	-	6.0	-	dBm
		f = 4200 MHz [1]	-	6.0	-	dBm
$IP3_i$	input third-order intercept point	f = 3400 MHz; Δf = 1 MHz/10 MHz [1]	-1.0	2.0	-	dBm
		f = 3800 MHz; Δf = 1 MHz/10 MHz [1]	1.0	4.0	-	dBm
		f = 4200 MHz; Δf = 1 MHz/10 MHz [1]	1.0	4.0	-	dBm
RL_{in}	input return loss	f = 3400 MHz	9.0	12.0	-	dB
		f = 3800 MHz	9.0	12.0	-	dB
		f = 4200 MHz	-	22.0	-	dB
RL_{out}	output return loss	f = 3400 MHz	9.0	12.0	-	dB
		f = 3800 MHz	9.0	12.0	-	dB
		f = 4200 MHz	-	9.0	-	dB
ISL	isolation	f = 3400 MHz	20.0	22.0	24.0	dB
		f = 3800 MHz	20.0	22.0	24.0	dB
		f = 4200 MHz	20.0	22.0	24.0	dB
K	Rollett stability factor	f = 10 MHz - 10 GHz [1]	1	-	-	-
t_{on}	turn-on time	time from $V_{I(CTRL)}$ ON, to 90 % of the gain [1]	-	0.4	1.0	µs
t_{off}	turn-off time	time from $V_{I(CTRL)}$ OFF, to 10 % of the gain [1]	-	0.25	1.0	µs

Table 9. Characteristics *...continued*

3400 MHz ≤ f ≤ 4200 MHz; V_{CC} = 2.8 V; T_{amb} = 25 °C; input matched 50 Ω using application diagram from Figure 3 and component values as in Table 12. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bypass mode						
I_{CC}	supply current	$V_{I(CTRL)}$ < 0.25 V	-	-	1.0	µA
G_p	power gain	f = 3400 MHz	-4.0	-3.2	-2.4	dB
		f = 3800 MHz	-4.0	-3.2	-2.4	dB
		f = 4200 MHz	-4.8	-4.0	-3.2.	dB
ISL	isolation	f = 3400 MHz	2.4	3.2	4.0	dB
		f = 3800 MHz	2.4	3.2	4.0	dB
		f = 4200 MHz	3.2	4.0	4.8	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 3400 MHz [1]	5.5	7.0	-	dBm
		f = 3800 MHz [1]	6.0	7.5	-	dBm
		f = 4200 MHz [1]	5.5	7.0	-	dBm
$IP3_i$	input third-order intercept point	f = 3400 MHz [1]	20.5	23.5	-	dBm
		f = 3800 MHz [1]	19.0	22.0	-	dBm
		f = 4200 MHz [1]	18.0	21.0	-	dBm
RL_{in}	input return loss	f = 3400 MHz	6.5	8.0	-	dB
		f = 3800 MHz	7.5	9.0	-	dB
		f = 4200 MHz	7.5	9.0	-	dB
RL_{out}	output return loss	f = 3400 MHz	5.5	7.0	-	dB
		f = 3800 MHz	6.5	8.0	-	dB
		f = 4200 MHz	6.5	8.0	-	dB
$\Delta\varphi_{S21}$	gain phase step variation	between gain mode and bypass mode				
		f = 3400 MHz [1]	-5.0	-	+5.0	deg
		f = 3800 MHz [1]	-5.0	-	+5.0	deg
		f = 4200 MHz [1]	-5.0	-	+5.0	deg

[1] Guaranteed by design; not tested in production
[2] PCB losses are subtracted.

Table 10. Characteristics

4400 MHz ≤ f ≤ 5000 MHz; V_{CC} = 1.8 V; T_{amb} = 25 °C; input matched 50 Ω using application diagram from Figure 4 and component values as in Table 13. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain mode						
G_p	power gain	f = 4400 MHz	-	12.5	-	dB
		f = 5000 MHz	-	10.0	-	dB
NF	noise figure	f = 4400 MHz [1]	-	1.0	-	dB
		f = 5000 MHz [1]	-	1.3	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 4400 MHz	-	-8.5	-	dBm
		f = 5000 MHz	-	-7.5	-	dBm
$P_{o(1dB)}$	output power at 1 dB gain compression	f = 4400 MHz	-	2.5	-	dBm
		f = 5000 MHz	-	1.0	-	dBm
$IP3_i$	input third-order intercept point	f = 4400 MHz; Δf = 1 MHz/10 MHz	-	2.0	-	dBm
		f = 5000 MHz; Δf = 1 MHz/10 MHz	-	2.0	-	dBm
RL_{in}	input return loss	f = 4400 MHz	-	17.0	-	dB
		f = 5000 MHz	-	14.0	-	dB
RL_{out}	output return loss	f = 4400 MHz	-	15.0	-	dB
		f = 5000 MHz	-	10.0	-	dB
ISL	isolation	f = 4400 MHz	-	22.0	-	dB
		f = 5000 MHz	-	22.0	-	dB
Bypass mode						
G_p	power gain	f = 4400 MHz	-	-3.8	-	dB
		f = 5000 MHz	-	-7.2	-	dB
ISL	isolation	f = 4400 MHz	-	3.8	-	dB
		f = 5000 MHz	-	7.2	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 4400 MHz	-	7.0	-	dBm
		f = 5000 MHz	-	6.0	-	dBm
$IP3_i$	input third-order intercept point	f = 4400 MHz	-	22.0	-	dBm
		f = 5000 MHz	-	19.0	-	dBm
RL_{in}	input return loss	f = 4400 MHz	-	10.0	-	dB
		f = 5000 MHz	-	6.0	-	dB
RL_{out}	output return loss	f = 4400 MHz	-	22.0	-	dB
		f = 5000 MHz	-	21.0	-	dB
$\Delta\varphi_{S21}$	gain phase step variation	between gain mode and bypass mode				
		f = 4400 MHz [2]	-5.0	-	+5.0	deg
		f = 5000 MHz [2]	-5.0	-	+5.0	deg

[1] PCB losses are subtracted.

[2] Guaranteed by design; not tested in production

Table 11. Characteristics

4400 MHz ≤ f ≤ 5000 MHz; V_{CC} = 2.8 V; T_{amb} = 25 °C; input matched 50 Ω using application diagram from Figure 4 and component values as in Table 13. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain mode						
G_p	power gain	f = 4400 MHz	-	13.0	-	dB
		f = 5000 MHz	-	10.5	-	dB
NF	noise figure	f = 4400 MHz [1]	-	1.0	-	dB
		f = 5000 MHz [1]	-	1.3	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 4400 MHz	-	-6.0	-	dBm
		f = 5000 MHz	-	-5.0	-	dBm
$P_{o(1dB)}$	output power at 1 dB gain compression	f = 4400 MHz	-	5.0	-	dBm
		f = 5000 MHz	-	4.5	-	dBm
$IP3_i$	input third-order intercept point	f = 4400 MHz; Δf = 1 MHz/10 MHz	-	3.0	-	dBm
		f = 5000 MHz; Δf = 1 MHz/10 MHz	-	3.0	-	dBm
RL_{in}	input return loss	f = 4400 MHz	-	17.0	-	dB
		f = 5000 MHz	-	14.0	-	dB
RL_{out}	output return loss	f = 4400 MHz	-	15.0	-	dB
		f = 5000 MHz	-	10.0	-	dB
ISL	isolation	f = 4400 MHz	-	22.0	-	dB
		f = 5000 MHz	-	22.0	-	dB

Table 11. Characteristics...*continued*

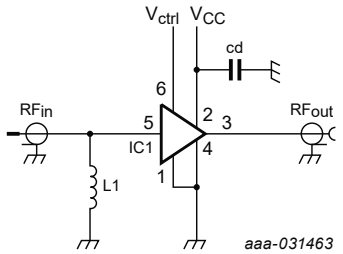
4400 MHz ≤ f ≤ 5000 MHz; V_{CC} = 2.8 V; T_{amb} = 25 °C; input matched 50 Ω using application diagram from Figure 4 and component values as in Table 13. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bypass mode						
G_p	power gain	f = 4400 MHz	-	-3.6	-	dB
		f = 5000 MHz	-	-7.0	-	dB
ISL	isolation	f = 4400 MHz	-	3.6	-	dB
		f = 5000 MHz	-	7.0	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 4400 MHz	-	7.0	-	dBm
		f = 5000 MHz	-	6.0	-	dBm
$IP3_i$	input third-order intercept point	f = 4400 MHz	-	22.0	-	dBm
		f = 5000 MHz	-	19.0	-	dBm
RL_{in}	input return loss	f = 4400 MHz	-	10.0	-	dB
		f = 5000 MHz	-	6.0	-	dB
RL_{out}	output return loss	f = 4400 MHz	-	22.0	-	dB
		f = 5000 MHz	-	21.0	-	dB
$\Delta\varphi_{S21}$	gain phase step variation	between gain mode and bypass mode				
		f = 4400 MHz [2]	-5.0	-	+5.0	deg
		f = 5000 MHz [2]	-5.0	-	+5.0	deg

[1] PCB losses are subtracted.
[2] Guaranteed by design; not tested in production

13 Application information

13.1 LTE/5G NR application



For a list of components, see Table 12.

Figure 3. Schematics LTE/5G NR evaluation board 3300 MHz-4200 MHz

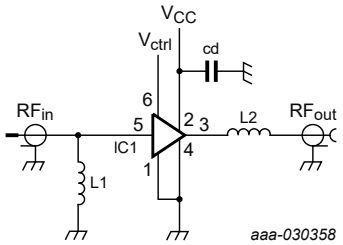
For improving coexistence in applications, using e.g. LTE B3, refer to Application Note AN11795.

Table 12. List of components

For schematics, see Figure 3

Component	Description	Value	Remarks
C_d	decoupling capacitor	1 µF	The total capacitance on the V_{CC} node must be at least 1 µF at a maximum distance of 15 mm from the V_{CC} pin. Typically, such capacitance is already present at the output of the V_{CC} voltage regulator.
IC1	BGS8U5		NXP
L1	high-quality matching inductor	2.2 nH	Murata LQW15A

13.2 5G NR application



For a list of components, see Table 13.

Figure 4. Schematics 5G NR evaluation board 4400 MHz-5000 MHz

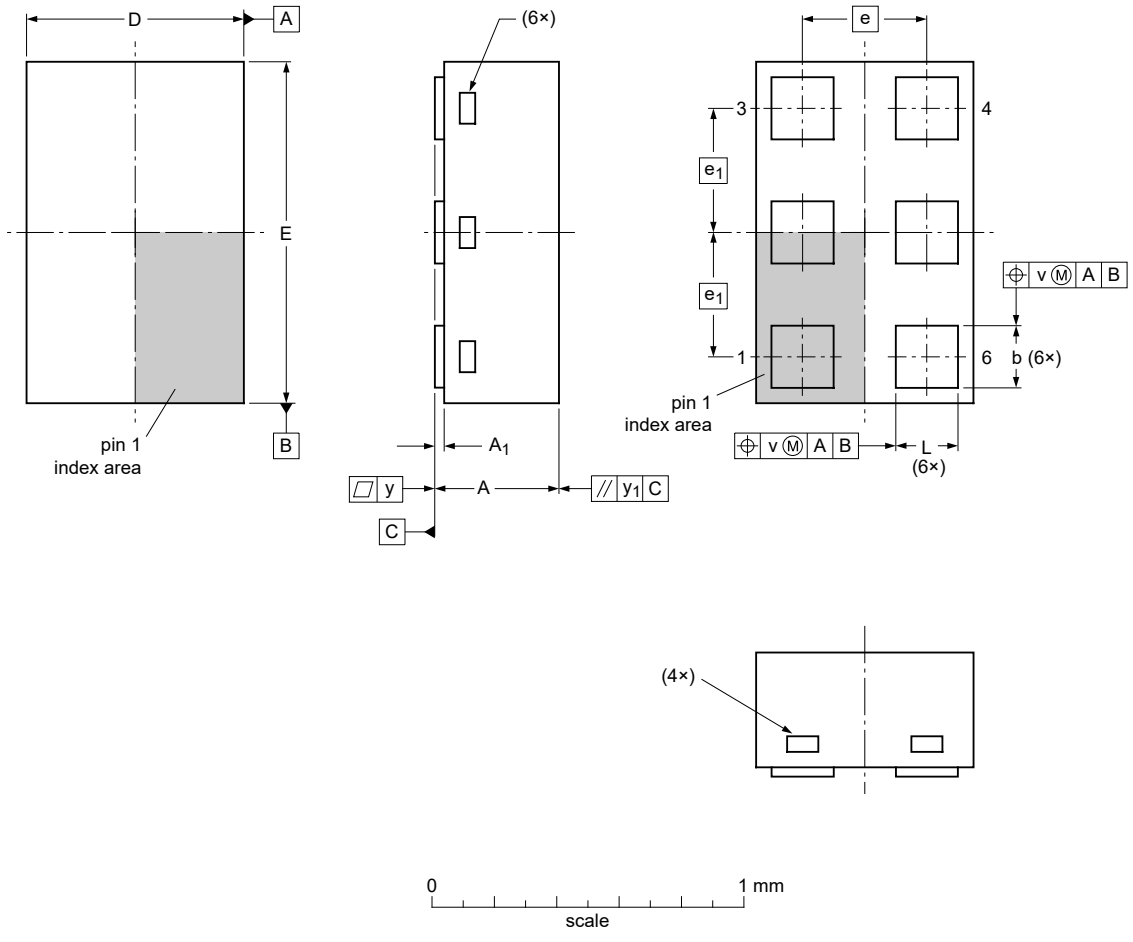
Table 13. List of components

For schematics, see Figure 4

Component	Description	Value	Remarks
C_d	decoupling capacitor	1 µF	The total capacitance on the V_{CC} node must be at least 1 µF at a maximum distance of 15 mm from the V_{CC} pin. Typically, such capacitance is already present at the output of the V_{CC} voltage regulator.
IC1	BGS8U5		NXP
L1	high-quality matching inductor	2.2 nH	Murata LQW15A
L2	high-quality matching inductor	1.0 nH	Murata LQG15A

14 Package outline

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1.1 x 0.7 x 0.37 mm **SOT1232**



Dimensions (mm are the original dimensions)

Unit		A	A_1	D	E	e_1	e	b	L	V	Y	Y_1
	min	0.34		0.65	1.05			0.17	0.17			
mm	nom	0.37		0.70	1.10	0.4	0.4	0.20	0.20	0.1	0.05	0.1
	max	0.40	0.04	0.75	1.15			0.25	0.25			

Note
1. Dimension A is including plating thickness.

sot1232_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1232						~~13-04-12~~ 13-11-08

Figure 5. Package outline SOT1232 (XSON6)

15 Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.
Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

16 Abbreviations

Table 14. Abbreviations

Acronym	Description
ESD	electrostatic discharge
HBM	human body model
MMIC	monolithic microwave-integrated circuit
MUF	molded underfill
LTE	long-term evolution
5G NR	fifth generation new radio
PCB	printed-circuit board
SiGe:C	silicon germanium carbon

17 Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGS8U5 v.5	20211201	Product data sheet	-	BGS8U5 v.4
modification	changed status from Company confidential to Public			
BGS8U5 v.4	20181031	Product data sheet	-	BGS8U5 v.3
modification	adapted extra frequencies and values for different conditions.			
BGS8U5 v.3	20180307	Product data sheet	-	BGS8U5 v.2.0
modification	min values changed on RL_{out} parameter in the characteristics chapter			
BGS8U5 v.2.0	20180206	Product data sheet	-	BGS8U5 v.1.3
modification	min and max value added at isolation parameter in the characteristics chapter			
BGS8U5 v.1.3	20180131	Product data sheet	-	BGS8U5 v.1
BGS8U5 v.1	20171222	Product data sheet	-	-

18 Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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