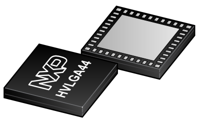


BGU8821/A

Dual channel low-noise high linearity amplifier with DSA and SPDT

Rev. 6 — 15 April 2020 **Product data sheet**

1 General description

The BGU8821/A, also known as the BTS5201L/A, is a highly integrated dual channel digitally controlled low noise amplifier (LNA) with digital step attenuator (DSA) and a single-pole double-through (SPDT) switch. The BGU8821/A supports receivers (main and diversity) in both TDD and FDD systems. It has a first stage LNA optimized for sensitivity, followed by a DSA and output stage amplifier. To support highly integrated solutions and reduce platform costs a standalone SPDT switch is included.

The BGU8821/A is optimized for frequency band 700 MHz - 1000 MHz, but supports 452.5 MHz - 457.5 MHz as well.

The BGU8821/A is controlled via SPI bus, supporting both 3- and 4-wire configurations. Additionally, in TDD systems the LNAs and DSA can also be controlled via direct-access pins.

The BGU8821/A is housed in a small footprint (5 mm x 5 mm x 0.72 mm) 44-pin leadless package.

2 Features and benefits

- Dual channel (diversity and main) highly integrated LNA + DSA
- Frequency bands 452.5 MHz - 457.5 MHz and 700 MHz - 1000 MHz
- Noise figure = 0.6 dB
- High linearity: $IP3_O$ = 38 dBm
- High input return loss >12 dB
- High output return loss > 12 dB
- Unconditionally stable up to 20 GHz
- Digital step attenuator with 31 dB range and 1 dB step
- High linearity SPDT, $P_{i(1dB)}$ = 35 dBm, $IP3_i$ = 50 dBm
- Programmable via 3 wire or 4-wire SPI (Read/write)
- Small 44-terminal leadless package 5 mm × 5 mm × 0.72 mm
- ESD protection on all terminals
- Moisture sensitivity level 3
- +5 V single supply

3 Applications

- Wireless infrastructure
- 5G ready
- Low noise and high linearity applications
- LTE, W-CDMA, CDMA, GSM
- General-purpose wireless applications
- TDD or FDD systems
- Suitable for small cells

4 Quick reference data

Table 1. Quick reference data BGU8821/A LNA1

f = 900 MHz; V_{CC} = 5 V; T_{amb} = 25 °C; input and output 50 Ω; unless otherwise specified. All RF parameters are measured in an application board as shown in Figure 44 with components listed in Table 33 optimized for f = 900 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	LNA1 enable	-	54	64	mA
		Disable	-	3	-	mA
G_p	power gain	[1]	15.9	19	-	dB
NF	noise figure	[1]	-	0.6	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression	[1]	17.9	21	-	dBm
$IP3_O$	output third-order intercept point	2-tone; tone spacing = 1 MHz; P_i = -15 dBm per tone [1]	34	38	-	dBm

[1] Connector and Printed-Circuit Board (PCB) losses have been de-embedded for all RF parameters.

Table 2. Quick reference data BGU8821/A DSA+LNA2

f = 900 MHz; V_{CC} = 5 V; T_{amb} = 25 °C; input and output 50 Ω; unless otherwise specified. All RF parameters are measured in an application board as shown in Figure 44 with components listed in Table 33 optimized for f = 900 MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	LNA2 enable	-	57	67	mA
		Disable	-	5	-	mA
G_p	power gain	[1]	14.5	18	-	dB
NF	noise figure	[1]	-	1.6	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression	[1]	18.0	22	-	dBm
$IP3_O$	output third-order intercept point	2-tone; tone spacing = 1 MHz; P_i = -15 dBm per tone [1]	34	39	-	dBm

[1] Connector and Printed-Circuit Board (PCB) losses have been de-embedded for all RF parameters.

Table 3. Quick reference data BGU8821/A SPDT

f = 900 MHz; V_{CC} = 5 V; T_{amb} = 25 °C; input and output 50 Ω; unless otherwise specified. All RF parameters are measured in an application board as shown in Figure 44 with components listed in Table 33 optimized for f = 900 MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current		-	2.1	-	mA
α_{ins}	insertion loss	[1]	-	1.3	1.6	dB
RL_{in}	input return loss	all SPDT	-	17	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression		-	35	-	dBm
$IP3_i$	input third-order intercept point	2-tone; tone spacing = 1 MHz; P_i = +5 dBm per tone	-	54	-	dBm

[1] Connector and Printed-Circuit Board (PCB) losses have been de-embedded for all RF parameters.

5 Ordering information

Table 4. Table 4. Ordering information

Type number	Orderable part number	Package		
		Name	Description	Version
BGU8821/A	BGU8821/AY	HVLGA44	plastic thermal enhanced very thin profile land grid array package; no leads; 44 terminals; body 5 × 5 × 0.72 mm	SOT1431-1

6 Functional diagram

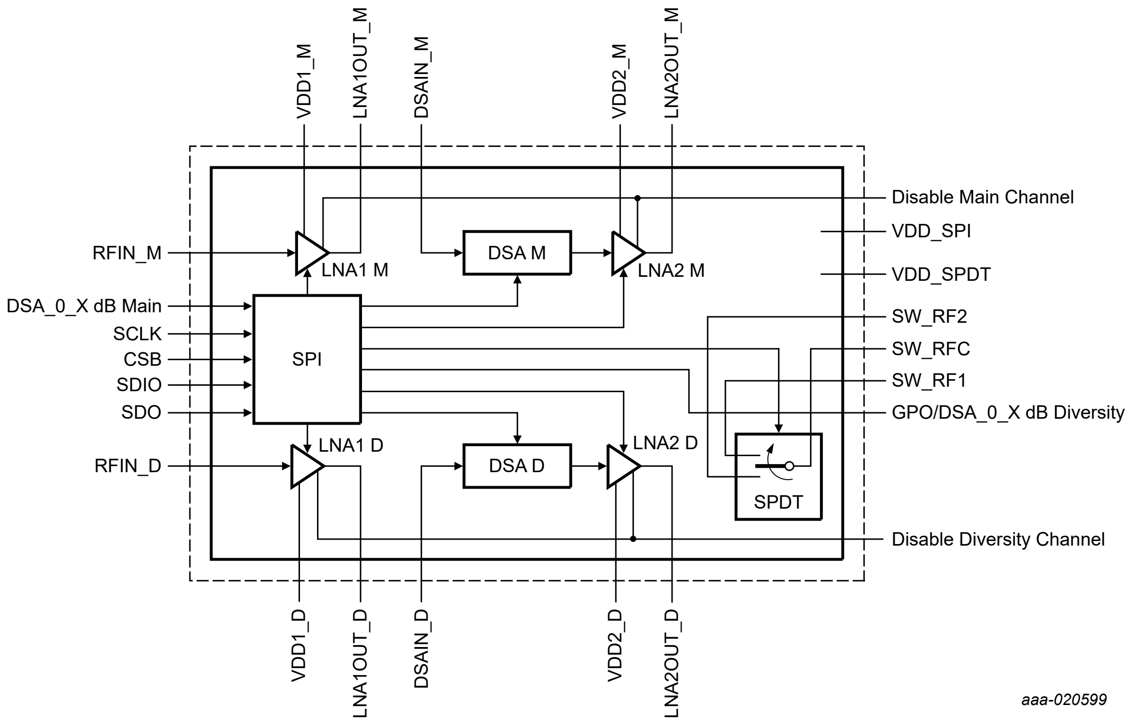
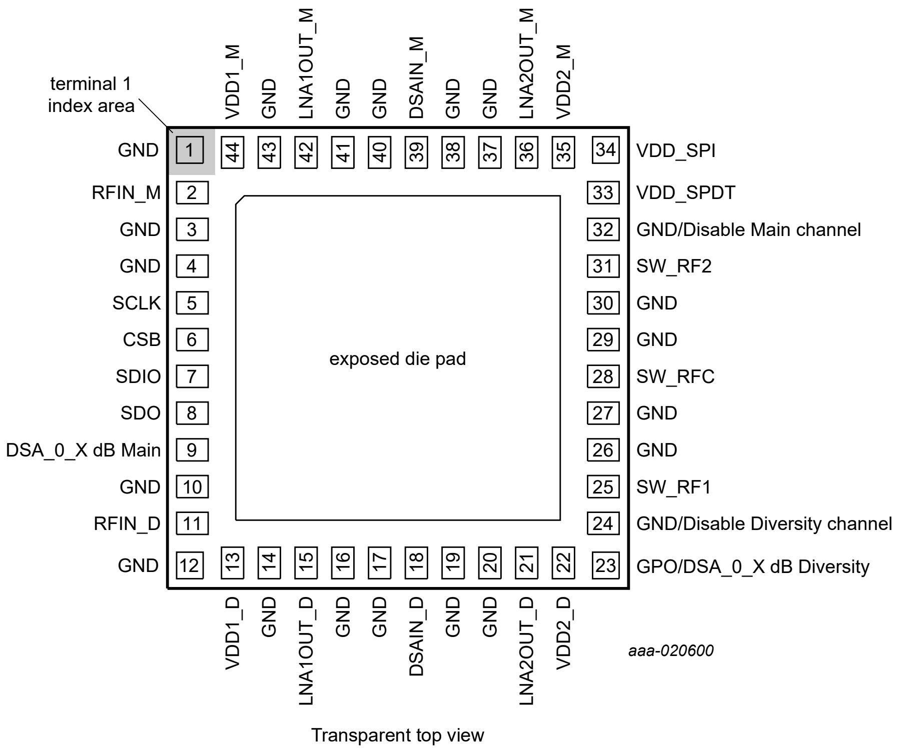


Figure 1. Functional diagram

7 Pinning information

7.1 Pinning



Multiple power and ground pins allows for independent supply domains to improve cross channel isolation and between blocks in one single channel. In, order to reduce series inductance at all RF ports and RF grounding a small package footprint was chosen.

Figure 2. Pin configuration

7.2 Pin description

Table 5. Pin description

Symbol	Pin	Description
GND	1, 3, 4, 10, 12, 14,16, 17, 19, 20, 26, 27, 29, 30, 37, 38,40, 41,43	Ground
RFIN_M	2	RF Input to LNA1, main channel. An external DC block is required. External SMD is required for matching.
SCLK	5	Clock input for SPI
CSB	6	Chip select active low
SDIO	7	Serial data in/out. Push-Pull pin
SDO	8	Serial data out. Push-Pull pin
DSA_0_X dB Main	9	Direct-access DSA setting between minimum attenuation and X dB attenuation programmed prior to TDD mode, main channel

Symbol	Pin	Description
RFIN_D	11	RF Input to LNA1, diversity channel. An external DC block is required. External SMD is required for matching.
VDD1_D	13	Supply to LNA1, diversity channel. Decoupling capacitors are required
LNA1OUT_D	15	RF output of LNA1, diversity channel. An external DC block + BIAS choke are required.
DSAIN_D	18	RF input to DSA, diversity channel. An external DC block + matching SMD are required.
LNA2OUT_D	21	RF output of LNA2, diversity channel. An external DC block + BIAS choke are required.
VDD2_D	22	Supply to LNA2, diversity channel. Decoupling capacitors are required.
GPO/DSA_0_X dB Diversity	23	GPO (General Purpose Output). Leave open when not used. Direct-access DSA setting between minimum attenuation and X dB attenuation programmed prior to TDD mode diversity channel
GND/Disable Diversity Channel	24	Ground or Disable Diversity Channel
SW_RF1	25	Switch RF path 1. An external DC block is required
SW_RFC	28	Switch RF common. An external DC block is required
SW_RF2	31	Switch RF path 2. An external DC block is required
GND/Disable Main Channel	32	Ground or Disable Main Channel
VDD_SPDT	33	V_{DD} into SPDT, decoupling capacitors are required
VDD_SPI	34	V_{DD} into SPI, decoupling capacitors are required
VDD2_M	35	Supply to LNA2, main channel. Decoupling capacitors are required
LNA2OUT_M	36	RF output of LNA2, main channel. An external DC block + BIAS choke are required.
DSAIN_M	39	RF input to DSA, main channel. An external DC block + matching SMD are required.
LNA1OUT_M	42	RF output from LNA1, main channel. An external DC block + BIAS choke are required.
VDD1_M	44	Supply to LNA2, diversity channel. Decoupling capacitors are required.
GND	Exposed die pad	Ground

8 Functional description

8.1 Direct-Access Functionality for Main and Diversity Channels in TDD Systems

In addition to SPI in TDD systems the LNAs and DSA can also be controlled via direct-access pins. Pins 32 and 24 are used for Direct Disable mode for Main and Diversity channels correspondingly.

Pins 9 and 23 are used for Direct DSA Attenuation mode for Main and Diversity channels correspondingly.

By default, the BGU8821/A starts up in direct-access mode. SPI bus remains fully functional. <VDD_SPI> pin has to be connected to power supply. Reset command <SPI_RST> must be applied.

8.1.1 Direct Disable mode

In Direct Disable mode Main and Diversity channels can be disabled independently without accessing SPI bus.

Pin 32 < Disable Main Channel> shall be set to HIGH to disable Main channel (LNA1_M and LNA2_M of the Main channel are disabled (set in low current mode).

Pin 24 < Disable Diversity Channel> shall be set to HIGH to disable Diversity channel (LNA1_D and LNA2_D of the Diversity channel are disabled (set in low current mode).

VIH voltage for those pins is limited to 2.75 V, as indicated in Table 31.

Direct Disable mode functionality has similar effect as if both LNA1 and LNA2 of Main or Diversity channels have been disabled via LNA Enable bits (register 0x10h, bits [7-6] for Main channel and bits [5-4] for Diversity channel).

8.1.2 Direct DSA Attenuation mode

In Direct DSA Attenuation mode, Main and Diversity DSAs can be toggled independently without accessing SPI bus.

Pin 9 <DSA_0_X_dB Main> can be toggled to set DSA_M between Minimum Attenuation (level LOW) and predefined X dB attenuation (level HIGH). X dB attenuation is defined in DSA_M_TDD_ATTN (register 0x16h, bits [6-2]). Default reset value is 15 dB.

Table 6. Direct DSA Attenuation mode for Main channel truth table

*Legend: * reset value*

Pin 9	DIRECT_DSA_M	DSA_M Attenuation	Description
DSA_0_X dB Main	*register 0x13h, bit [1]*		
0	0*	Min attenuation I_L	
1	0*	I_L x X dB Attenuation	X dB is set in register 0x16h, default value is 15 dB
x	1	SPI setting	DSA_M controlled by SPI using register 0x11h, default value is Min attenuation, I_L

Pin 23 <GPO/DSA_0_X_dB Diversity> can be toggled to set DSA_M between Minimum Attenuation (level LOW) and predefined X dB attenuation (level HIGH). X dB attenuation is defined in DSA_D_TDD_ATTN (register 0x17h, bits [6-2]). Default reset value is 15 dB.

Table 7. Direct DSA Attenuation mode for Diversity channel truth table

*Legend: * reset value*

Pin 23	DIRECT_DSA_D	DSA_D Attenuation	Description
DSA_0_X dB Diversity	*register 0x13h, bit [2]*		
0	0*	Min attenuation I_L	
1	0*	I_L x X dB Attenuation	X dB is set in register 0x17h, default value is 15 dB
GPO functionality	1	SPI setting	DSA_D controlled by SPI using register 0x12h, default value is Min attenuation, I_L

By default, the BGU8821/A starts up in Direct DSA Attenuation mode. This mode can be switched off via register 0x13h, bits [1] (for the Main channel) and [2] (for the Diversity channel). While Direct DSA Attenuation mode for Diversity channel is active, GPO functionality is not available.

When DIRECT_DSA_D (register 0x13h bit [2]) is set HIGH, Direct DSA Attenuation mode for Diversity channel is switched off and Pin 23 is used as <GPO> pin.

8.2 Serial Peripheral interface (SPI) Bus

The Serial Peripheral Interface (SPI) bus allows simple interfacing with many industry microprocessors; it provides access to all the registers that define the operation of the BGU8821/A.

8.2.1 Hardware Interface description

The SPI functionality includes registers and an address decoder to support both read and write operations. Register mapping is organized as a 15-bit address register and an 8-bit data register. In order to avoid register coupling, data should always be sent as an 8-bit sequence.

Register addresses 0x00h – 0x06h, 0x10h – 0x13h, 0x16h – 0x17h and 0x0Ch – 0x0Fh set the operation of the BGU8821/A. Any other address used does not affect the behavior of the device (e.g. device does not stall).

The BGU8821/A supports a 3-wire or 4-wire SPI bus operation mode. <SDIO> is used as a bidirectional pin in 3-wire mode. During the write cycle, it is used as an input pin and during the read cycle as output pin. In 4-wire bus mode, <SDIO> and <SDO> are used as unidirectional input and output pins correspondingly. <CLK> acts as the serial clock input. The status of <CSB> defines whether the SPI interface of the device is enabled (<CSB> is LOW) or disabled (<CSB> is HIGH). Programming clock edges (rising edges) at <CLK> input and data at the <SDIO> input are ignored until LOW-level is applied to the <CSB> input.

When the BGU8821/A is in power-down mode or there is no power supplied, the <SDIO> and <CSB> pins become high-impedance and do not disturb the SPI bus.

8.2.2 Programming registers

The programming word is set through the input <SDIO> pin and a shift register, while <CSB> level is LOW. To release the SPI bus, <CSB> is set HIGH again.

The rising edge of the clock pulse <CLK> shifts each data bit value into the shift register.

The BGU8821/A supports single-byte and multi-byte (streaming) read/write access (register 0x01h bit [7]). In single-byte access, the new settings of the programmed register are applied on the last rising edge of <CLK> of data byte period. In multi-byte (streaming) access mode register address is auto-incremented or auto-decremented (depends on register 0x00h bits [5] and [2]) for the next 8-bit programming word.

By default, the data is entered with the most significant bit (MSB) first and the least significant bit (LSB) last. Register 0x00h bits [6] and [1] can be used to reverse the order (LSB bit first).

Figure 3 and Figure 4 illustrate SPI read and write cycles for 3-wire and 4-wire modes.

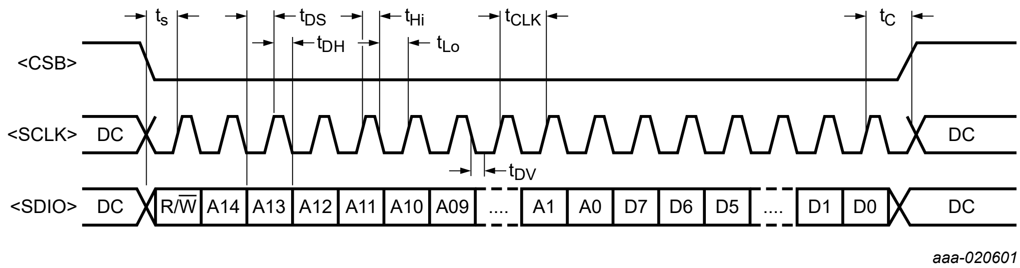


Figure 3. SPI Single byte write 3-wire SPI bus

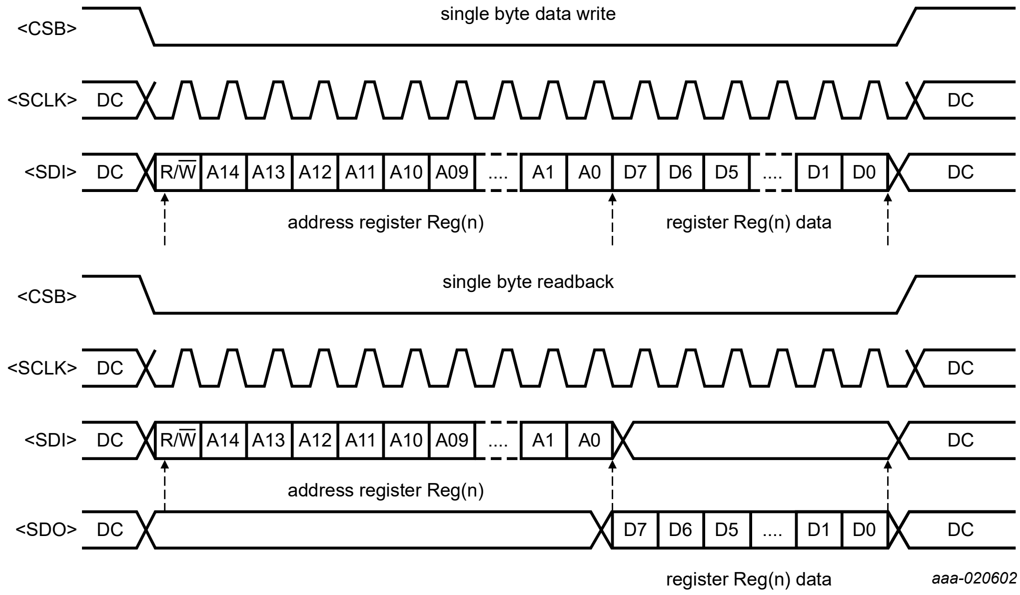


Figure 4. SPI Single byte Read/Write 4-wire SPI bus

8.2.3 Power up Sequence

The BGU8821/A powers-up with the default register list content after supply voltage is applied to the $V_{DD(SPI)}$ pin.

8.2.4 SPI control registers

Register addresses 0x00h to 0x02h and 0x0Fh are dedicated to SPI control settings. Register 0x00h is mirror register, it will change to level HIGH if both corresponding bits are set HIGH.

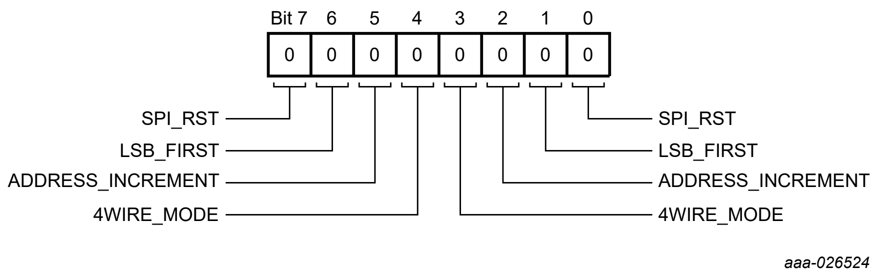


Figure 5. Register address 0x00h

Table 8. Register address 0×00h

*Legend: * reset value*

Bits	Name	Access	Value	Description
7	SPI_RST	W		SPI reset bit. All registers are reverted to default state when bit is set HIGH
7	SPI_RST	W	0*	Normal operation
			1	Reset registers from address 0x02h up to 0x17h to default states. Bit shall be HIGH together with bit [0]. Bit value resets back to LOW level after command is executed
6	LSB_FIRST	R/W		Sets MSB_FIRST (default) or LSB_FIRST mode of operation
			0*	MSB first mode. The data is entered with MSB first and LSB last.
			1	LSB first mode. The data is entered with LSB first and MSB last. Bit shall be set HIGH together with bit [1]
5	ADDRESS_INCREMENT	R/W		Sets register address read/write order for the streaming (multi-byte) SPI access mode
			0*	Auto-decrementing register address order in the streaming mode
			1	Auto-incrementing register address order in the streaming mode. Bit shall be set HIGH together with bit [2]
4	4WIRE_MODE	R/W		Switches SPI bus between 3-wire and 4-wire modes
			0*	3-wire mode with <SDIO> as bidirectional input and output pin
			1	4-wire mode with <SDIO> as unidirectional input and <SDO> as unidirectional output pins. Bit shall be set HIGH together with bit [3]

Bits	Name	Access	Value	Description
3	4WIRE_MODE	R/W	Switches SPI bus between 3-wire and 4-wire modes	
			0*	3-wire mode with <SDIO> as bidirectional input and output pin
			1	4-wire mode with <SDIO> as unidirectional input and <SDO> as unidirectional output pins. Bit shall be set HIGH together with bit [4]
2	ADRESS_INCREMENT	R/W	Sets register address read/write order for the streaming (multi-byte) SPI access mode	
			0*	Auto-decrementing register address order in the streaming mode
			1	Auto-incrementing register address order in the streaming mode. Bit shall be set HIGH together with bit [5]
1	LSB_FIRST	R/W	Sets MSB_FIRST (default) or LSB_FIRST mode of operation	
			0*	MSB_FIRST mode. The data is entered with MSB first and LSB last
			1	LSB_FIRST mode. The data is entered with LSB first and MSB last. Bit shall be set HIGH together with bit [6]
0	SPI_FIRST	W	SPI reset bit. All registers are reverted to default state when bit is set HIGH	
			0*	Normal operation
			1	Resets all registers from address 0x02h up to 0x17h to default states. Bit shall be set HIGH together with bit [7]. Bit value resets back to LOW level after command is executed.

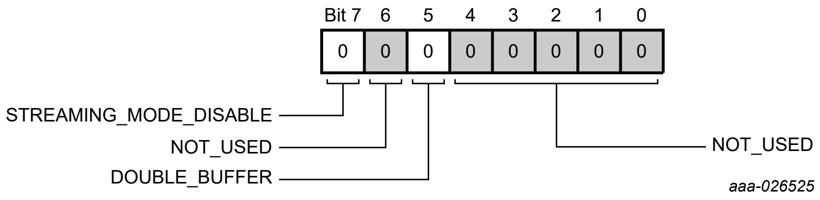


Figure 6. Register address 0x01h

Table 9. Register address 0×01h

*Legend: * reset value*

Bits	Name	Access	Value	Description
7	STREAMING_MODE_ DISABLE	R/W	streaming (multi-byte) read/write access is enabled by default (level LOW). Addresses will be auto-incremented or auto-decremented, based on register 0x00h, bit [5] and bit [2]. Setting HIGH disables streaming mode and switches to single-byte read/write access	
			0*	Streaming (multi-byte) read/write access
			1	Single-byre read/write access
6	NOT_USED	R	Not used	
5	DOUBLE_BUFFER	R/W	Enables Double-buffer mode for register 0x02h	
			0*	Read-back from active registers
			1	Read-back from buffer registers
4-0	NOT_USED	R	Not used	

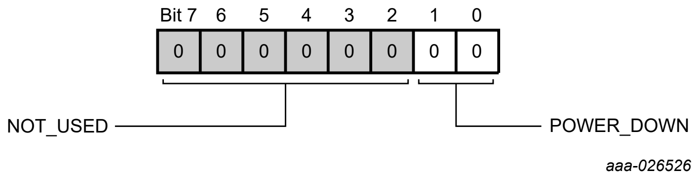


Figure 7. Register address 0x02h

Table 10. Register address 0×02h

*Legend: * reset value*

Bits	Name	Access	Value	Description
7-2	NOT_USED	R	Not used	
1-0	POWER_DOWN	R/W	Sets power-down mode. In power-down mode all LNAs are disabled, DSA's are in high attenuation mode. SPI bus is accessible and fully functional. This register is double buffered. Active value is effective after writing register 0x0Fh, bit [0]. Read value depends on setting of register 0x01h, bit [5]	
			00*	Normal operation
			01	
			10	
			11	Power-down mode

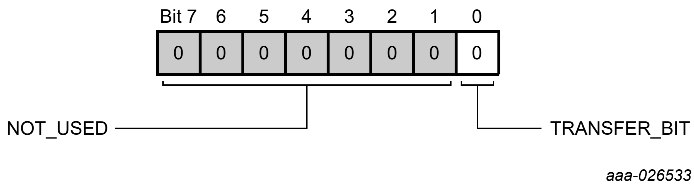


Figure 8. Register address 0x0Fh

Table 11. Register address 0×0Fh

*Legend: * reset value*

Bits	Name	Access	Value	Description
7-1	NOT_USED	R	Not used	
0	TRANSFER_BIT	W	Transfer bit must be set HIGH to transfer the contents of the buffer into the active register 0x02h	
			0*	No transfer
			1	Transfer data into active registers. Bit value resets back to LOW level after command is executed

8.2.5 Identification registers

Register addresses 0x03h to 0x06h, 0x0Ch and 0x0Dh are read-only registers and are used for identification (such as vendor ID, chip ID, chip version, etc).

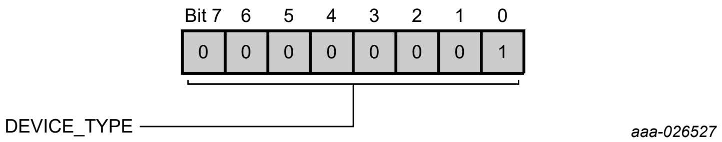


Figure 9. Register address 0x03h

Table 12. Register address 0×03h

*Legend: * reset value*

Bits	Name	Access	Value	Description
7-0	DEVICE_TYPE	R	Sets device type: RF CHIP	
			00000001*	

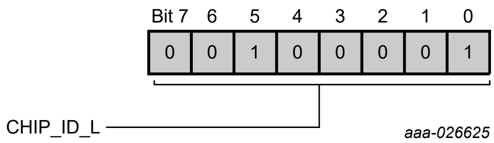


Figure 10. Register address 0x04h

Table 13. Register address 0×04h

*Legend: * reset value*

Bits	Name	Access	Value	Description
7-0	CHIP_ID_L	R	Low byte of Chip ID: 0x8821h	
			00100001*	

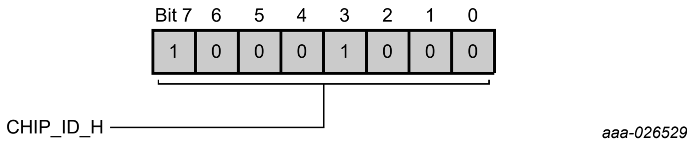


Figure 11. Register address 0x05h

Table 14. Register address 0×05h

*Legend: * reset value*

Bits	Name	Access	Value	Description
7-0	CHIP_ID_H	R	High byte of Chip ID: 0x8821h	
			10001000*	

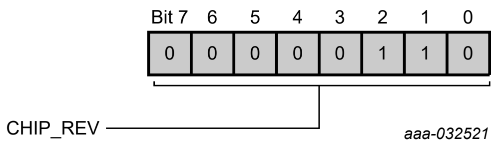


Figure 12. Register address 0x06h

Table 15. Register address 0×06h

*Legend: * reset value*

Bits	Name	Access	Value	Description
7-0	CHIP_REV	R	Chip Revision: 0x06h	
			00000110*	

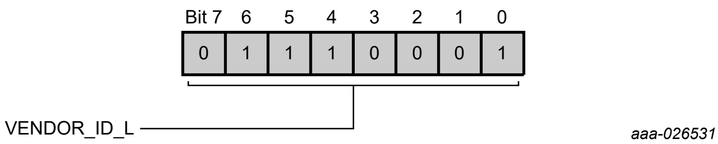


Figure 13. Register address 0x0Ch

Table 16. Register address 0×0Ch

*Legend: * reset value*

Bits	Name	Access	Value	Description
7-0	VENDOR_ID_L	R	Low byte of Vendor ID: 0x471h - NXP Semiconductors	
			01110001*	

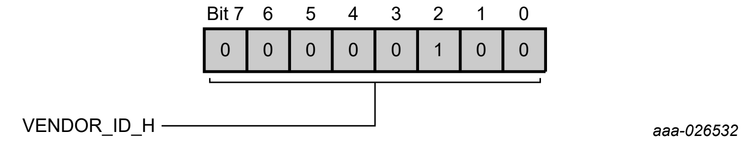


Figure 14. Register address 0x0Dh

Table 17. Register address 0×0Dh

*Legend: * reset value*

Bits	Name	Access	Value	Description
7-0	VENDOR_ID_H	R	High byte of Vendor ID: 0x471h - NXP Semiconductors	
			0000100*	

8.2.6 Functional registers

Register addresses 0x10h – 0x13h, 0x16h, and 0x17h are used to set BGU8821/A functionality when accessed in write mode and to provide status update when accessed in read mode.

Registers 0x10h – 0x13h, 0x16h, and 0x17h are not double buffered. Transfer bit (register 0×0Fh, bit [0]) is not needed for these registers.

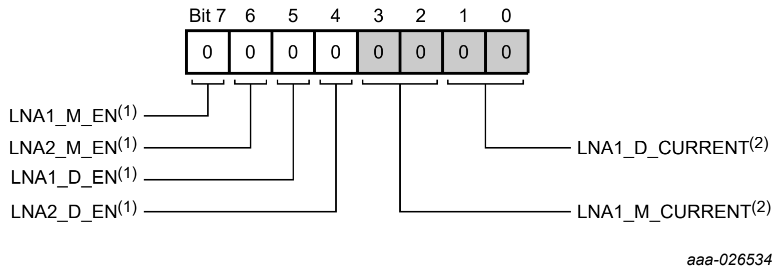


Figure 15. Register address 0x10h

Table 18. Register address 0×10h

*Legend: * reset value*

Bits	Name	Access	Value	Description
7	LNA1_M_EN[1]	R/W	Enables LNA1 in Main Channel	
			0	LNA1_M is disabled (in low current mode)
			1*	LNA1_M is enabled
6	LNA2_M_EN[1]	R/W	Enables LNA2 in Main Channel	
			0	LNA2_M is disabled (in low current mode)
			1*	LNA2_M is enabled
5	LNA1_D_EN[1]	R/W	Enables LNA1 in Diversity Channel	
			0	LNA1_D is disabled (in low current mode)
			1*	LNA1_D is enabled

Bits	Name	Access	Value	Description
4	LNA2_D_EN[1]	R/W	Enables LNA2 in Diversity Channel	
			0	LNA2_D is disabled (in low current mode)
			1*	LNA2_D is enabled
3-2	LNA1_M_CURRENT[2]	R	LNA1_M current monitor status	
			00*	Normal operation
			10	N/A
			01	Abnormal low current (min/typ/max => 9/23/33 mA)
			11	Abnormal high current (min/typ/max => 80/100/171 mA)
1-0	LNA1_D_CURRENT[2]	R/W	LNA1_D current monitor status	
			00*	Normal operation
			10	N/A
			01	Abnormal low current (min/typ/max => 9/23/33 mA)
			11	Abnormal high current (min/typ/max => 80/100/171 mA)

[1] After reset/start-up LNAs are enabled.
[2] Current monitor shall not be used with RF signals above +5 dBm.

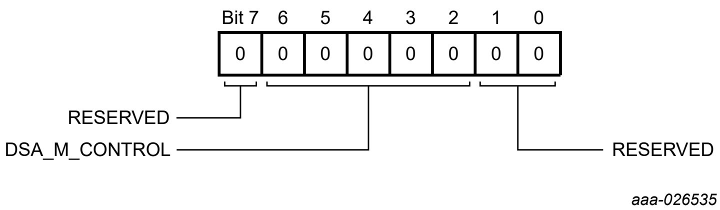


Figure 16. Register address 0x11h

Table 19. Register address 0×11h

*Legend: * reset value*

Bits	Name	Access	Value	Description
7	RESERVED	R/W	Reserved bit. Shall be kept LOW	
			0*	
6-2	DSA_M_CONTROL	R/W	Main Channel DSA 5-bit attenuation control	
			00000*	Minimum Attenuation, equal to I_L
			00001	I_L + 1 dB Attenuation
			00010	I_L + 2 dB Attenuation
			...	
			11111	I_L + 31 dB Attenuation
1-0	RESERVED	R/W	Reserved bits. Shall be kept LOW	
			0*	

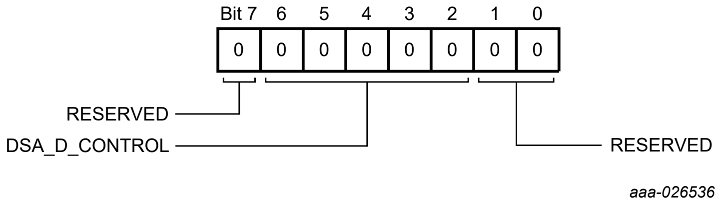


Figure 17. Register address 0x12h

Table 20. Register address 0×12h

*Legend: * reset value*

Bits	Name	Access	Value	Description
7	RESERVED	R/W	Reserved bit. Shall be kept LOW	
			0*	
6-2	DSA_D_CONTROL	R/W	Diversity Channel DSA 5-bit attenuation control	
			00000*	Minimum Attenuation, equal to I_L
			00001	I_L + 1 dB Attenuation
			00010	I_L + 2 dB Attenuation
			...	
			11111	I_L + 31 dB Attenuation
1-0	RESERVED	R/W	Reserved bits. Shall be kept LOW	
			0*	

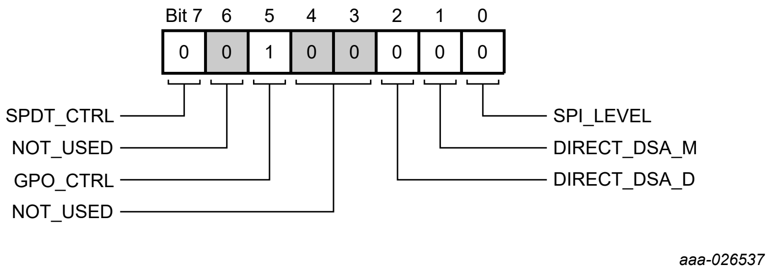


Figure 18. Register address 0x13h

Table 21. Register address 0×13h

*Legend: * reset value*

Bits	Name	Access	Value	Description
7	SPDT_CTRL	R/W	SPDT control bit. Connects SW_RFC input to SW_RF1 output (default) or to SW_RF2 output	
			0*	SW_RFC connected to SW_RF1
			1	SW_RFC connected to SW_RF2
6	NOT_USED	R	Not used	

Bits	Name	Access	Value	Description
5	GPO_CTRL	R/W	GPO (pin 23) control bit. GPO functionality is disabled, when device is in direct-access mode (register 0x13h bit [2] is LOW)	
			0	GPO LOW
			1*	GPO HIGH
4-3	NOT_USED	R	Not used	
2	DIRECT_DSA_D	R/W	Disables direct access for DSA_D (DSA in Diversity channel)	
			0*	Direct access is enabled. DSA_D can be toggled between I_L and prior programmed value x dB (set via register 0x17h) by pin 23. GPO functionality is disabled.
			1	Direct access is disabled. DSA can be set via register 0x12h.
1	DIRECT_DSA_M	R/W	Disables direct access for DSA_M (DSA in Main channel)	
			0*	Direct access is enabled. DSA_M can be toggled between I_L and prior programmed value x dB (set via register 0x16h) by pin 9.
			1	Direct access is disabled. DSA can be set via register 0x11h.
0	SPI_LEVEL	R/W	Sets the V_{OH} voltage to be used by SPI	
			0*	V_{OH} = 1.8 V
			1	V_{OH} = 3.3 V

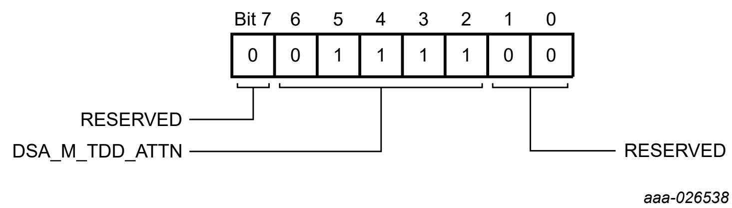


Figure 19. Register address 0x16h

Table 22. Register address 0×16h

*Legend: * reset value*

Bits	Name	Access	Value	Description
7	RESERVED	R/W	Reserved bit. Shall be kept LOW	
			0*	
6-2	DSA_M_TDD_ATTN	R/W	Main channel DSA attenuation level for direct-access mode in TDD systems. Attenuation is toggled by pin 9	
			00000	Minimum Attenuation, equal to I_L
			00001	I_L + 1 dB Attenuation
			01111*	I_L + 15 dB Attenuation
			...	

Bits	Name	Access	Value	Description
			11111	I_L + 31 dB Attenuation
1-0	RESERVED	R/W	Reserved bits. Shall be kept LOW	
			0*	

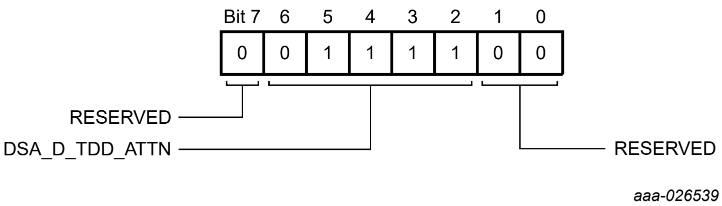


Figure 20. Register address 0x17h

Table 23. Register address 0×17h

*Legend: * reset value*

Bits	Name	Access	Value	Description
7	RESERVED	R/W	Reserved bit. Shall be kept LOW	
			0*	
6-2	DSA_D_TDD_ATTN	R/W	Diversity channel DSA attenuation level for direct-access mode in TDD systems. Attenuation is toggled by pin 23	
			00000	Minimum Attenuation, equal to I_L
			00001	I_L + 1 dB Attenuation
			01111*	I_L + 15 dB Attenuation
			...	
			11111	I_L + 31 dB Attenuation
1-0	RESERVED	R/W	Reserved bits. Shall be kept LOW	
			0*	

8.3 Device Functionality

The BGU8821/A supports both main and diversity receiver channels in both TDD and FDD systems. It has a first stage LNA optimized for sensitivity followed by a digital step attenuator and output stage amplifier. The first stage LNA output is routed outside the device, so there is a possibility to use the device in different system configurations (e.g. connect frequency selective filters in-between output of the first stage LNA and DSA input, refer to Functional Diagram in Section 6).

Main and Diversity channels are controlled separately, via addressing different registers in device's memory. LNAs can be set in power-down mode to save current consumption depending on system configuration (address 0x10h, refer to Table 18).

Attenuation levels of DSAs can be set with steps of 1 dB and total range of 31 dB. Attenuation can be written to the address 0x11h for Main channel (Table 19) and the address 0x12h for Diversity channel (Table 20).

To support highly integrated solutions and reduce platform costs a standalone SPDT switch is included. Switch is controlled at address 0x13h (refer to Table 21).

All RF inputs and outputs are single-ended and matched to 50 Ω (external matching components may be required, refer to Application information in Section 14). The BGU8821/A is controlled via SPI bus, supporting both 3- and 4-wire configurations. Full description of SPI interface is provided in Section 8.2. In TDD systems, the LNAs and DSA can also be controlled via direct-access pins. The direct-access functionality is described in Section 8.1.

9 Limiting values

Table 24. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	for all supply pins	-	6	V
$P_{i(RF)CW}$	continuous waveform RF input power	for 2 hrs all RF input pins	-	20	dBm
		at SPDT ports for 2 hrs		30	dBm
T_{stg}	storage temperature		-40	+150	°C
T_j	junction temperature		-	150	°C
P	power dissipation	T_{case} ≤ 105 °C [1]	-	1.7	W
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) [2]	-	1.0	kV
		Charged Device Model (CDM) [3]	-	0.5	kV

[1] Case is ground solder pad.
[2] According to ANSI/ESDA/JEDEC standard JS-001-2010. For pins 2, 11 (RFIN_M, RFIN_D) limiting value is 1 kV, for all other pins limiting value is 2 kV
[3] According to JEDEC standard 22-C101B.

10 Recommended operating conditions

Table 25. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.75	5	5.25	V
Z_0	characteristic impedance		-	50	-	Ω
T_{case}	case temperature		-40	-	+105	°C

11 Thermal characteristics

Table 26. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	junction to case thermal resistance	Soldered on NXP evaluation board, T_{amb} = 95 °C [1] [2]	29	K/W

[1] Based on simulation, T_{case} = 105 °C under the mentioned conditions. Case is the center ground solder pad.
[2] Thermal resistance measured using on die thermal sensing diodes.

12 Characteristics

Table 27. Characteristics BGU8821/A LNA1 for Main and Diversity Channel

f = 900 MHz; V_{CC} = 5 V; T_{amb} = 25 °C; input and output 50 Ω; unless otherwise specified. All RF parameters are measured in an application board as shown in Figure 44 with components listed in Table 33 optimized for f = 900 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	LNA1 Enable	-	54	64	mA
		Disable	-	3	-	mA
G_p	power gain	[1]	15.9	19	-	dB
NF	noise figure	At room temperature [1]	-	0.6	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression	[1]	17.9	21	-	dBm
$IP3_O$	output third-order intercept point	2-tone; tone spacing = 1 MHz; P_i = -15 dBm per tone [1]	34	38	-	dBm
RL_{in}	input return loss		-	17	-	dB
RL_{out}	output return loss		-	14	-	dB
$t_{s(pon)}$	power-on settling time	Matched conditions; after SPI last raising clock edge and RF amplitude output 10 % to 90 % of steady state	-	530	-	ns
$t_{s(poff)}$	power-off settling time	Matched conditions; after SPI last raising clock edge and RF amplitude output 90 % to 10 % of steady state	-	15	-	ns
K	Rollett stability factor	up to f = 20 GHz	1	-	-	-

[1] Connector and Printed-Circuit Board (PCB) losses have been de-embedded for all RF parameters.

Table 28. Characteristics BGU8821/A DSA+LNA2 for Main and Diversity

f = 900 MHz; V_{CC} = 5 V; T_{amb} = 25 °C; input and output 50 Ω; unless otherwise specified. All RF parameters are measured in an application board as shown in Figure 44 with components listed in Table 33 optimized for f = 900 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	DSA + LNA2 Enable	-	57	67	mA
		Disable	-	5	-	mA
G_p	power gain	[1]	14.5	18	-	dB
NF	noise figure	[1]	-	1.6	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression	[1]	18	22	-	dBm
$IP3_O$	output third-order intercept point	2-tone; tone spacing = 1 MHz; P_i = -15 dBm per tone [1]	34	39	-	dBm
RL_{in}	input return loss	Over all attenuator settings	-	15	-	dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RL_{out}	output return loss	Over all attenuator settings	-	16	-	dB
$t_{s(pon)}$	power-on settling time	Matched conditions; after SPI last raising clock edge and RF amplitude output 10 % to 90 % of steady state	-	530	-	ns
$t_{s(poff)}$	power-off settling time	Matched conditions; after SPI last raising clock edge and RF amplitude output 90 % to 10 % of steady state	-	15	-	ns
G_{range}	gain range	Digital step attenuator gain	-	31	-	dB
G_{step}	gain step	DSA gain step	-	1	-	dB
ΔG	gain variation	DSA gain variation over attenuation setting	- (0.3 + 5 % Att)	-	(0.3 + 5 % Att)	dB
$t_{resp(\alpha)}$	attenuation response time	LNA enable; RF amplitude output 10 % delta attenuation to 90 % delta attenuation of steady state with max.0.5 dB overshoot	-	50	-	ns

[1] Connector and Printed-Circuit Board (PCB) losses have been de-embedded for all RF parameters.

Table 29. Characteristics SPDT RF switch

f = 900 MHz; V_{CC} = 5 V; T_{amb} = 25 °C; input and output 50 Ω; unless otherwise specified. All RF parameters are measured in an application board as shown in Figure 44 with components listed in Table 33 optimized for f = 900 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	SPDT Supply voltage	-	2.1	-	mA
α_{ins}	insertion loss	[1]	-	1.3	1.6	dB
$P_{i(1dB)}$	input power at 1 dB gain compression		-	35	-	dBm
$IP3_i$	input third-order intercept point	2-tone; tone spacing = 1 MHz; P_i = +5 dBm per tone	-	54	-	dBm
RL_{in}	input return loss	port SW_RF1	-	17	-	dB
RL_{out}	output return loss	port SW_RF2	-	17	-	dB
RL_{out}	output return loss	port SW_RFC	-	17	-	dB
$t_{d(QV)}$	data output valid delay time	From last, SPI data bit is clocked in to 10 % of RF output steady state (pin 28), ON state	-	725	-	ns
		From last, SPI data bit is clocked in to 10 % of RF output steady state (pin 28), OFF state	-	50	-	ns
ISL	isolation	SPDT port	-	51	-	dB

[1] Connector and Printed-Circuit Board (PCB) losses have been de-embedded for all RF parameters.

Table 30. Characteristics BGU8821/A port isolation of IC

f = 900 MHz; V_{CC} = 5 V; T_{amb} = 25 °C; input and output 50 Ω; unless otherwise specified. All RF parameters are measured in an application board as shown in Figure 44 with components listed in Table 33 optimized for f = 900 MHz. Guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\alpha_{isol(ch\text{-}ch)}$	isolation between channels	Isolation from LNA1 output main (pin 42) to DSAM (pin 39) input in the main channel. Likewise for diversity (pin 15) to (pin 18)	-	68	-	dB
		Isolation for LNA2D (pin 32) output to LNA1M (pin 9) input in the cross channel. Likewise pin(24) to pin (2)	-	80	-	dB
		Isolation between main and diversity channels at input (pin 2 and pin 9)	-	50	-	dB
		Isolation between LNA2 main and diversity output to SW_RF ports	-	56	-	dB

Table 31. Characteristics BGU8821/A logical inputs/outputs

V_{DD} = 5 V; Typical values at T_{amb} = 25 °C; Output load 30 pF.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(SPI)}$	SPI supply voltage		4.75	5	5.25	V
$I_{DD(SPI)}$	SPI supply current	pin 34	-	-	10	mA
V_{IL}	LOW-level input voltage		-0.3	-	0.4	V
V_{IH}	HIGH-level input voltage	1.8 V mode	1.2	1.8	3.6	V
		3.3 V mode	2.6	3.3	3.6	V
		for pin 24 and 32	-	-	2.75	V
V_{OL}	LOW-level output voltage	SPI (SDO, SDIO, and GPO); for all digital pins	0	-	0.4	V
V_{OH}	HIGH-level output voltage	SPI (SDO, SDIO, and GPO); for all digital pins and 3.3 V tolerant programmable by register 0×13h bit [0]"0" = 1.8 V default "1" = 3.3 V	1.4	1.8	2.1	V
I_{IL}	LOW-level input current	V_{IL}= 0 V	-150	-	150	µA
I_{IH}	HIGH-level input current	V_{IH}= 1.8 V	-150	-	150	µA
I_{OL}	LOW-level output current	for all digital output pins (incl. GPO); Current sourcing from 1.8 V	+4	-	-	mA
I_{OH}	HIGH-level output current	for all digital output pins (incl. GPO); Current sinking to ground	-	-	-4	mA
I_{LO}	output leakage current	3-state output leakage for all logic levels	-87	-	30	µA

Table 32. Characteristics BGU8821/A SPI timing

V_{DD} = 5 V; Typical values at T_{amb} = 25 °C; Output load 30 pF. Guaranteed by design.

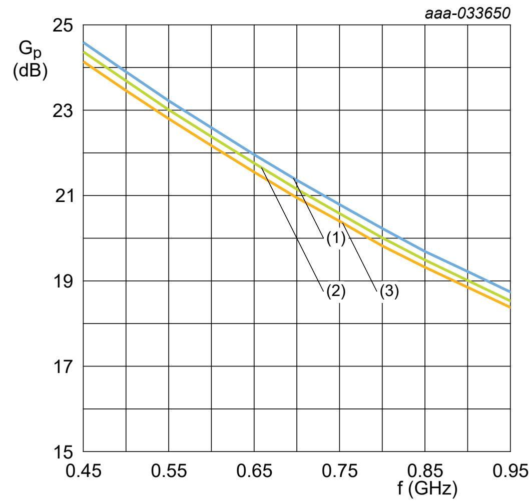
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{su(SDIO)}$	SDIO set-up time	Serial data IO setup to serial CLK rising edge setup time		-	5	-	ns
$t_{h(SDIO)}$	SDIO hold time	Serial CLK rising edge to serial data IO hold time		-	3	-	ns
t_{SCLKH}	SCLK HIGH time	Logic "High" time of Serial SPI clock		-	27	-	ns
t_{SCLKL}	SCLK LOW time	Logic "Low" time of Serial SPI clock		-	29	-	ns
t_s	settling time	CSB falling edge to serial CLK rising edge setup time		-	4.1	-	ns
				-	3.0	-	ns
$t_{d(DV)}$	data input valid delay time	Serial CLK falling edge to validate data in SDIO/SDO time: To V_{IH}, V_{IL} or 3-state level		-	16	-	ns
T_{clk}	clock period	SPI SCLK rising edge to rising edge at write mode	[1]	40	-	-	ns

[1] t_{dv}: in case of slave writes to master T_{clk} 60 ns max.

13 Graphics

All plots are created based on the measurements of a typical sample.

13.1 LNA1 primary frequencies



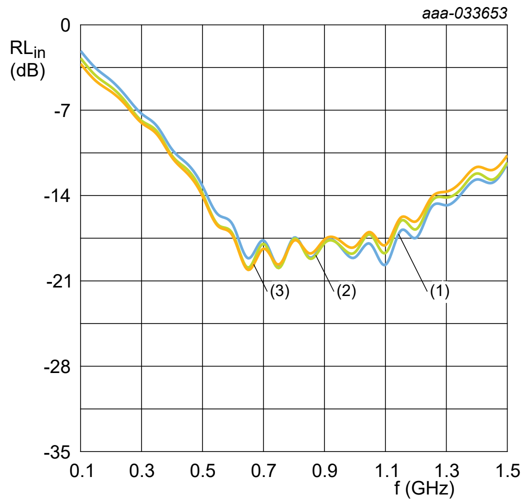
V_{DD}= 5 V; Matched for 700 MHz - 1000 MHz

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 21. LNA1_M&D Power gain as a function of frequency, typical values



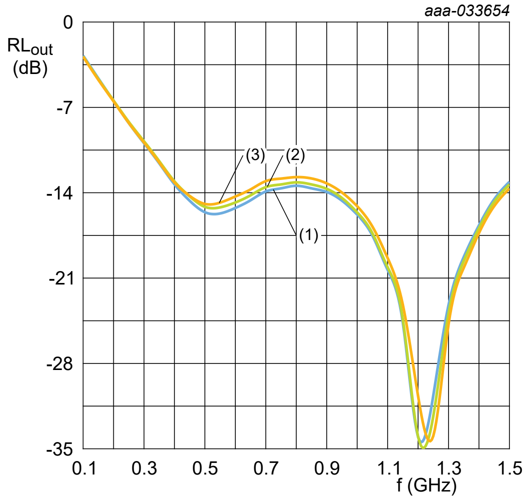
V_{DD}= 5 V; Matched for 700 MHz - 1000 MHz

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

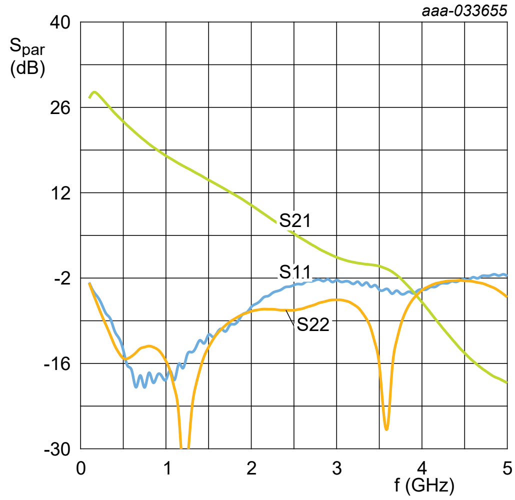
(3) T_{amb}= +95 °C

Figure 22. LNA1_M&D Input return loss as a function of frequency, typical values



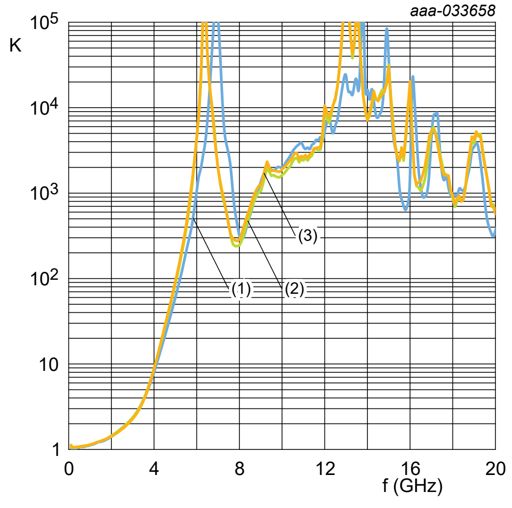
V_{DD}= 5 V; Matched for 700 MHz - 1000 MHz
(1) T_{amb}= -40 °C
(2) T_{amb}= +25 °C
(3) T_{amb}= +95 °C

Figure 23. LNA1_M&D Output return loss as a function of frequency, typical values



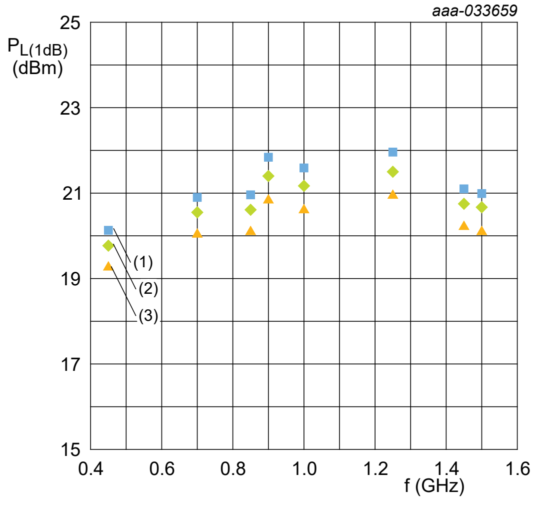
V_{DD}= 5 V; T_{amb}= +25 °C; Matched for 700 MHz - 1000 MHz

Figure 24. LNA1_M&D S-parameters as a function of frequency, typical values



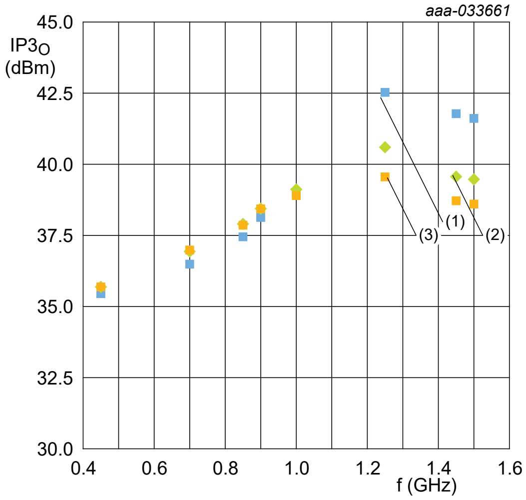
V_{DD}= 5 V; Matched for 700 MHz - 1000 MHz
(1) T_{amb}= -40 °C
(2) T_{amb}= +25 °C
(3) T_{amb}= +95 °C

Figure 25. LNA1_M&D Rollett stability factor as a function of frequency, typical values



V_{DD}= 5 V; Matched for 700 MHz - 1000 MHz
(1) T_{amb}= -40 °C
(2) T_{amb}= +25 °C
(3) T_{amb}= +95 °C

Figure 26. LNA1_M&D Output 1 dB compression point, typical values



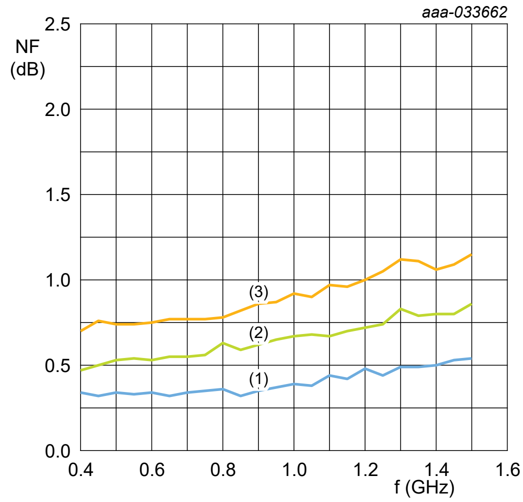
V_{DD}= 5 V; Output tone power +5 dBm; Delta frequency 1 MHz; Matched for 700 MHz - 1000 MHz

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 27. LNA1_M&D Output third-order intercept point, typical values



V_{DD}= 5 V; Matched for 700 MHz - 1000 MHz

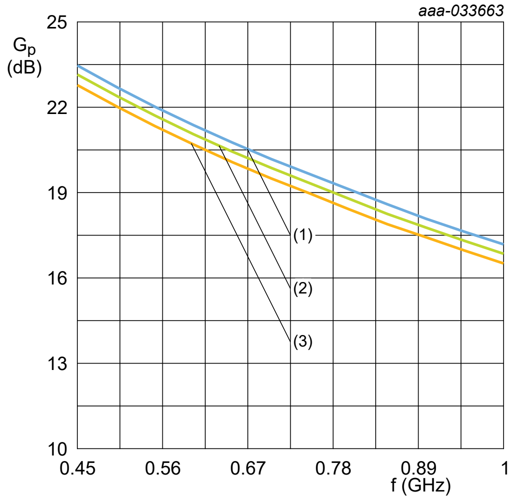
(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 28. LNA1_M&D Noise figure as a function of frequency, typical values

13.2 DSA + LNA2



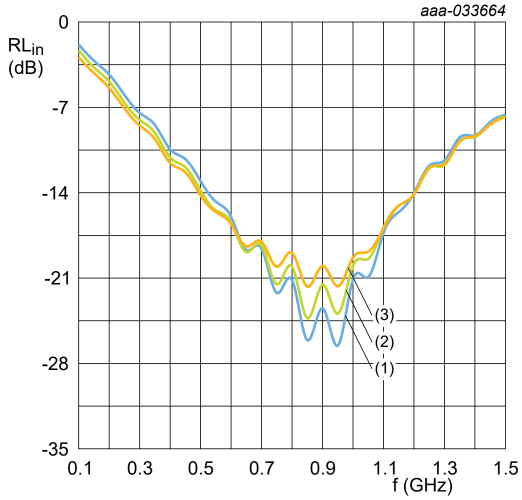
V_{DD}= 5 V; 0 dB attenuation; Matched for 700 MHz - 1000 MHz

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 29. DSA+LNA2 M&D Power gain as a function of frequency, typical values



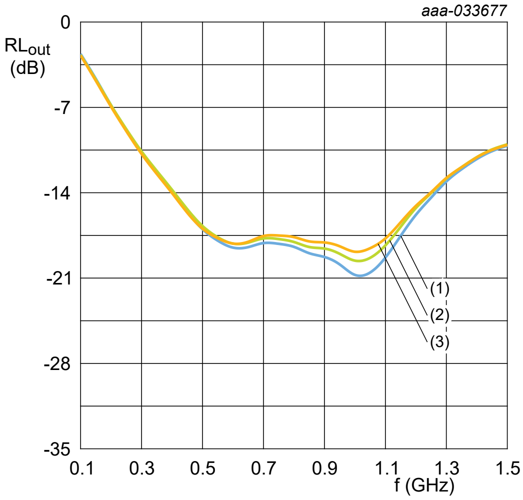
V_{DD}= 5 V; 0 dB attenuation; Matched for 700 MHz - 1000 MHz

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 30. DSA+LNA2 M&D Input return loss as a function of frequency, typical values



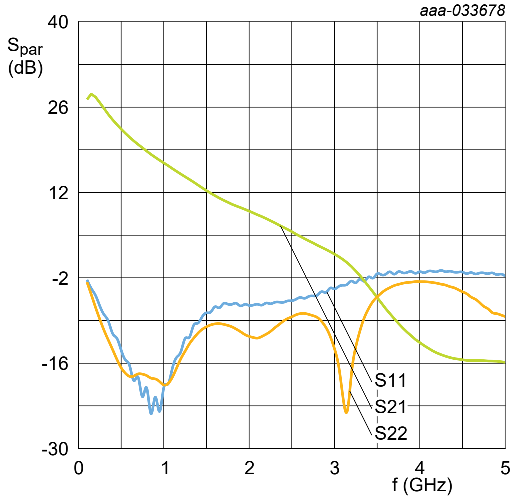
V_{DD}= 5 V; 0 dB attenuation; Matched for 700 MHz - 1000 MHz

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

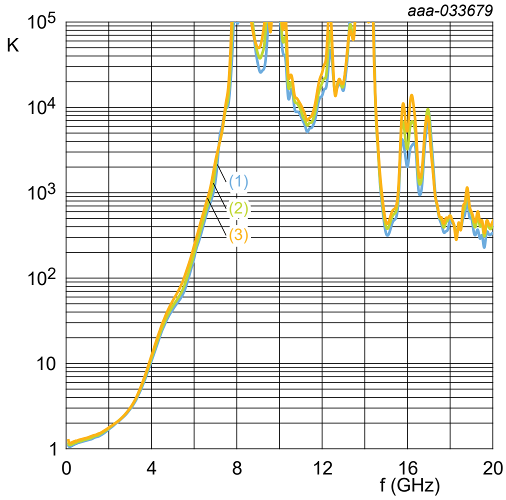
(3) T_{amb}= +95 °C

Figure 31. DSA+LNA2 M&D Output return loss as a function of frequency, typical values.



V_{DD}= 5 V; T_{amb}=-25 °C; 0 dB attenuation; Matched for 700 MHz - 1000 MHz

Figure 32. DSA+LNA2 M&D S-parameters as a function of frequency, typical values



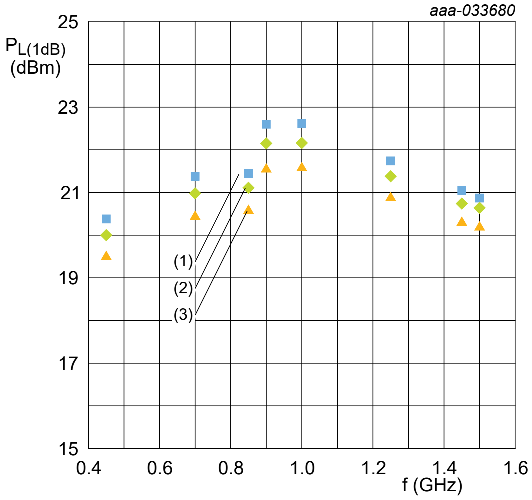
V_{DD}= 5 V; 0 dB attenuation; Matched for 700 MHz - 1000 MHz

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 33. DSA+LNA2 M&D Rollett stability factor as a function of frequency, typical values



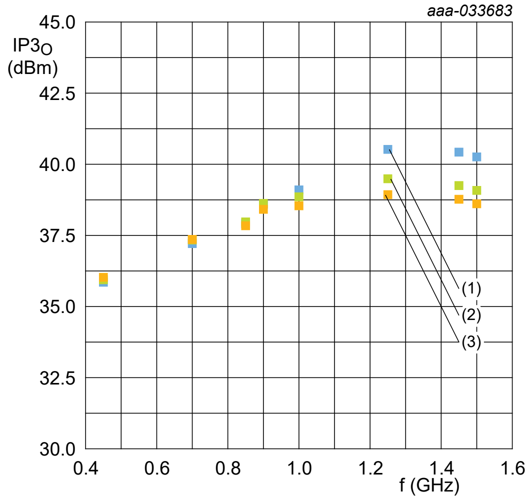
V_{DD}= 5 V; 0 dB attenuation; Matched for 700 MHz - 1000 MHz

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 34. DSA+LNA2 M&D Output 1 dB compression point as a function of frequency, typical values



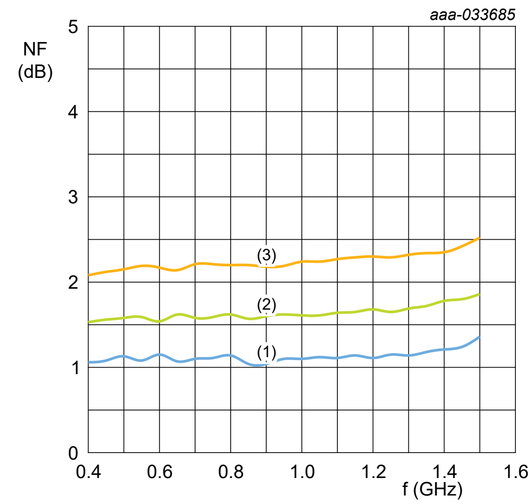
V_{DD}= 5 V; Output tone power + 5 dBm delta frequency 1 MHz; 0 dB attenuation; Matched for 700 MHz - 1000 MHz

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 35. DSA+LNA2 M&D Output third-order intercept point as a function of frequency, typical values



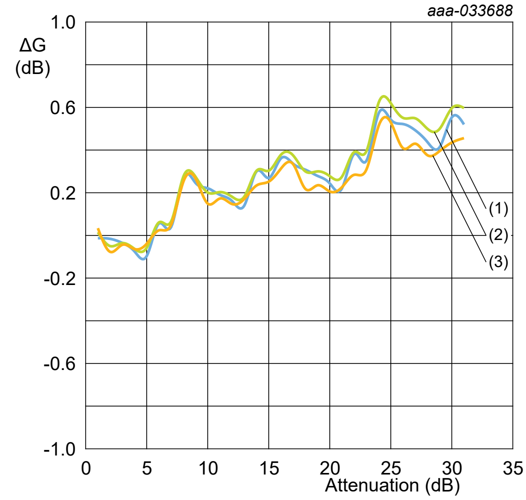
V_{DD}= 5 V; 0 dB attenuation; Matched for 700 MHz - 1000 MHz

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 36. DSA+LNA2 M&D Noise figure as a function of frequency, typical values



V_{DD}= 5 V; f = 900 MHz

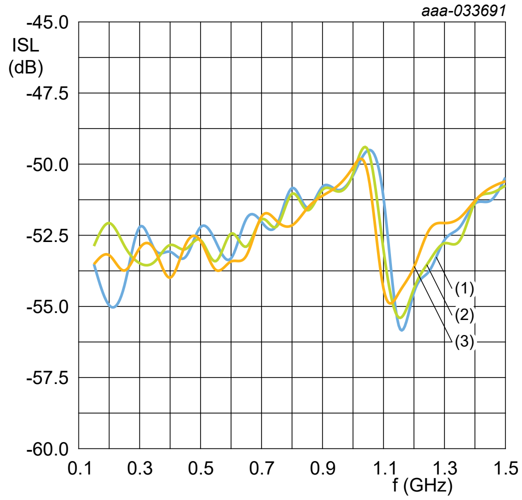
(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 37. DSA+LNA2_M&D DSA gain variation versus attenuation step

13.3 SPDT



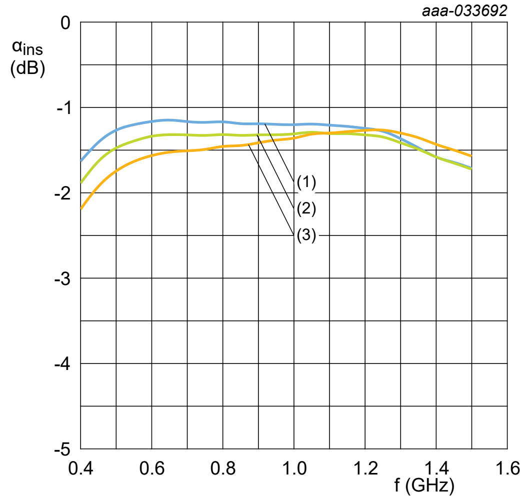
V_{DD}= 5 V

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 38. RFin_M to RFin_D channel isolation



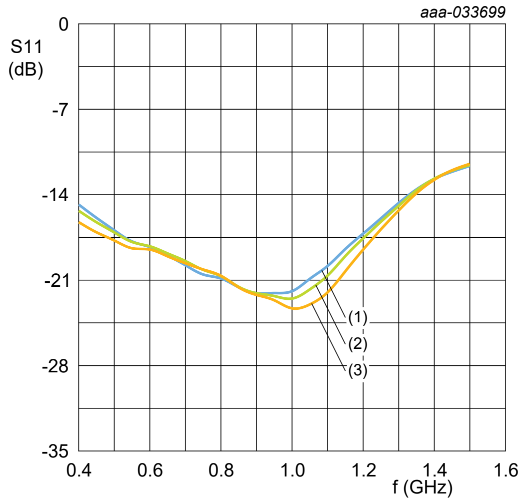
V_{DD}= 5 V

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 39. Insertion loss SWRF1/2 to SWRFC as function of frequency, typical values



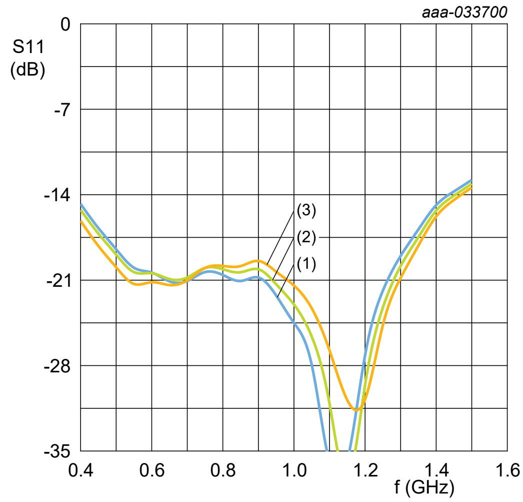
V_{DD}= 5 V

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 40. S11 of SWRFC when switched to SWRF1/2 as function of frequency, typical values



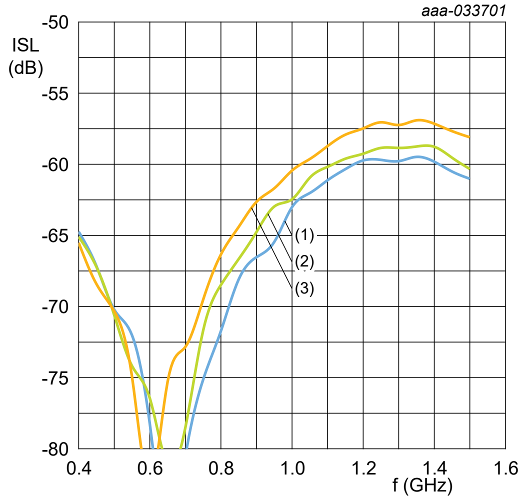
V_{DD}= 5 V

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 41. S11 of SWRF1/2 when switched to SWRFC as function of frequency, typical values



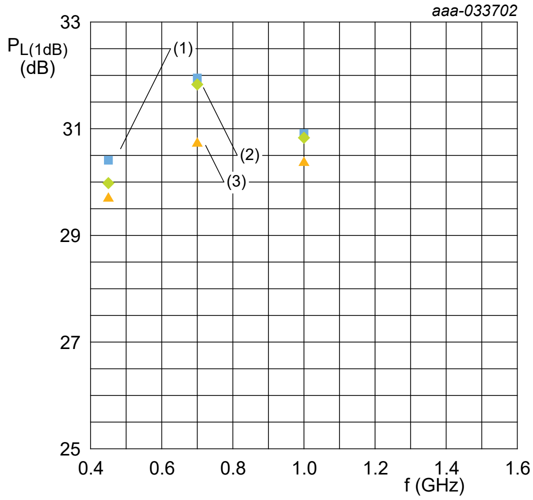
V_{DD}= 5 V

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 42. SPDT isolation SWRF1 to SWRF2 as function of frequency, typical values



V_{DD}= 5 V

(1) T_{amb}= -40 °C

(2) T_{amb}= +25 °C

(3) T_{amb}= +95 °C

Figure 43. SPDT 1 dB compression point as function of frequency, typical values

14 Application information

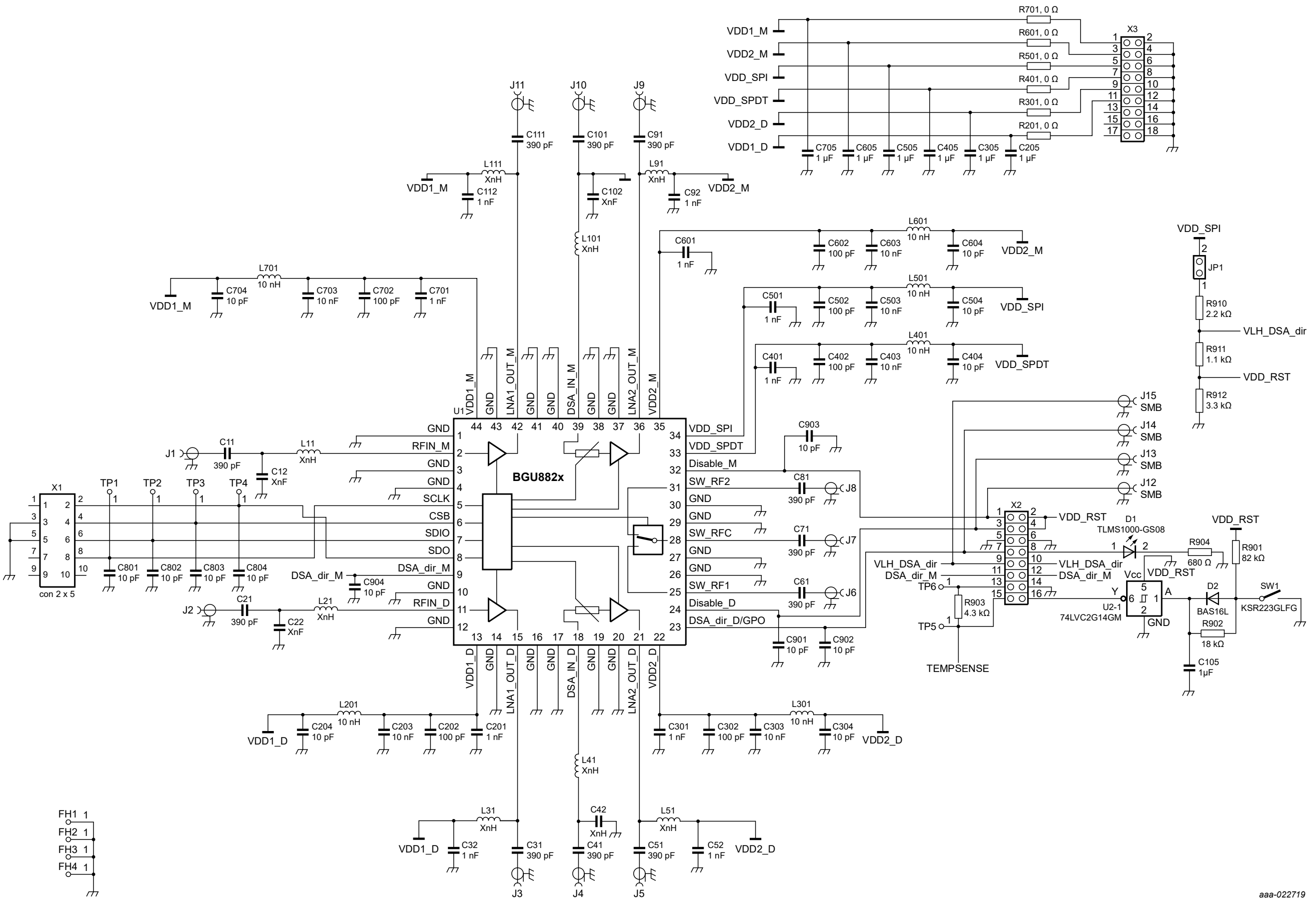


Figure 44. Application diagram

Table 33. List of components

Component	Designation	Value	Manufacturer	Quantity
C12, C22	GJM1554C1H1R8BB01 +/- 0.1 pF	1.8 pF	Murata	2
C42, C102,	GJM1554C1H1R1WB01 +/-0.05 pF	1.1 pF	Murata	2
C11, C21, C31, C41, C51, C61, C71, C81, C91, C101, C111	GRM1555C1E391JA01	390 pF	Murata	11
C105, C205, C305, C405, C505, C605, C705	GRM188R71E105KA	1 μF	Murata	7
C32, C52, C92, C112, C201, C301, C401, C501, C601, C701	GRM1555CH101JA01D	1 nF	Murata	10
C202, C302, C402, C502, C602, C702	GRM155R71H102KA01D	100 pF	Murata	6
C203, C303, C403, C503, C603, C703	GRM155R71H103KA88D	10 nF	Murata	6
C204, C304, C404, C504, C604, C704, C801, C802, C803, C804, C901, C902	GRM1555C1H100JA01D	10 pF	Murata	13
D1	TLMS1000-GS08	1328308	FARNELL	1
D1	BAS16L	BAS16L	NXP	1
J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11	Connector SMA142-0701-841		FARNELL	11
L11, L21	LQP15MN1N8W02D +/- 0.1.nH	3.9 nH	Murata	4
L41, L101	LQW15AN1N5B00D +/- 0.1 nH	4.7 nH	Murata	2
L31, L51, L91, L111	LQG15HH33NG02 2 %	33 nH	Murata	4
L201, L301, L401, L501, L601, L701	LQW15AN10NJ00	10 nH	Murata	2
R904	402	680 R	Murata	6
R201, R301, R401, R501, R601, R701	402	0 R		1
R901	402	82k		6
R902	402	18k		1
R903	402	4k3		1
R910	402	2.2k		1
R911	402	1.1k		1
R912	402	3.3k		1
SW1	KSR223GLFG	2320064	FARNELL	1
U1	BGU8821/A		NXP	1

Component	Designation	Value	Manufacturer	Quantity
U2	74LVC2G14GM		NXP	1
X1	WIRE-BOARD CONNECTOR, HEADER 10POS, 2MM	1835819	FARNELL	1
X2, X3	TE CONNECTIVITY / AMP-4-103322-2-BARETTE SECABLE DOUBLE	1098460	FARNELL	1
TP1, TP2, TP3, TP4, TP5, TP6	3 points HEADER, VERTICAL, pitch 2.54 mm	5217805	FARNELL	1

Table 34. Typical performance BGU8821/A LNA1_M/D application board V_{CC} = 5 V

All RF parameters are measured at the application board as shown in Figure 44 with the components as listed in Table 33 optimized for: f = 700 MHz to 1000 MHz, V_{CC} = 5 V, T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Frequency					Unit
				450	700	850	900	1000	MHz
G	gain		[1]	24.4	21.2	19.5	19.0	18.1	dB
RL_{in}	input return loss			11.6	19.1	19.3	18.1	18.2	dB
RL_{out}	output return loss			14.1	15.0	13.9	13.9	15.2	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		[1]	19.6	20.4	20.4	21.3	21.0	dBm
$IP3_O$	output third-order intercept point	Δf = 1 MHz	[1] [2]	35.6	36.9	37.8	38.4	39.0	dBm
NF	noise figure			0.51	0.54	0.54	0.58	0.65	dB

[1] Connector and board losses have been de-embedded.

[2] 2-Tone; tone spacing = 1 MHz; P_o = 5 dBm per tone

Table 35. Typical performance BGU8821/A DSA+LNA2_M/D application board V_{CC} = 5 V

All RF parameters are measured at the application board as shown in Figure 44 with the components as listed in Table 33 optimized for: f = 700 MHz to 1000 MHz, V_{CC} = 5 V, T_{amb} = 25 °C. DSA in minimum attenuation.

Symbol	Parameter	Conditions		Frequency					Unit
				450	700	850	900	1000	MHz
G	gain		[1]	23.2	19.9	18.3	17.8	16.8	dB
RL_{in}	input return loss			12.9	20.9	17.9	15.9	13.8	dB
RL_{out}	output return loss			14.9	16.2	16.1	16.0	15.6	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		[1]	20.0	21.3	21.2	21.8	21.8	dBm
$IP3_O$	output third-order intercept point	Δf = 1 MHz	[1] [2]	35.5	36.9	37.8	38.4	39.1	dBm
NF	noise figure		[1]	1.5	1.6	1.6	1.6	1.7	dB

[1] Connector and board losses have been de-embedded.

[2] 2-Tone; tone spacing = 1 MHz; P_o = 5 dBm per tone

Table 36. Typical performance BGU8821/A SPDT application board V_{CC} = 5 V

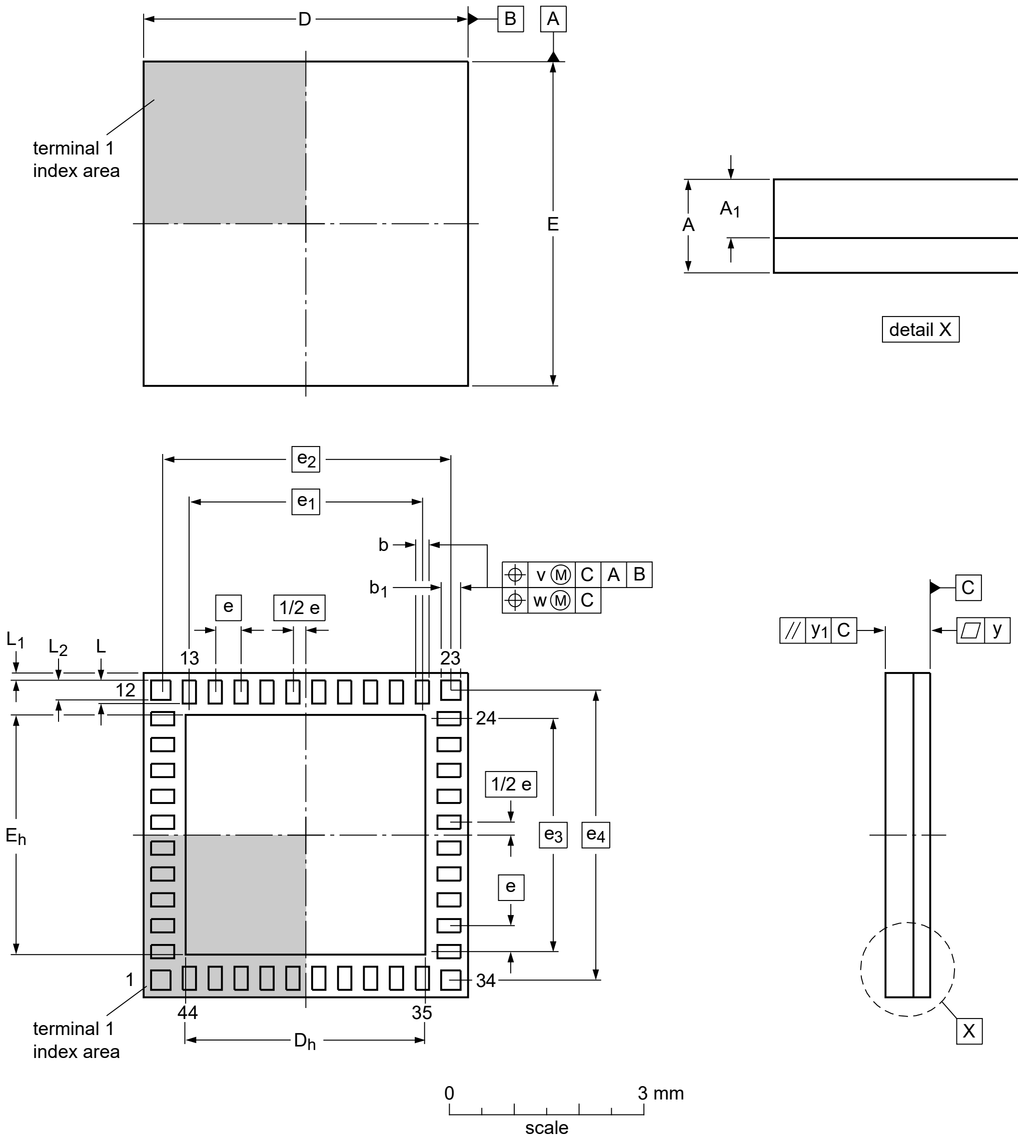
All RF parameters are measured at the application board as shown in Figure 44 with the components as listed in Table 33.

Symbol	Parameter	Conditions		Frequency					Unit
		Switch position		450	700	850	900	1000	MHz
α_{ins}	insertion loss	SWRF1/2 to SWRFC	[1]	1.5	1.2	1.3	1.3	1.2	dB
RL_{in}	input return loss	SW_RF1 to SW_RFC	[1] [2]	18.4	19.5	17.8	17.5	18.9	dB
		SW_RF2 to SW_RFC	[1] [3]	18.1	19.6	19.1	19.2	20.7	dB
RL_{out}	output return loss	SW_RF1/2 to SW_RFC	[1] [4]	16.9	19.1	19.1	19.2	20.0	dB
ISL	isolation	SW_RF1 to SW_RFC	[1] [5]	57.4	56.0	54.1	53.6	52.0	dB
		SW_RF1 to SW_RFC	[1] [6]	61.1	62.9	59.6	59.0	58.3	dB
		SW_RF2 to SW_RFC	[1] [7]	57.6	53.8	52.5	51.6	50.4	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		[1]	33.6	35.2	35.2	35.1	34.9	dBm
$IP3_O$	output third-order intercept point	Δf = 1 MHz	[8]	53.5	53.3	54.1	54.0	54.5	dBm

[1] Connector and board losses have been de-embedded.
[2] input is SW_RF1.
[3] input is SW_RF2.
[4] output is SW_RFC.
[5] Isolation from SW_RF2 to SW_RFC.
[6] Isolation from SW_RF1 to SW_RF2.
[7] Isolation from SW_RF1 to SW_RFC.
[8] 2-Tone; tone spacing = 1 MHz; P_o = 5 dBm per tone

15 Package outline

HVLGA44: plastic thermal enhanced very thin profile land grid array package; 44 terminals; SOT1431-1



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	b_1	D	D_h	E	E_h	e	e_1	e_2	e_3	e_4	L	L_1	L_2	v	w	y	y_1
mm	max	0.82	0.50	0.25	0.35	5.1	3.75	5.1	3.75						0.40	0.15	0.35				
	nom	0.72	0.45	0.20	0.30	5.0	3.70	5.0	3.70	0.4	3.6	4.5	3.6	4.5	0.35	0.10	0.30	0.15	0.05	0.08	0.1
	min	0.62	0.40	0.15	0.25	4.9	3.65	4.9	3.65						0.30	0.05	0.25				

sot1431-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1431-1		- - -				~~16-06-28~~ 16-08-12

Figure 45. HVLGA44: plastic thermal enhanced very thin profile land grid array package; no leads; 44 terminals

16 Abbreviations

Table 37. Abbreviations

Acronym	Description
CDMA	code division multiple-access
ESD	electrostatic discharge
FDD	frequency-division duplexing
GSM	global system for mobile communication
LNA	low-noise amplifier
LTE	long-term evolution
RF	radio frequency
TDD	time-division duplexing
W-CDMA	wideband code division multiple-access

17 Revision history

Table 38. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGU8821/A v.6	20200415	Product data sheet	-	BGU8821/A v.5
modification	• Security status changed from Company confidential to Public			
BGU8821/A v.5	20200409	Product data sheet	-	BGU8821/A v.4
modification	• changed the R/W into R/$\overline{W}$ for both figures in the Programming registers topic • corrected the title for figure 4			
BGU8821/A v.4	20200218	Product data sheet	-	BGU8821/A v.3
modification	• changed access value for bit 4-7 to R/W in functional register address 0x 10h • removed read-back value is always "0" • adapted the first footnote to: After reset/start-up LNAs are enabled			
BGU8821/A v.3	20190415	Product data sheet	-	BGU8821/A v.2.2
modification	• adapted and repaired the graphics • Inserted orderable part number in Ordering information table			
BGU8821/A v.2.2	20190405	Product data sheet	-	BGU8821/A v.2.1
modification	• Corrected typos in graphics			
BGU8821/A v.2.1	20181205	Product data sheet	-	BGU8821/A v.2
modification	• adapted register address 0x06h			
BGU8821/A v.2	20181129	Product data sheet	-	BGU8821/A v.1
modification	• added /A to the name of the product because of updated version			
BGU8821/A v.1	20170223	Product data sheet	-	-

18 Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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