MC68HC05T1

Technical Summary

8-Bit Microcontroller Unit

Introduction

The MC68HC05T1 is a member of Motorola's high-density, complementary metal-oxide semiconductor (HCMOS) M68HC05 Family of 8-bit microcontroller units (MCUs). The M68HC05 Family is based on the customer-specified integrated circuit (CSIC) design strategy. All MCUs in the family use the popular M68HC05 central processor unit (CPU), and the family includes a selection of subsystems, memory sizes and types, and package types.

The MC68HC05T1 is a 40-pin device based on the MC68HC05C4. The addition of a programmable on-screen display (OSD) subsystem with 1024 bytes of character ROM makes the MC68HC05T1 ideally suited for TV and VCR applications. Other on-chip resources include 320 bytes of static RAM (SRAM), 7952 bytes of ROM, a pulse-length modulation digital-to-analog (D/A) converter, an analog-to-digital (A/D) converter, and a synchronous serial input/output (I/O) port.

Refer to this technical summary for the architecture of the MC68HC05T1 and a brief description of its subsystems and memory space. For MC68HC05T1 evaluation support tools, refer to *Evaluation Products*, Motorola document number BR292/D.

Features

- Popular M68HC05 CPU
- Memory-Mapped I/O Registers
- 7952 Bytes of User ROM
- 320 Bytes of User SRAM
- 29 Bidirectional I/O Pins and One Input-Only Pin
- Synchronous Serial I/O Port (SIOP)
- Programmable On-Screen Display (OSD)
- Nine-Channel Pulse-Length Modulation D/A Converter (Mask Optional Open Drain Outputs)
- Six-bit, Single-Channel A/D Converter
- Fully Static Operation (No Minimum Clock Speed)
- On-Chip Oscillator with Crystal/Ceramic Resonator Connections
- 16-Bit Capture/Compare Timer
- Self-Check Mode
- Power-Saving STOP and WAIT Modes
- Single 5.0-Volt Power Requirement
- 8 × 8 Unsigned Multiply Instruction
- Edge-Sensitive or Edge- and Level-Sensitive Interrupt Trigger (Mask Option)
- Most Significant Bit (MSB) First or Least Significant Bit (LSB) First SIOP Data Format (Mask Option)
- Computer Operating Properly (COP) Timer (Mask Option)
- 40-Pin Dual In-Line Package (DIP)
- 44-Pin Plastic Leaded Chip Carrier (PLCC)

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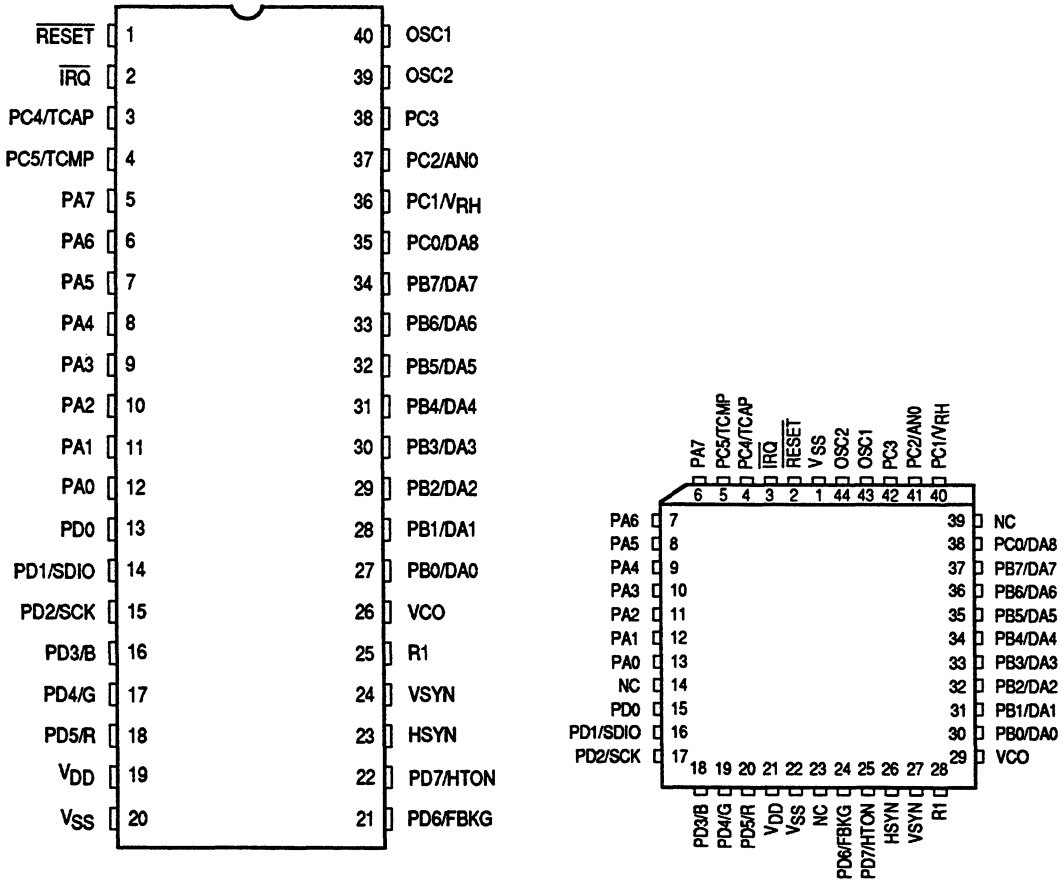
Pin Assignments

The following figures show the pin assignments of the 40-pin DIP and the 44-pin PLCC.



Pin Assignments

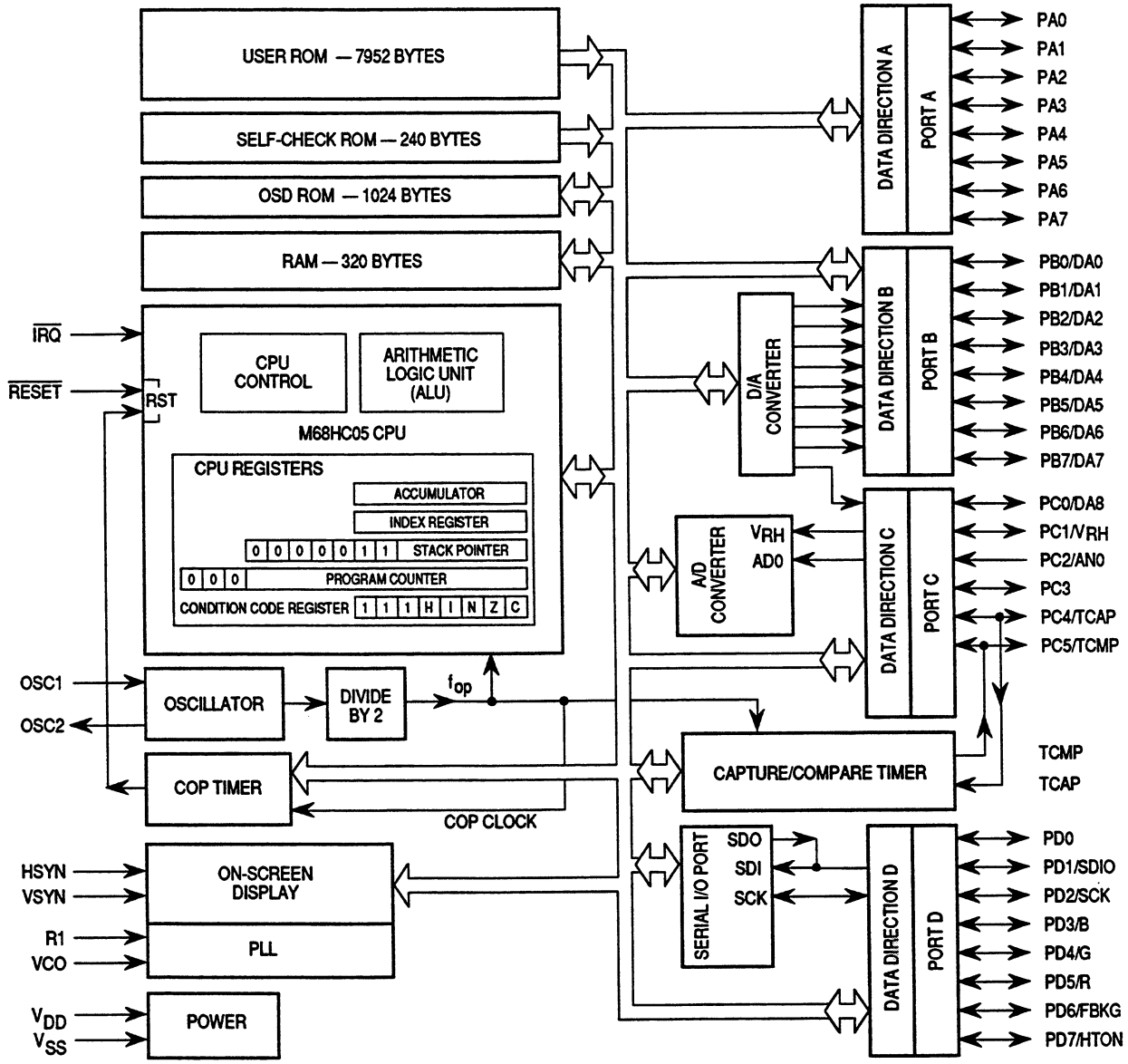
Order Numbers

Use the following numbers when ordering these package types.

Package Type	Order Number
40-Pin DIP	MC68HC05T1P
44-Pin PLCC	MC68HC05T1FN

MCU Structure

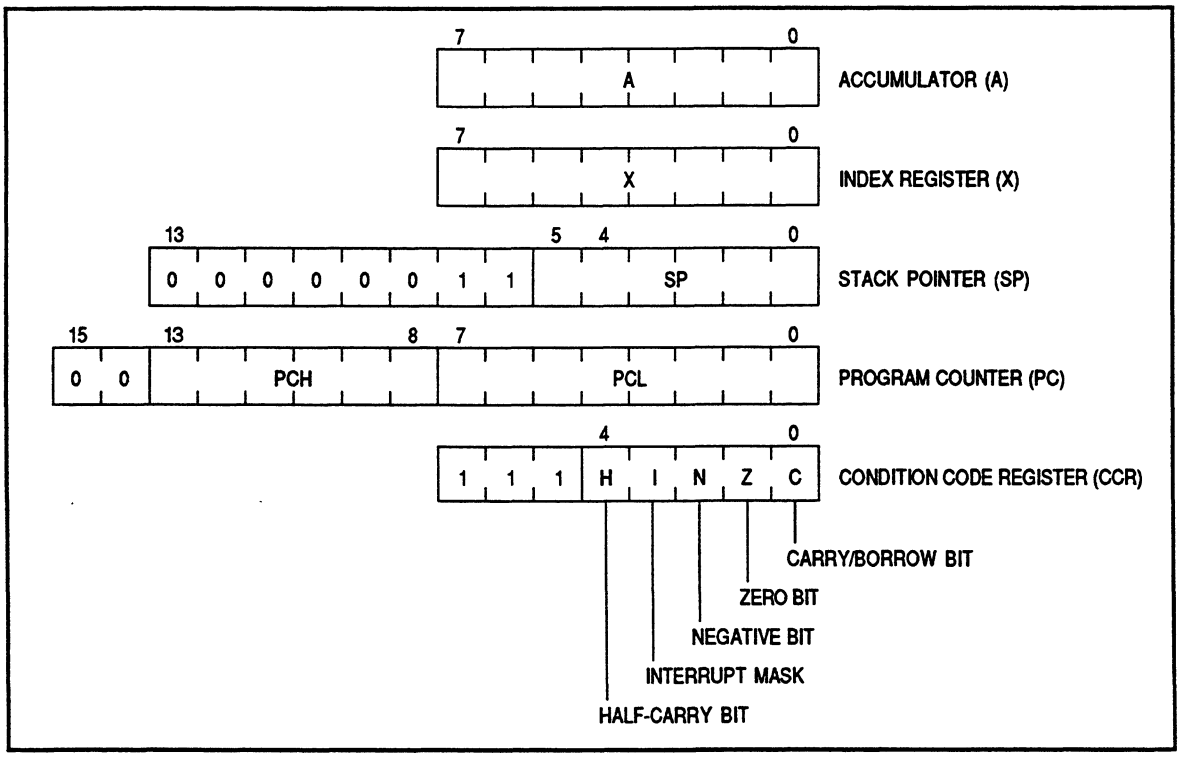
The following figure shows the organization of the MC68HC05T1.



MCU Block Diagram

Central Processor Unit Registers

Five CPU registers are available to the programmer.



CPU Registers

The 8-bit accumulator holds operands and results of arithmetic and nonarithmetic operations.

The 8-bit index register is used for indexed addressing.

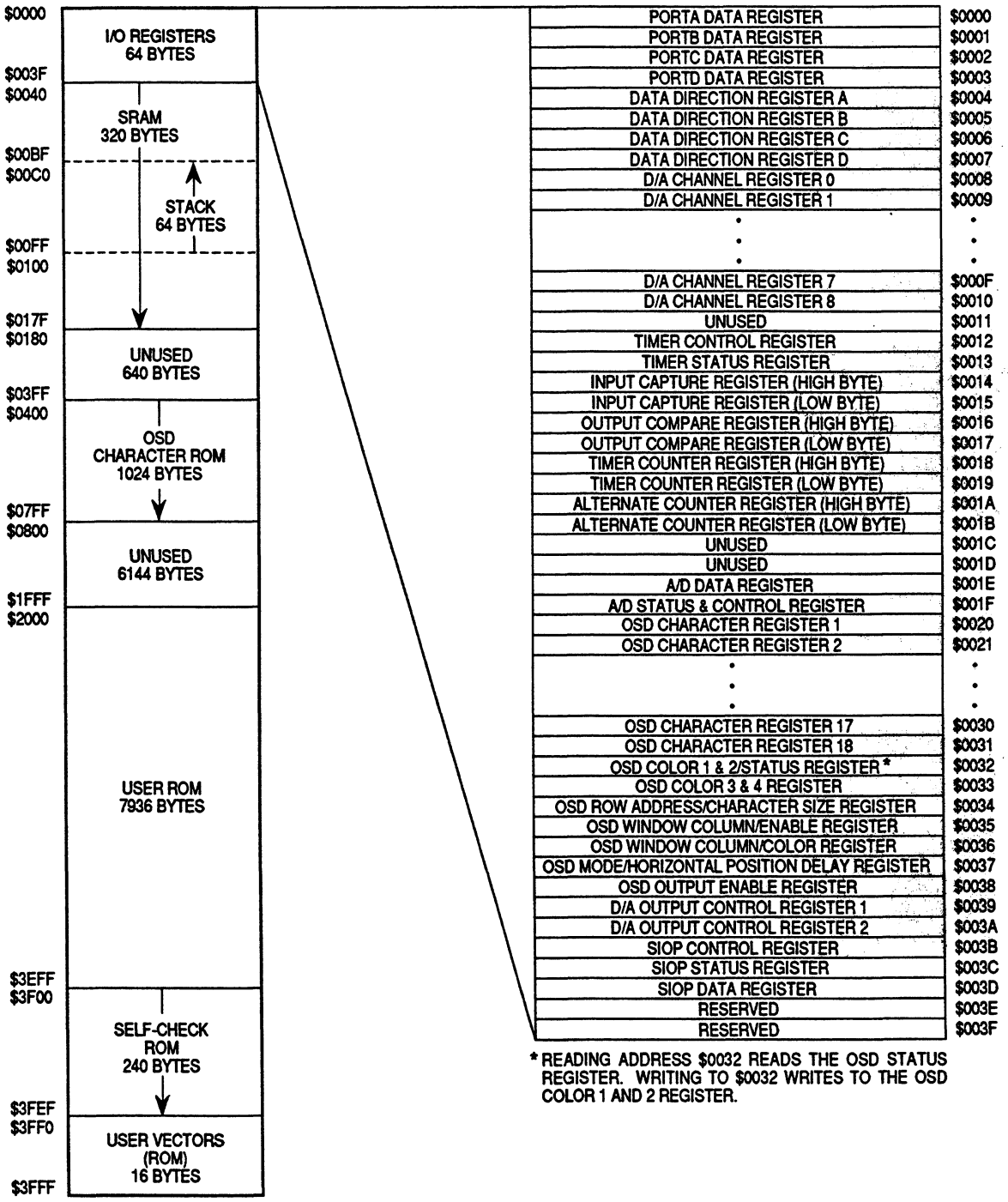
The 12-bit stack pointer contains the address of the next free location on the stack.

The 13-bit program counter contains the address of the next byte to be fetched.

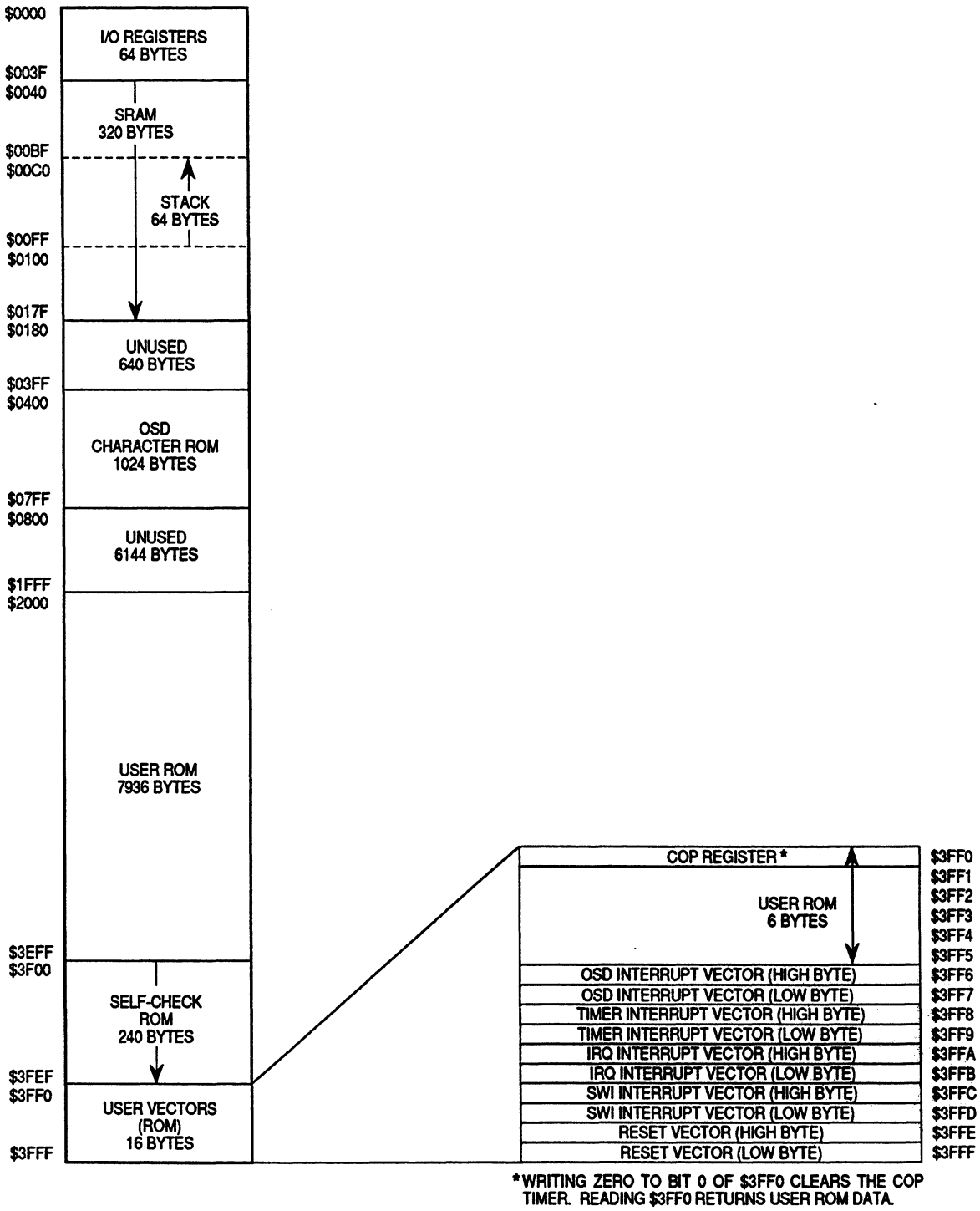
The 5-bit condition code register has four bits that indicate the results of the instruction just executed. A fifth bit is the interrupt mask.

Memory Map

The MC68HC05T1 can address 16K bytes of memory space. The following figures show the organization of the on-chip memory.



Memory Map



Memory Map (Continued)

$0000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$0001	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$0002	0	0	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$0004	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0	DDRA
$0005	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRA0	DDRB
$0006	0	0	DDRC5	DDRC4	DDRC3	1	DDRC1	DDRC0	DDRC
$0007	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0	DDRD
$0008	0	0	DA5	DA4	DA3	DA2	DA1	DA0	DAC0
$0009	0	0	DA5	DA4	DA3	DA2	DA1	DA0	DAC1
$000A	0	0	DA5	DA4	DA3	DA2	DA1	DA0	DAC2
$000B	0	0	DA5	DA4	DA3	DA2	DA1	DA0	DAC3
$000C	0	0	DA5	DA4	DA3	DA2	DA1	DA0	DAC4
$000D	0	0	DA5	DA4	DA3	DA2	DA1	DA0	DAC5
$000E	0	0	DA5	DA4	DA3	DA2	DA1	DA0	DAC6
$000F	0	0	DA5	DA4	DA3	DA2	DA1	DA0	DAC7
$0010	0	0	DA5	DA4	DA3	DA2	DA1	DA0	DAC8
$0011	—	—	—	—	—	—	—	—	UNUSED
$0012	ICIE	OCIE	TOIE	0	0	COE	IEDG	OLVL	TCR
$0013	ICF	OCF	TOF	0	0	0	0	0	TSR
$0014	Bit 15	14	13	12	11	10	9	Bit 8	ICR (HIGH)
$0015	Bit 7	6	5	4	3	2	1	Bit 0	ICR (LOW)
$0016	Bit 15	14	13	12	11	10	9	Bit 8	OCR (HIGH)
$0017	Bit 7	6	5	4	3	2	1	Bit 0	OCR (LOW)
$0018	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (HIGH)
$0019	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (LOW)
$001A	Bit 15	14	13	12	11	10	9	Bit 8	ALTCNT (HIGH)
$001B	Bit 7	6	5	4	3	2	1	Bit 0	ALTCNT (LOW)
$001C	—	—	—	—	—	—	—	—	UNUSED
$001D	—	—	—	—	—	—	—	—	UNUSED
$001E	Bit 7	6	5	4	3	2	1	Bit 0	ADRR
$001F	—	0	0	0	CH1	CH0	COCO	ADON	ADSCR

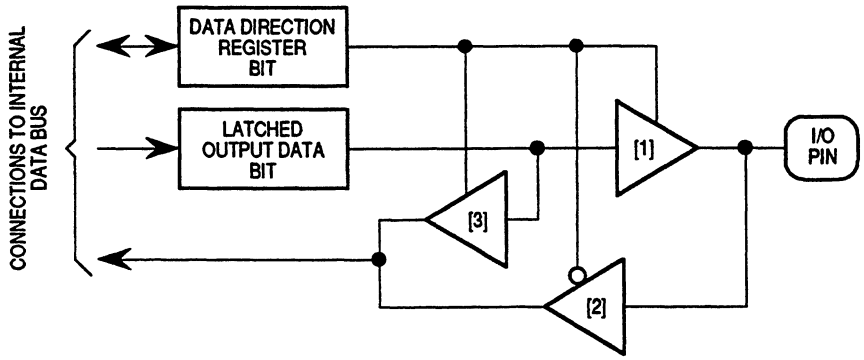
I/O Registers

$0020	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR1
$0021	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR2
$0022	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR3
$0023	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR4
$0024	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR5
$0025	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR6
$0026	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR7
$0027	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR8
$0028	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR9
$0029	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR10
$002A	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR11
$002B	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR12
$002C	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR13
$002D	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR14
$002E	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR15
$002F	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR16
$0030	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR17
$0031	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0	OSDCR18
$0032	1	1	1	1	VSYN	1	HSYN	OSDFL	OSDC12/SR (READ)
$0032	BOE	—	R2	G2	B2	R1	G1	B1	OSDC12/SR (WRITE)
$0033	—	—	R4	G4	B4	R3	G3	B3	OSDC34R
$0034	CHWS	CHHS	INV	OIEN	RA3	RA2	RA1	RA0	OSDRA/CSR
$0035	WINEN	OSDEN	PLLEN	WB4	WB3	WB2	WB1	WB0	OSDWC/ER
$0036	R	G	B	WE4	WE3	WE2	WE1	WE0	OSDWC/CR
$0037	MODE	SFG2	SFG1	HD4	HD3	HD2	HD1	HD0	OSDM/HPDR
$0038	HTON	FBKG	R	G	B	—	—	—	OSDOER
$0039	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	DACOC0
$003A	0	0	0	0	0	0	0	DA8	DACOC1
$003B	0	SPE	TR	MSTR	0	0	F1	F0	SCR
$003C	SPIF	DCOL	0	0	0	0	0	0	SSR
$003D	Bit 7	6	5	4	3	2	1	Bit 0	SDR
$003E	—	—	—	—	—	—	—	—	RESERVED
$003F	—	—	—	—	—	—	—	—	RESERVED

I/O Registers (Continued)

I/O Port Registers

The MC68HC05T1 has 29 I/O pins and one input-only pin. The contents of the data direction registers (DDRs) determine whether each I/O pin is an input or an output.



[1] This output buffer enables the latched data to drive the pin when DDR bit is 1 (output mode).
[2] This input buffer is enabled when DDR bit is 0 (input mode).
[3] This input buffer is enabled when DDR bit is 1 (output mode).

Parallel I/O Circuit

When an I/O pin is programmed as an output, reading the associated port bit actually reads the value of the output data latch and not the voltage on the pin itself. When a pin is programmed as an input, reading the port bit reads the voltage level on the I/O pin. The output data latch can always be written, regardless of the state of its DDR bit.

I/O Pin Functions

R/$\overline{W}$	DDR	I/O Pin Functions
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch, which drives the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in output mode. The output data latch is read.

Note: R/$\overline{W}$ is an internal signal.

PORTA — Port A Data Register **$0000**

	Bit 7	6	5	4	3	2	1	Bit 0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	NOT CHANGED BY RESET							

Port A is an 8-bit bidirectional port. At power-up, all eight pins are configured as inputs.

DDRA — Port A Data Direction Register **$0004**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
RESET:	0	0	0	0	0	0	0	0

DDRA7–DDRA0 — Port A Data Direction Bits

These read/write bits determine whether the PA7–PA0 pins are inputs or outputs.

1 = Corresponding port pin configured as output

0 = Corresponding port pin configured as input

PORTB — Port B Data Register **$0001**

	Bit 7	6	5	4	3	2	1	Bit 0
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
RESET:	NOT CHANGED BY RESET							
ALTERNATE FUNCTION:	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

Port B is an 8-bit bidirectional port that shares its pins with the D/A converter when the D/A converter is enabled.

DDRB — Port B Data Direction Register **$0005**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
RESET:	0	0	0	0	0	0	0	0

DDRB7–DDRB5 — Port B Data Direction Bits

These read/write bits determine whether the port B pins are inputs or outputs.

1 = Corresponding port pin configured as output

0 = Corresponding port pin configured as input

PORTC — Port C Data Register **$0002**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	PC5	PC4	PC3	PC2	PC1	PC0
RESET:	NOT CHANGED BY RESET							
ALTERNATE FUNCTION:			TCMP	TCAP		AN0	V_{RH}	DA8

Port C is a 6-bit port with five bidirectional pins and one input-only pin. Port C shares pins PC5 and PC4 with the capture/compare timer when timer interrupts are enabled. PC2, PC1, and PC0 are shared by the A/D converter when it is enabled.

DDRC — Port C Data Direction Register **$0006**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	DDRC5	DDRC4	DDRC3	1	DDRC1	DDRC0
RESET:	0	0	0	0	0	0	0	0

DDRC7–DDRC0 — Port C Data Direction Bits

These read/write bits determine whether pins PC5–PC3 and PC1–PC0 are inputs or outputs. PC2/AN0 is an input-only pin, but bit 2 of the port C data direction register reads as a one.

1 = Corresponding port pin configured as output

0 = Corresponding port pin configured as input

PORTD — Port D Data Register **$0003**

	Bit 7	6	5	4	3	2	1	Bit 0
	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	NOT CHANGED BY RESET							
ALTERNATE FUNCTION:	HTON	FBKG	R	G	B	SCK	SDIO	—

Port D is an 8-bit bidirectional port. Port D shares pins PD2 and PD1 with the SIOP when the SIOP is enabled. Pins PD7–PD3 are shared by the OSD system when it is enabled.

DDRD — Port D Data Direction Register **$0007**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
RESET:	0	0	0	0	0	0	0	0

DDRD7–DDRD0 — Port D Data Direction Bit

These read/write bits determine whether the port C pins are inputs or outputs.

1 = Corresponding port pin configured as output

0 = Corresponding port pin configured as input

Resets and Interrupts

A CPU reset occurs under the following conditions:

- Power-on reset (POR) — A POR is generated when a positive transition occurs on the V_{DD} pin.
- External reset — A reset is generated when a logical zero is applied to the $\overline{\text{RESET}}$ pin.
- Computer operating properly (COP) timer reset — The COP timer resets the CPU if not cleared by a program sequence within a specific period of time. The COP timer system is used to detect software errors.

The following internal actions occur on reset:

- All implemented data direction bits are cleared, making all I/O pins inputs.
- The stack pointer is loaded with $FF.
- The interrupt mask (I) in the condition code register is set, inhibiting interrupts.
- The capture/compare timer clock divider stages are reset. The capture/compare timer is cleared. All timer interrupt enable bits (ICIE, OCIE, and TOIE) are cleared to disable timer interrupts.
- The STOP latch is cleared to enable MCU clocks.
- The WAIT latch is cleared to wake the CPU from the WAIT mode.
- The program counter is loaded with the reset vector.

The CPU can be interrupted in the following ways:

- Software interrupt (SWI) — The SWI instruction causes a nonmaskable interrupt to be executed.
- Timer interrupt — One of the three timer interrupt flags (OCF, ICF, or TOF) is set.
- External interrupt — A falling edge occurs on the $\overline{\text{IRQ}}$ pin.
- On-screen display (OSD) interrupt — The OSD interrupt flag is set.

The following actions occur as a result of an interrupt:

- The CPU registers are stored in the stack in the order PCL, PCH, X, A, CCR.
- The interrupt mask (I) in the condition code register is set to prevent additional interrupts.
- The program counter is loaded with the appropriate interrupt vector (SWI, timer, or external).
- The RTI (return from interrupt) instruction causes the CPU registers to be recovered from the stack in the order CCR, A, X, PCH, PCL. Normal processing resumes.

Pulse-Length Modulation D/A Converter

The digital-to-analog converter produces nine channels of pulse-length modulated output. Contents of the D/A channel registers determine the duty cycle of each channel with 6-bit resolution.

DAC0–DAC8 — D/A Channel Registers 0-8 **$0008–$0010**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	DA5	DA4	DA3	DA2	DA1	DA0
RESET:	0	0	0	0	0	0	0	0

DA5–DA0 — D/A Data Bits

These read/write bits determine the duty cycle of the signals on the DAC output pins. Values of $00 to $3F (corresponding to duty cycles of 0/64 to 63/64) can be programmed in the D/A channel registers. A value of $00 in a D/A channel register produces a 0% duty cycle on the pin for that channel. A value of $20 produces a 50% duty cycle (32/64). A value of $3F produces a high output for 63/64 of the cycle.

DAC Output Programming

Value in DAC Output Register	Duty Cycle of Signal on Corresponding DAC Output
00000000	0/64
00000001	1/64
00000010	2/64
. . .	. . .
00111101	61/64
00111110	62/64
00111111	63/64

DACOCR0–DACOCR1 — DAC Output Control Registers 0 and 1 **$0039–$003A**

	Bit 7	6	5	4	3	2	1	Bit 0	
$0039	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	DACOC0
RESET:	0	0	0	0	0	0	0	0	

	Bit 7	6	5	4	3	2	1	Bit 0	
$003A	0	0	0	0	0	0	0	DA8	DACOC1
RESET:	0	0	0	0	0	0	0	0	

DA8–DA0 — DAC Output Control Bits

These read/write bits determine whether the PB0/DA0–PC0/DA8 pins function as parallel I/O pins or as D/A converter outputs.

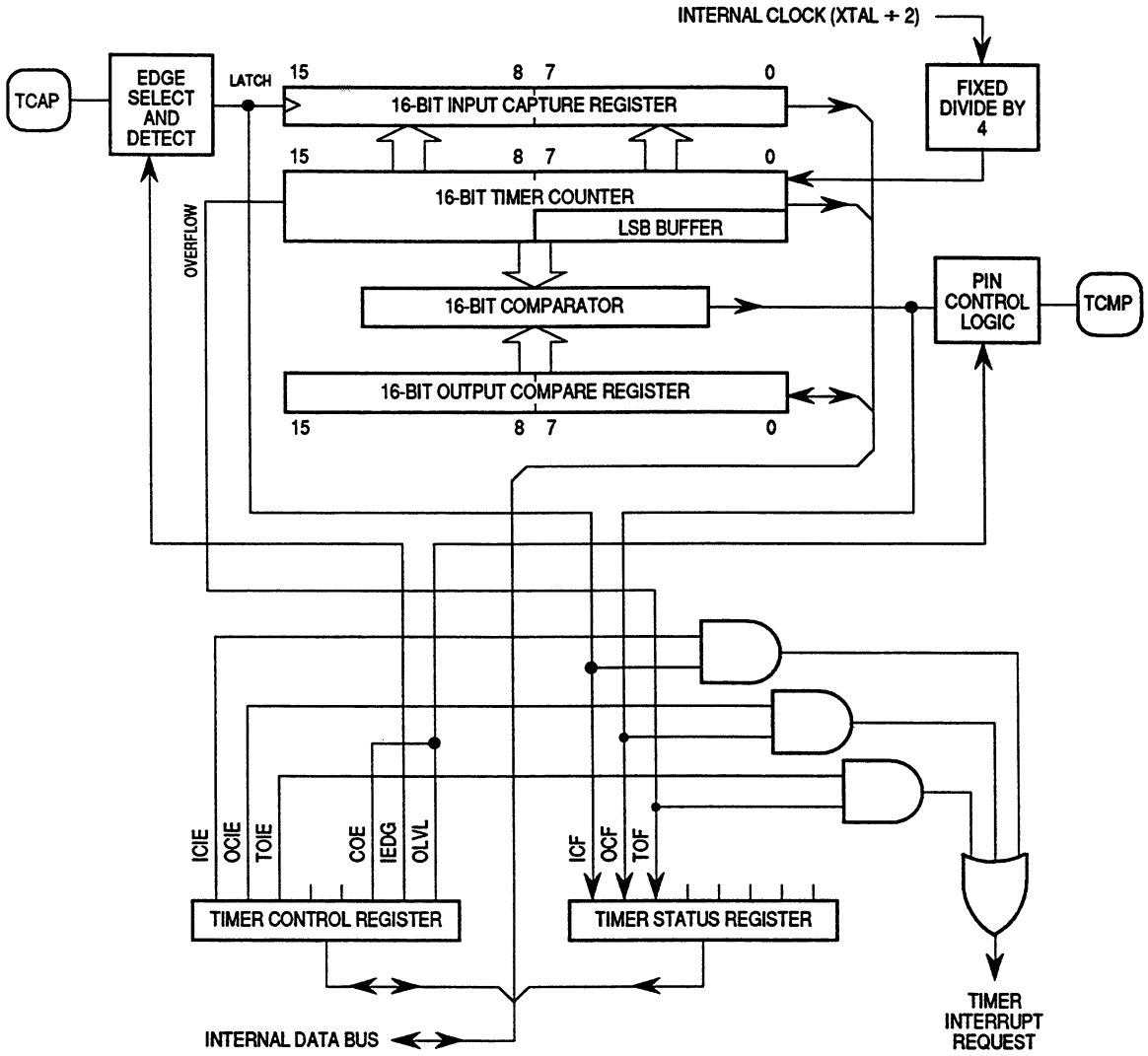
1 = Corresponding pin is a D/A converter output

0 = Corresponding pin is a parallel I/O pin

Capture/Compare Timer

The core of the capture/compare timer subsystem is a free-running 16-bit counter. The input capture function latches the counter value and generates an interrupt request when a selected edge (either falling or rising) occurs on the TCAP input pin. Software can later read this value to determine when the edge occurred.

The output compare function transfers a selected bit (either 1 or 0) to the TCMP output pin and generates an interrupt request when the counter value matches the value programmed in the output compare register.



Capture/Compare Timer Block Diagram

TCR — Timer Control Register **$0012**

	Bit 7	6	5	4	3	2	1	Bit 0
	ICIE	OCIE	TOIE	0	0	COE	IEDG	OLVL
RESET:	0	0	0	0	0	0	U	0

(U = UNCHANGED)

ICIE — Input Capture Interrupt Enable

This read/write bit enables input capture interrupts.

1 = ICF interrupt enabled
0 = ICF interrupt disabled

OCIE — Output Compare Interrupt Enable

This read/write bit enables output compare interrupts.

1 = OCF interrupt enabled
0 = OCF interrupt disabled

TOIE — Timer Overflow Interrupt Enable

This read/write bit enables timer overflow interrupts.

1 = TOF interrupt enabled
0 = TOF interrupt disabled

COE — Compare Output Enable

This read/write bit configures the PC5/TCMP pin as the timer compare output.

1 = TCMP output enabled
0 = TCMP output disabled (pin PC5 available as I/O pin)

IEDG — Input Edge

This read/write bit determines whether a rising or falling edge on the TCAP pin causes a transfer of the counter contents to the input capture register.

1 = Rising edge transfers counter contents
0 = Falling edge transfers counter contents

OLVL — Output Level

This read/write bit determines the output level on the TCMP pin when a successful output compare occurs.

1 = TCMP pin set on compare
0 = TCMP pin cleared on compare

TSR — Timer Status Register **$0013**

	Bit 7	6	5	4	3	2	1	Bit 0
	ICF	OCF	TOF	0	0	0	0	0
RESET:	U	U	U	0	0	0	0	0

(U = UNCHANGED)

ICF — Input Capture Flag

This read-only bit is set when a selected edge occurs on the TCAP pin. Clear the ICF bit by reading the timer status register with ICF set, and then reading the low byte of the input capture register.

OCF — Output Compare Flag

This read-only bit is set when the counter value matches contents of the output compare register. Clear the OCF bit by reading the timer status register with OCF set, and then reading the low byte of the output compare register.

TOF — Timer Overflow Flag

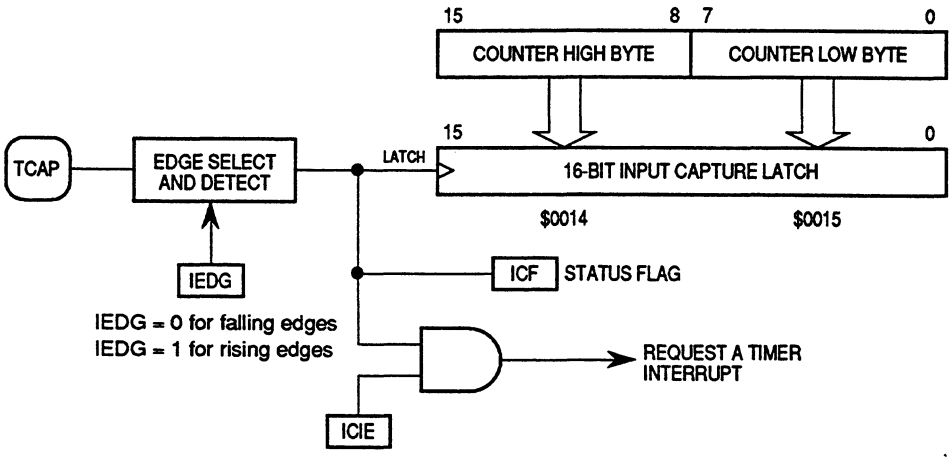
This read-only bit is set when the counter rolls over from $FFFF to $0000. Clear the TOF bit by reading the timer status register with TOF set, and then reading the low byte of the timer counter register.

ICR — Input Capture Register **$0014–$0015**

$0014	Bit 15	14	13	12	11	10	9	Bit 8	ICR (HIGH)
$0015	Bit 7	6	5	4	3	2	1	Bit 0	ICR (LOW)

Reset does not affect the input capture register.

When a selected edge occurs on the TCAP pin, the current value of the counter is latched into the input capture register. Reading the high byte of the input capture register inhibits further captures until the low byte is read. Writing to the input capture register has no effect.



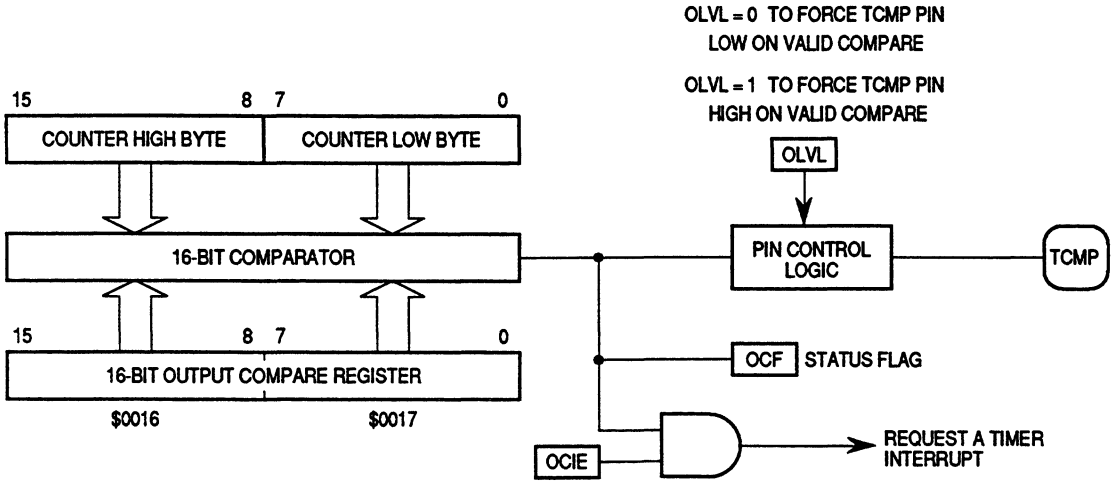
Input Capture Operation

OCR — Output Compare Register **$0016–$0017**

$0016	Bit 15	14	13	12	11	10	9	Bit 8	OCR (HIGH)
$0017	Bit 7	6	5	4	3	2	1	Bit 0	OCR (LOW)

Reset does not change the output compare register.

When the value of the counter matches the value in the output compare register, the planned TCMP pin action takes place. Writing to the high byte of the output compare register inhibits timer compares until the low byte is written.



Output Compare Operation

TCNT — Timer Counter Register **$0018–$0019**

$0018	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (HIGH)
$0019	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (LOW)

On reset, the timer counter register resets to $FFFC.

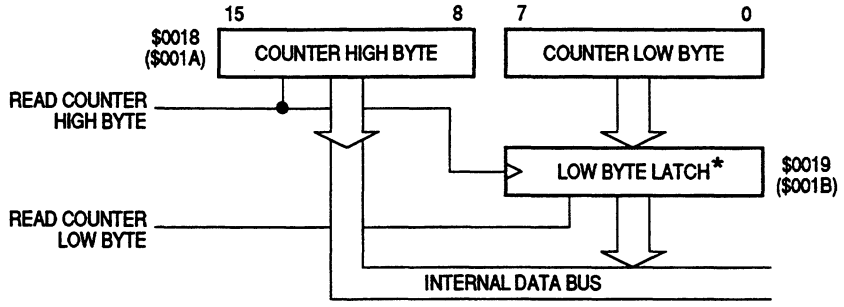
The timer counter register contains the current counter value. Reading the high byte causes the low byte to be latched into a buffer. Reading the low byte buffer after reading the timer status register (TSR) clears the TOF bit. Writing to the timer counter register has no effect.

ALTCNT — Alternate Counter Register **$001A–$001B**

$001A	Bit 15	14	13	12	11	10	9	Bit 8	ALTCNT (HIGH)
$001B	Bit 7	6	5	4	3	2	1	Bit 0	ALTCNT (LOW)

On reset, the alternate counter register resets to $FFFC.

The alternate counter register contains the current counter value. Reading the high byte causes the low byte to be latched into a buffer. Reading the alternate counter register does not affect the TOF bit. Writing to the alternate counter register has no effect.



*The low byte latch is normally transparent. It latches when the high byte of the counter is read and becomes transparent again when the low byte of the counter is read.

16-Bit Counter Reads

A/D Converter

The 8-bit analog-to-digital converter performs ratiometric conversion by successive approximation. Pin V_{RH} supplies the high reference voltage. Operating frequency must be 1 MHz or greater. The analog input is pin PC2/AN0.

ADRR — A/D Result Register **$001E**

	Bit 7	6	5	4	3	2	1	Bit 0
RESET:	NOT CHANGED BY RESET							

ADDR is a read-only register that contains the result of the most recent A/D conversion.

ADSCR — A/D Status and Control Register **$001F**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	0	0	0	CH1	CH0	COCO	ADON
RESET:	—	0	0	0	0	0	0	0

CH1–CH0 — Channel Select
These read/write bits select one of four A/D converter input channels.

A/D Input Selection

CH1[1:0]	Input Selected
00	AN0, Port C, Bit 2
01	V_{RH}
10	$V_{RH} \div 2$
11	V_{SS}

COCO — Conversion Complete
This read-only bit is automatically set when an A/D conversion is complete.
1 = Conversion result in A/D result register
0 = Conversion result not available

ADON — A/D Converter On
This read/write bit enables the A/D converter.
1 = A/D converter enabled
0 = A/D converter disabled

On-Screen Display

The features of the fully programmable on-screen display (OSD) include the following:

- Programmable 10-row by 18-column display
- 64 user-defined 8-dot by 11-dot or 8-dot by 13-dot characters
- Standard, double-wide, double-high, and double-wide/double-high characters
- Programmable horizontal display positioning
- Eight character colors; four colors per row; character-by-character color select
- Eight window colors
- Three-statable, polarity-programmable red (R), green (G), and blue (B) outputs
- Three-statable fast luminance-blanking output (mask-optional polarity)
- Three-statable half-tone output (mask-optional polarity)
- Half-dot shift for character rounding by hardware
- Black outline generation by hardware
- Continuous horizontal and vertical line capability for linear scales
- Four line/field frequency modes:
  — 15.75 kHz/60 Hz
  — 31.5 kHz/120 Hz
  — 15.625 kHz/50 Hz
  — 31.25 kHz/100 Hz

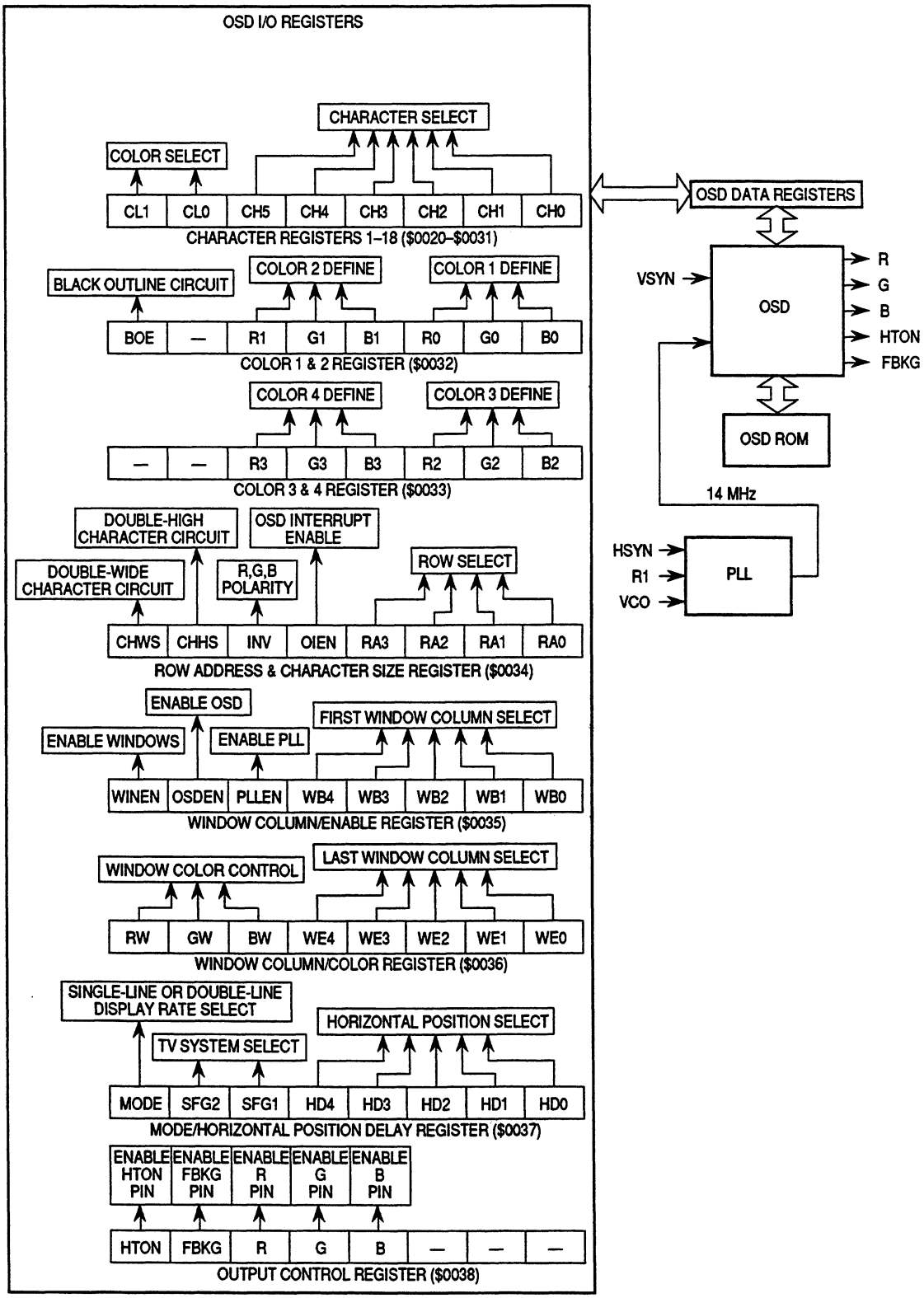
Programming Overview

The on-screen display (OSD) single-row memory map architecture uses buffered registers to generate each row of the display. A set of read/write buffer registers is available to the programmer, and a set of corresponding data latches actually drives the OSD character and window generation logic.

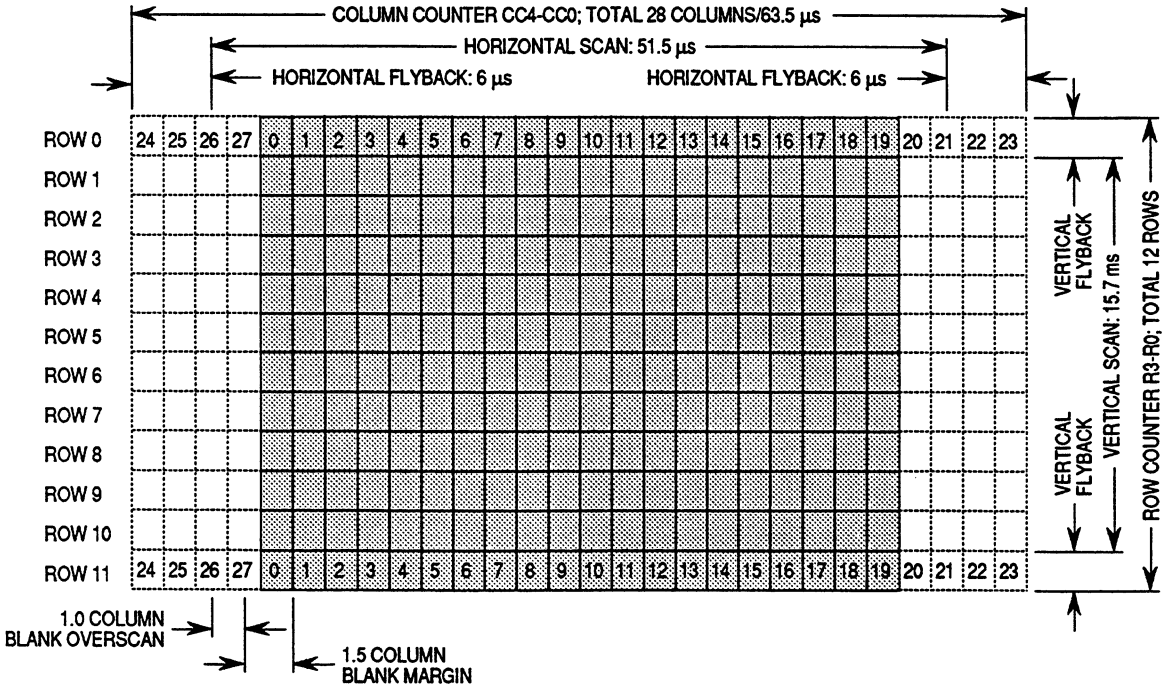
OSD timing logic feeds a line-rate signal to a line counter. Overflows from the line counter drive a row counter. The OSD continuously compares the output of the row counter with the state of the RA3–RA0 bits shifted into the data latches from the OSD row address/character size register. When a match occurs, a maskable interrupt notifies the CPU that the data for the next row of the display are available in the data latches. At this time, the OSD begins the display of the data currently in the data latches. During each scan line, OSD logic reads the 18 character codes from the OSD character latches and the scan line number from the line counter. The character codes and the scan line number form the character ROM addresses from which the OSD logic fetches the bit pattern for each scan line.

The bit pattern data then passes through half-dot shift and black outline circuits and through a parallel-in serial-out register to obtain the luminance signal. The luminance signal passes through a color encoder to generate the R, G, and B signals. Finally, OSD circuitry adds the video attributes and windowing data to complete the chrominance signal.

While the data latches drive the display, the program writes the data for the next row into the buffer registers. At the completion of the last scan line of the displayed row, the data in the buffer registers shifts into the data latches.

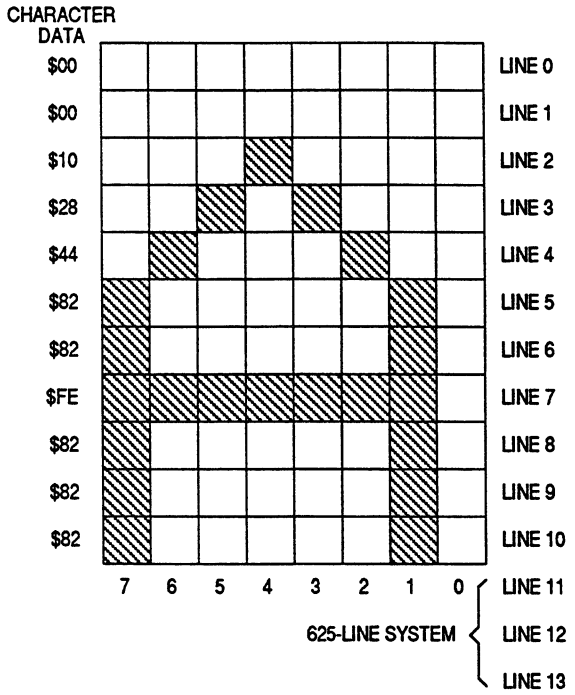


OSD Block Diagram



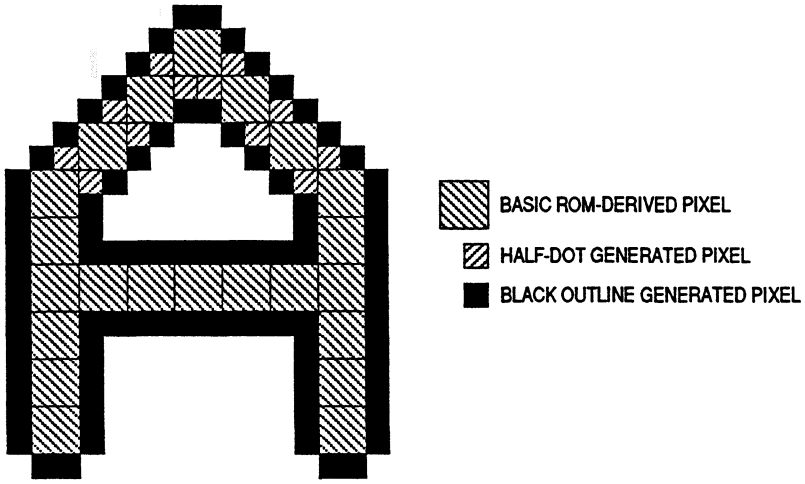
Full Screen Character Display

The following figure is an example of the 64 8-bit by 11-bit user-defined character matrices.



Character Matrix

In a 525-line system, 11 bytes define each character. The 11 bytes for the first character in the character ROM reside in addresses $0400–$040A. For ease of addressing, there are 16 bytes reserved for each character, so the 11 bytes for the second character reside in addresses $0410–$041A.



Half-Dot Shift and Black Outline Generation

OSD I/O Registers

Twenty-five registers are available to the programmer to control the on-screen display. The 25 buffer registers allow programming of the following video data for each row of the display:

- **Select column, character, and character color.** There are 18 OSD character registers, one for each column. Each OSD character register contains the following control bits:
  — Five bits to select one of 64 characters from the character ROM
  — Two bits to select one of four colors for that character

- **Define the four colors and enable black outlining.** There are two OSD color registers, one for colors 1 and 2, and one for colors 3 and 4. Each of the four colors can be any combination of the R, G, and B primary colors. The register for colors 1 and 2 also contains a bit to enable the generation of a black outline around the characters.

- **Select row, character size, enable OSD interrupts, and select R, G, and B output polarity.** The OSD row address/character size register contains the following control bits:
  — Four bits to select one of 10 rows
  — One bit to select double-wide characters
  — One bit to select double-high characters
  — One bit to enable OSD interrupts
  — One bit to select active-high or active-low R, G, and B outputs

- **Enable the OSD, select first window column, enable windowing, and enable the phase-lock circuit.** The OSD window column/enable register contains the following control bits:
  — Five bits to select the first window column
  — One bit to enable windowing
  — One bit to enable the OSD system
  — One bit to enable the phase-lock circuit

- **Select the last window column, and select window color.** The OSD window column/color register contains the following control bits:
  — Five bits to select the last window column
  — Three bits to select the window color

- **Select line frequency, field frequency, and horizontal positioning.** The OSD horizontal position delay register contains the following control bits:
  — One bit to select a single-line or double-line rate display
  — Two bits to select field frequency
  — Five bits to select horizontal positioning in half-column steps

- **Enable OSD outputs.** The OSD output control register contains five bits to enable the halftone (HTON), fast blanking (FBKG), and R,G, and B outputs.

OSDCR1–OSDCR18 — Character Registers 1–18 **$0020–$0031**

	Bit 7	6	5	4	3	2	1	Bit 0
	CL1	CL0	CH5	CH4	CH3	CH2	CH1	CH0
RESET:	NOT CHANGED BY RESET							

The 18 character registers select the characters and their colors for the 18 row positions.

CL1, CL0 — Color
These read/write bits select one of four colors for the designated character.

Color Selection

CL[1:0]	Color
00	1
01	2
10	3
11	4

NOTE: Define colors 1–4 in registers OSDC12R and OSDC34R ($0032 and $0033).

CH5–CH0 — Character

These read/write bits select one of the 64 characters from the character ROM.

Character Selection

CH[5:0]	Character
000000	0
000001	1
000010	2
. . .	. . .
111101	61
111110	62
111111	63

OSDC12/SR — Color 1 and 2/Status Register **$0032**

	Bit 7	6	5	4	3	2	1	Bit 0	
	1	1	1	1	VSYN	1	HSYN	OSDFL	(READ)
RESET:	1	1	1	1	U	1	U	U	
	(U = UNCHANGED)								
ALTERNATE FUNCTION:	BOE	—	R1	G1	B1	R0	B0	G0	(WRITE)
RESET:	0	—	0	0	0	0	0	0	

Reading address $0032 reads the three status bits in the status register.

VSYN — Vertical Sync Pulse

This read-only bit indicates the presence of a vertical flyback signal on the VSYN pin.

1 = Vertical flyback signal present

0 = Vertical flyback signal not present

HSYN — Horizontal Sync Pulse

This read-only bit indicates the presence of a horizontal flyback signal on the HSYN pin.

1 = Horizontal flyback signal present

0 = Horizontal flyback signal not present

OSDFL — OSD Flag

This read-only bit indicates that the row counter has counted up to the number of the next row to be displayed. If the OSD interrupt enable bit, OIEN, is set, an OSD interrupt occurs. The CPU automatically clears the OSDFL bit when it fetches the OSD interrupt vector.

1 = Row counter matches bits RA3–RA0 bits in row address/character size register ($0034)

0 = Row counter output does not match bits RA3–RA0

Writing to address $0032 writes the control bits in the OSD color 1 and 2 register. This register defines color 1 and color 2 and enables the black outline function.

BOE — Black Outline Enable

This read/write bit causes a black outline to be generated around the illuminated pixels of each character.

1 = Black outline enabled
0 = Black outline disabled

R1, G1, B1 — Color 2

These read/write bits control the R, B, and G color guns for color 2.

1 = Color gun on
0 = Color gun off

R0, G0, B0 — Color 1

These read/write bits control the R, B, and G color guns for color 1.

1 = Color gun on
0 = Color gun off

Color Definition

Rx:Gx:Bx	Color
000	Black
001	Blue
010	Green
011	Cyan
100	Red
101	Purple
110	Yellow
111	White

OSDC34R — Color 3 and 4 Register **$0033**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	R3	G3	B3	R2	G2	B2
RESET:	—	—	0	0	0	0	0	0

This register defines color 3 and color 4.

R3, G3, B3 — Color 4

These read/write bits control the R, B, and G color guns for color 4.

1 = Color gun on
0 = Color gun off

R2, G2, B2 — Color 3

These read/write bits control the R, B, and G color guns for color 3.

1 = Color gun on

0 = Color gun off

OSDRA/CSR — Row Address/Character Size Register **$0034**

	Bit 7	6	5	4	3	2	1	Bit 0
	CHWS	CHHS	INV	OIEN	RA3	RA2	RA1	RA0
RESET:	0	0	0	0	0	0	0	0

This register selects one of the 10 display rows. It also contains bits to control character size, polarity of the R, G, and B outputs, and one bit to enable OSD interrupts.

CHWS — Character Width Select

This read/write bit produces double-wide characters on the designated row. When the CHWS bit is set, only the character registers at even addresses are used, starting with CR1 at $0020.

1 = Double-wide characters enabled

0 = Double-wide characters disabled

CHHS — Character Height Select

This read/write bit produces double-high characters on the designated row.

1 = Double-high characters enabled

0 = Double-high characters disabled

INV — Invert

This read/write bit selects either active-high or active-low R, G, and B outputs.

1 = Active-low outputs

0 = Active-high outputs

OIEN — OSD Interrupt Enable

This read/write bit enables OSD interrupts.

1 = OSD interrupts enabled

0 = OSD interrupts disabled

RA3–RA0 — Row Address

These read/write bits select one of the ten character rows.

Row Selection

RA[3:0]	Row
0001	1
0010	2
0011	3
. . .	. . .
1000	8
1001	9
1010	10

OSDWC/ER — Window Column/Enable Register **$0035**

	Bit 7	6	5	4	3	2	1	Bit 0
	WINEN	OSDEN	PLLEN	WB4	WB3	WB2	WB1	WB0
RESET:	0	0	0	0	0	0	0	0

This register selects the first column of the window. It also contains bits to enable the OSD system, the phase-locked loop (PLL) system, and the windowing function.

WINEN — Window Enable

This read/write bit enables the generation of window (background) colors.

1 = Windows enabled
0 = Windows disabled

OSDEN — OSD Enable

This read/write bit enables the OSD.

1 = OSD enabled
0 = OSD disabled

PLLEN — PLL Enable

This read/write bit enables the 14-MHz oscillator of the PLL. Disable the PLL when in STOP mode, and whenever OSD data is not being displayed.

1 = PLL enabled
0 = PLL disabled

WB4–WB0 — Window Begin

These read/write bits select the column number for the leftmost column of the window.

First Window Column Selection

WB[4:0]	First Window Column
00001	1
00010	2
00011	3
. . .	. . .
10000	16
10001	17
10010	18

OSDWC/CR — Window Column/Color Register **$0036**

	Bit 7	6	5	4	3	2	1	Bit 0
	RW	GW	BW	WE4	WE3	WE2	WE1	WE0
RESET:	0	0	0	0	0	0	0	0

This register selects the last column of the window. It also contains bits to control the window background color.

RW, GW, BW — Red Window, Green Window, Blue Window

These read/write bits control the color guns for the background color.

1 = Color gun on

0 = Color gun off

WE4–WE0 — Window End

These read/write bits select the column number for the rightmost column of the window.

Last Window Column Selection

WE[4:0]	Last Window Column
00001	1
00010	2
00011	3
. . .	. . .
10000	16
10001	17
10010	18

OSDM/HPDR — Mode/Horizontal Position Delay Register **$0037**

	Bit 7	6	5	4	3	2	1	Bit 0
	MODE	SFG2	SFG1	HD4	HD3	HD2	HD1	HD0
RESET:	0	0	0	0	0	0	0	0

This register positions the row of characters relative to the left edge of the raster. It also contains bits to control line frequency and field frequency.

MODE — Display Mode

This read/write bit selects the frequency for single-line or double-line display rate.

1 = Line frequency = 31,250 Hz or 31,468 Hz or 31,500 Hz

0 = Line frequency = 15,625 Hz or 15,734 Hz or 15,750 Hz

Line Frequencies

MODE	Line Frequencies (Hz)		
0	15,625	15,734	15,750
1	31,250	31,468	31,500

SFG2, SFG1 — System Flag 1, 2

These read/write bits select one of four field frequencies.

Field Frequencies

SFG[1:0]	Field Frequency (Hz)	Line Frequency (Hz)
00	60	15,750 or 15,734
01	50	15,625
10	120	31,500 or 31,468
11	100	31,250

HD4–HD1 — Horizontal Delay

These read/write bits determine the horizontal positioning of the display in 32 half-column steps.

Horizontal Delay

HD[4:0]	Columns from Left Edge of Raster
00001	1/2
00010	1
00011	1 1/2
. . .	. . .
11101	15
11110	15 1/2
11111	16

OSDOER — Output Enable Register **$0038**

	Bit 7	6	5	4	3	2	1	Bit 0
	HTON	FBKG	R	G	B	—	—	—
RESET:	0	0	0	0	0	—	—	—

HTON — Half Tone

This read/write bit enables the half-tone (HTON) output. The HTON signal can be used to drive the luminance of the window background color to fractional intensity.

1 = HTON output enabled
0 = HTON output disabled; PD7 is a port D I/O pin

FBKG — Fast Blanking

This read/write bit enables the fast blanking (FBKG) output. The FBKG signal can be used to blank the external video source so that the combination of the on-screen display and the external video source is not additive.

1 = FBKG output enabled
0 = FBKG output disabled; PD6 is a port D I/O pin

R — Red

This read/write bit enables the R output.

1 = R output enabled
0 = R output disabled; PD5 is a port D I/O pin

G — Green

This read/write bit enables the G output.

1 = G output enabled
0 = G output disabled; PD4 is a port D I/O pin

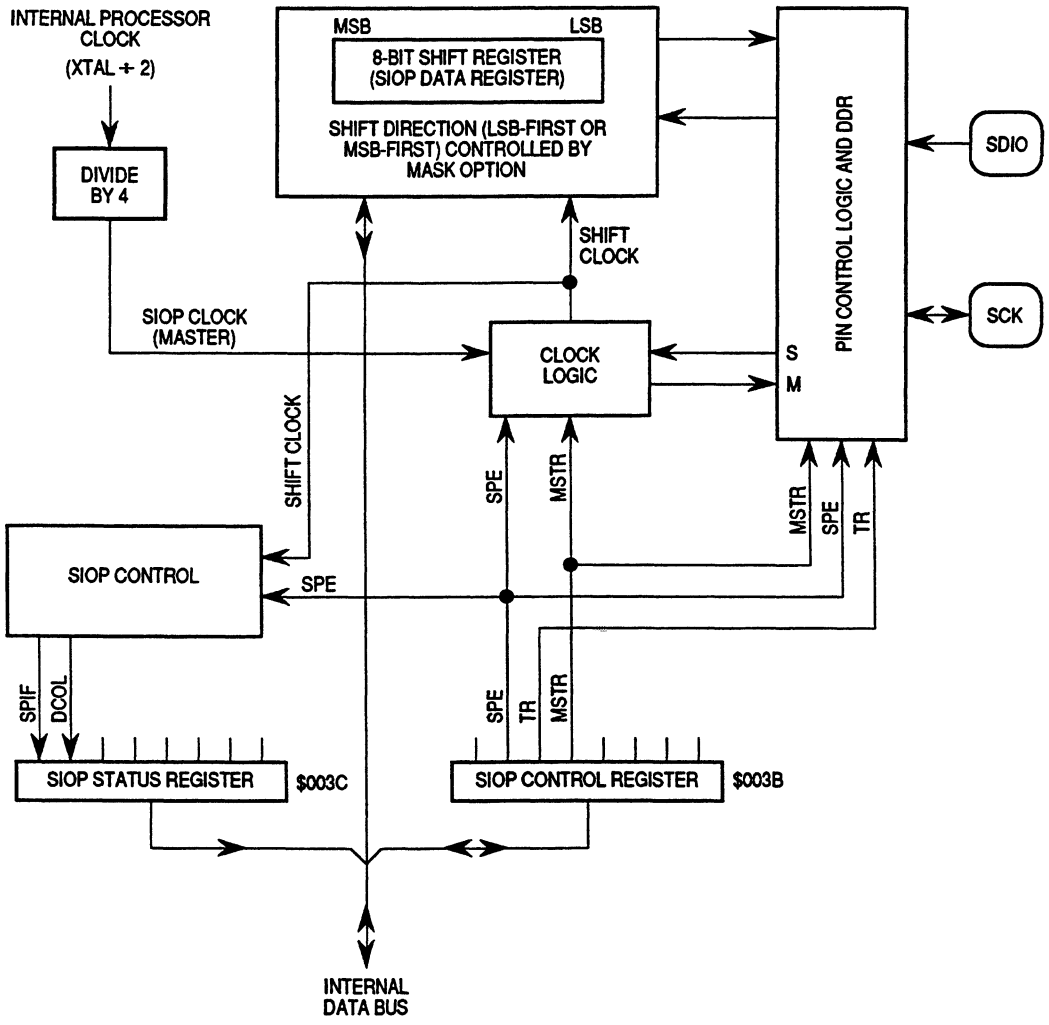
B — Blue

This read/write bit enables the B output.

1 = B output enabled
0 = B output disabled; PD3 is a port D I/O pin

Serial I/O Port

The serial I/O port (SIOP) allows simple high-speed synchronous serial data transfer between the MC68HC05T1 and peripheral devices. The SIOP can be used with simple shift registers to expand the number of parallel I/O pins controlled by the MCU. A large number of more powerful peripherals such as A/D converters and real time clocks are also compatible with this interface.



SIOP Block Diagram

SCR — SIOP Control Register **$003B**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	SPE	TR	MSTR	0	0	F1	F0
RESET:	0	0	0	0	1	0	0	0

SPE — SIOP Enable

This read/write bit enables the SIOP.

1 = SIOP on and pins SDIO and SCK dedicated to SIOP

0 = SIOP off and pins PD1 and PD2 available for general-purpose I/O

TR — Transmit

This read/write bit determines whether the SDIO pin is an input or an output.

1 = SDIO pin configured as serial output

0 = SDIO pin configured as serial input

MSTR — Master Mode

This read/write bit configures the SIOP for master mode. Setting MSTR initializes SCK as the SIOP clock output. Clearing MSTR initializes SCK as the SIOP clock input.

1 = SIOP configured as master

0 = SIOP configured as slave

F1, F0 — SCK Frequency

When the SIOP is in master mode, these read/write bits control the frequency of the SCK output.

SCK Frequency Select

F[1:0]	SCK Frequency
00	Internal Clock ÷ 4
01	Internal Clock ÷ 8
10	Internal Clock ÷ 16
11	Internal Clock ÷ 32

NOTE: Internal clock = crystal/ceramic resonator frequency ÷ 2

SSR — SIOP Status Register **$003C**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIF	DCOL	0	0	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

SPIF — SIOP Peripheral Interface Flag

This clearable, read-only bit is set automatically at the end of a serial transfer. Clear the SPIF bit by reading the SIOP status register with SPIF set, and then reading or writing the SIOP data register.

DCOL — Data Collision

This clearable, read-only bit is set if the SIOP data register is read or written during a transfer. Clear the DCOL bit by reading the SIOP status register with the SPIF bit set, and then reading or writing the SIOP data register.

SDR — SIOP Data Register **$003D**

	Bit 7	6	5	4	3	2	1	Bit 0
RESET:	NOT CHANGED BY RESET							

With the SIOP configured as master, writing to this register initiates a serial transfer.

COP Timer

The MC68HC05T1 contains a computer operating properly (COP) timer as a mask option that automatically times out if not cleared by a program sequence within a specific time. The COP timer is used to detect software errors. If the COP timer times out, it generates a reset. The timeout period is 64 ms at an internal clock rate of 2 MHz. To prevent a COP timeout, write a logical zero to bit 0 (COPR) of the COP control register at location $3FF0. Writing a zero to COPR resets the COP timer and begins the timeout period again.

COP — COP Register **$3FF0**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	—	—	—	—	—	COPR
RESET:	—	—	—	—	—	—	—	0

COPR — COP Timer Reset

Writing a zero to this write-only bit resets the COP timer. Reading address $3FF0 returns the user ROM data at that location.

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