MOTOROLA
SEMICONDUCTOR PRODUCT BRIEF

Order this document by:
DSP56307EVMP/D

DSP56307EVM

Advance Information

DSP56307EVM Evaluation Module

The DSP56307 Evaluation Module (DSP56307EVM) is a low-cost platform for developing real-time software and hardware products to support a new generation of wireless, telecommunications, and multimedia applications. The DSP56307EVM targets applications requiring a large amount of on-chip memory such as wireless infrastructure applications. The Enhanced Filter Coprocessor (EFCOP) can accelerate general filtering algorithms, such as finite impulse response (FIR) filters, infinite impulse response (IIR) filters; the EFCOP can also adapt FIR filters as multi-channel filters used in echo cancellation , correlation, and general-purpose convolution-based algorithms. The user can download software to on-chip or on-board RAM, then run and debug it. The user can also connect hardware, such as external memories and analog-to-digital (A/D) or digital-to-analog (D/A) converters, for product development. The 24-bit precision of the DSP56307 Digital Signal Processor (DSP) combined with the on-board 64K of external SRAM and Crystal Semiconductor's CS4218 stereo, CD-quality, audio codec ideally suits the DSP56307EVM for implementing and demonstrating many communications and audio processing algorithms. It is also an effective tool for learning the architecture and instruction set of the DSP56307 processor. **Figure 1** shows the functional block diagram for the DSP56307EVM.

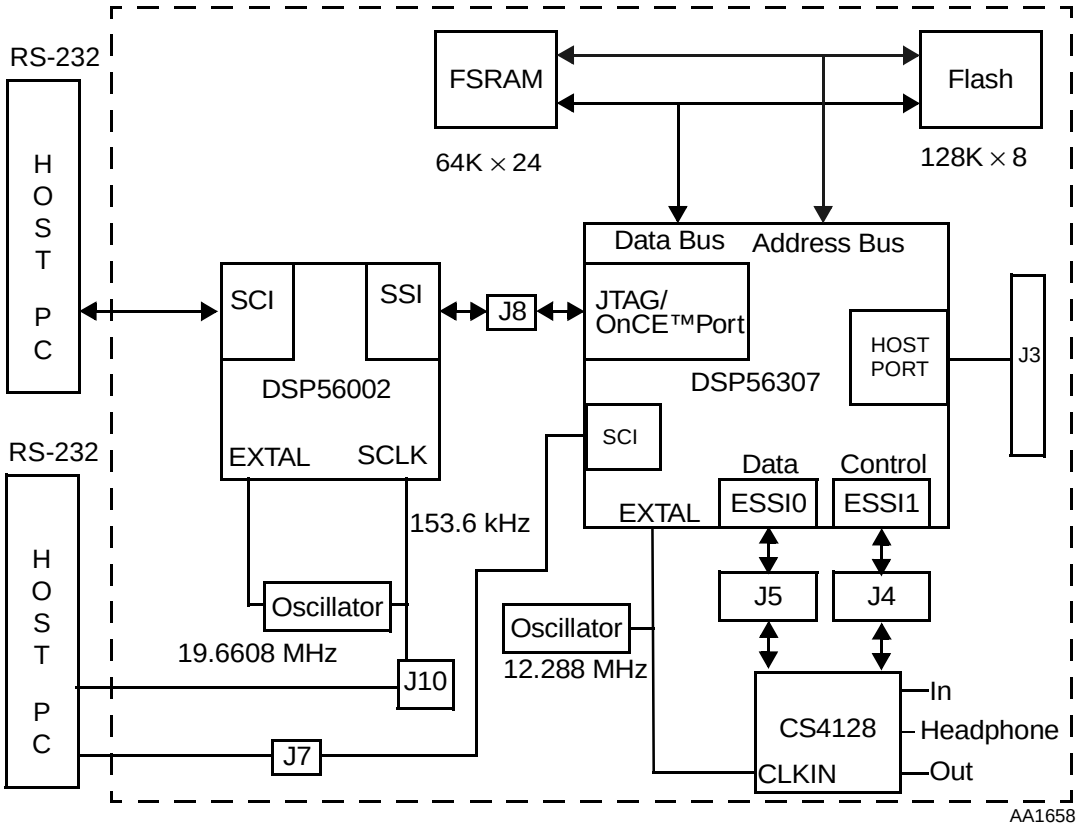

Figure 1 DSP56307EVM Functional Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FEATURES

Hardware

- 24-bit DSP56307 Digital Signal Processor
  - High -Performance DSP56300 core
    - 100 Million Instructions Per Second (MIPS) with a 100-MHz clock at 2.5-V core and 3.3 V I/O
    - Object code compatible with the DSP56000 core
    - Highly-parallel instruction set
    - Data Arithmetic Logic Unit (ALU)
    - Fully pipelined 24-x 24-bit parallel multiplier-accumulator
    - 56-bit parallel barrel shifter
    - Conditional ALU instructions
    - 24-bit or 16-bit arithmetic support under software control
    - Position Independent Code (PIC) support
    - Addressing modes optimized for DSP applications (including immediate offsets)
    - On-chip memory-expandable hardware stack
    - Nested hardware DO loops
    - Fast auto-return interrupts
    - On-chip concurrent six-channel DMA controller
    - On-chip Phase-Locked Loop (PLL)
    - On-Chip Emulation (OnCE™) module
    - JTAG port
    - Address tracing mode reflects internal program RAM accesses at the external port
  - Enhanced Filter Coprocessor (EFCOP)
    - On-chip filtering and echo-cancellation coprocessor runs in parallel to the DSP core

– On-chip memories
  • 64K on-chip RAM total
  • Program RAM, instruction cache, X data RAM, and Y data RAM are programmable:

Program RAM Size	Instruction Cache Size	X Data RAM Size*	Y Data RAM Size*	Instruction Cache	Switch Mode	MSW1	MSW0
16K × 24-bit	0	24K × 24-bit	24K × 24-bit	disabled	disabled	0/1	0/1
15K × 24-bit	1024 × 24-bit	24K × 24-bit	24K × 24-bit	enabled	disabled	0/1	0/1
48K × 24-bit	0	8K × 24-bit	8K × 24-bit	disabled	enabled	0	0
47K × 24-bit	1024 × 24-bit	8K × 24-bit	8K × 24-bit	enabled	enabled	0	0
40K × 24-bit	0	12K × 24-bit	12K × 24-bit	disabled	enabled	0	1
39K × 24-bit	1024 × 24-bit	12K × 24-bit	12K × 24-bit	enabled	enabled	0	1
32K × 24-bit	0	16K × 24-bit	16K × 24-bit	disabled	enabled	1	0
31K × 24-bit	1024 × 24-bit	16K × 24-bit	16K × 24-bit	enabled	enabled	1	0
24K × 24-bit	0	20K × 24-bit	20K × 24-bit	disabled	enabled	1	1
23K × 24-bit	1024 × 24-bit	20K × 24-bit	20K × 24-bit	enabled	enabled	1	1
*Includes 4 K × 24-bit shared memory (i.e., memory shared by the core and the EFCOP)							

• 192 x 24-bit bootstrap ROM

– Off-chip memory expansion
  • Data memory expansion to two memory spaces of 16M × 24-bit words each
    – 16M x 24-bit for DRAM
    – 4M x 24-bit for SRAM
  • Program memory expansion to one memory space of 16M × 24-bit words
    – 16M x 24-bit for DRAM
    – 4M x 24-bit for SRAM
  • External memory expansion port
  • Chip select logic for glueless interface to static random access memory (SRAM)
  • On-chip DRAM Controller for glueless interface to dynamic random access memory (DRAM)

– On-chip peripherals
  • Enhanced DSP56000-like 8-bit parallel Host Interface (HI08)
  • Two Enhanced Synchronous Serial Interfaces (ESSI)
  • Serial Communications Interface (SCI) with baud rate generator
  • Triple timer module
  • Up to 34 programmable General-Purpose Input/Output (GPIO) pins, depending on which peripherals are enabled

  - Reduced power dissipation
    - Very low-power CMOS design
    - Wait and stop low-power standby modes
    - Fully-static logic, operation frequency down to 0 Hz (dc)
    - Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)
- 64K x 24-bit fast static RAM for expansion memory
- 128K x 8-bit Flash Programmable Erasable Read Only Memory (PEROM) for stand-alone operation
- 16-bit CD-quality audio codec
  - Two channels of 16-bit A/D conversion
  - Two channels of 16-bit D/A conversion
  - Software-selectable 8-bit and 16-bit data formats, including μ-law and A-law companding
  - Stereo jacks for audio input, output, and headphones
- Command converter
  - DSP56002 for high-speed OnCE/JTAG command conversion software
  - JTAG connector for use with the Application Development System (ADS) command converter card
  - RS–232 serial port
- Connectors
  - Host-port connector
  - Host interface RS–232 connector
  - ESSI0 connector
  - ESSI1 connector
  - SCI connector

Software

- Motorola’s DSP563xx cross assembler
  - Produces DSP56307 binary code from source code using labels, sections, and macro definitions incorporating the DSP’s complete instruction set, all addressing modes, and all memory spaces
  - Offers macros, expression evaluation, and functions for strings, data conversion, and transcendentals
  - Creates reports for cross-references, instruction cycle count, and memory usage

  - Provides extensive error checking and reporting
- Domain Technologies debug software with Windows™-based user interface
  - Symbolic debugging
  - Windows for data, code, DSP registers, commands, peripherals, etc.
  - Data and registers displayed in fractional, decimal, or hexadecimal format
  - Graphical display of memory segments
  - Up to eight simultaneous software breakpoints
  - Built–in–line assembler and disassembler

User Requirements

The user must provide the following:

- Power supply (7–9 V ac or dc, 500 mA with 2.1 mm coaxial connector)
- RS-232 cable (DB9 plug to DB9 receptacle)
- Audio source and a cable with 1/8-inch stereo plugs
- IBM PC-compatible computer (486 class or higher) running Windows 3.1 (or higher) with an RS-232 serial port capable of 9,600 to 115,200 bits-per-second operation, 8 Mbytes RAM, 3-1/2 inch diskette drive, CD-ROM drive, hard drive with 20 Mbytes of free disk space, and a mouse

SUPPORTING DOCUMENTATION

The first three documents listed in **Table 1** are required for a complete description of the DSP56307 chip and are necessary to design properly with the part. The fourth and fifth documents describe the DSP56307 Evaluation Module, including installation and use and are provided with the module. Additional copies are available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola Semiconductor Sales Office
- Motorola Literature Distribution Center
- The World Wide Web (WWW) *http://www.mot.com/SPS/DSP/documentation*.

You can order DSP56307 literature using the document order number provided in the table below.

Table 1 Documentation List

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56307 User's Manual	Detailed functional description of the DSP56307 memory configuration, operation, and register programming	DSP56307UM/D
DSP56307 Technical Data	DSP56307 features list and physical, electrical, timing, and package specifications	DSP56307/D
DSP56307EVM Product Brief	Overview description of the DSP56307EVM, including block diagram and list of features	DSP56307EVMP/D
DSP56307EVM User's Manual	Detailed functional description of the DSP56307EVM, including requirements, installation, and general operating guidelines	DSP56307EMUM/D

How to reach us:

USA/Europe/Locations Not Listed:
Motorola Literature Distribution
P.O. Box 5405
Denver, Colorado 80217
1 (800) 441-2447 (within US)
1 (303) 675-2140 (outside US)
1 (303) 675-2150 (direct FAX)

Mfax™:
RMFAX0@email.sps.mot.com
TOUCHTONE (602) 244-6609

Asia/Pacific:
Motorola Semiconductors H.K. Ltd.
8B Tai Ping Industrial Park
51 Ting Kok Road
Tai Po, N.T., Hong Kong
852-2662928

Technical Resource Center:
1 (800) 521-6274

DSP Helpline
dsphelp@dsp.sps.mot.com

Japan:
Nippon Motorola Ltd.
Tatsumi-SPD-JLDC
6F Seibu-Butsuryu-Center
3-14-2 Tatsumi Koto-Ku
Tokyo 135, Japan
81-3-3521-8315

Internet:
www.motorola-dsp.com