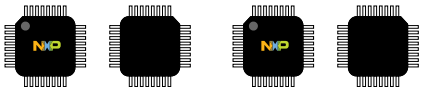
Kinetis KM35 Sub-Family Data Sheet

MKM35Z256VLL7
MKM35Z256VLQ7
MKM35Z512VLL7
MKM35Z512VLQ7



100 LQFP
14 mm × 14 mm Pitch
0.5 mm

144 LQFP
20 mm × 20 mm Pitch
0.5 mm

Enabling high accuracy, secure 1-, 2- and 3-phase electricity metering solutions through a powerful analog front end (AFE), auto-compensated iRTC with hardware tamper detection, segment LCD controller, rich security protection and multiple low power features in a 32-bit Arm® Cortex®-M0+ MCU. This product offers:

- Enabling single-chip 1-, 2- and 3-phase metering designs
  - AFE, Security and HMI. Single crystal implementation
  - Single point of calibration during manufacture
- Highest accuracy metrology with regional feature support
  - Multiple ΣΔ ADCs with PGA
  - Supports neutral disconnect use case
- Compliance with WELMEC/OIML recommendations
  - Memory and peripheral protection
  - Hardware tamper detect with time stamping
  - Low-power RTC, battery backup with tamper memory

Core

- Arm® Cortex®-M0+ core up to 75 MHz
- Metering specific Memory Mapped Arithmetic Unit (MMAU)

Clocks

- 75 MHz high-accuracy internal reference clock
- 32 kHz, and 4 MHz internal reference clock
- 1 kHz LPO clock
- 32.768 kHz crystal oscillator in iRTC power domain
- 1 MHz to 32 MHz crystal oscillator
- FLL and PLL

System peripherals

- Memory Protection Unit (MPU)
- 4-channel DMA controller
- Watchdog and EWM
- Low-leakage Wakeup Unit (LLWU)
- SWD debug interface and Micro Trace Buffer (MTB)
- Bit Manipulation Engine (BME)
- Inter-peripheral Crossbar Switch (XBAR)

Analog Modules

- 4 AFE channels (4× 24-bit ΣΔ ADCs with PGA)
- 16-channel 16-bit SAR ADC with 4 result registers
- High-speed analog comparator containing a 6-bit DAC and programmable reference input
- Internal 1.2 V reference voltage 10–15 ppm/°C

Memories

- Up to 512 KB program flash memory
- Up to 64 KB SRAM

Operating Characteristics

- Voltage range: 1.71 to 3.6 V (without AFE)
- Voltage range: 2.7 to 3.6 V (with AFE)
- Temperature range (ambient): –40 to 105 °C

Low power features

- 13 power modes to provide power optimization based on application requirements
- 8.82 mA @ 75 MHz run current
- Less than 220 µA very low power run current
- 6.05 µA very low power stop current
- Down to 261 nA deep sleep current
- V_{BAT} domain current < 1 µA with iRTC operational
- Low-power boot with less than 2.33 mA peak current

Communication interfaces

- 16-bit SPI modules
- Low-power UART module
- UART module complying with ISO7816-3
- Basic UART module
- I^2C with SMBus

Timers

- Quad Timer (QTMR)
- Periodic Interrupt Timer (PIT)
- Low Power Timer (LPTMR)
- Programmable Delay Block (PDB)
- Independent Real Time Clock (iRTC)

Human-machine interface

- Up to 4×60 (8×56, 6×58) segment LCD controller operating in all low-power modes
- General purpose input/output (GPIO)

Security and integrity modules

- Memory Mapped Cryptographic Acceleration Unit (MMCAU) for AES encryption
- Random Number Generator (RNGA), complying with NIST: SP800-90
- Programmable Cyclic Redundancy Check (PCRC)
- 80-bit unique identification number per chip

The following figure shows the functional modules in the chip.

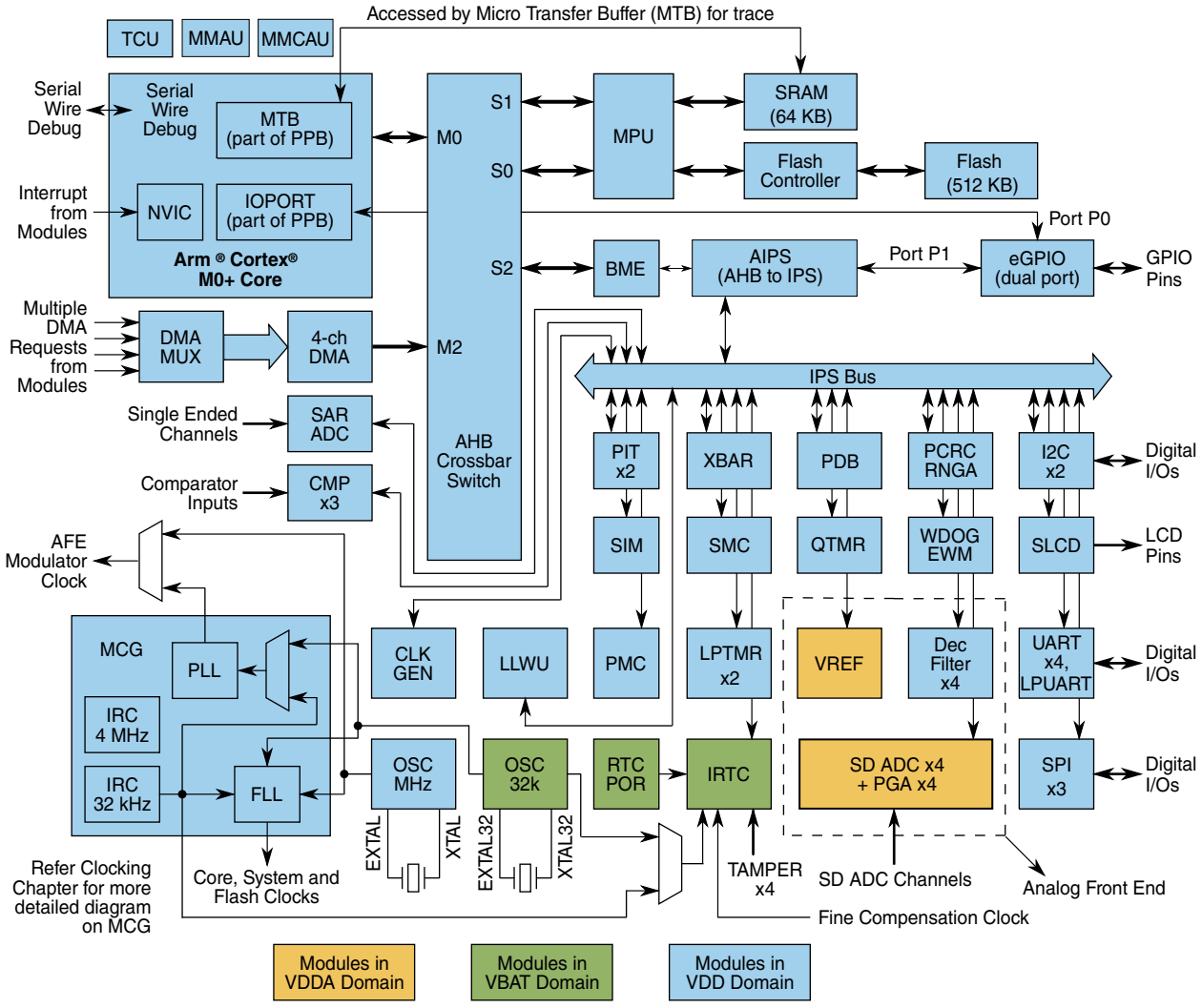


Figure 1. Functional block diagram

Ordering Information

Part Number [1]	Memory		ADC Channels	Maximum number of GPIOs	Security	SLCD	Package Type	Packaging Type
	Flash (KB)	SRAM (KB)						
MKM35Z256VLL7	256	64	12	72	CRC, MMCAU, RNG	Yes	LQFP 100	Tray
MKM35Z256VLQ7	256	64	16	99	CRC, MMCAU, RNG	Yes	LQFP 144	Tray
MKM35Z256VLL7R	256	64	12	72	CRC, MMCAU, RNG	Yes	LQFP 100	Reel
MKM35Z256VLQ7R	256	64	16	99	CRC, MMCAU, RNG	Yes	LQFP 144	Reel
MKM35Z512VLL7	512	64	12	72	CRC, MMCAU, RNG	Yes	LQFP 100	Tray
MKM35Z512VLQ7	512	64	16	99	CRC, MMCAU, RNG	Yes	LQFP 144	Tray
MKM35Z512VLL7R	512	64	12	72	CRC, MMCAU, RNG	Yes	LQFP 100	Reel
MKM35Z512VLQ7R	512	64	16	99	CRC, MMCAU, RNG	Yes	LQFP 144	Reel

1. To confirm current availability of orderable part numbers, go to http://www.nxp.com and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KM3xPB [1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KM35P144M75SF0RM
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document: KM35P144M75SF0
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_M_P90A
Package Drawing	Package dimensions are provided in package drawings.	100-LQFP: 98ASS23308W [1] 144-LQFP: 98ASS23177W [1]

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

Table of Contents

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model (All pins except RESET pin)	–4000	+4000	V	
	Electrostatic discharge voltage, human body model (RESET pin only)	–2500	+2500	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model (for corner pins)	–750	+750	V	
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	

1. Determined according to JEDEC Standard JS-001-2014, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JS-001-2014, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

1.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.6	V
V_{DIO}	Digital input voltage (except $\overline{RESET}$, EXTAL, and XTAL)	–0.3	V_{DD} + 0.3	V
$V_{DTamper}$	Tamper input voltage	–0.3	V_{BAT} + 0.3	V
V_{AIO}	Analog[1], $\overline{RESET}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{BAT}	RTC battery supply voltage	–0.3	3.6	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

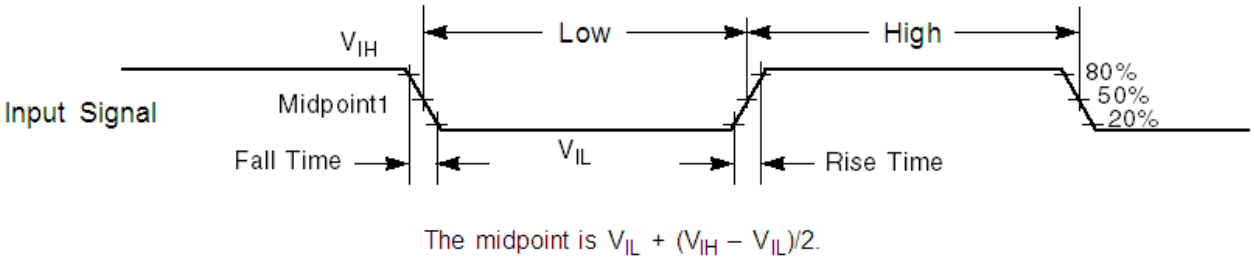


Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage when AFE is operational	2.7	3.6	V	
	Supply voltage when AFE is NOT operational	1.71	3.6	V	
V_{DDA}	Analog supply voltage	2.7	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	1
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICDIO}	Digital pin negative DC injection current — single pin • V_{IN} < V_{SS}–0.3 V	–5	—	mA	
I_{ICAIO}	Analog[2], EXTAL, and XTAL pin DC injection current — single pin • V_{IN} < V_{SS}–0.3 V (Negative current injection) • V_{IN} > V_{DD}+0.3 V (Positive current injection)	 –3 —	 — +3	mA	
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 –25 —	 — +25	mA	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. V_{BAT} always needs to be there for the chip to be operational.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	

Table continues on the next page...

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage.

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — low-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = 5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = 2.5 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{OL}	Output low voltage — low-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pull-up resistors	30	60	kΩ	1
R_{PD}	Internal pull-down resistors	30	60	kΩ	2

1. Measured at V_{input} = V_{SS}.
2. Measured at V_{input} = V_{DD}.

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 75 MHz
- Bus clock = 25 MHz
- Flash clock = 25 MHz
- Temperature: –40 °C, 25 °C, and 105 °C
- V_{DD}: 1.71 V, 3.3 V, and 3.6 V

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execute the first instruction across the operating temperature range of the chip.	563		659	µs	1
	• VLLS0 → RUN	—	370	382	µs	
	• VLLS1 → RUN	—	370	382	µs	
	• VLLS2 → RUN	—	270	275	µs	
	• VLLS3 → RUN	—	270	275	µs	
	• VLPS → RUN	—	5	6	µs	
	• STOP → RUN	—	5	6	µs	

1. Normal boot (FTFA_OPT[LPBOOT]=1)

2.2.5 Power consumption operating behaviors

NOTE

The maximum (Max.) values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3×sigma).

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 3.0 V	—	8.82	9.15	mA	
	• @ 3.0 V	—	8.80	9.13	mA	
	• 25 °C • –40 °C • 105 °C	—	9.19	9.59	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					2
	• @ 3.0 V	—	12.38	12.83	mA	
	• @ 3.0 V	—	12.32	12.76	mA	
	• 25 °C • –40 °C • 105 °C	—	12.67	13.1	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V— all peripheral clocks disabled and Flash is not in low-power					2
	• 25 °C	—	5.78	5.90	mA	
	• –40 °C	—	5.76	5.88	mA	
	• 105 °C	—	6.34	6.52	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V— all peripheral clocks disabled and Flash disabled (put in low-power)					2
	• 25 °C	—	4.56	4.6	mA	
	• –40 °C	—	4.56	4.68	mA	
	• 105 °C	—	4.98	5.15	mA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled					3
	• 25 °C	—	212	500	µA	
	• –40 °C	—	212	470	µA	
	• 105 °C	—	550	900	µA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled					4
	• 25 °C	—	343	530	µA	
	• –40 °C	—	327	507	µA	
	• 105 °C	—	638	1000	µA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled					5
	• 25 °C	—	133	350	µA	
	• –40 °C	—	132	330	µA	
	• 105 °C	—	475	800	µA	
I_{DD_STOP}	Stop mode current at 3.0 V					
	• 25 °C	—	406	730	µA	
	• –40 °C	—	386	700	µA	
	• 105 °C	—	792	898	µA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• 25 °C	—	6.05	46	µA	
	• –40 °C	—	2.68	44	µA	
	• 105 °C	—	347	700	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• 25 °C	—	2.78	3.86	µA	
	• –40 °C	—	2.16	3.85	µA	
	• 105 °C	—	61.9	85.0	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• 25 °C	—	2.45	3.06	µA	
	• –40 °C	—	2.10	3.04	µA	
	• 105 °C	—	40.2	59.5	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• 25 °C	—	1.20	2.14	µA	
	• –40 °C	—	1.07	1.84	µA	
	• 105 °C	—	30.8	38.8	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• 25 °C	—	0.261	0.67	µA	
	• –40 °C	—	0.222	0.64	µA	
	• 105 °C	—	29.1	38.0	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	• 25 °C	—	0.559	0.790	µA	
	• –40 °C	—	0.494	0.784	µA	
	• 105 °C	—	29.5	38.4	µA	
I_{DD_VBAT}	Average current with RTC and 32 kHz disabled at 3.0 V and VDD is OFF					
	• 25 °C	—	0.243	1.00	µA	
	• –40 °C	—	0.143	0.95	µA	
	• 105 °C	—	6.05	15	µA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes

I_{DD_VBAT}	Average current when VDD is OFF and LFSR and Tamper clocks set to 2 Hz.
	• @ 3.0 V
	  • 25 °C
	  • –40 °C
	  • 105 °C
		—	1.42
			1.24
			8.04
				3.00
				2.96
				16.0
					µA
					µA
					µA
						6, 7

1. See all related analog peripheral specifications for I_{DDA}.
2. 75 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FBE mode. All peripheral clocks disabled.
3. 2 MHz core/system clock, and 1 MHz bus/flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing while (1) loop from flash.
4. 2 MHz core/system clock, and 1 MHz bus/flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing while (1) loop from flash.
5. 2 MHz core/system clock, and 1 MHz bus/flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. No flash accesses; some activity on DMA & RAM assumed.
6. Includes 32 kHz oscillator current and RTC operation.
7. An external power switch for VBAT should be present on board to have better battery life and keep VBAT pin powered in all conditions. There is no internal power switch in RTC.

2.2.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for “EMC design.”

2.2.7 Capacitance attributes

Table 7. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF
$C_{IN\_D\_io60}$	Input capacitance: fast digital pins	—	9	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 8. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	75	MHz	
f_{BUS}	Bus clock	—	25	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{AFE}	AFE Modulator clock	—	6.5	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	1	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{AFE}	AFE Modulator clock[2]	—	1.6	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.
2. AFE working in low-power mode.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I^2C signals.

Table 9. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Asynchronous path	16	—	ns	
	External reset pulse width (digital glitch filter disabled)	100	—	ns	2
	Port rise and fall time				
	• Slew disabled				
	• $1.71 \le V_{DD} \le 2.7$ V	—	8	ns	
	• $2.7 \le V_{DD} \le 3.6$ V	—	5	ns	
	• Slew enabled				
	• $1.71 \le V_{DD} \le 2.7$ V	—	27	ns	
	• $2.7 \le V_{DD} \le 3.6$ V	—	16	ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 10. Thermal operating requirements

Symbol	Description	Min.	Max.[1]	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

1. Maximum T_A can be exceeded ***only if*** the user ensures that T_J does ***not*** exceed maximum T_J . The simplest method to determine T_J is:

   $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

2.4.2 Thermal attributes

Rating	Board Type[1]	Symbol	100 LQFP	144 LQFP	Unit
Junction to Ambient Thermal Resistance[2]	JESD51-7, 2s2p	$R_{\theta JA}$	48.6	41.7	°C/W
Junction-to-Top of Package Thermal Characterization Parameter [2]	JESD51-7, 2s2p	Ψ_{JT}	0.52	0.63	°C/W

1. Thermal test board meets JEDEC specification for this package (JESD51-7).
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 Single Wire Debug (SWD)

Table 11. SWD switching characteristics at 2.7 V (2.7–3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	20	MHz	
Inputs, t_{SUI}	Data setup time	5	ns	1
inputs, t_{HI}	Data hold time	0	ns	1
after clock edge, t_{DVO}	Data valid Time	32	ns	1
t_{HO}	Data Valid Hold	0	ns	1

1. Input transition assumed = 1 ns. Output transition assumed = 50 pF.

Table 12. Switching characteristics at 1.7 V (1.7–3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	18	MHz	
Inputs, t_{SUI}	Data setup time	4.7	ns	1
inputs, t_{HI}	Data hold time	0	ns	1
after clock edge, t_{DVO}	Data valid Time	49.4	ns	2
t_{HO}	Data Valid Hold	0	ns	1

1. Input transition assumed = 1 ns. Output transition assumed = 50 pF.
2. Frequency of SWD clock (18 MHz) is applicable only in case the input setup time of the device outside is not more than 6.15 ns, else the frequency of SWD clock would need to be lowered.

3.1.2 Analog Front End (AFE)

AFE switching characteristics at (2.7 V–3.6 V)

Case 1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to AFE clock defined at pad PTB7, PTE3, and PTK4).

Table 13. AFE switching characteristics (2.7 V–3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	10	MHz	
Inputs, t_{SUI}	Data setup time	5	ns	1
inputs, t_{HI}	Data hold time	0	ns	1

1. Input Transition: 1 ns. Output Load: 50 pF.

Case 2: Clock is going Out and Data is coming In (XBAR ports timed with respect to generated clock defined at the XBAR out ports).

Table 14. AFE switching characteristics (2.7 V–3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	6.2	MHz	
Inputs, t_{SUI}	Data setup time	36	ns	1
inputs, t_{HI}	Data hold time	0	ns	1

1. Input Transition: 1 ns. Output Load: 50 pF.

AFE switching characteristics at (1.7 V–3.6 V)

Case 1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to AFE clock defined at pad PTB7, PTE3, and PTK4).

Table 15. AFE switching characteristics (1.7 V–3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	13	MHz	
Inputs, t_{SUI}	Data setup time	30	ns	1
inputs, t_{HI}	Data hold time	5	ns	1

1. Input Transition: 1 ns. Output Load: 50 pF.

Case 2: Clock is going Out and Data is coming In (XBAR ports timed with respect to generated clock defined at XBAR out ports).

Table 16. AFE switching characteristics (1.7 V–3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	6.5	MHz	
Inputs, t_{SUI}	Data setup time	36	ns	1
inputs, t_{HI}	Data hold time	0	ns	1

1. Input Transition: 1 ns. Output Load: 50 pF.

3.2 Clock modules

3.2.1 MCG specifications

Table 17. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C		—	32.768	—	kHz	
Δf_{ints_t}	Total deviation of internal reference frequency (slow clock) over voltage and temperature		—	+0.5/-0.7	—	%	
Δf_{ints_t}	Total deviation of internal reference frequency (slow clock) over fixed voltage and full operating temperature range		-2	—	+2	%	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7		$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70 °C		—	± 0.4	—	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25 °C		—	4	—	MHz	
Δf_{intf_t}	Total deviation of internal reference frequency (fast clock) over voltage and temperature — factory trimmed at nominal V_{DD} and 25 °C		—	+1/-2	—	%	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{dco}	DCO output frequency range	Low-range (DRS=00) 640 × f_{ints_t}	20	20.97	22	MHz	2, 3
		Mid-range (DRS=01) 1280 × f_{ints_t}	40	41.94	45	MHz	
		Mid-high range (DRS=10) 1920 × f_{ints_t}	60	62.91	67	MHz	
		High-range (DRS=11) 2560 × f_{ints_t}	80	83.89	90	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low-range (DRS=00) 732 × f_{ints_t}	—	23.99	—	MHz	4, 5, 6

Table continues on the next page...

Table 17. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
		Mid-range (DRS=01) 1464 × f_{ints_t}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{ints_t}	—	71.99	—	MHz	
		High-range (DRS=11) 2929 × f_{ints_t}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter		—	70	140	ps	7
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	8
PLL							
f_{vco}	VCO operating frequency		11.71875	12.288	14.6484375	MHz	
I_{pll}	PLL operating current • IO 3.3 V current • Max core voltage current		—	300 100	—	μA	
f_{pll_ref}	PLL reference frequency range		31.25	32.768	39.0625	kHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 12 MHz				700	ps	
D_{lock}	Lock entry frequency tolerance		± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance		± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time		—	—	150×10^{-6} + 1075(1/f_{pll_ref})	s	

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. Chip maximum freq is 75 MHz, so high-range of DCO cannot be used and should not be configured.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. Chip max freq is 75 MHz, so High-range of DCO cannot be used and should not be configured.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.2.2 Oscillator electrical specifications

3.2.2.1 Oscillator DC electrical specifications

Table 18. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 1 MHz	—	200	—	µA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 1 MHz	—	300	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
	• 1 MHz resonator	—	6.6	—	kΩ	
	• 2 MHz resonator	—	3.3	—	kΩ	

Table continues on the next page...

Table 18. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• 4 MHz resonator	—	0	—	kΩ	
	• 8 MHz resonator	—	0	—	kΩ	
	• 16 MHz resonator	—	0	—	kΩ	
	• 20 MHz resonator	—	0	—	kΩ	
	• 32 MHz resonator	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation.
3. C_x and C_y can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

3.2.2.2 Oscillator frequency specifications

Table 19. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	1	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—		—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—		—	ms	

Table continues on the next page...

Table 19. Oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.2.3 32 kHz oscillator electrical characteristics

3.2.3.1 32 kHz Oscillator Maximum Ratings

NOTE

Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

Table 20. 32 kHz oscillator absolute maximum ratings

Num	Symbol	Description	Min.	Max.	Unit
1	$V_{DD33OSC}$	RTC oscillator (A_IP_OSC_3v32kVLP_NN_C90LP) Module 3.3V Analog Supply Voltage	–0.3	3.6	V
2	V_{EXTAL}	EXTAL Input Voltage	–0.3	3.6	V
3	V_{XTAL}	XTAL Input Voltage	–0.3	3.6	V
4	T_A	Operating Temperature Range (Packaged)	–40	135	°C

Table continues on the next page...

Table 20. 32 kHz oscillator absolute maximum ratings (continued)

Num	Symbol	Description	Min.	Max.	Unit
5	T_J	Operating Temperature Range (Junction)	–40	135	°C
6	T_{stg}	Storage Temperature Range	–65	150	°C

3.2.3.2 32 kHz oscillator DC electrical specifications

Table 21. 32 kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.2.3.3 32 kHz oscillator frequency specifications

Table 22. 32 kHz Crystal and Oscillator Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Crystal frequency	—	32.768	—	kHz	
T_A	Operating temperature	-40	—	105	°C	1
	Total crystal frequency tolerance	-500	—	500	ppm	2,3
C_L	Load capacitance	—	12.5	—	pF	2
ESR	Equivalent series resistance	—	—	80	kOhms	2
t_{start}	Crystal start-up time	—	1000	—	ms	4
$f_{ec\_extal32}$	External input clock frequency	—	32.768	—	kHz	5
v_{ec_xtal32}	External input clock amplitude	0.7	—	V_{DD}	V	6

1. Full temperature range of this device. A reduced range can be chosen to meet application needs.
2. Recommended crystal specification.
3. Sum of crystal initial frequency tolerance, crystal frequency stability, and aging tolerances given by crystal vendor.
4. Time from oscillator enable to clock stable. Dependent on the complete hardware configuration of the oscillator.
5. External oscillator connected to EXTAL32K. XTAL32K must be unconnected.
6. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of VSS to VDD.

3.3 Memories and memory interfaces

3.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.3.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—			ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.3.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—		ms	1
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	—
t_{ersall}	Erase All Blocks execution time	—			ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.3.1.3 Flash high voltage current behaviors

Table 25. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.3.1.4 Reliability specifications

Table 26. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 105 °C.

3.4 Analog

3.4.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

3.4.1.1 16-bit ADC operating conditions

Table 27. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	–100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	–100	0	+100	mV	2

Table continues on the next page...

Table 27. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{REFH}	ADC reference voltage high	Absolute	V_{DDA}	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low	Absolute	V_{SSA}	V_{SSA}	V_{SSA}	V	4
V_{ADIN}	Input voltage		V_{SSA}	—	V_{DDA}	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	5
f_{ADCK}	ADC conversion clock frequency	≤ 12-bit mode	1.0	—	18.0	MHz	6
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	6
C_{rate}	ADC conversion rate	≤ 12-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	kS/s	7
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	kS/s	7

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. V_{REFH} is internally tied to V_{DDA}.
4. V_{REFL} is internally tied to V_{SSA}.
5. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
6. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
7. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

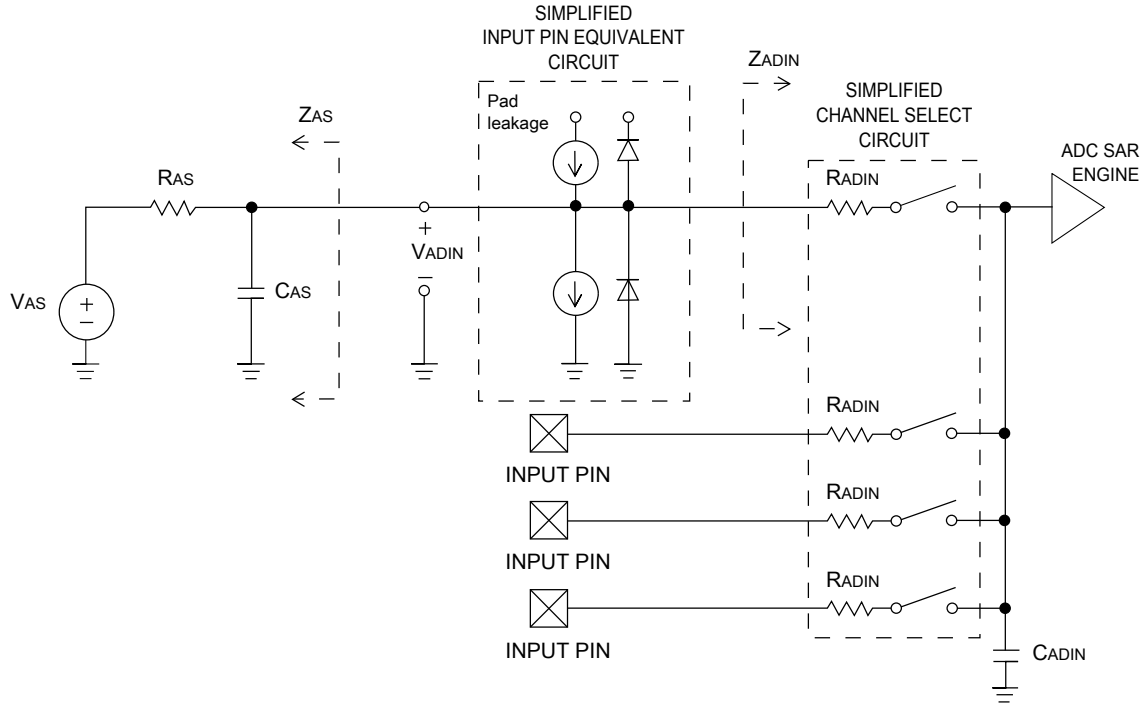


Figure 3. ADC input impedance equivalency diagram

3.4.1.2 16-bit ADC electrical characteristics

Table 28. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	t_{ADACK} = $1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to +0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9	LSB[4]	5

Table continues on the next page...

Table 28. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
		• <12-bit modes			–0.7 to +0.5		
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• 16-bit modes • 12-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit single-ended mode • Avg = 32	 — —	 –94 –85	 — —	dB dB	7
SFDR	Spurious free dynamic range	16-bit single-ended mode • Avg = 32	 82 78	 95 90	 — — 	dB dB	7
E_{IL}	Input leakage error		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

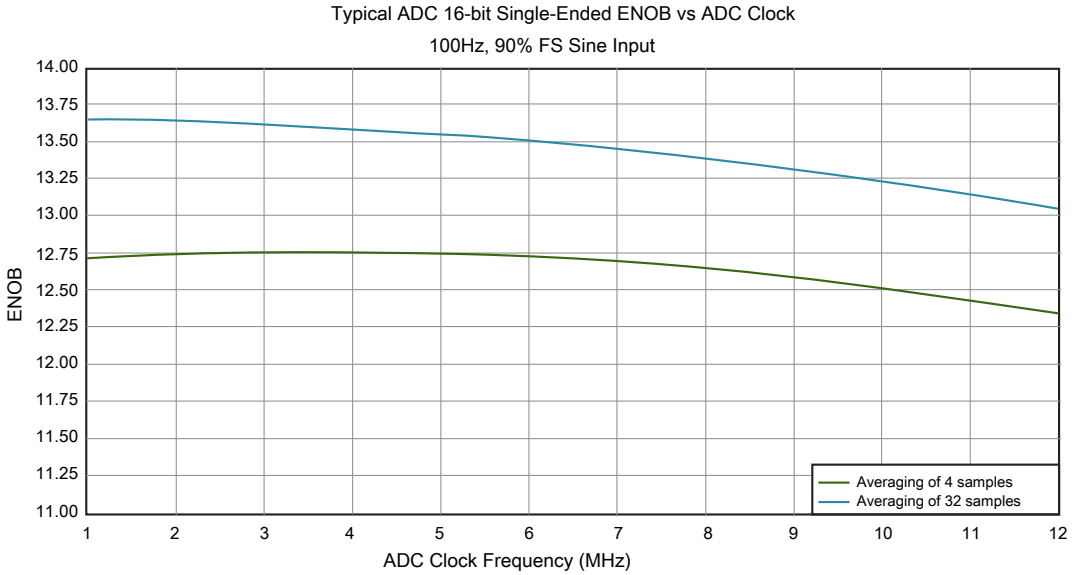


Figure 4. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.4.2 CMP and 6-bit DAC electrical specifications

Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, high-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V

Table continues on the next page...

Table 29. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

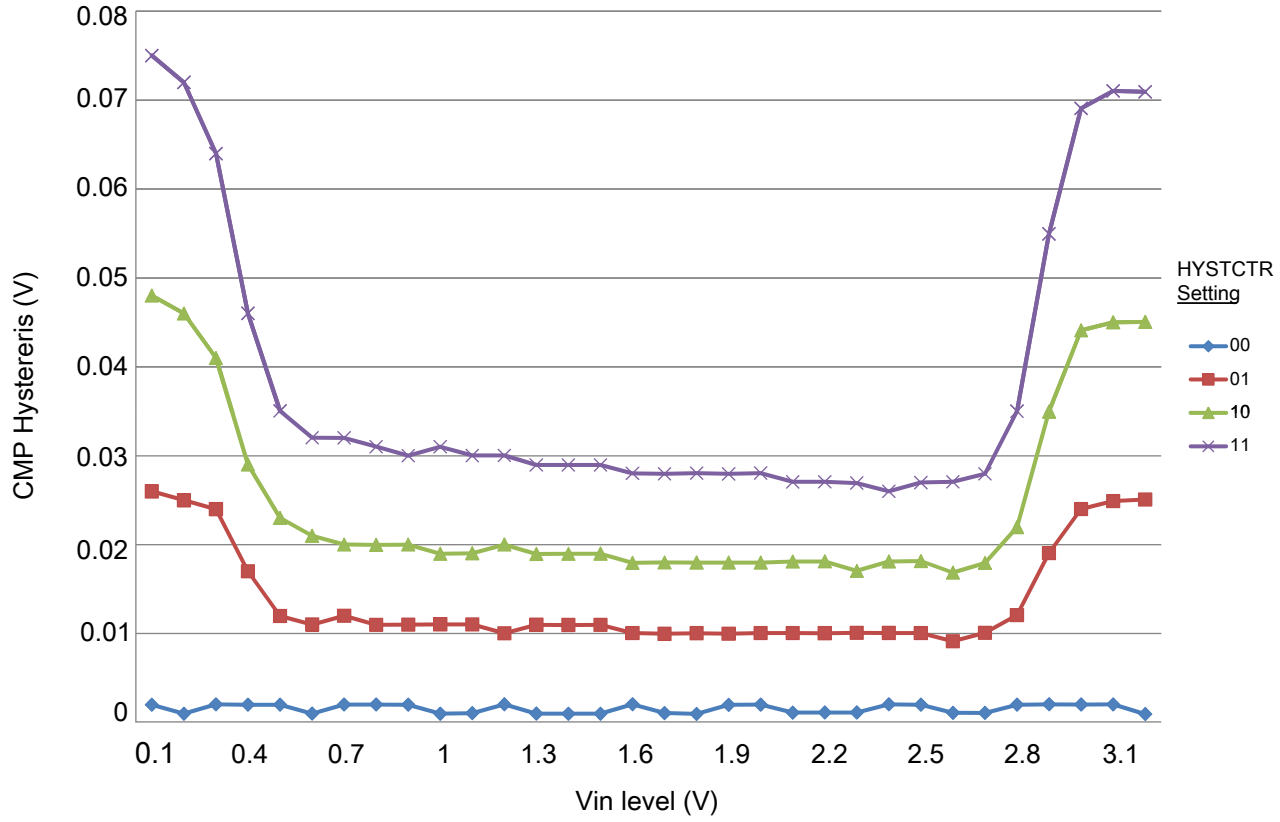


Figure 5. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

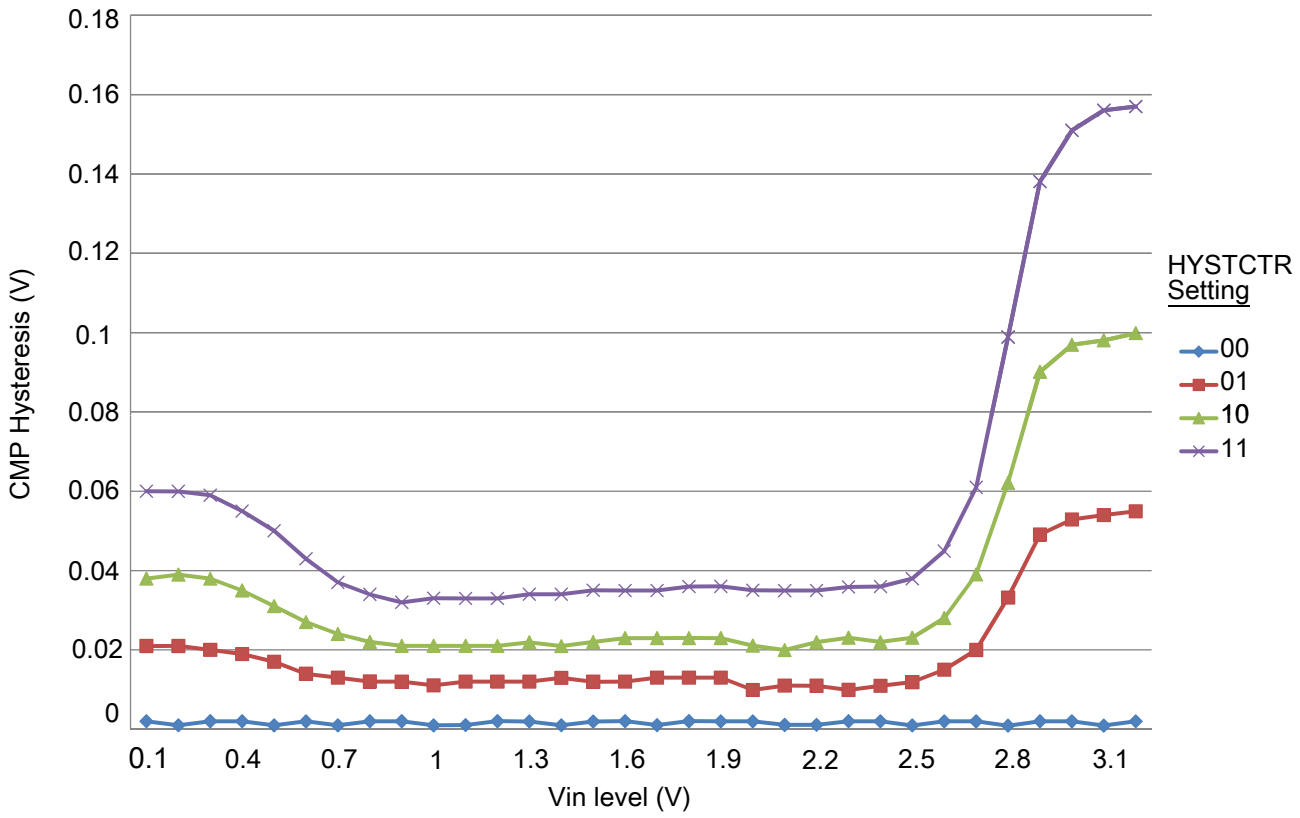


Figure 6. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.4.3 Voltage reference electrical specifications

Table 30. 1.2 VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	2.7 [1]	3.6	V	
T_A	Temperature	–40	105	°C	
C_L	Output load capacitance	100		nF	2, 3

1. AFE is enabled.
2. C_L must be connected between VREFH and VREFL.
3. The load capacitance should not exceed ±25% of the nominal specified C_L value over the operating temperature range of the device.

Table 31. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VREFH	Voltage reference output with factory trim at nominal V_{DDA} and temperature = 25 °C	1.1915	1.195	1.2027	V	
VREFH	Voltage reference output with — factory trim	1.1584	—	1.2376	V	
VREFH	Voltage reference output — user trim	1.178	—	1.202	V	
VREFL	Voltage reference output	0.38	0.4	0.42	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{tdrift}	Temperature drift when ICOMP = 0 across full temperature range	—	18	—	ppm/ºC	
	Temperature drift when ICOMP = 1 across full temperature range	—	6	—	ppm/°C	1
	Temperature drift when ICOMP = 1 across -40 ºC to 70 ºC	—	5	—	ppm/°C	1, 2
	Temperature drift when ICOMP = 1 across 0 ºC to 50 ºC	—	3	—	ppm/°C	1, 2
Ac	Aging coefficient	—	—	400	uV/yr	
I_{bg}	Bandgap only current	—	—	80	µA	2
I_{lp}	Low-power buffer current	—	—	0.19	mA	2
I_{hp}	High-power buffer current	—	—	0.5	mA	2
I_{LOAD}	VREF buffer current	–2	—	2	mA	3, 4
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	µV	2, 5
T_{stup}	Buffer startup time	—	—	200	µs	
$T_{chop\_osc\_stup}$	Internal bandgap start-up delay with chop oscilator enabled	—	—	20	ms	
V_{vdrift}	Voltage drift (VREFHmax -VREFHmin across the full voltage range)	—	0.5	—	mV	2

1. ICOMP=1 is recommended to get best temperature drift. CHOPEN bit = 1 is also recommended.
2. See the chip's Reference Manual for the appropriate settings of VREF Status and Control register.
3. 2 mA I_{LOAD} is only achievable for above 2.7 V V_{DDA} condition.
4. See the chip's Reference Manual for the appropriate settings of SIM Miscellaneous Control register.
5. Load regulation voltage is the difference between VREFH voltage with no load vs. voltage with defined load.

NOTE

Temperature drift per degree is ((VREFHmax-VREFHmin)/ (temperature range)/VREFHmin) in ppm/ºC.

3.4.4 AFE electrical specifications

3.4.4.1 ΣΔ ADC + PGA specifications

Table 32. ΣΔ ADC + PGA specifications

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
f_{Nyq}	Input bandwidth	Normal Mode	1.5	1.5	1.5	kHz	
		Low-Power Mode	1.5	1.5	1.5		
V_{CM}	Input Common Mode Reference		0		0.8	V	
VIN_{diff}	Differential input range	Gain = 1 (PGA ON/OFF)[2]		± 500		mV	
		Gain = 2		± 250		mV	
		Gain = 4		± 125		mV	
		Gain = 8		± 62		mV	
		Gain = 16		± 31		mV	
		Gain = 32		± 15		mV	
SNR	Signal to Noise Ratio	Normal Mode				dB	
		• f_{IN}=50 Hz; gain=01, common mode=0 V, V_{pp}=1000 mV (full range diff.)	90	92			
		• f_{IN}=50 Hz; gain=02, common mode=0 V, V_{pp}= 500 mV (differential ended)	88	90			
		• f_{IN}=50 Hz; gain=04, common mode=0 V, V_{pp}= 250 mV (differential ended)	82	86			
		• f_{IN}=50 Hz; gain=08, common mode=0 V, V_{pp}= 125 mV (differential ended)	76	82			
		• f_{IN}=50 Hz; gain=16, common mode=0 V, V_{pp}= 62 mV (differential ended)	70	78			
		• f_{IN}=50 Hz; gain=32, common mode=0 V, V_{pp}= 31 mV (differential ended)	64	74			
		Low-Power Mode				dB	
		• f_{IN}=50 Hz; gain=01, common mode=0 V, V_{pp}=1000 mV (full range diff.)	82	82			
		• f_{IN}=50 Hz; gain=02, common mode=0 V, V_{pp}= 500 mV (differential ended)	76	78			
		• f_{IN}=50 Hz; gain=04, common mode=0 V, V_{pp}= 250 mV (differential ended)	70	74			
		• f_{IN}=50 Hz; gain=08, common mode=0 V, V_{pp}= 125 mV (differential ended)	64	70			

Table continues on the next page...

Table 32. ΣΔ ADC + PGA specifications (continued)

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
		• f_{IN}=50 Hz; gain=16, common mode=0 V, V_{pp}= 62 mV (differential ended) • f_{IN}=50 Hz; gain=32, common mode=0 V, V_{pp}= 31 mV (differential ended)	58 52	66 62			
SINAD	Signal-to-Noise + Distortion Ratio	Normal Mode • f_{IN}=50 Hz; gain=01, common mode=0 V, V_{pp}=500 mV (differential ended)		78		dB	
		Low-Power Mode • f_{IN}=50 Hz; gain=01, common mode=0 V, V_{pp}=500 mV (differential ended)		74		dB	
CMMR	Common Mode Rejection Ratio	• f_{IN}=50 Hz; gain=01, common mode=0 V, Vid=100 mV • f_{IN}=50 Hz; gain=32, common mode=0 V, V_{id}=100 mV		70 70		dB	
E_{offset}	Offset Error	Gain=01, V_{pp}=1000 mV (full range diff.)			± 5	mV	
$\Delta Offset_{Temp}$	Offset Temperature Drift [3]	Gain=01, V_{pp}=1000 mV (full range diff.)			± 25	ppm/°C	
$\Delta Gain_{Temp}$	Gain Temperature Drift - Gain error caused by temperature drifts [4]	• Gain=01, V_{pp}=500 mV (differential ended) • Gain=32, V_{pp}=15 mV (differential ended)			± 75	ppm/°C	
$PSRR_{AC}$	AC Power Supply Rejection Ratio	Gain=01, VCC = 3 V ± 100 mV, f_{IN} = 50 Hz		60		dB	
XT	Crosstalk (with the input of the affected channel grounded)	Gain=01, V_{id} = 500 mV, f_{IN} = 50 Hz			-100	dB	
f_{MCLK}	Modulator Clock Frequency Range	Normal Mode Low-Power Mode	0.03 0.03		6.5 1.6	MHz	
I_{DDA_PGA}	Current consumption by PGA (each channel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048) Low-Power Mode (f_{MCLK} = 0.768 MHz, OSR= 256)			2.6 0	mA	5
I_{DDA_ADC}	Current Consumption by ADC (each channel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048) Low-Power Mode (f_{MCLK} = 0.768 MHz, OSR= 256)			1.4 0.5	mA	

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{MCLK} = 6.144 MHz, OSR = 2048 for Normal mode and f_{MCLK} = 768 kHz, OSR = 256 for low-power mode unless otherwise stated. All values are for reference only and are not tested in production.
2. The full-scale input range in single-ended mode is 0.5 V_{pp}.
3. Represents combined offset temperature drift of the PGA, SD ADC, and Internal 1.2 VREF blocks; Defined by shorting both differential inputs to ground.

4. Represents combined gain temperature drift of the PGA, SD ADC and Internal 1.2 VREF blocks.
5. PGA is disabled in low-power modes.

3.4.4.2 ΣΔ ADC Standalone specifications

Table 33. ΣΔ ADC standalone specifications

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
f_{Nyq}	Input bandwidth	Normal Mode	1.5	1.5	1.5	kHz	
		Low-Power Mode	1.5	1.5	1.5		
V_{CM}	Input Common Mode Reference		0		0.8	V	
VIN_{diff}	Input range	Differential		± 500		mV	
		Single-Ended		± 250		mV	
SNR	Signal to Noise Ratio	Normal Mode • f_{IN}=50 Hz; common mode=0 V, V_{pp}= 500 mV (differential ended) • f_{IN}=50 Hz; common mode=0 V, V_{pp}= 500 mV (full range se.) Low-Power Mode • f_{IN}=50 Hz; common mode=0 V, V_{pp}=500 mV (diff.) • f_{IN}=50 Hz; common mode=0 V, V_{pp}=500 mV (full range se.)	88 76	90 78		dB	
$\Delta Gain_{Temp}$	Gain Temperate Drift - Gain error caused by temperature drifts [2]	• Gain bypassed V_{pp} = 500 mV (differential) • PGA bypassed V_{pp} = 500 mV (differential), V_{CM} = 0 V			55	ppm/°C	
$\Delta Offset_{Temp}$	Offset Temperate Drift - Offset error caused by temperature drifts [3]	• Gain bypassed Vpp = 500 mV (differential), V_{CM} = 0 V			30	ppm/°C	
SINAD	Signal-to-Noise + Distortion Ratio	Normal Mode • f_{IN}=50 Hz; common mode=0 V, V_{pp}= 500 mV (diff.) • f_{IN}=50 Hz; common mode=0 V, V_{pp}= 500 mV (full range se.) Low-Power Mode • f_{IN}=50 Hz; common mode=0 V, V_{pp}=500 mV (diff.) • f_{IN}=50 Hz; common mode=0 V, V_{pp}=500 mV (full range se.)		80 74		dB	
CMMR	Common Mode Rejection Ratio	• f_{IN}=50 Hz; common mode=0 V, V_{id}=100 mV		90		dB	

Table continues on the next page...

Table 33. ΣΔ ADC standalone specifications (continued)

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
$PSRR_{AC}$	AC Power Supply Rejection Ratio	Gain=01, VCC = 3 V ± 100 mV, f_{IN} = 50 Hz		60		dB	
XT	Crosstalk	Gain=01, V_{id} = 500 mV, f_{IN} = 50 Hz			-100	dB	
f_{MCLK}	Modulator Clock Frequency Range	Normal Mode Low-Power Mode	0.03 0.03		6.5 1.6	MHz	
I_{DDA_ADC}	Current Consumption by ADC (each channel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048) Low-Power Mode (f_{MCLK} = 0.768 MHz, OSR= 256)			1.4 0.5	mA	

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{MCLK} = 6.144 MHz, OSR = 2048 for Normal mode and f_{MCLK} = 768 kHz, OSR = 256 for low-power mode unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Represents combined gain temperature drift of the SD ADC, and Internal 1.2 VREF blocks.
3. Represents combined offset temperature drift of the SD ADC, and Internal 1.2 VREF blocks; Defined by shorting both differential inputs to ground.

3.4.4.3 External modulator interface

The external modulator interface on this device comprises of a Clock signal and 1-bit data signal. Depending on the modulator device being used, the interface works as follows:

- Clock supplied to external modulator which drives data on rising edge and the KM35 device captures it on falling edge or next rising edge.
- Clock and data are supplied by external modulator and KM35 device can sample it on falling edge or next rising edge.

Depending on control bit in AFE, the sampling edge is changed.

3.5 Timers

See General switching specifications.

3.6 Communication interfaces

3.6.1 I2C switching specifications

See General switching specifications.

3.6.2 UART switching specifications

See General switching specifications.

3.6.3 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 34. SPI master mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For both SPI0 and SPI1, f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$

Table 35. SPI master mode timing on slew rate enabled pads

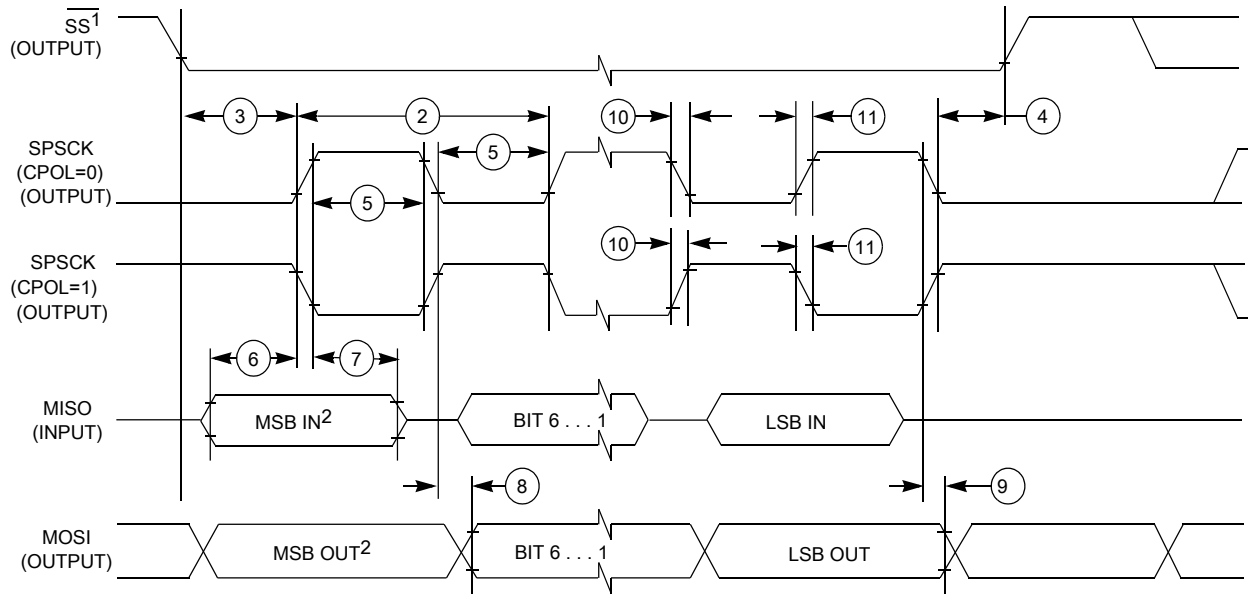
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1

Table continues on the next page...

Table 35. SPI master mode timing on slew rate enabled pads (continued)

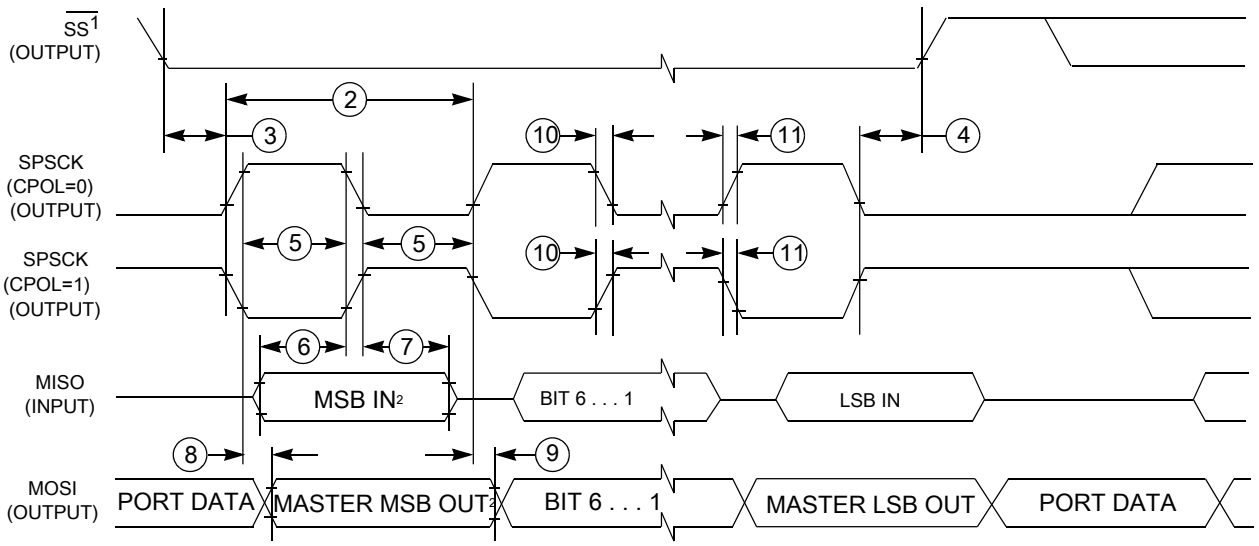
Num.	Symbol	Description	Min.	Max.	Unit	Note
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For both SPI0 and SPI1, f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 7. SPI master mode timing (CPHA = 0)



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 8. SPI master mode timing (CPHA = 1)

Table 36. SPI slave mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For both SPI0 and SPI1, f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

Table 37. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For both SPI0 and SPI1, f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

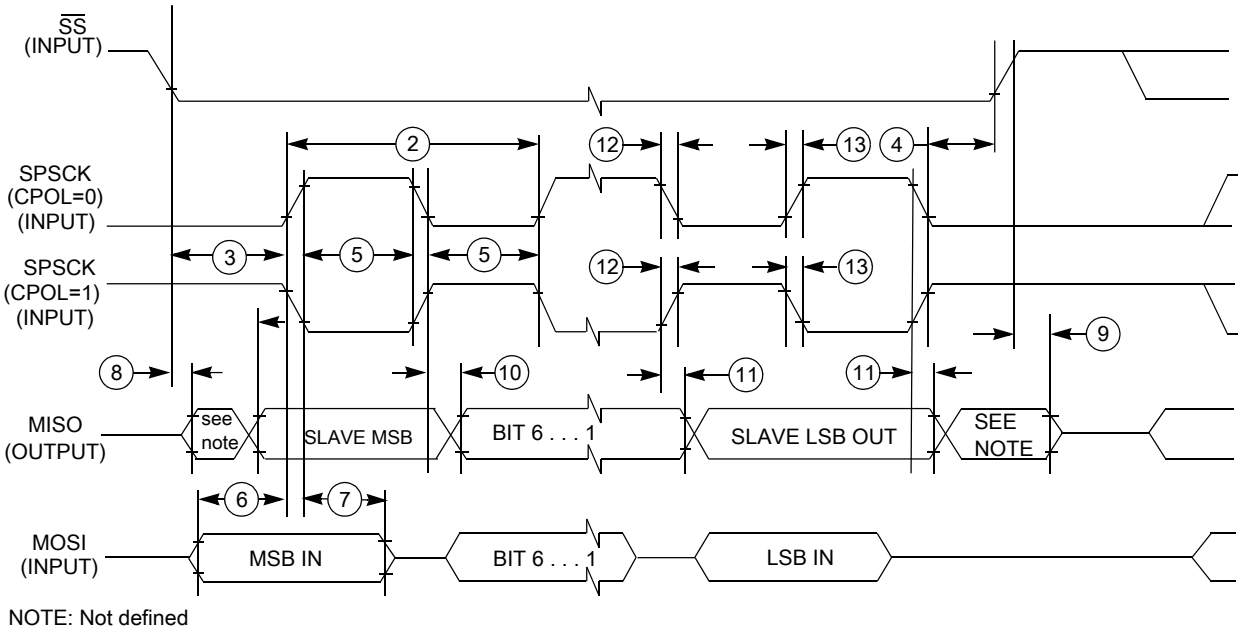


Figure 9. SPI slave mode timing (CPHA = 0)

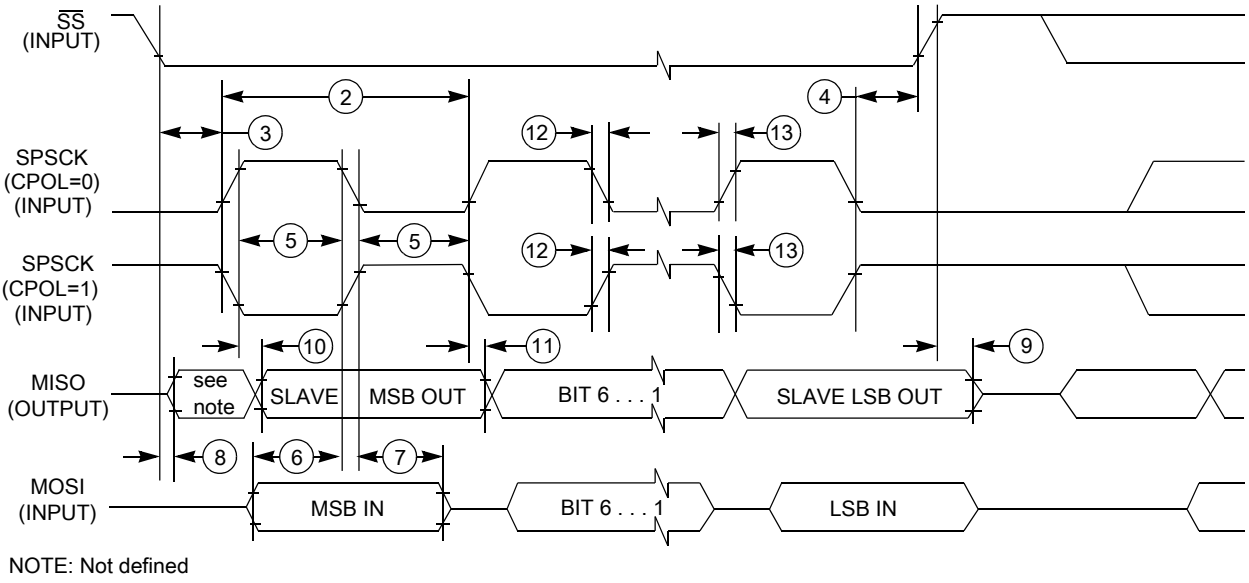


Figure 10. SPI slave mode timing (CPHA = 1)

3.7 Human-Machine Interfaces (HMI)

3.7.1 LCD electrical characteristics

Table 38. LCD electricals

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{Frame}	LCD frame frequency					
	• GCR[FFR]=0	23.3	—	73.1	Hz	
	• GCR[FFR]=1	46.6	—	146.2	Hz	
C_{LCD}	LCD charge pump capacitance — nominal value	—	100	—	nF	
C_{BYLCD}	LCD bypass capacitance — nominal value	—	100	—	nF	1
C_{Glass}	LCD glass capacitance	—	2000	8000	pF	2
V_{IREG}	V_{IREG}				V	3
	• RVTRIM=0000	—	0.91	—		
	• RVTRIM=1000	—	0.92	—		
	• RVTRIM=0100	—	0.93	—		
	• RVTRIM=1100	—	0.94	—		
	• RVTRIM=0010	—	0.96	—		
	• RVTRIM=1010	—	0.97	—		
	• RVTRIM=0110	—	0.98	—		
		—	0.99	—		

Table continues on the next page...

Table 38. LCD electricals (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• RVTRIM=1110	—	1.01	—		
	• RVTRIM=0001	—	1.02	—		
	• RVTRIM=1001	—	1.03	—		
	• RVTRIM=0101	—	1.05	—		
	• RVTRIM=1101	—	1.06	—		
	• RVTRIM=0011	—	1.07	—		
	• RVTRIM=1011	—	1.08	—		
	• RVTRIM=0111	—	1.09	—		
	• RVTRIM=1111					
Δ_{RTRIM}	V_{IREG} TRIM resolution	—	—	3.0	% V_{IREG}	
I_{VIREG}	V_{IREG} current adder — RVEN = 1	—	1	—	µA	
I_{RBIAS}	RBIAS current adder					
	• LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF)	—	10	—	µA	
	• LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	—	1	—	µA	
R_{RBIAS}	RBIAS resistor values					
	• LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF)	—	0.28	—	MΩ	
	• LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	—	2.98	—	MΩ	
VLL1	VLL1 voltage	—	—	V_{IREG}	V	4
VLL2	VLL2 voltage	—	—	2 x V_{IREG}	V	4
VLL3	VLL3 voltage	—	—	3 x V_{IREG}	V	4
VLL1	VLL1 voltage	—	—	V_{DDA} / 3	V	5
VLL2	VLL2 voltage	—	—	V_{DDA} / 1.5	V	5
VLL3	VLL3 voltage	—	—	V_{DDA}	V	5

1. The actual value used could vary with tolerance.
2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3. V_{IREG} maximum should never be externally driven to any level other than V_{DD} - 0.15 V
4. VLL1, VLL2 and VLL3 are a function of V_{IREG} only when the regulator is enabled (GCR[RVEN]=1) and the charge pump is enabled (GCR[CPSEL]=1).
5. VLL1, VLL2 and VLL3 are a function of V_{DDA} only under either of the following conditions:
   - The charge pump is enabled (GCR[CPSEL]=1), the regulator is disabled (GCR[RVEN]=0), and VLL3 = V_{DDA} through the internal power switch (GCR[VSUPPLY]=0).
   - The resistor bias string is enabled (GCR[CPSEL]=0), the regulator is disabled (GCR[RVEN]=0), and VLL3 is connected to V_{DDA} externally (GCR[VSUPPLY]=1).

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
100-pin LQFP	98ASS23308W
144-pin LQFP	98ASS23177W

5 Pinout

5.1 KM35 Signal multiplexing and pin assignments

NOTE

If use SLCD Fault Detection function, then corresponding SLCD functions at ALT6 or ALT7 need to be enabled. Otherwise don't need to enable them.

Table 39. Signal Multiplexing and Pin Assignments

100 LQFP	144 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	143	PTI4	LCD_P44	LCD_P44	PTI4	—	—	—	—	—	LCD_P44
—	144	NC	NC	NC	—	—	—	—	—	—	—
—	1	NC	NC	NC	—	—	—	—	—	—	—
—	2	NC	NC	NC	—	—	—	—	—	—	—
—	3	PTI5	LCD_P45	LCD_P45	PTI5	—	—	—	—	—	LCD_P45
1	4	PTA0/ LLWU_P16	LCD_P23	LCD_P23	PTA0/ LLWU_P16	—	—	—	—	—	LCD_P23

Table continues on the next page...

Table 39. Signal Multiplexing and Pin Assignments (continued)

100 LQFP	144 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
2	5	PTA1	LCD_P24	LCD_P24	PTA1	—	—	—	—	—	LCD_P24
—	6	PTI6	LCD_P46	LCD_P46	PTI6	UART2_RX	—	—	—	—	LCD_P46
—	7	PTI7	LCD_P47	LCD_P47	PTI7	UART2_TX	—	—	—	—	LCD_P47
3	8	PTA2	LCD_P25	LCD_P25	PTA2	—	—	—	—	—	LCD_P25
4	9	PTA3	LCD_P26	LCD_P26	PTA3	—	—	—	—	—	LCD_P26
5	10	PTA4/ LLWU_P15	NMI_b	LCD_P27	PTA4/ LLWU_P15	—	—	—	—	LCD_P27	NMI_b
6	11	PTA5	LCD_P28	LCD_P28	PTA5	CMP0_OUT	—	—	—	—	LCD_P28
7	12	PTA6/ LLWU_P14	LCD_P29	LCD_P29	PTA6/ LLWU_P14	XBAR_IN0	—	—	—	—	LCD_P29
8	13	PTA7	LCD_P30	LCD_P30	PTA7	XBAR_OUT0	—	—	—	—	LCD_P30
—	14	PTJ0	LCD_P48	LCD_P48	PTJ0	I2C1_SDA	—	—	—	—	LCD_P48
—	15	PTJ1	LCD_P49	LCD_P49	PTJ1	I2C1_SCL	—	—	—	—	LCD_P49
9	16	PTB0	LCD_P31	LCD_P31	PTB0	—	—	—	—	—	LCD_P31
—	17	PTJ2	LCD_P50	LCD_P50	PTJ2	—	—	—	—	—	LCD_P50
10	18	VDD	VDD	VDD	—	—	—	—	—	—	—
11	19	VSS	VSS	VSS	—	—	—	—	—	—	—
12	20	PTB1/ LLWU_P17	LCD_P32	LCD_P32	PTB1/ LLWU_P17	—	—	—	—	—	LCD_P32
13	21	PTB2	LCD_P33	LCD_P33	PTB2	SPI2_PCS0	—	—	—	—	LCD_P33
14	22	PTB3	LCD_P34	LCD_P34	PTB3	SPI2_SCK	—	—	—	—	LCD_P34
15	23	PTB4	LCD_P35	LCD_P35	PTB4	SPI2_MISO	—	—	—	—	LCD_P35
16	24	PTB5	LCD_P36	LCD_P36	PTB5	SPI2_MOSI	—	—	—	—	LCD_P36

Table continues on the next page...

Table 39. Signal Multiplexing and Pin Assignments (continued)

100 LQFP	144 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
17	25	PTB6	LCD_P37/ CMP1_IN0	LCD_P37/ CMP1_IN0	PTB6	—	—	—	—	—	LCD_P37
18	26	PTB7	LCD_P38	LCD_P38	PTB7	AFE_CLK	—	—	—	—	LCD_P38
19	27	PTC0	LCD_P39	LCD_P39	PTC0	UART3_RTS_b	XBAR_IN1	PDB0_EXTRG	—	—	LCD_P39
20	28	PTC1	LCD_P40/ CMP1_IN1	LCD_P40/ CMP1_IN1	PTC1	UART3_CTS_b	—	—	—	—	LCD_P40
21	29	PTC2	LCD_P41	LCD_P41	PTC2	UART3_TX	XBAR_OUT1	—	—	—	LCD_P41
22	30	PTC3/ LLWU_P13	LCD_P42/ CMP0_IN3	LCD_P42/ CMP0_IN3	PTC3/ LLWU_P13	UART3_RX	—	—	—	—	LCD_P42
23	31	PTC4	LCD_P43	LCD_P43	PTC4	—	—	—	—	—	LCD_P43
24	32	VBAT	VBAT	VBAT	—	—	—	—	—	—	—
25	33	XTAL32	XTAL32	XTAL32	—	—	—	—	—	—	—
26	34	EXTAL32	EXTAL32	EXTAL32	—	—	—	—	—	—	—
—	35	NC	NC	NC	—	—	—	—	—	—	—
—	36	NC	NC	NC	—	—	—	—	—	—	—
—	37	NC	NC	NC	—	—	—	—	—	—	—
—	38	NC	NC	NC	—	—	—	—	—	—	—
27	39	VSS	VSS	VSS	—	—	—	—	—	—	—
28	40	TAMPER2	TAMPER2	TAMPER2	—	—	—	—	—	—	—
29	41	TAMPER1	TAMPER1	TAMPER1	—	—	—	—	—	—	—
30	42	TAMPER0	TAMPER0	TAMPER0	—	—	—	—	—	—	—
31	43	AFE_VDDA	AFE_VDDA	AFE_VDDA	—	—	—	—	—	—	—
32	44	AFE_VSSA	AFE_VSSA	AFE_VSSA	—	—	—	—	—	—	—
33	45	AFE_SDADP0	AFE_SDADP0	AFE_SDADP0	—	—	—	—	—	—	—
34	46	AFE_SDADM0	AFE_SDADM0	AFE_SDADM0	—	—	—	—	—	—	—

Table continues on the next page...

Table 39. Signal Multiplexing and Pin Assignments (continued)

100 LQFP	144 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
35	47	AFE_SDADP1	AFE_SDADP1	AFE_SDADP1	—	—	—	—	—	—	—
36	48	AFE_SDADM1	AFE_SDADM1	AFE_SDADM1	—	—	—	—	—	—	—
37	49	VREFH	VREFH	VREFH	—	—	—	—	—	—	—
38	50	VREFL	VREFL	VREFL	—	—	—	—	—	—	—
39	51	AFE_SDADP2/CMP1_IN2	AFE_SDADP2/CMP1_IN2	AFE_SDADP2/CMP1_IN2	—	—	—	—	—	—	—
40	52	AFE_SDADM2/CMP1_IN3	AFE_SDADM2/CMP1_IN3	AFE_SDADM2/CMP1_IN3	—	—	—	—	—	—	—
41	53	VREF	VREF	VREF	—	—	—	—	—	—	—
42	54	AFE_SDADP3/CMP1_IN4	AFE_SDADP3/CMP1_IN4	AFE_SDADP3/CMP1_IN4	—	—	—	—	—	—	—
43	55	AFE_SDADM3/CMP1_IN5	AFE_SDADM3/CMP1_IN5	AFE_SDADM3/CMP1_IN5	—	—	—	—	—	—	—
—	56	NC	NC	NC	—	—	—	—	—	—	—
—	57	NC	NC	NC	—	—	—	—	—	—	—
44	58	PTC5/LLWU_P12	ADC0_SE0/CMP2_IN0	ADC0_SE0/CMP2_IN0	PTC5/LLWU_P12	UART0_RTS_b	—	LPTMR1_ALT1	—	—	—
45	59	PTC6	ADC0_SE1/CMP2_IN1	ADC0_SE1/CMP2_IN1	PTC6	UART0_CTS_b	QTMR0_TMR1	PDB0_EXTRG	—	—	—
46	60	PTC7	ADC0_SE2/CMP2_IN2	ADC0_SE2/CMP2_IN2	PTC7	UART0_TX	XBAR_OUT2	—	—	—	—
47	61	PTD0/LLWU_P11	CMP0_IN0	CMP0_IN0	PTD0/LLWU_P11	UART0_RX	XBAR_IN2	—	—	—	—
—	62	PTJ3	DISABLED	—	PTJ3	LPUART0_RTS_b	CMP2_OUT	—	—	—	—
—	63	PTJ4	DISABLED	—	PTJ4	LPUART0_CTS_b	LPTMR1_ALT1	—	—	—	—

Table continues on the next page...

Table 39. Signal Multiplexing and Pin Assignments (continued)

100 LQFP	144 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
48	64	PTD1	DISABLED	—	PTD1	UART1_TX	SPI0_PCS0	XBAR_OUT3	QTMR0_TMR3	—	—
49	65	PTD2/LLWU_P10	CMP0_IN1	CMP0_IN1	PTD2/LLWU_P10	UART1_RX	SPI0_SCK	XBAR_IN3	—	—	—
—	66	PTJ5	DISABLED	—	PTJ5	LPUART0_TX	—	—	—	—	—
—	67	PTJ6/LLWU_P18	DISABLED	—	PTJ6/LLWU_P18	LPUART0_RX	—	—	—	—	—
—	68	PTJ7	DISABLED	—	PTJ7	LPTMR1_ALT2	—	—	—	—	—
50	69	PTD3	DISABLED	—	PTD3	UART1_CTS_b	SPI0_MOSI	LPTMR1_ALT2	—	—	—
—	70	PTK0	ADC0_SE12	ADC0_SE12	PTK0	LPTMR1_ALT3	—	—	—	—	—
—	71	NC	NC	NC	—	—	—	—	—	—	—
—	72	NC	NC	NC	—	—	—	—	—	—	—
—	73	NC	NC	NC	—	—	—	—	—	—	—
—	74	NC	NC	NC	—	—	—	—	—	—	—
—	75	PTK1	ADC0_SE13	ADC0_SE13	PTK1	—	—	—	—	—	—
51	76	PTD4/LLWU_P9	ADC0_SE3	ADC0_SE3	PTD4/LLWU_P9	UART1_RTS_b	SPI0_MISO	LPTMR1_ALT3	—	—	—
52	77	PTD5	ADC0_SE4a	ADC0_SE4a	PTD5	LPTMR0_ALT3	QTMR0_TMR0	UART3_CTS_b	—	—	—
53	78	PTD6/LLWU_P8	ADC0_SE5a	ADC0_SE5a	PTD6/LLWU_P8	LPTMR0_ALT2	CMP1_OUT	UART3_RTS_b	—	—	—
54	79	PTD7/LLWU_P7	CMP0_IN4	CMP0_IN4	PTD7/LLWU_P7	I2C0_SCL	XBAR_IN4	UART3_RX	—	—	—
55	80	PTE0	DISABLED	—	PTE0	I2C0_SDA	XBAR_OUT4	UART3_TX	CLKOUT	—	—
—	81	PTK2	ADC0_SE14	ADC0_SE14	PTK2	UART0_TX	—	—	—	—	—
—	82	PTK3/LLWU_P19	ADC0_SE15	ADC0_SE15	PTK3/LLWU_P19	UART0_RX	—	—	—	—	—
56	83	PTE1	RESET_b	—	PTE1	—	—	—	—	—	RESET_b
57	84	PTE2	EXTAL	EXTAL	PTE2	EWM_IN	XBAR_IN6	I2C1_SDA	—	—	—

Table continues on the next page...

Table 39. Signal Multiplexing and Pin Assignments (continued)

100 LQFP	144 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
58	85	PTE3	XTAL	XTAL	PTE3	EWM_OUT_b	AFE_CLK	I2C1_SCL	—	—	—
59	86	VSS	VSS	VSS	—	—	—	—	—	—	—
60	87	VSSA	VSSA	VSSA	—	—	—	—	—	—	—
61	88	VDDA	VDDA	VDDA	—	—	—	—	—	—	—
62	89	VDD	VDD	VDD	—	—	—	—	—	—	—
63	90	PTE4	DISABLED	—	PTE4	LPTMR0_ALT1	UART2_CTS_b	EWM_IN	—	—	—
64	91	PTE5/ LLWU_P6	DISABLED	—	PTE5/ LLWU_P6	QTMR0_TMR3	UART2_RTS_b	EWM_OUT_b	—	—	—
65	92	PTE6/ LLWU_P5	SWD_DIO	CMP0_IN2	PTE6/ LLWU_P5	XBAR_IN5	UART2_RX	—	I2C0_SCL	—	SWD_DIO
66	93	PTE7	SWD_CLK	ADC0_SE6a	PTE7	XBAR_OUT5	UART2_TX	—	I2C0_SDA	—	SWD_CLK
67	94	PTF0/ LLWU_P4	ADC0_SE7a/ CMP2_IN3	ADC0_SE7a/ CMP2_IN3	PTF0/ LLWU_P4	RTC_CLKOUT	QTMR0_TMR2	CMP0_OUT	—	—	—
68	95	PTF1	LCD_P0/ ADC0_SE8/ CMP2_IN4	LCD_P0/ ADC0_SE8/ CMP2_IN4	PTF1	QTMR0_TMR0	XBAR_OUT6	—	—	—	LCD_P0
69	96	PTF2	LCD_P1/ ADC0_SE9/ CMP2_IN5	LCD_P1/ ADC0_SE9/ CMP2_IN5	PTF2	CMP1_OUT	RTC_CLKOUT	—	—	—	LCD_P1
—	97	PTK4	LCD_P51	LCD_P51	PTK4	XBAR_IN9	AFE_CLK	—	—	—	LCD_P51
—	98	PTK5	DISABLED	—	PTK5	UART1_RX	—	—	—	—	—
—	99	PTK6	DISABLED	—	PTK6	UART1_TX	—	—	—	—	—
70	100	PTF3/ LLWU_P20	LCD_P2	LCD_P2	PTF3/ LLWU_P20	SPI1_PCS0	LPTMR0_ALT2	UART0_RX	—	—	LCD_P2
71	101	PTF4	LCD_P3	LCD_P3	PTF4	SPI1_SCK	LPTMR0_ALT1	UART0_TX	—	—	LCD_P3
72	102	PTF5	LCD_P4	LCD_P4	PTF5	SPI1_MISO	I2C1_SCL	—	—	—	LCD_P4

Table continues on the next page...

Table 39. Signal Multiplexing and Pin Assignments (continued)

100 LQFP	144 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
73	103	PTF6/ LLWU_P3	LCD_P5	LCD_P5	PTF6/ LLWU_P3	SPI1_MOSI	I2C1_SDA	—	—	—	LCD_P5
74	104	PTF7	LCD_P6	LCD_P6	PTF7	QTMR0_TMR2	CLKOUT	CMP2_OUT	—	—	LCD_P6
—	105	PTK7	LCD_P52	LCD_P52	PTK7	I2C0_SCL	XBAR_OUT9	—	—	—	LCD_P52
—	106	PTL0	LCD_P53	LCD_P53	PTL0	I2C0_SDA	—	—	—	—	LCD_P53
—	107	NC	NC	NC	—	—	—	—	—	—	—
—	108	NC	NC	NC	—	—	—	—	—	—	—
—	109	NC	NC	NC	—	—	—	—	—	—	—
75	110	PTG0	LCD_P7	LCD_P7	PTG0	QTMR0_TMR1	LPTMR0_ALT3	—	—	—	LCD_P7
76	111	PTG1/ LLWU_P2	LCD_P8/ ADC0_SE10	LCD_P8/ ADC0_SE10	PTG1/ LLWU_P2	—	LPTMR0_ALT1	—	—	—	LCD_P8
77	112	PTG2/ LLWU_P1	LCD_P9/ ADC0_SE11	LCD_P9/ ADC0_SE11	PTG2/ LLWU_P1	SPI0_PCS0	—	—	—	—	LCD_P9
78	113	PTG3	LCD_P10	LCD_P10	PTG3	SPI0_SCK	I2C0_SCL	—	—	—	LCD_P10
79	114	PTG4	LCD_P11	LCD_P11	PTG4	SPI0_MOSI	I2C0_SDA	—	—	—	LCD_P11
80	115	PTG5	LCD_P12	LCD_P12	PTG5	SPI0_MISO	LPTMR0_ALT2	—	—	—	LCD_P12
81	116	PTG6/ LLWU_P0	LCD_P13	LCD_P13	PTG6/ LLWU_P0	—	LPTMR0_ALT3	—	—	—	LCD_P13
82	117	PTG7	LCD_P14	LCD_P14	PTG7	—	LPTMR1_ALT1	—	—	—	LCD_P14
83	118	PTH0	LCD_P15	LCD_P15	PTH0	LPUART0_CTS_b	—	—	—	—	LCD_P15
84	119	PTH1	LCD_P16	LCD_P16	PTH1	LPUART0_RTS_b	—	—	—	—	LCD_P16
85	120	PTH2	LCD_P17	LCD_P17	PTH2	LPUART0_RX	—	—	—	—	LCD_P17
86	121	PTH3	LCD_P18	LCD_P18	PTH3	LPUART0_TX	—	—	—	—	LCD_P18
87	122	PTH4	LCD_P19	LCD_P19	PTH4	—	LPTMR1_ALT2	—	—	—	LCD_P19

Table continues on the next page...

Table 39. Signal Multiplexing and Pin Assignments (continued)

100 LQFP	144 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
88	123	PTH5	LCD_P20	LCD_P20	PTH5	—	LPTMR1_ALT3	—	—	—	LCD_P20
89	124	PTH6	DISABLED	—	PTH6	UART1_CTS_b	SPI1_PCS0	XBAR_IN7	—	—	—
90	125	PTH7	DISABLED	—	PTH7	UART1_RTS_b	SPI1_SCK	XBAR_OUT7	—	—	—
91	126	PTI0/ LLWU_P21	CMP0_IN5	CMP0_IN5	PTI0/ LLWU_P21	UART1_RX	XBAR_IN8	SPI1_MISO	SPI1_MOSI	—	—
92	127	PTI1	DISABLED	—	PTI1	UART1_TX	XBAR_OUT8	SPI1_MOSI	SPI1_MISO	—	—
—	128	PTL1	LCD_P54	LCD_P54	PTL1	XBAR_IN10	—	—	—	—	LCD_P54
—	129	PTL2	LCD_P55	LCD_P55	PTL2	XBAR_OUT10	—	—	—	—	LCD_P55
93	130	PTI2/ LLWU_P22	LCD_P21	LCD_P21	PTI2/ LLWU_P22	LPUART0_RX	—	—	—	—	LCD_P21
94	131	PTI3	LCD_P22	LCD_P22	PTI3	LPUART0_TX	CMP2_OUT	—	—	—	LCD_P22
95	132	VSS	VSS	VSS	—	—	—	—	—	—	—
—	133	VDD	VDD	VDD	—	—	—	—	—	—	—
96	134	VLL3	VLL3	VLL3	—	—	—	—	—	—	—
97	135	VLL2	VLL2/ LCD_P60	VLL2/ LCD_P60	PTM0	—	—	—	—	—	LCD_P60
98	136	VLL1	VLL1/ LCD_P61	VLL1/ LCD_P61	PTM1	—	—	—	—	—	LCD_P61
99	137	VCAP2	VCAP2/ LCD_P62	VCAP2/ LCD_P62	PTM2	—	—	—	—	—	LCD_P62
100	138	VCAP1	VCAP1/ LCD_P63	VCAP1/ LCD_P63	PTM3	—	—	—	—	—	LCD_P63
—	139	PTL3	LCD_P56	LCD_P56	PTL3	EWM_IN	—	—	—	—	LCD_P56
—	140	PTL4	LCD_P57	LCD_P57	PTL4	EWM_OUT_b	—	—	—	—	LCD_P57
—	141	PTL5/ LLWU_P23	LCD_P58	LCD_P58	PTL5/ LLWU_P23	—	—	—	—	—	LCD_P58
—	142	PTL6	LCD_P59	LCD_P59	PTL6	—	—	—	—	—	LCD_P59

5.2 KM35 Pinouts

5.2.1 100-pin LQFP

The following figure represents the KM35 100 LQFP pinouts.

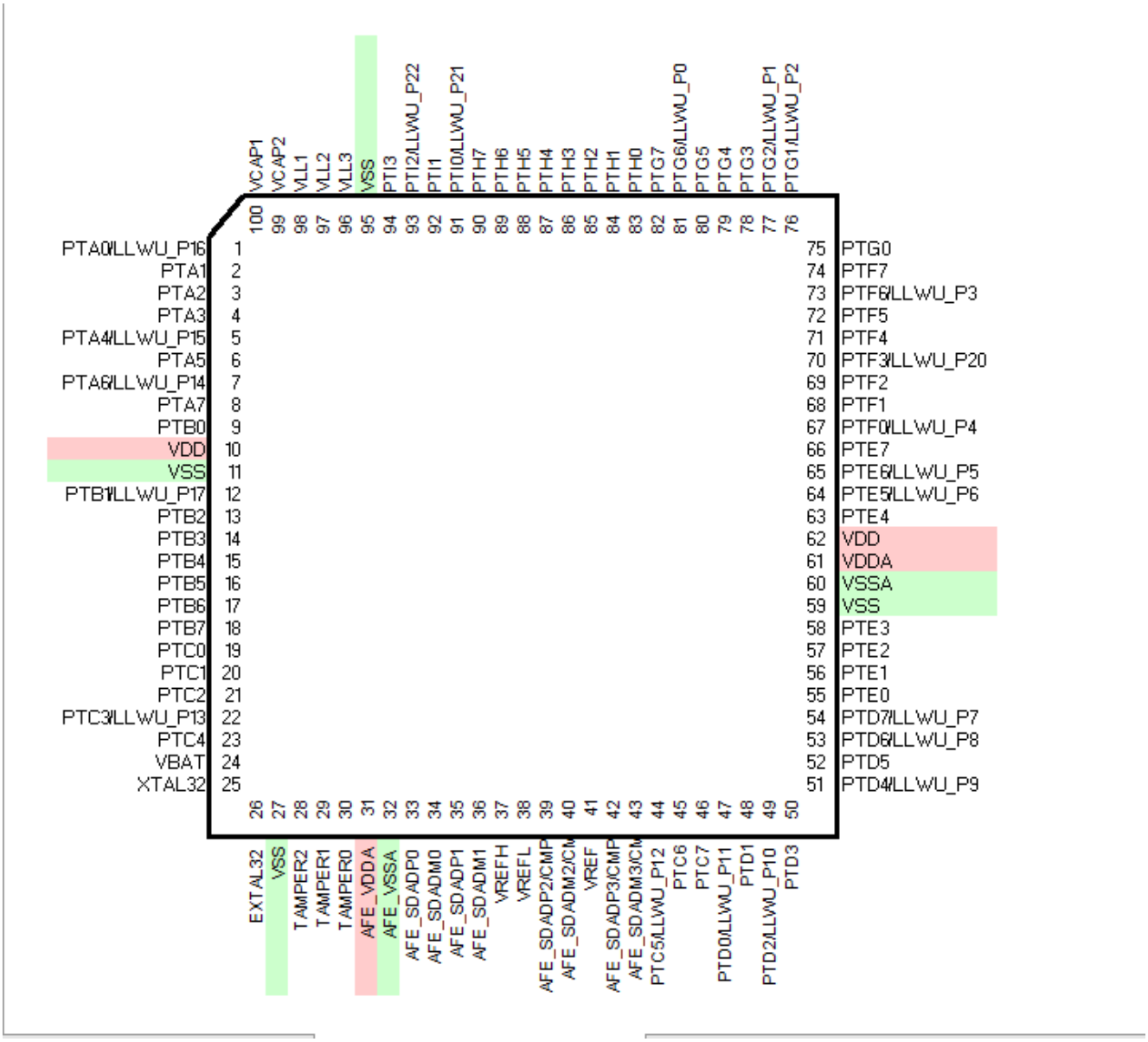


Figure 11. 100-pin LQFP Pinout Diagram

5.2.2 144-pin LQFP

The following figure represents the KM35 144 LQFP pinouts:

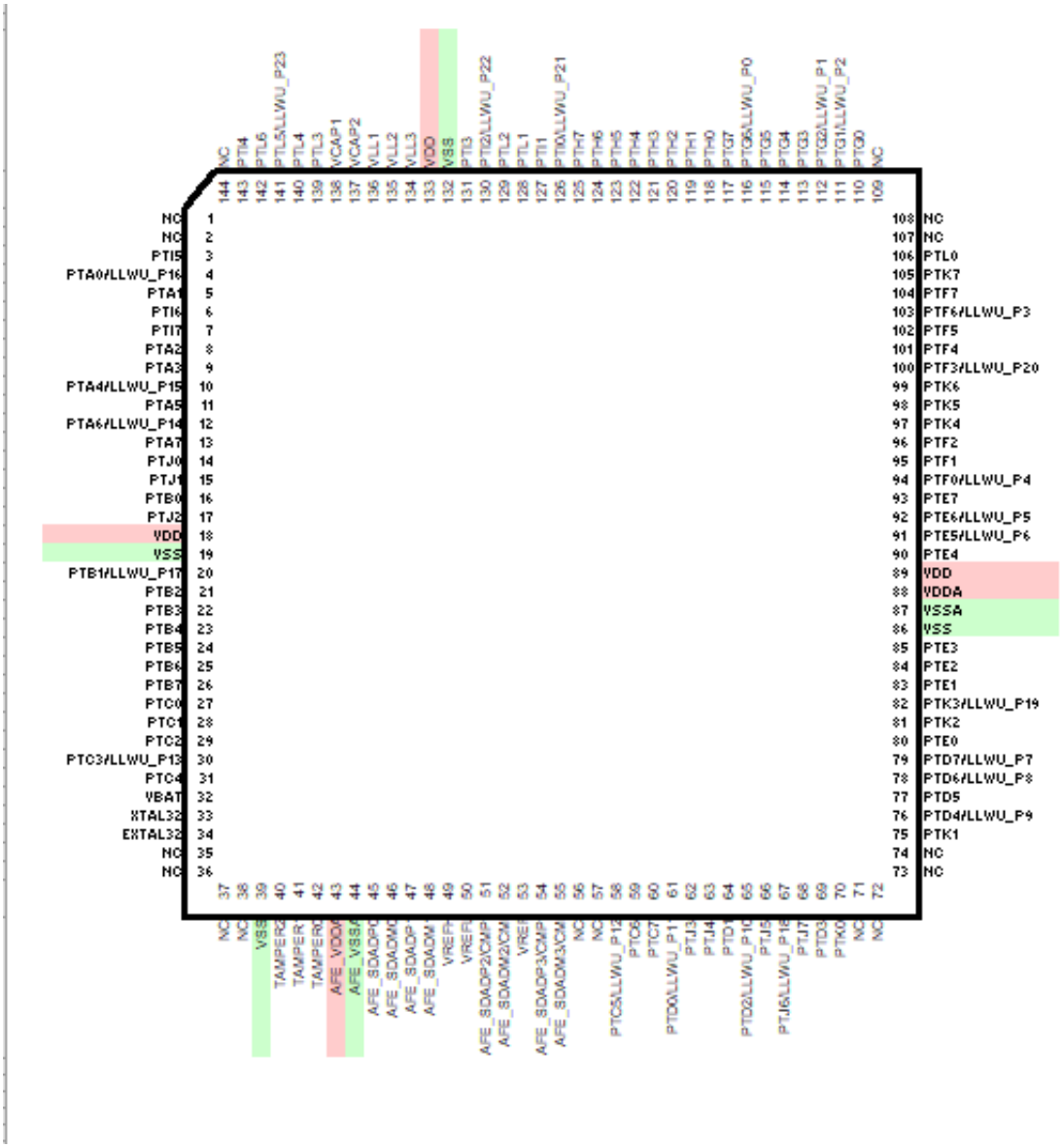


Figure 12. 144-pin LQFP Pinout Diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers:

- MKM35Z256VLL7
- MKM35Z256VLQ7
- MKM35Z512VLL7
- MKM35Z512VLQ7

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KM## A FFF R T PP CC N

7.3 Fields

Following table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Pre-qualification
KM##	Kinetis family	• KM35
A	Key attribute	• Z = Cortex®-M0+
FFF	Program flash memory size	• 256 = 256 KB • 512 = 512 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main

Table continues on the next page...

Field	Description	Values
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LL = 100 LQFP (14 mm x 14 mm) • LQ = 144 LQFP (20 mm × 20 mm)
CC	Maximum CPU frequency (MHz)	• 7 = 75 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

- MKM35Z512VLL7

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

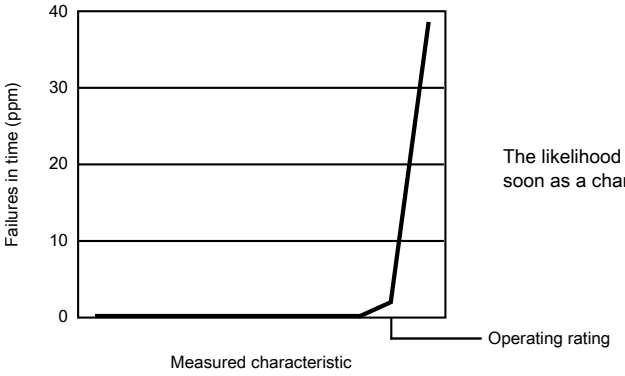
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

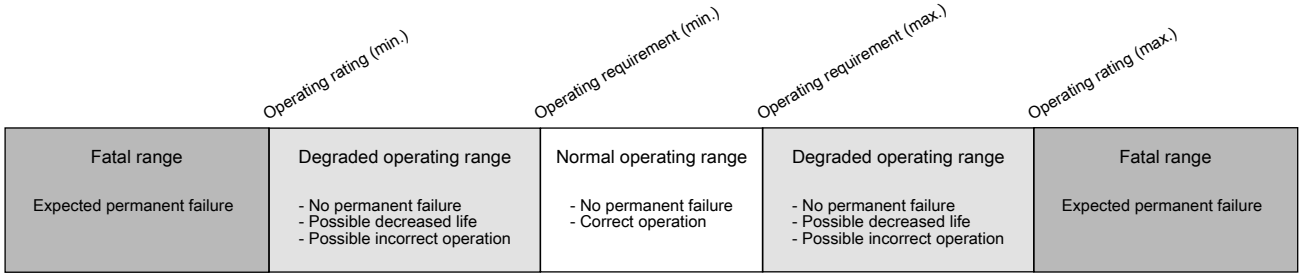
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

8.5 Result of exceeding a rating

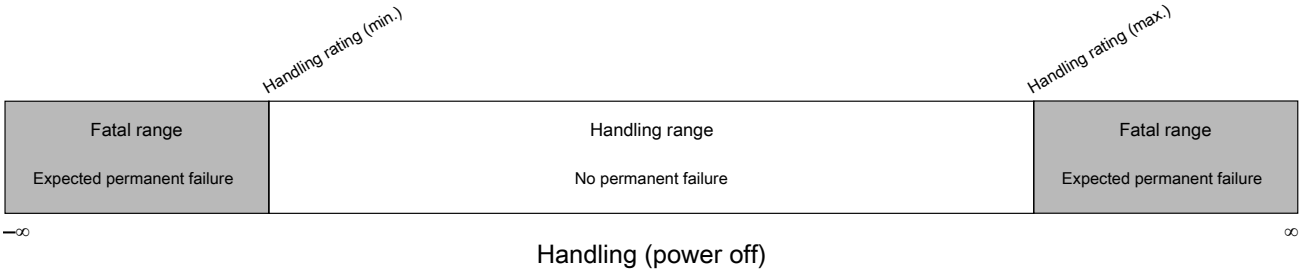


The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

8.6 Relationship between ratings and operating requirements



Operating (power on)



Handling (power off)

8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

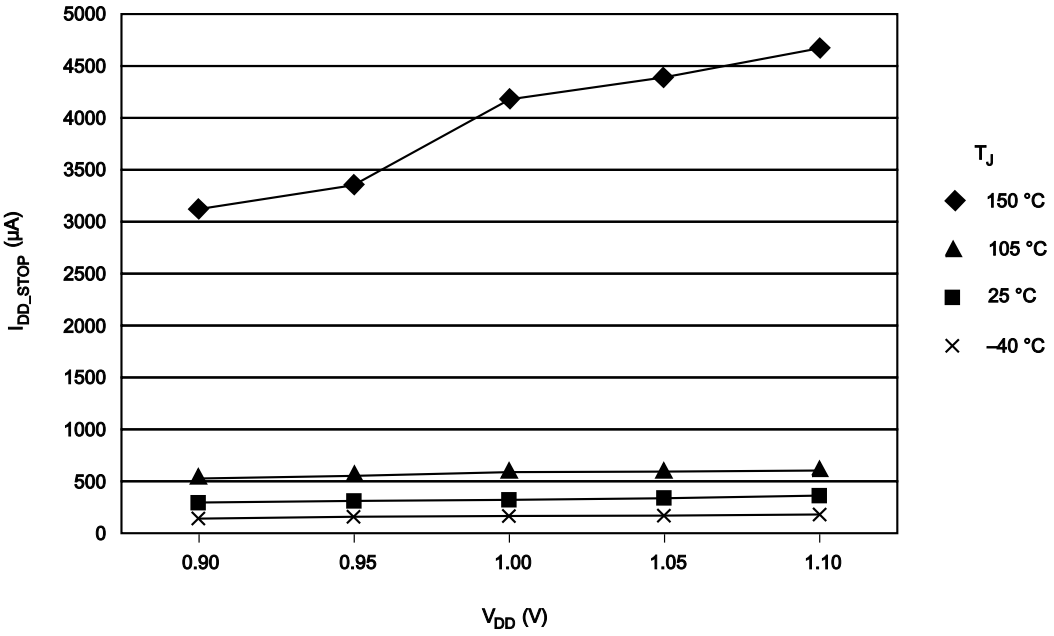
8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

9 Revision History

The following table provides a revision history for this document.

Table 40. Revision History

Rev. No.	Date	Substantial Changes
Rev.0	08/2019	Initial release
Rev.1	12/2019	• Updated the footnotes of ESD handling ratings • Updated Thermal Attributes • Removed EzPort column from KM35 Signal Multiplexing and Pin Assignments

Table continues on the next page...

Table 40. Revision History (continued)

Rev. No.	Date	Substantial Changes
Rev.2	03/2020	• ADdedd IDD values in Power consumption operating behaviors • EDitorial updates • Updated Low power features in Front Matter

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