Freescale Semiconductor
Advance Information

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LP1071

802.11a/b/g Baseband System Solution

1 Introduction

1.1 The LP1070 Family

Freescale Semiconductor's 802.11 LP1070 family consists of high-performance, highly optimized PHY and MAC baseband Wireless LAN processors that fully implement the IEEE 802.11a, 802.11b and 802.11g PHY standards. These baseband processors are poised to revolutionize the Wireless LAN industry by setting new standards for power consumption, size, cost and performance.

The LP1070 family is based on Freescale's proprietary Wireless Broadband Signal Processor™ (WBSP™), an innovative and revolutionary receiver architecture that significantly reduces size and power consumption while providing maximum flexibility to support multiple wireless standards with no additional overhead.

In addition to their superior performance and ultra low power consumption, the LP1070 processors provide the customers with the flexibility to tailor the chip characteristics to their needs. With software control, the

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terminal manufacturers can tune the chip performance to get the exact balance they opt for when it comes to power consumption and performance.

1.2 General Description

The high-performance LP1071 baseband processor integrates the IEEE 802.11a/b/g PHY and full MAC functionality with the industry's smallest package and the lowest power consumption compared to any baseband processor in the market.

The LP1071 was designed to target embedded devices and small form factor SDIO WLAN devices. Its support for SDIO host interface combined with its ultra low power consumption and small size make it the optimal solution for mobile devices. It has been designed with a generic RF interface that lets it interface with virtually any RF components in the market. It has been fully tested to interface with RF solutions from Maxim and Airoha, thus providing terminal manufacturers with added flexibility in selecting the most appropriate RF parts based on their application and form factor.

The LP1071's integrated ADC and DAC reduce the terminal manufacturers' bill of material and overall system cost. The integrated internal memory eliminates the need for external MAC memory, further reducing cost and saving valuable board space for small form factor devices.

The LP1071 also provides the highest level of WLAN security by fully supporting WPA and AES.

1.3 Feature Highlights

- Full compliance with 802.11a/b/g
- Ultra low power consumption, maximizing battery life and minimizing heat dissipation
- Ultra small package: 9.0 x 9.0 x 1.0 (max) mm
- Fully embedded ARM7TDMI® microprocessor for no load on the host processor, leading to maximum flexibility in supporting different host platforms
- Implementations of 802.11e Draft, for support of Quality of Service (QoS) real-time applications
- 802.11i support, including WPA and AES, for enhanced security
- Automatic power management to reduce power consumption
- On-chip ADC and DAC to reduce system BOM and save on board area
- On-Chip PLL for clock generation
- On-chip ROM/RAM eliminating the need for external MAC memory
- Direct memory access (DMA) to reduce CPU utilization
- High throughput achieved using DMA
- Support of SDIO host interface
- Serial EEPROM interface for initialization and device booting
- Eight General Purpose I/O (GPIO) pins for added flexibility
- UART interface to support diagnostic tools and general data transfer
- JTAG Interface for testing and debugging
- Hardware engines for WEP, TKIP and AES support for less processor load

- Supports Direct Conversion (Zero-IF) radio architecture, saving RF components thus reducing BOM cost and simplifying board layout
- Generic RF interface that lets it work with virtually an WLAN RF components. Currently fully tested with RF from Maxim and Airoha.
- Total Flexibility in meeting customer requirements by providing software-controlled trade-off between competing performance metrics.

2 Specifications

Table 1. Specifications

Feature	Details
Network Standard Support	IEEE 802.11a/b/g
Network Architectures	Infrastructure, AdHoc
Data Rates	802.11 a/g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11b: 1, 2, 5.5, 11 Mbps
Modulation Techniques	BPSK, QPSK, 16QAM, 64QAM, CCK, OFDM, DSSS
Security	40- and 128-bit WEP, TKIP, WPA, AES
Receiver Sensitivity	802.11g 6 Mbps: –91.0 dBm 9 Mbps: –90.5 dBm 12 Mbps: –88.6 dBm 18 Mbps: –86.4 dBm 24 Mbps: –81.4 dBm 36 Mbps: –79.9 dBm 48 Mbps: –76.1 dBm 54Mbps: –73.1 dBm 802.11b 1 Mbps: –97.4 dBm 2 Mbps: –94.1 dBm 5.5Mbps: –92.5 dBm 11Mbps: –88.9 dBm
Power Consumption	Receive: 150 mW avg (@54Mbps) Listen: 132 mW Sleep: Less than1 mW
Supply Voltage	I/O: 3.3 ± 0.3 Vdc Core: 1.8 ± 5% Vdc
Operating Temperature	0°C to +70°C; < 95% humidity
Host Interface	SDIO, compliant with SDIO Card Specifications, Version 1.00
Other Interfaces	JTAG 8 GPIO pins One UART Serial EEPROM
Operating System Support	Microsoft Windows CE.net 3.0, 4.2, 5.0 Microsoft Pocket PC 2002, 2003
Packaging Options	144-pin VFBGA, 9.0 x 9.0 x 1.0 (max) mm

Table 1. Specifications (continued)

Feature	Details
Semiconductor Technology	0.18 micron
RF Support	Airoha, Maxim
Certification	Wi-Fi® (incl. WPA), WQHL, FCC Part 15

3 Functional Description

Figure 1 is a functional block diagram of the LP1071, which is divided into three main subsystems.

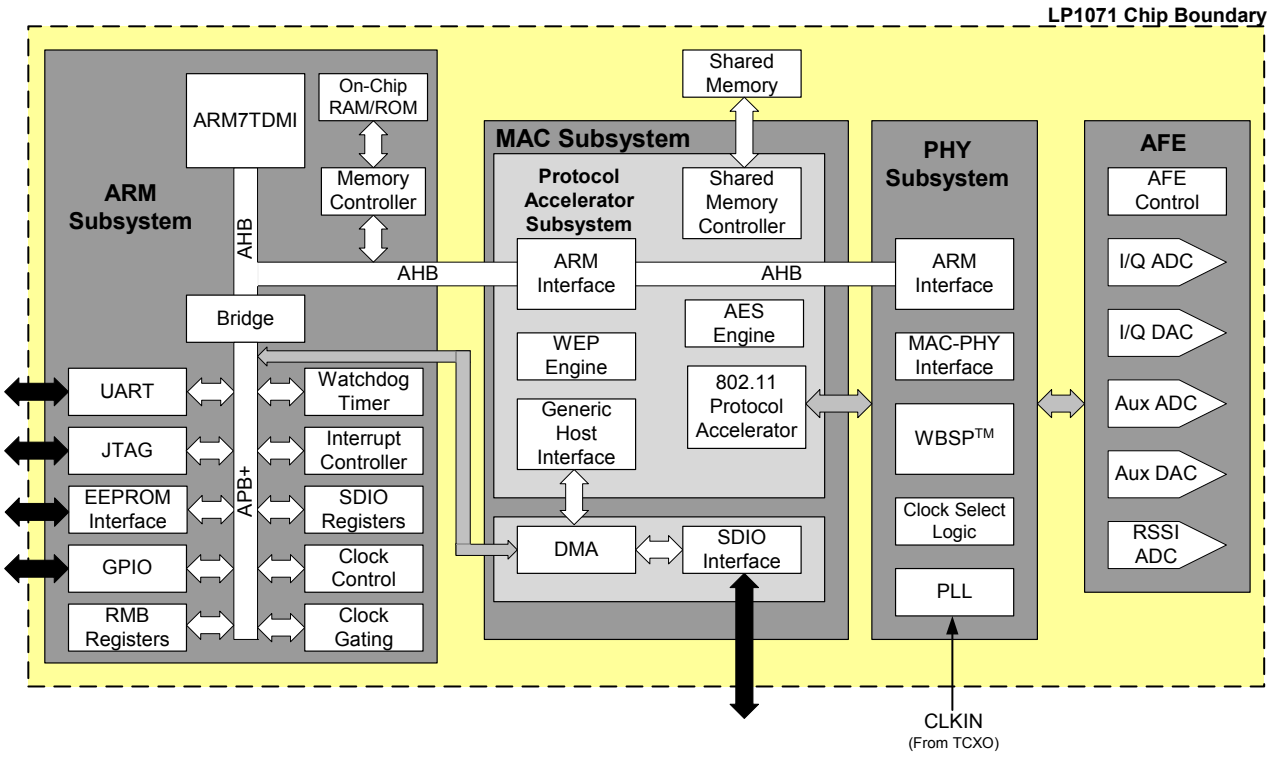

Figure 1. Functional Block Diagram

3.1 Embedded Processor Subsystem

The embedded Processor Subsystem consists of the following:

- An embedded ARM7TDMI microprocessor running at 88 MHz
- An ARM® Peripheral Subsystem accessed via an extended APB (APB+) bus

3.1.1 UART

The UART is used for testing and diagnostic purposes and is capable of supporting data transfer rates of up to 115.2 kbps.

3.1.2 JTAG

TBA

3.1.3 Serial EEPROM Interface

The LP1071 supports an external serial EEPROM for storing the boot loader, MAC address, calibration data and any other vendor-specific data. The LP1071 supports serial EEPROMs of sizes from 8 Kbit (organized as 1024 entries of 8 bits each, or 1024 x 8) up to 512 Kbit (organized as 65,536 x 8). Serial EEPROMs from the following vendors have been tested and verified to work with the LP1071:

- ATMEL (http://www.atmel.com)
- ST Microelectronics (http://www.st.com)
- Microchip Technology (http://www.microchip.com)
- Catalyst Semiconductor (http://www.catsemi.com)
- Integrated Silicon Solutions, Inc. (http://www.issi.com)

The EEPROM is supported through GPIOs. There is no dedicated hardware to support either I^2C or SPI serial EEPROMs.

The operating frequency of the serial EEPROM port is 400 kHz with a supply voltage of 3.0 V.

3.1.4 GPIO

To support vendor-specific needs, the LP1071 provides eight bi-directional General Purpose Input Output (GPIO) pins. Each pin can be independently configured as an input, output or an interrupt source. On reset, the GPIOs default as inputs, i.e. output drivers enables will be inactive.

3.1.5 RMB Registers

This block contains all the reset logic for both CPUs contained in the BRC and chip-wide reset control. It also defines controls for memory address re-mapping.

3.1.6 Watchdog

TBA

3.1.7 Interrupt Controller

TBA

3.1.8 SDIO Registers

TBA

3.1.9 Clock Control

TBA

3.1.10 Clock Gating

This block contains all the control logic required to gate individual sub-block clocks.

3.2 Media Access Control (MAC) Subsystem

3.2.1 Protocol Accelerator Subsystem (PAS)

The main function of the Protocol Accelerator Subsystem is to provide hardware acceleration functions for the MAC Software to perform the time critical aspects of the 802.11 protocol.

The PAS contains the following:

- Shared Memory Controller – provides arbitrated access to the shared memory (MAC memory)
- WEP Hardware Engine
- AES Hardware Engine
- 802.11 Protocol Accelerator – for support of time-critical MAC functions
- Generic Host Interface

3.2.2 AES Block

The contents of the AES block are:

- AES encryption/decryption core that performs AES encryption/decryption of a 128-bit block.
- Offset Codebook (OCB) mode encipher/decipher wrapper that performs OCB mode key generation for the AES core.
- DMA controller and Shared Memory Interface that controls the reading/writing of data blocks from/to the PAS shared memory controller.
- Control Registers, used to configure the operation of the AES block.

3.2.3 WEP Block

TBA

3.3 PHY Subsystem

TBA

3.4 Analog Front End (AFE)

The Analog Front End (AFE) block consists of three Analog-to-Digital Converters (ADCs) and two Digital-to-Analog Converters (DACs) as given in Table 2.

Table 2. AFE Components

Component	Description	Resolution	Clock
I/Q ADC	A 2-channel ADC whose digital output serves as input to digital baseband and whose input is the differential signal from the RF (RX mode).	8-bit	22 Msps
I/Q DAC	A 2-channel DAC whose digital input is from baseband and output is a differential signal for the RF (TX mode).	8-bit	44 Msps
RSSI ADC	A single ended, single channel ADC	6-bit	10 Msps
Auxiliary ADC	A single ended, single channel ADC	8-bit	1 Msps
Auxiliary DAC	A single ended, single channel DAC	8-bit	20 Msps

3.4.1 I/Q ADC

I/Q ADC specifications are shown in Table 3.

Table 3. I/Q ADC Specifications

Parameter	Condition	Min	Typ	Max	Units
Resolution	—	—	8	—	bit
Maximum Sampling Frequency	—	22	—	—	MHz
Signal Bandwidth	—	—	11	—	MHz
Input impedance	Fixed capacitance Switched capacitance @Fs	— —	1 1	— —	pF pF
Latency	—	—	4	—	cycles
Integral Nonlinearity (INL)	—	—	±1.0	—	LSB
Differential Nonlinearity (DNL)	—	—	± 0.5	—	LSB
Total Harmonic Distortion (THD)	Fin= 1MHz Fin= 10MHz	— —	–48.5 –47	— —	dB dB
SNR	Fin= 1MHz Fin= 10MHz	— —	48.5 47	— —	dB dB
ENOB	Fin= 1MHz Fin= 10MHz	— —	7.2 7.0	— —	bit bit
Channel-to-Channel mismatch	Gain Phase	— —	0.2 0.5	— —	dB Degree
DC offset after calibration	—	–1	—	+1	LSB
Wake-up time	From Shutdown From Standby	— —	— —	1 10	ms µs

3.4.2 I/Q DAC

I/Q DAC specifications are shown in Table 4.

Table 4. I/Q DAC

Parameter	Condition	Min	Typ	Max	Units
Resolution	—	—	8	—	bit
Maximum Update rate	—	44	—	—	MHz
3dB Signal Bandwidth	—	—	11	—	MHz
Output common-mode voltage	—	0.7	Vcmo[1]	1.5	V
Load	—	10		5	Kohm pF
Integral Nonlinearity (INL)	—	—	±1.0	—	LSB
Differential Nonlinearity (DNL)	—	—	± 0.5	—	LSB
Total Harmonic Distortion (THD)	Fin= 1MHz Fin= 10MHz	— —	-48.5 -47	— —	dB dB
SNR	Fin= 1MHz Fin= 10MHz	— —	48.5 47	— —	dB dB
ENOB	Fin= 1MHz Fin= 10MHz	— —	7.2 7.0	— —	bit bit
Channel-to-Channel mismatch	Gain Phase	— —	0.2 0.5	— —	dB Degree
DC offset after calibration	—	-1	—	+1	LSB
Wake-up time	From Shutdown From Standby	— —	— —	10 2	µs µs

1 See Analog input pin for definition of I/Q DAC output common-mode level.

3.4.3 RSSI ADC

RSSI ADC specifications are shown in Table 5.

Table 5. RSSI ADC Specifications

Parameter	Condition	Min	Typ	Max	Units
Resolution	—	—	6	—	bit
Maximum Sampling Frequency	—	10	—	—	MHz
Input Voltage Range	—	0	—	3	V
Latency	—	—	3	—	cycles
Integral Nonlinearity (INL)	—	—	±1.0	—	LSB

Table 5. RSSI ADC Specifications (continued)

Parameter	Condition	Min	Typ	Max	Units
Differential Nonlinearity (DNL)	—	—	± 0.5	—	LSB
ENOB	Fin = 100 kHz	—	5.5	—	bit

3.4.4 Aux ADC

Aux ADC specifications are shown in Table 6.

Table 6. Aux ADC Specifications

Parameter	Condition	Min	Typ	Max	Units
Resolution	—	—	8	—	bit
Maximum Sampling Rate	—	1	—	—	MHz
Input Voltage Range	—	0	—	AVdd	V
Latency	—	—	9	—	cycles
Integral Nonlinearity (INL)	—	—	±1.0	—	LSB
Differential Nonlinearity (DNL)	—	—	± 0.5	—	LSB
ENOB	Fin= 100 kHz	—	7.2	—	bit
Channel-to-Channel mismatch	Gain Phase	— —	0.2 0.5	— —	dB Degree
Wake-up time	From Shutdown From Standby	— —	— —	10 2	µs µs

3.4.5 Aux DAC

AUX DAC specifications are shown in Table 7.

Table 7. Aux DAC Specifications

Parameter	Condition	Min	Typ	Max	Units
Resolution	—	—	8	—	bit
Maximum Update rate	—	20	—		MHz
Output voltage for full scale input[1]	—	0.1	—	2.4	V
Load	—	5		 10	kOhm pF
Propagation delay (tpd)	—	—	5	—	ns
Settling time (ts)	—	—	80	—	ns
Integral Nonlinearity (INL)	—	—	±1.0	—	LSB
Differential Nonlinearity (DNL)	—	—	± 0.5	—	LSB

Table 7. Aux DAC Specifications (continued)

Parameter	Condition	Min	Typ	Max	Units
ENOB	Fin= 1MHz	—	7.2	—	bit
Wake-up time	From Shutdown From Standby	— —	— —	10 2	µs µs

1 Due to saturation of the output buffer, INL and DNL are not applicable for output voltages below 200 mV. Output is monotonic above 0.1 V.

4 LP1071 Interfaces

4.1 SDIO Host Interface

The LP1071 supports SDIO Card Specifications, Version 1.00 (http://www.sdcard.org). The LP1071 SDIO host interface supports the I/O mode of the SD Card Specifications.

4.1.1 SDIO Supported Features

The features supported by the LP1071 SDIO host interface are:

- SD 1-Bit Mode
- SD 4-Bit Mode
- Low Speed
- Full Speed (25 MHz)
- Interrupt
- CMD52 during Data Transfer
- CMD53 Multi Block Transfer
- Interrupt during 4-bit Multiple Block Data Transfer
- Combo Card (I/O mode only)

4.1.2 SDIO Function 0/1

For Function 0 registers descriptions, refer to SDIO Card Specification. For Function 1, the SDIO registers occupy a 128 Kbyte space as defined in the SDIO specification. Figure 2 illustrates SDIO Function 1 128 Kbyte Memory Map and Table 8 details its registers.

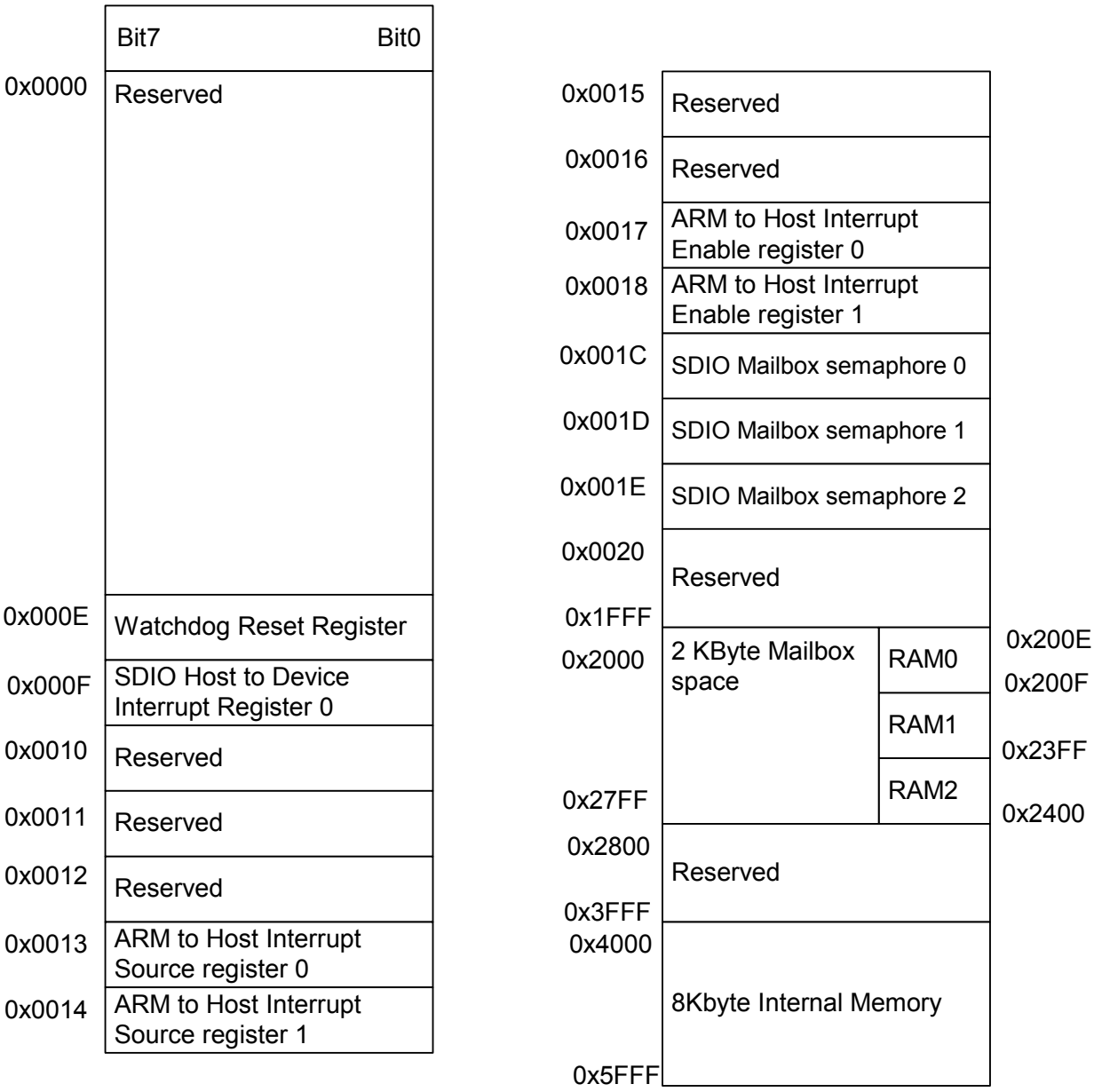

Figure 2. SDIO Function 1 128 Kbyte Memory Map

Table 8. SDIO Function 1 Registers

Bit	Name	Description	ARM Access	HOST Access	Reset
Watchdog Status Register (offset 0x000E)					
0	Wdog_reset	This is a read only bit that when '1' indicates that the LP1071 ASIC has had a watchdog reset occur.	R	R	0
7:1	Reserved	—	—	—	—
SDIO Host to Device Interrupt request register 0 (0x000F)					
7:0	Write_sdio_arm_int	Each bit in this register is 1 of 8 ARM interrupt requests from the SDIO Host to the device ARM. The Host should request an interrupt by writing a "1" to the corresponding bit in this register. The register will be read as a "1" until the ARM clears the register. Once the ARM has cleared the register then the corresponding bit will be read as "0" again.	—	RW	0's
Device to SDIO Host Interrupt Source register 0 (0x0013)					
7:0	Arm_to_sdio_int_clr[7:0] for writes. Arm_to_sdio_int_src[7:0] for reads.	This register contains the interrupt pending status of the SDIO Host interrupt from the device. The device is capable of generating up to 8 individual requests. Each bit in this register is ANDed with the corresponding ARM to SDIO Host Interrupt enable register. The ANDed bits are then ORed together to generate a single SDIO Host interrupt in the cccr register space. To clear a particular interrupt bit the SDIO Host should write a "1" to that particular bit in this register.	—	RW	0's
Device to SDIO Host Interrupt Source register 1 (0x0014)					
2:0	Arm_to_sdio_int_clr[10:8] for writes. Arm_to_sdio_int_src[10:8] for reads.	This register contains the interrupt pending status of the SDIO Host semaphore 0-2 host granted indication. When the Host requests a semaphore the corresponding interrupt will be triggered when the host has been granted the interrupt. Bit 0 is semaphore 0; bit 1 is semaphore 1; and bit 2 is semaphore 2. Each bit in this register is ANDed with the corresponding ARM to SDIO Host Interrupt enable register. The ANDed bits are then ORed together to generate a single SDIO Host interrupt in the cccr register space. To clear a particular interrupt bit the SDIO Host should write a "1" to that particular bit in this register.	—	RW	0's
7:3	Reserved	—	—	—	—

Table 8. SDIO Function 1 Registers (continued)

Bit	Name	Description	ARM Access	HOST Access	Reset
Device to SDIO Host Interrupt Enable 0 (0x0017)					
7:0	Arm_to_sdio_inte_en[7:0]	Individual bit enables for each of the device to host interrupt source bits. Setting the corresponding bit to a “1” enables the interrupt; “0” disables the interrupt. The SDIO Host can disable all interrupts by disabling the main SDIO host interrupt in the CCCR register.	—	RW	0’s
Device to SDIO Host Interrupt Enable 1 (0x0018)					
2:0	Arm_to_sdio_inte_en[10:8]	Individual bit enables for each of the device to host interrupt source bits. Setting the corresponding bit to a “1” enables the interrupt; “0” disables the interrupt. The SDIO Host can disable all interrupts by disabling the main SDIO host interrupt in the CCCR register. Bit 0 is enable for semaphore 0 granted; bit 1 is semaphore 1; and bit 2 is semaphore 2.	—	RW	0’s
7:3	—	Reserved	—	—	—
SDIO Host Mailbox Semaphore 0 Register (offset 0x001C)					
1:0	Sdio_mbxp_0_sema	2 bit semaphore register to control whether the host or the device has access to the shared mailbox ram 0. The host should write a “01” to this register to request the shared ram 0. After writing “01” the host should read this register. If the value is “01” then the host owns access to the mailbox. If the value read is “11” then the device owns access to the mailbox. When the host is done utilizing the mailbox then it should release ownership of the mailbox by writing “00” to this register.	RW	RW	0’s
7:2	Reserved	—	—	—	—
SDIO Host Mailbox Semaphore 1 Register (offset 0x001D)					
1:0	Sdio_mbxp_1_sema	2 bit semaphore register to control whether the host or the device has access to the shared mailbox ram 1. The host should write a “01” to this register to request the shared ram 1. After writing “01” the host should read this register. If the value is “01” then the host owns access to the mailbox. If the value read is “11” then the device owns access to the mailbox. When the host is done utilizing the mailbox then it should release ownership of the mailbox by writing “00” to this register.	RW	RW	0’s
7:2	Reserved	—	—	—	—

Table 8. SDIO Function 1 Registers (continued)

Bit	Name	Description	ARM Access	HOST Access	Reset
SDIO Host Mailbox Semaphore 2 Register (offset 0x001E)					
1:0	Sdio_mbxp_2_sema	2 bit semaphore register to control whether the host or the device has access to the shared mailbox ram 2. The host should write a “01” to this register to request the shared ram 2. After writing “01” the host should read this register. If the value is “01” then the host owns access to the mailbox. If the value read is “11” then the device owns access to the mailbox. When the host is done utilizing the mailbox then it should release ownership of the mailbox by writing “00” to this register.	RW	RW	0’s
7:2	Reserved	—	—	—	—
992 byte Mailbox RAM 1 (offset 0x200F to 0x23FF)					
7:0	Mbox_rdata_1[15:0]	Shared SDIO Mailbox. Both the ARM and Host can use the mailbox for message exchange between the SDIO device and the SDIO Host. Prior to accessing the SDIO Mailbox the Host should request and be granted the mailbox via the mailbox semaphore 1 register described above. Once the Host has been granted access to the mailbox it may read/write the mailbox however it likes. If the Host has not been granted access to the mailbox it will not be able to read or write the mailbox. Once the Host is finished with the mailbox it should release control of the mailbox as described in the mailbox semaphore 1 register.	RW	RW	—
1 Kbyte Mailbox RAM 2 (offset 0x2400 to 0x27FF)					
7:0	Mbox_rdata_2[15:0]	Shared SDIO Mailbox. Both the ARM and Host can use the mailbox for message exchange between the SDIO device and the SDIO Host. Prior to accessing the SDIO Mailbox the Host should request and be granted the mailbox via the mailbox semaphore 2 register described above. Once the Host has been granted access to the mailbox it may read/write the mailbox however it likes. If the Host has not been granted access to the mailbox it will not be able to read or write the mailbox. Once the Host is finished with the mailbox it should release control of the mailbox as described in the mailbox semaphore 2 register.	RW	RW	—

Table 8. SDIO Function 1 Registers (continued)

Bit	Name	Description	ARM Access	HOST Access	Reset
8 Kbyte Internal Memory Buffer RAM (offset 0x4000 to 0x5FFF)					
7:0	Imem_rdat[15:0]	This is an internal memory buffer for specific use by the SDIO device. Data is read or written to this memory via SDIO cmd 53 reads or writes. Then, the SDIO DMA controller is used to move the data from the internal memory buffer to/from shared memory under device (ARM) control.	—	RW	—

4.2 RF Interface

4.2.1 Serial Programmable Interface (SPI)

- The SPI is composed of 3 signals:
  1. RF_SIF_0_SCLK (serial clock)
  2. RF_SIF_1_CS_N (chip select)
  3. RF_SIF_2_DIN (data input)
- The serial information is sent to the RF transceiver in 18 bit bursts framed by chip select. The 18 bits comprises of leading 14 (or less) data bits and trailing 4 address bits
- Programming clock edges are ignored until chip select goes active low.
- All bits are shifted in on the rising edge of the clock and latched in when chip select returns inactive high. (permissible for the clock in either state)
- The interface can be programmed in any operating mode.
- Serial information is clocked in with the most significant bit (MSB) first.
- The address bits for the internal registers are decoded on the rising edge of chip select.
- The rising edge of chip select initiates an internal parallel load pulse that latches the last 18-bit serially shifted-in data into the internal register.

5 Timers/Reset

The TCXO generates the 40 MHz RFIC 800 mV clipped sine wave reference clock.

The TCXO output is converted to a digital signal via a clock squarer input pad circuit. The 40 MHz TCXO reference is used to generate the 40 MHz IQDAC clock and the 20 MHz IQADC clock. The PLL synthesizes a reference from the 40 MHz reference. The reference is then used to generate the BRC, ARM, PAS and Symbol Processor clocks, the 44 MHz IQ DAC clock and the 22 MHz IQ ADC clock. When the TCXO and PLL are powered down the only active clock source is the 32 kHz XTAL, a.k.a. the Slow Clock.

The TCXO, PLL and XTAL clock references all include bypass MUXes which allow the individual clock reference to be driven by an external signal.

Figure 3 illustrates the high level clocking of the LP1071 with the associated pins.

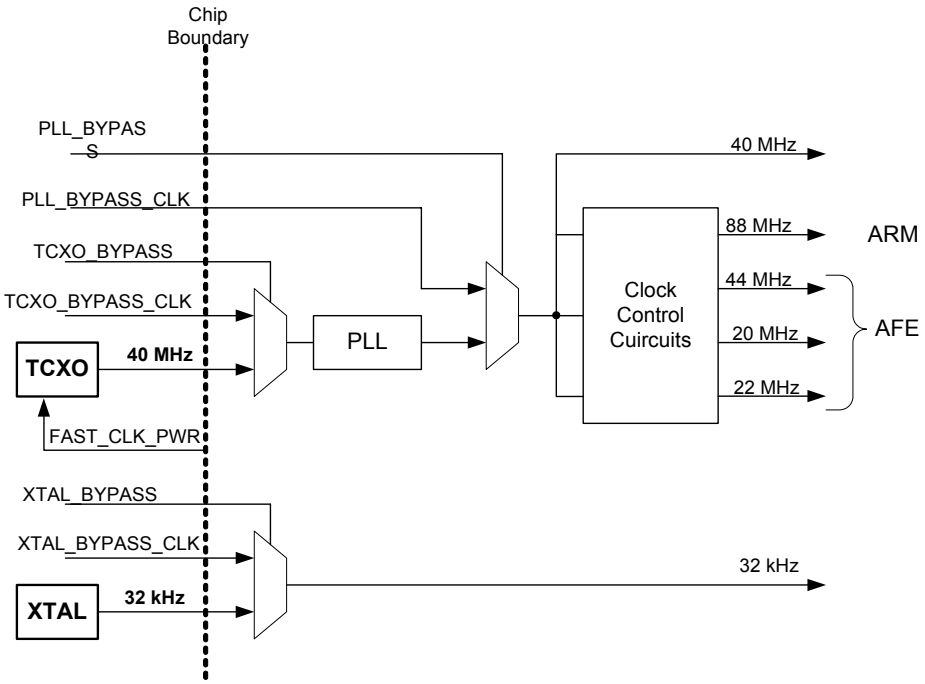

Figure 3. LP1071 Clocks

5.1 System Clock

The LP1071 is clocked using an external crystal oscillator (XO) or a temperature compensated crystal oscillator (TCXO) running at 40MHz with a frequency resolution of ± 20 ppm or better.

5.2 PLL Block

PLL Bypass

5.3 Low Frequency Clock

The LP1071 uses a low power 32 kHz crystal oscillator to maintain the timing during sleep.

6 Pinout and Footprint

6.1 Pinout

See Table 9 for the pin description.

Table 9. Pin Description

Pad Name	Pad Type	Direction	Description	Pin
Power and Ground Pads				
VDD_IO	pvdd2dgz	N/A	3.3 V I/O power pad (22 mA per pad max current)	K1

Table 9. Pin Description (continued)

Pad Name	Pad Type	Direction	Description	Pin
VDD_IO	pvdd2dgz	N/A	3.3 V I/O power pad (22 mA per pad max current)	L2
VDD_IO	pvdd2dgz	N/A	3.3 V I/O power pad (22 mA per pad max current)	M5
VDD_IO	pvdd2dgz	N/A	3.3 V I/O power pad (22 mA per pad max current)	K10
VDD_IO	pvdd2dgz	N/A	3.3 V I/O power pad (22 mA per pad max current)	M11
VDD_IO	pvdd2dgz	N/A	3.3 V I/O power pad (22 mA per pad max current)	C11
VSS_IO	pvss2dgz	N/A	I/O ground pad (94 mA max current)	H4
VSS_IO	pvss2dgz	N/A	I/O ground pad (94 mA max current)	J4
VSS_IO	pvss2dgz	N/A	I/O ground pad (94 mA max current)	J6
VSS_IO	pvss2dgz	N/A	I/O ground pad (94 mA max current)	J9
VSS_IO	pvss2dgz	N/A	I/O ground pad (94 mA max current)	H8
VSS_IO	pvss2dgz	N/A	I/O ground pad (94 mA max current)	H9
VSS_IO	pvss2dgz	N/A	I/O ground pad (94 mA max current)	F9
VSS_IO	pvss2dgz	N/A	I/O ground pad (94 mA max current)	E9
VDD_CORE	pvdd1dgz	N/A	1.8 V core power pad (31 mA per pad max current)	G1
VDD_CORE	pvdd1dgz	N/A	1.8 V core power pad (31 mA per pad max current)	M7
VDD_CORE	pvdd1dgz	N/A	1.8 V core power pad (31 mA per pad max current)	L11
VDD_CORE	pvdd1dgz	N/A	1.8 V core power pad (31 mA per pad max current)	G12
VDD_CORE	pvdd1dgz	N/A	1.8 V core power pad (31 mA per pad max current)	D9
VDD_CORE	pvdd1dgz	N/A	1.8 V core power pad (31 mA per pad max current)	A12
VSS_CORE	pvss1dgz	N/A	core ground pad (25 mA per pad max current)	G4
VSS_CORE	pvss1dgz	N/A	core ground pad (25 mA per pad max current)	J7
VSS_CORE	pvss1dgz	N/A	core ground pad (25 mA per pad max current)	J8
VSS_CORE	pvss1dgz	N/A	core ground pad (25 mA per pad max current)	G9
VSS_CORE	pvss1dgz	N/A	core ground pad (25 mA per pad max current)	D8
VSS_CORE	pvss1dgz	N/A	core ground pad (25 mA per pad max current)	

Table 9. Pin Description (continued)

Pad Name	Pad Type	Direction	Description	Pin
Clocks and Resets and Mode				
EMBEDDED_RESET_N	pdisdgz	input	Embedded board reset	E10
PLL_BYPASS	pdidgz	input	Bypass the internal PLL and use PLL_BYPASS_CLK	A9
PLL_BYPASS_CLK	pdidgz	input	PLL bypass clock input	A10
AVDD_PLL	pdiana2p	N/A	Analog 3.3 volt	D2
AVSS_PLL	pdiana2p	N/A	Analog ground	D1
TAVDDPOWER	pvdd3p	N/A	3.3 volt power for ESD Diodes	E3
TAVssPOWER	pvss3p	N/A	3.3 volt power for ESD Diodes	A3
DVDD_PLL	pdiana2p	N/A	1.8 volt digital power for PLL	F3
DVSS_PLL	pdiana2p	N/A	1.8 volt digital ground for PLL	E2
TXCO_BYPASS	pdidgz	input	Bypass the TCXO and use the TCXO_BYPASS_CLK	B10
TXCO_BYPASS_CLK	pdidgz	input	TCXO bypass clock	A11
XTAL_BYPASS	pdidgz	input	Bypass the XTAL oscillator and use the XTAL_BYPASS_CLK	D11
XTAL_BYPASS_CLK	pdidgz	input	XTAL bypass clock	C12
FAST_CLK_POWER	pdo02cdg	output	Enable the TCXO	B9
XTAL_32K_XIN	pdxoe4dg	analog	32 kHz crystal (NOTE: Must be placed next to PVDD1DGZ.)	B12
XTAL_32K_XOUT		analog	32 kHz crystal	B11
RESET_N	pdisdgz	Input	Chip Reset	D10
CHIP_MODE0	pdidgz	Input	Chip Mode Select	G3
CHIP_MODE1	pdidgz	Input	Chip Mode Select	H2
CHIP_MODE2	pdidgz	Input	Chip Mode Select	H1
CHIP_MODE3	pdidgz	Input	Chip Mode Select	H3
JTAG				
JTAG_RESET	pdudgz	Input	Tap reset	L7
JTAG_CLOCK	pdisdgz	input	Tap clock	L8
JTAG_DI	pdudgz	input	Tap data in	M8
JTAG_DO	pdo02cdg	output	Tap data out	K8
JTAG_MODE	pdudgz	input	Tap Mode	K9
ARM Sub-system Signals				
ARM_GPIO0	pdb04dgz	bi-dir	General Purpose I/O	M2
ARM_GPIO1	pdb04dgz	bi-dir	General Purpose I/O	L3
ARM_GPIO2	pdb04dgz	bi-dir	General Purpose I/O	K4
ARM_GPIO3	pdb04dgz	bi-dir	General Purpose I/O	L4

Table 9. Pin Description (continued)

Pad Name	Pad Type	Direction	Description	Pin
ARM_GPIO4	pdb04dgz	bi-dir	General Purpose I/O	M3
ARM_GPIO5	pdb04dgz	bi-dir	General Purpose I/O	M4
ARM_GPIO6	pdb04dgz	bi-dir	General Purpose I/O	K5
ARM_GPIO7	pdb04dgz	bi-dir	General Purpose I/O	L5
ARM_UART_0_DI	pdb04dgz	Input	UART input data.	K6
ARM_UART_0_DO	pdb04dgz	output	UART output data.	M6
ARM_EEPROM_DAT_GPIO	pdb04dgz	bi-dir	General Purpose I/O dedicated for EEPROM.	L6
ARM_EEPROM_CLK_GPIO	pdb04dgz	bi-dir	General Purpose I/O dedicated for EEPROM.	K7
SDIO Signals (other signals on interface are 1 Vdd and 2 Vss pins)				
CD/DAT3 (connector pin 1)	pduw04dgz	bi-dir	card detect/data 3.	J1
DAT[2] (connector pin 9)	pdu04dgz	bi-dir	data 2.	J2
DAT[1] (connector pin 8)	pdu04dgz	bi-dir	data 1/interrupt.	J3
DAT[0] (connector pin 7)	pdu04dgz	bi-dir	data 0/busy indication.	K2
CMD (connector pin 2)	pdu04dgz	bi-dir	command/response.	K3
CLK (connector pin 5)	pdisdgz	input	clock	L1
AFE Interface				
AGND	pdiana2p	N/A	Analog ground	D6
AGNDIQADC	pdiana2p	N/A	Analog ground	D7
AGNDIQDAC_1	pdiana2p	N/A	Analog ground	A6
AGNDREF	pdiana2p	N/A	Analog Reference negative supply	
AVDD	pdiana2p	N/A	Analog 3.3 volt	B3
AVDDIQADC	pdiana2p	N/A	Analog 3.3 volt	A5
AVDDIQDAC_1	pdiana2p	N/A	Analog 3.3 volt	B7
VDDIQADC	pvdd3p	N/A	3.3 volt power for ESD Diodes	B4
VSSIQADC	pvss3p	N/A	3.3 volt ground for ESD Diodes	C1
VDDIQDAC	pvdd3p	N/A	3.3 volt power for ESD Diodes	F4
DGND	pvss1dgz	N/A	Digital Ground	E4
DVDD	pvdd1dgz	N/A	Digital 1.8 Volt	B1
IBIAS	pdiana2p	N/A	Pin for monitoring or bypassing bias current, flowing out of the pin to agnd.	A1
VBG	pdiana2p	N/A	Voltage reference pin for decoupling (equal to 1.25 V). Connect 1 uF (ceramic) + 100 nF (ceramic) to agndref.	C4
VREFN	pdiana2p	input	ADC Negative reference for decoupling	A4
VREFP	pdiana2p	input	ADC Positive reference for decoupling	C6
AUXADCIN_0	pdiana2p	input	Muxed analog input to auxiliary ADC bit 0	D4

Table 9. Pin Description (continued)

Pad Name	Pad Type	Direction	Description	Pin
AUXADCIN_1	pdiana2p	input	Muxed analog input to auxiliary ADC bit 1	C3
AUXADCIN_2	pdiana2p	input	Muxed analog input to auxiliary ADC bit 2	A2
IADCINN	pdiana2p	input	Negative input of I-ADC	C7
IADCINP	pdiana2p	input	Positive input of I-ADC	B6
QADCINN	pdiana2p	input	Negative input of Q-ADC	C5
QADCINP	pdiana2p	input	Positive input of Q-ADC	D5
RSSIADCIN	pdiana2p	input	RSSI ADC input	C2
VOCM	pdiana2p	input	Input pin for definition of IQDAC output common-mode level	B8
AUXDACOUT	pdiana2p	output	Auxiliary DAC output	B2
IDACOUTP	pdiana2p	output	Positive output of I-DAC	C8
IDACOUTN	pdiana2p	output	Negative output of I-DAC	A7
QDACOUTP	pdiana2p	output	Positive output of Q-DAC	A8
QDACOUTN	pdiana2p	output	Negative output of Q-DAC	C9
EXT_BIAS	pdiana2p	input	External Bias for test	D3
TCXO Squarer				
AVDD_TCXO	pvdd3p	N/A	Analog 3.3 volt	F1
AVSS_TCXO	pvss3p	N/A	Analog ground	G2
CLKIN	pdiana2p	input	TCXO reference clock input	F2
RF Interface Signals				
RF_ANALOG_LDO	pdb04dgz	bi-dir	LDO enable for RF VCO power. Driven by PHY controller.	L9
RF_EN	pdb04dgz	bi-dir	RF enable. Driven by PHY controller.	L10
RF_RXEN	pdb04dgz	bi-dir	RF Rx enable. Driven by PHY controller.	M9
RF_TXEN	pdb04dgz	bi-dir	RF Tx enable. Driven by PHY controller.	M10
RF_PAEN1	pdb04dgz	bi-dir	RF PA enable 1. Driven by PHY controller.	L12
RF_PAEN2	pdb04dgz	bi-dir	RF PA enable 2. Driven by PHY controller.	K11
RF_SPARE1	pdb04dgz	bi-dir	RF spare 1 (not used). Driven by PHY controller.	J10
RF_VGA6	pdb04dgz	bi-dir	RF VGA setting. Driven by UWA	K12
RF_VGA5	pdb04dgz	bi-dir	RF VGA setting. Driven by UWA.	J12
RF_VGA4	pdb04dgz	bi-dir	RF VGA setting. Driven by UWA.	J11
RF_VGA3	pdo02cdg	output	RF VGA setting. Driven by UWA.	H12
RF_VGA2	pdo02cdg	output	RF VGA setting. Driven by UWA.	H10
RF_VGA1	pdo02cdg	output	RF VGA setting. Driven by UWA.	H11
RF_VGA0	pdo02cdg	output	RF VGA setting. Driven by UWA.	G10

Table 9. Pin Description (continued)

Pad Name	Pad Type	Direction	Description	Pin
RF_RXHP	pdo02cdg	output	RF Rx highpass filter setting. Driven by UWA.	F12
RF_ANTENNA_SEL	pdo02cdg	output	RF antenna select. Driven by ARM.	G11
RF_ANTENNA_SEL_N	pdo02cdg	output	RF antenna select. Driven by ARM.	F10
RF_SIF_2_DIN	pdo02cdg	output	RF 3-wire serial interface. Driven by ARM.	F11
RF_SIF_1_CS_N	pdo02cdg	output	RF 3-wire serial interface. Driven by ARM.	E11
RF_SIF_0_SCLK	pdo02cdg	output	RF 3-wire serial interface. Driven by ARM.	E12
RF_LOCK_DETECT	pdidgz	input	RF lock detect. Read by ARM.	D12

6.2 Pad Descriptions

pdxoe4dg	32 kHz crystal pad (1 pad w/2 pad connections)
pdisdgz	Schmitt triggered input 5 Volt tolerant
pdidgz	5 Volt tolerant input pad
pdudgz	5 Volt tolerant input pad w/internal pullup
pdusdgz	Schmitt Trigger Input Pad, 5V-Tolerant w/pullup
pdddgz	Input Pad With Pulldown, 5-VT IO
pdo02cdg	cmos 2 mA output
pdo04cdg	cmos 4 mA output
pdb04dgz	CMOS 3 state output pad w/input (5 volt tolerant)
pdb02dgz	CMOS 3 state output pad w/input (5 volt tolerant)
pdu02sdgz	CMOS 3-State Output Pad with Schmitt Trigger Input and Pullup, 5V-Tolerant
pdd04dgz	CMOS 3-State Output Pad with Input and Pulldown, 5V-Tolerant
pdd04dgz	CMOS 3-State Output Pad with Input and Pulldown, 5V-Tolerant
pdd08dgz	CMOS 3-State Output Pad with Input and Pulldown, 5V-Tolerant
pdt04dgz	CMOS 3-State Output Pad, 5V-Tolerant
pdu02dgz	CMOS 3-State Output Pad with Input and Pullup, 5V-Tolerant
pduw02dgz	3-State Output Pad with Input and Enable Controlled Pull-Up, 5V-Tolerant
pdiana2p	Low Frequency Analog I/O for use with power cut diodes (Note: It is recommended to utilize the secondary ESD protection circuit: ESND on these pads.

6.3 Footprint

	1	2	3	4	5	6	7	8	9	10	11	12
A	IBIAS	AUXADCIN_2	PVSS3P_2	VREFN	AVDDIQADC	AGNDIQDAC_1	IDACOUTN	QDACOUTP	PLL_BYPASS	PLL_BYPASS_CLK	TCXO_BYPASS_CLK	VDD_CORE_5
B	DVDD	AUXDACOUT	AVDD	PVDD3P_2	NC	IADCINP	AVDDIQDAC_1	VOCM	FAST_CLK_POWER	TCXO_BYPASS	XTAL_32K_XOUT	XTAL_32K_XIN
C	PVSS3P_1	RSSIADCIN	AUXADCIN_1	VBG	QADCINN	VREFP	IADCINN	IDACOUTP	QDACOUTN	NC	VDD_IO_6	XTAL_BYPASS_CLK
D	AVSS_PLL	AVDD_PLL	EXT_BIAS	AUXADCIN_0	QADCINP	AGND	AGNDIQADC	GND	GND	RESET_N	XTAL_BYPASS	RF_LOCK_DETECT
E	TAVSSPOWER	DVSS_PLL	TAVDDPOWER	DGND	GND	GND	GND	GND	GND	EMBEDDED_RESET_N	RF_SIF_1_CS_N	RF_SIF_0_SCLK
F	AVDD_TCXO	CLKIN	DVDD_PLL	PVDD3P_1	GND	GND	GND	GND	GND	RF_ANTENNA_SEL_N	RF_SIF_2_DIN	RF_RXHP
G	VDD_CORE_1	AVSS_TCXO	CHIP_MODE_0	GND	GND	GND	GND	GND	GND	RF_VGA_0	RF_ANTENNA_SEL	VDD_CORE_4
H	CHIP_MODE_2	CHIP_MODE_1	CHIP_MODE_3	GND	GND	GND	GND	GND	GND	RF_VGA_2	RF_VGA_1	RF_VGA_3
J	SD_DAT_3	SD_DAT_2	SD_DAT_1	GND	GND	GND	GND	GND	GND	RF_SPARE1	RF_VGA_4	RF_VGA_5
K	VDD_IO_1	SD_DAT_0	SD_CMD	ARM_GPIO_2	ARM_GPIO_6	ARM_UART_0_DI	ARM_EEPROM_CLK_GPIO	JTAG_DO	JTAG_MODE	VDD_IO_4	RF_PAEN2	RF_VGA_6
L	SD_CLK	VDD_IO_2	ARM_GPIO_1	ARM_GPIO_3	ARM_GPIO_7	ARM_EEPROM_DAT_GPIO	JTAG_RESET	JTAG_CLOCK	RF_ANALOG_LDO	RF_EN	VDD_CORE_3	RF_PAEN1
M	VDD_IO_2	ARM_GPIO_0	ARM_GPIO_4	ARM_GPIO_5	VDD_IO_3	ARM_UART_0_DO	VDD_CORE_2	JTAG_DI	RF_RXEN	RF_TXEN	VDD_IO_5	VDD_CORE_3

7 DC Electrical Specifications

7.1 Absolute Maximum Ratings

Absolute maximum ratings are shown in Table 10.

Table 10. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (3.0 V)	-0.3	4.0	V
Supply Voltage (1.8 V)	-0.3	2.2	V
Input Voltage	GND - 0.3	VDD + 0.3	V
DC Output Current	TBD	TBD	mA
Storage Temperature	TBD	TBD	^{o}C
Electrostatic Discharge Voltage	TBD	TBD	V

Operating the LP1071 under conditions that exceed Absolute Maximum Ratings may result in permanent damage to the device. Absolute maximum ratings are limiting values, and are considered individually, while all other parameters are within their specified operating ranges.

7.2 Recommended Operating Conditions

Recommended operating conditions are shown in Table 11.

Table 11. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply I/O Voltage	$V_{DD\_}IO$	3.0	3.6	V
Supply Core Voltage	$V_{DD\_}C$	1.71	1.89	V
Operating Temperature	T_A	0	70	^{o}C

Thermal dissipation (for multi-layer PCB) is shown in Table 12.

Table 12. Thermal Dissipation (for multi-layer PCB)

# PCB Layers	# PCB Vias	PCB Trace Density	θ_{JA} (°C/W)			Ψ_{JT} (°C/W)	θ_{JC} (°C/W)
			0 m/s	1 m/s	2 m/s		
1 (1s)	0	JEDEC	96.1	68.9	59.6	1.0	6.5
2 (2s)	36	JEDEC	81.7	60.2	52.6	0.9	6.2
	0	6%	66.9	51.3	45.8	0.7	6.0

7.3 DC Characteristics

DC characteristics are shown in Table 13.

Table 13. DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Units
Pre-driver Supply Voltage	V_{DD}	—	1.62	1.8	1.98	V
I/O Supply Voltage	V_{D33}	—	3.0	3.3	3.6	V

Table 13. DC Characteristics (continued)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Low-level input voltage	V_{IL}	—	-0.3	—	0.8	V
High-level input voltage	V_{IH}	—	2.0	—	5.5	V
Threshold point	V_T	—	1.46	1.58	1.75	V
Schmitt Trigger Low to High Thresh	V_{T+}	Schmitt	1.47	1.50	1.50	V
Schmitt Trigger High to Low Thresh	V_{T-}	Schmitt	0.90	0.94	0.96	V
Input Leakage Current	I_I	$V_I = V_{D33}$ or 0V	-10	—	10	µA
3-state leak current	I_{OZ}	$V_{OH} = V_{SS}$	-10	—	10	µA
		$V_{OL} = V_{DD}$	-10	—	10	µA
Output low voltage	V_{OL}	I_{OL} = 2,4,..., 24mA	—	—	0.4	V
Output high voltage	V_{OH}	I_{OH} =2,4,..., 24mA	2.4	—	—	V
Low Level Out Current @V_{OL}=0.4V	I_{OL}	2 mA	2.2	3.3	3.8	mA
		4 mA	4.5	6.6	7.6	mA
		8 mA	TBA	TBA	TBA	mA
		12 mA	1	19.7	22.7	mA
		16 mA	TBA	TBA	TBA	mA
		24 mA	2	39.5	45.4	mA
High Level Out Current @V_{OH}=2.4V	I_{OH}	2 mA	TBA	TBA	TBA	mA
		4 mA	TBA	TBA	TBA	mA
		8 mA	12.3	24.8	38	mA
		12 mA	18.5	37.1	56.9	mA
		16 mA	22.7	49.5	75.9	mA
		24 mA	36.9	74.3	113.9	mA

8 Timing Characteristics

8.1 AFE Interface

8.1.1 I/Q ADC

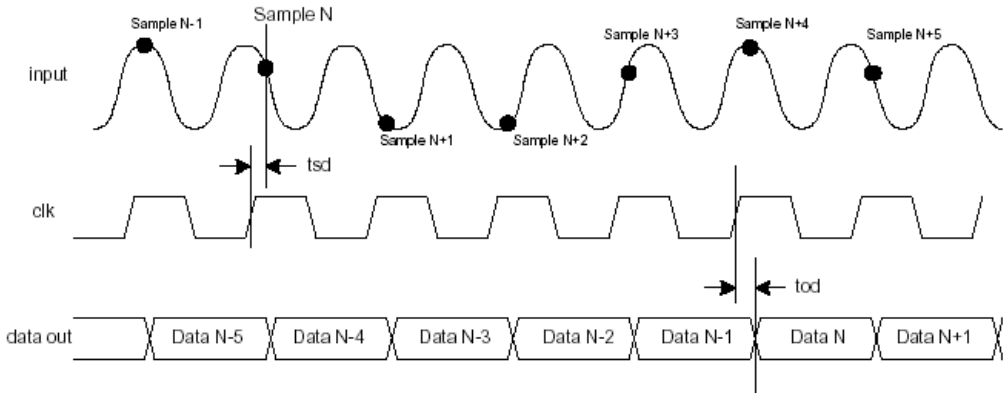

Figure 4. Timing of the Pipelining Operation in I/Q ADC

8.1.2 I/Q DAC

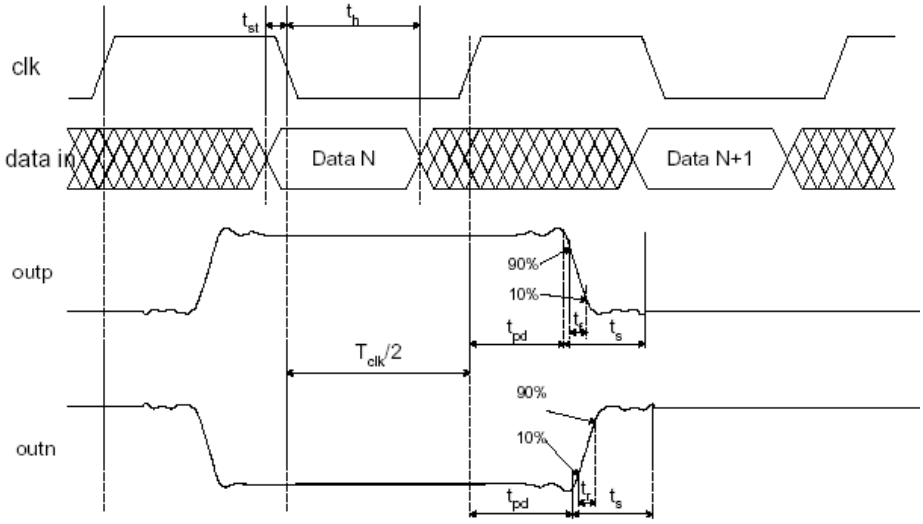

Figure 5. Timing Diagram of the I/Q DAC Inputs and Outputs

8.1.3 RSSI ADC

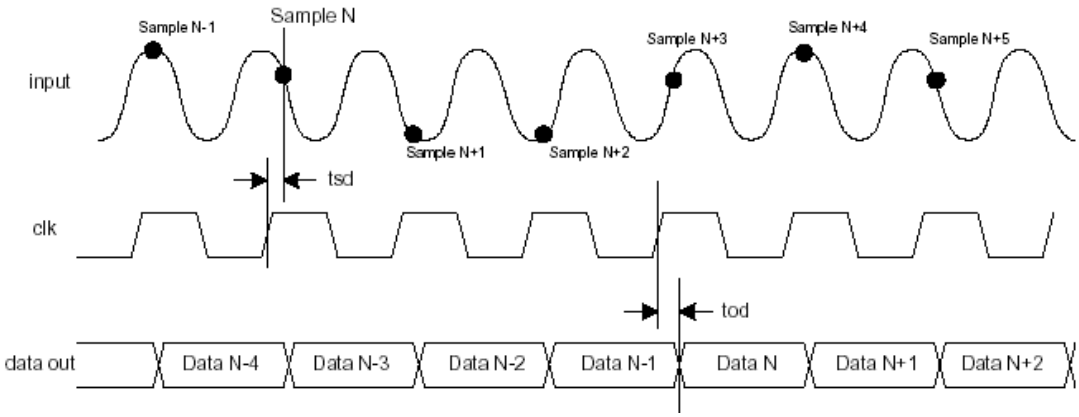

Figure 6. Timing of the RSSI ADC Pipelining Operation

8.1.4 Auxiliary ADC

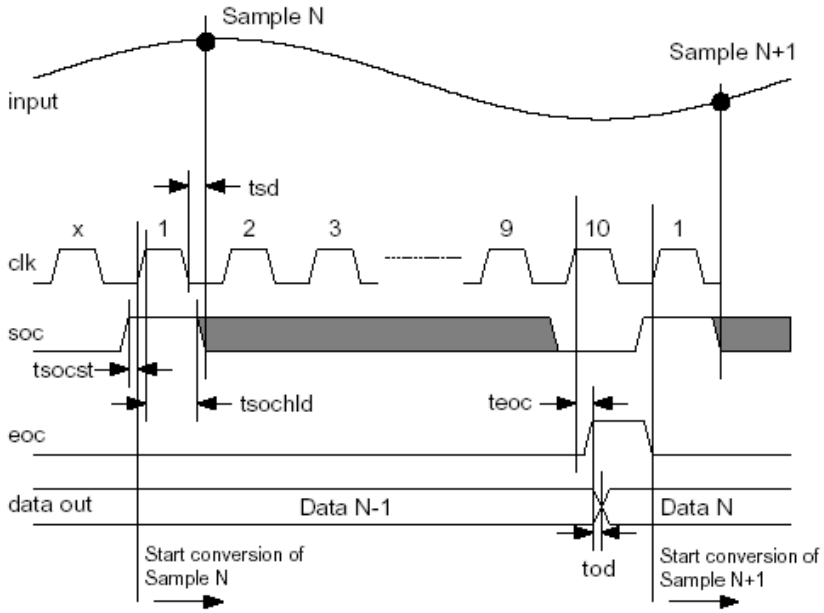

Figure 7. Timing of the Aux ADC Successive Approximation Operation

8.1.5 Auxiliary DAC

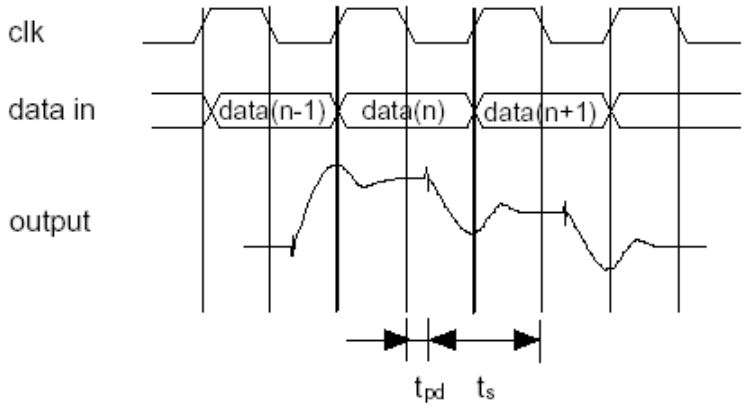

Figure 8. Conversion Cycle in Normal Operation for Aux DAC

Table 14. Aux DAC Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
tpd	Propagation delay	—	5	—	ns
ts	Settling time	—	80	—	ns

9 Mechanical Dimensions

The LP1071 is a 144-pin Very-thin Fine-pitch Ball Grid Array (VFBGA) package. All dimensions are mm.

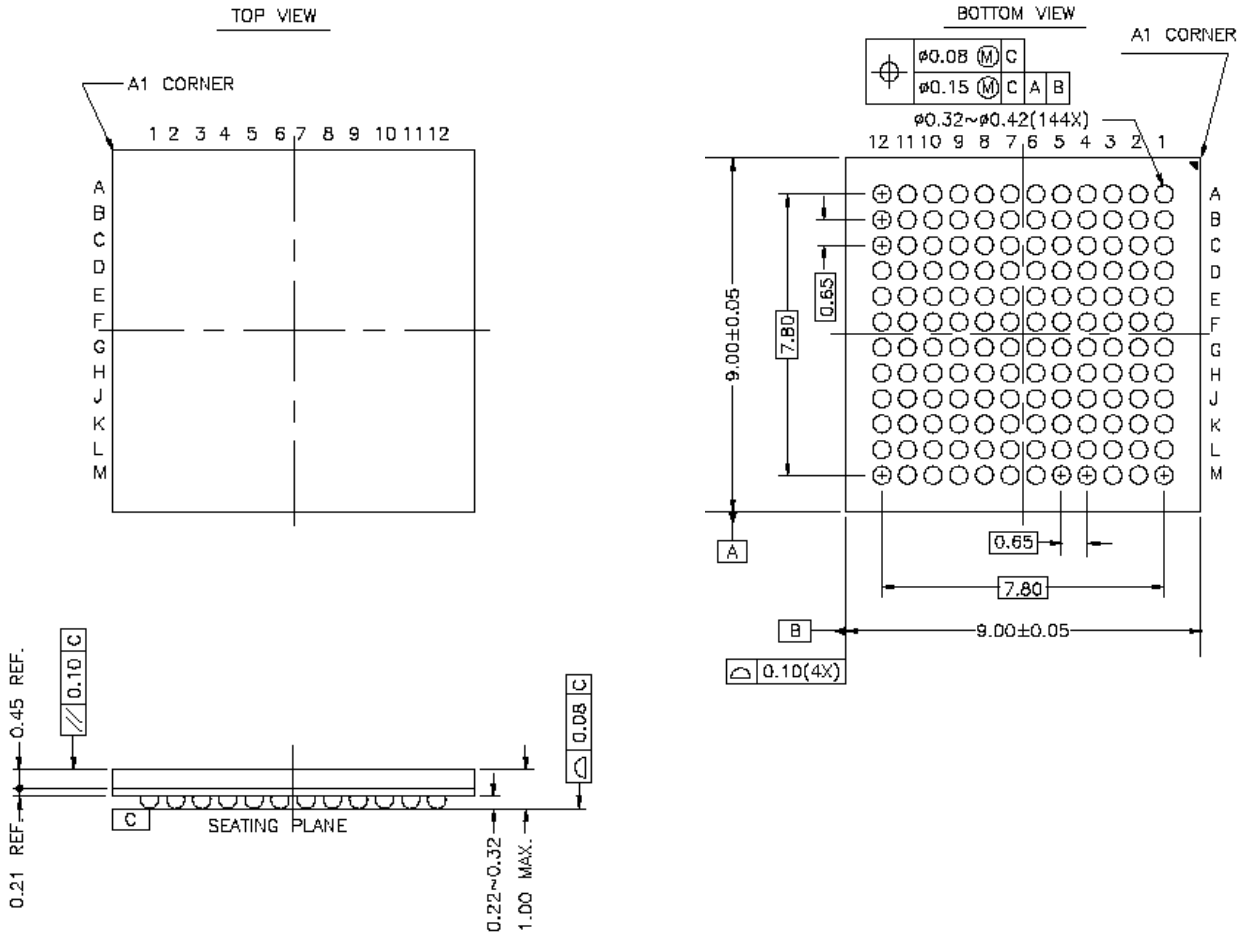

Figure 9. LP1071 Package

10 Development Support

In addition to the LP1071 baseband and MAC, Freescale provides developers with reference designs, development platform, software drivers, system development software, testing and debugging tools and a full set of technical documentation that includes:

- User Guide
- Data Sheet
- Schematics
- Gerber Files
- Application Notes

Freescale also provides multi-interface reference designs to aid device manufacturers with today's demanding time-to-market requirements.

11 Appendix: Comparison of LP1071 and LP1072

Table 15. Comparison of LP1071 and LP1072

Item	LP1071	LP1072
Network Standard Support	IEEE 802.11 a/b/g	
Network Architectures	Infrastructure, AdHoc	
Data Rates	802.11 a/g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11b: 1, 2, 5.5, 11 Mbps	
Modulation Techniques	BPSK, QPSK, 16QAM, 64QAM, CCK, OFDM, DSSS	
Security	40- and 128-bit WEP, TKIP, WPA, AES	
Receiver Sensitivity[1]	802.11g 6 Mbps: –91.0 dBm 9 Mbps: –90.5 dBm 12 Mbps: –88.6 dBm 18 Mbps: –86.4 dBm 24 Mbps: –81.4 dBm 36 Mbps: –79.9 dBm 48 Mbps: –76.1 dBm 54Mbps: –73.1 dBm 802.11b 1 Mbps: –97.4 dBm 2 Mbps: –94.1 dBm 5.5Mbps: –92.5 dBm 11Mbps: –88.9 dBm	
Power Consumption	Receive: 150 mW avg (@54Mbps) Listen: 132 mW Sleep: Less than 1 mW	
Supply Voltage	I/O: 3.0 – 3.6 Vdc Core: 1.8 ± 5% Vdc	
Operating Temperature	0 °C to +70 °C; < 95% humidity	
Host Interface	SDIO	SDIO CompactFlash Plus (CF+)
Other Interfaces	JTAG, 8 GPIOs, 1 UART, Serial / EEPROM	
Operating System Support	Microsoft Windows CE.net 3.0 and 4.2, 5.0 Microsoft Pocket PC 2002, 2003	
Package	144-pin VFBGA, 9 x 9 x 1.0 mm	200-pin VFBGA, 13 x 13 x 1.0 mm
Semiconductor Technology	0.18 micron	
RF Support	Airoha, Maxim	
Reference Designs	SDIO	CF+
Certification	Wi-Fi (incl. WPA), WHQL, FCC Part 15	

1 Using Maxim RF

12 Revision History

This document's updated format reflects that Freescale Semiconductor, Inc. acquired CommASIC on October 20, 2005. Since the release of the previous version of this document (Rev. 0.4), the technical content has not been updated.

NOTES

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