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**1.1 GHz Prescaler**

The MC12080 is a single modulus divide by 10, 20, 40, 80 prescaler for low power frequency division of a 1.1 GHz high frequency input signal. Divide ratio control inputs SW1, SW2 and SW3 select the required divide ratio of ÷10, ÷20, ÷40, or ÷80.

An external load resistor is required to terminate the output. A 820 Ω resistor is recommended to achieve a 1.2 V<sub>pp</sub> output swing, when dividing a 1.1 GHz input signal by the minimum divide by ratio of 10, assuming a 8.0 pF load. Output current can be minimized dependent on conditions such as output frequency, capacitive load being driven, and output voltage swing required. Typical values for load resistors are included in the V<sub>out</sub> specification for various divide ratios at 1.1 GHz input frequency.

- 1.1 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- Low Power 3.7mA Typical at V<sub>CC</sub> = 5.0 V
- Operating Temperature Range of -40 to 85°C

**FUNCTIONAL TABLE**

SW1	SW2	SW3	Divide Ratio
L	L	L	80
L	L	H	40
L	H	L	40
L	H	H	20
H	L	L	40
H	L	H	20
H	H	L	20
H	H	H	10

NOTE: SW1, SW2 and SW3: H = V<sub>CC</sub>, L = Open.

**MAXIMUM RATINGS**

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V <sub>CC</sub>	-0.5 to 7.0	Vdc
Operating Temperature Range	T <sub>A</sub>	-40 to 85	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to 150	°C
Maximum Output Current, Pin 4	I <sub>O</sub>	10	mA

NOTE: ESD data available upon request.

**MC12080**

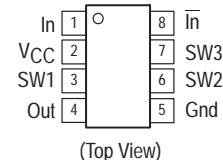
**MECL PLL COMPONENTS  
 ÷10/20/40/80 PRESCALER**

**SEMICONDUCTOR  
 TECHNICAL DATA**



**D SUFFIX**  
 PLASTIC PACKAGE  
 CASE 751  
 (SO-8, Tape and Reel Only)

**PIN CONNECTIONS**



**ORDERING INFORMATION**

Device	Operating Temperature Range	Package
MC12080DR2	T <sub>A</sub> = -40 to 85°C	SO-8

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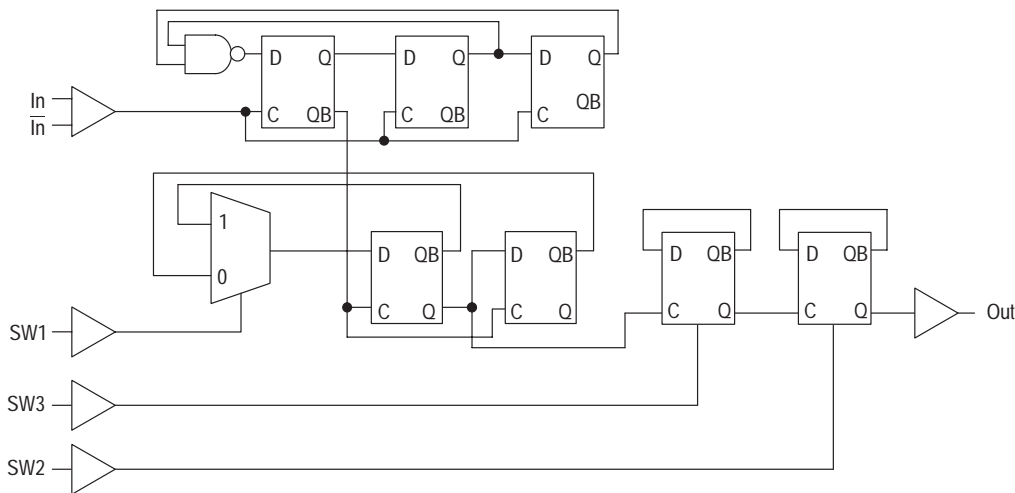
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**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.5$  to  $5.5$  V;  $T_A = -40$  to  $85^\circ\text{C}$ , unless otherwise noted.)

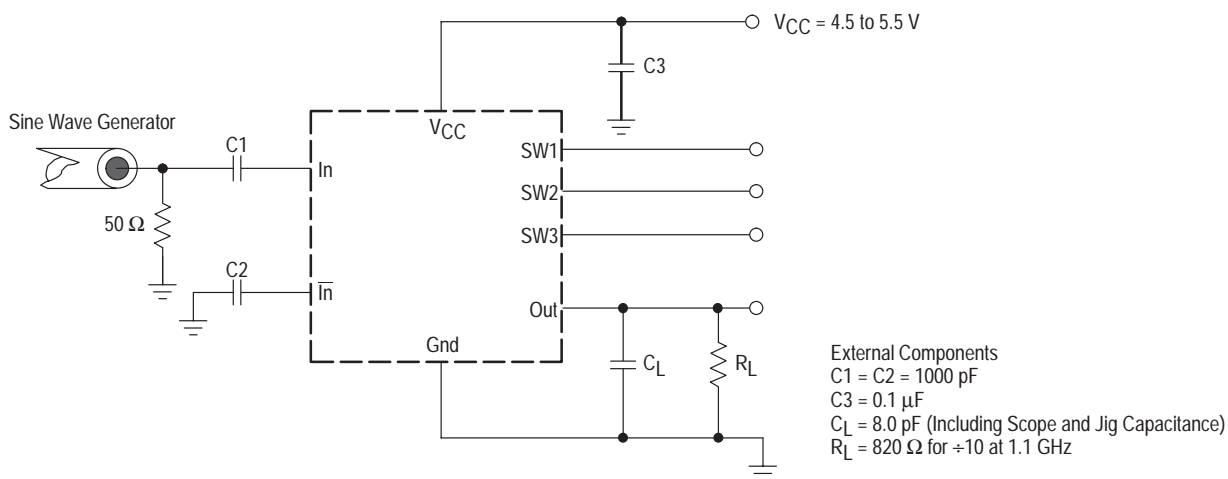
Parameter	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)	$f_t$	0.1	1.4	1.1	GHz
Supply Current Output (Pin 2)	$I_{CC}$	–	3.7	5.0	mA
Input Voltage Sensitivity 100 to 250 MHz 250 to 1100 MHz	$V_{in}$	400 100	– –	1000 1000	mVpp
Divide Ratio Control Input High (SW1, SW2, SW3)	$V_{IH}$	$V_{CC} - 0.5$ V	$V_{CC}$	$V_{CC} + 0.5$ V	V
Divide Ratio Control Input Low (SW1, SW2, SW3)	$V_{IL}$	Open	Open	Open	–
Output Voltage Swing [Note] $R_L = 820 \Omega$ , $I_O = 4.0$ mA for $\pm 10$ $R_L = 1.6$ k $\Omega$ , $I_O = 2.1$ mA for $\pm 20$ $R_L = 3.3$ k $\Omega$ , $I_O = 1.1$ mA for $\pm 40$ $R_L = 6.2$ k $\Omega$ , $I_O = 0.57$ mA for $\pm 80$	$V_{out}$	0.8	1.2	–	$V_{pp}$

**NOTE:** Assumes 8.0 pF load and 1.1 GHz input frequency (typical),  $I_O$  at  $V_{CC} = 5.0$  V and  $T_A = 25^\circ\text{C}$

**Figure 1. Logic Diagram**



**Figure 2. AC Test Circuit**



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Figure 3. Input Signal Amplitude versus Input Frequency

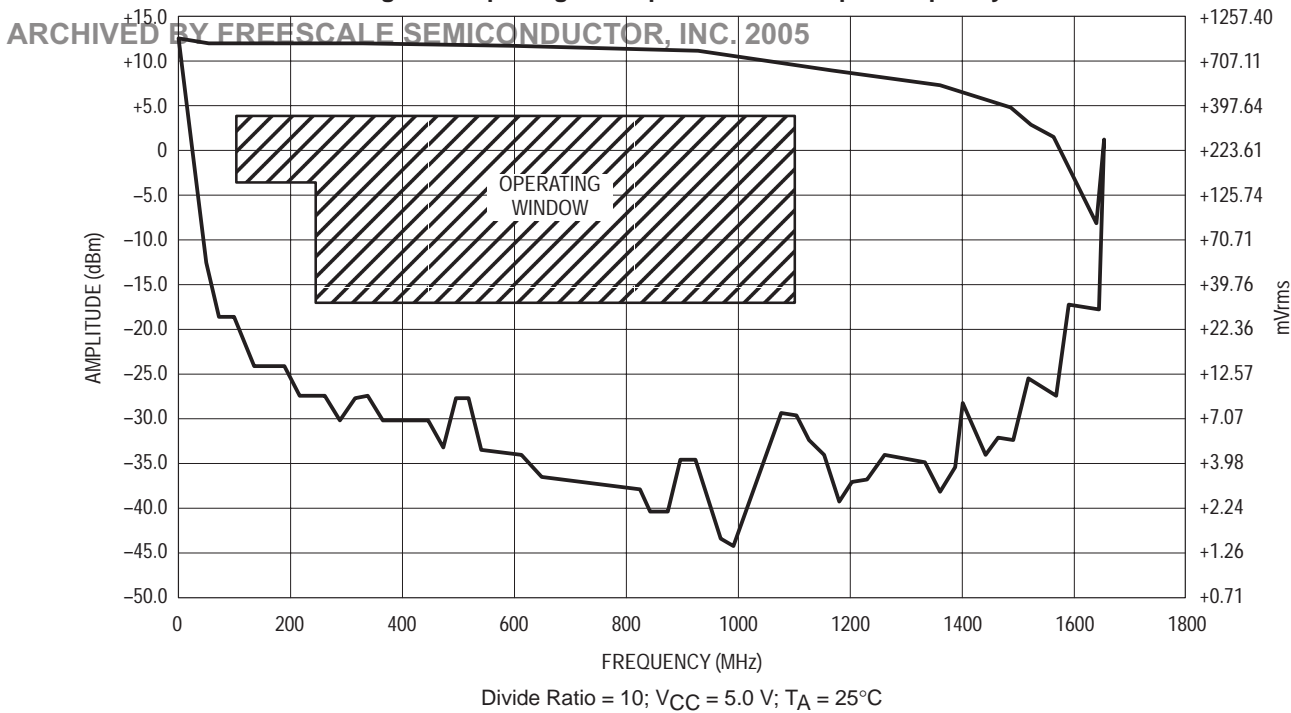
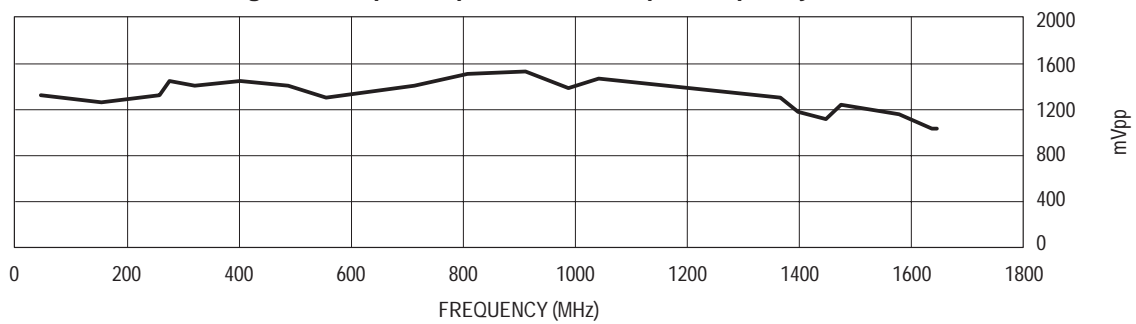


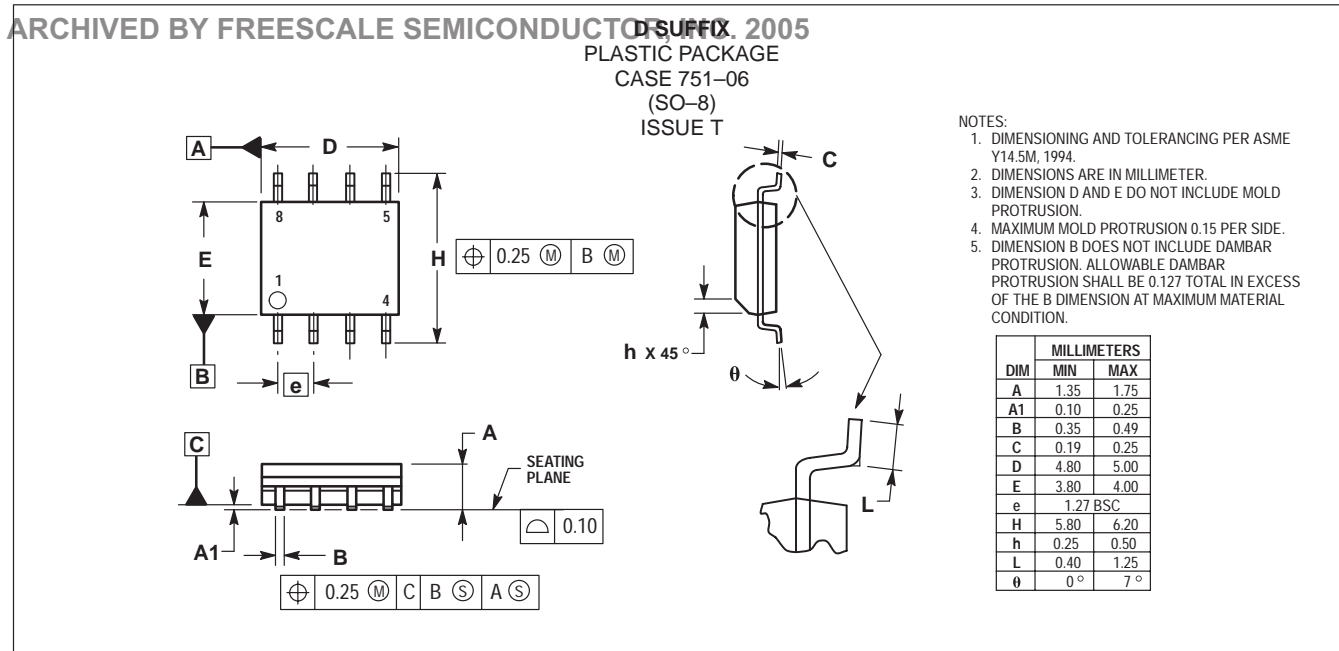
Figure 4. Output Amplitude versus Input Frequency



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OUTLINE DIMENSIONS



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