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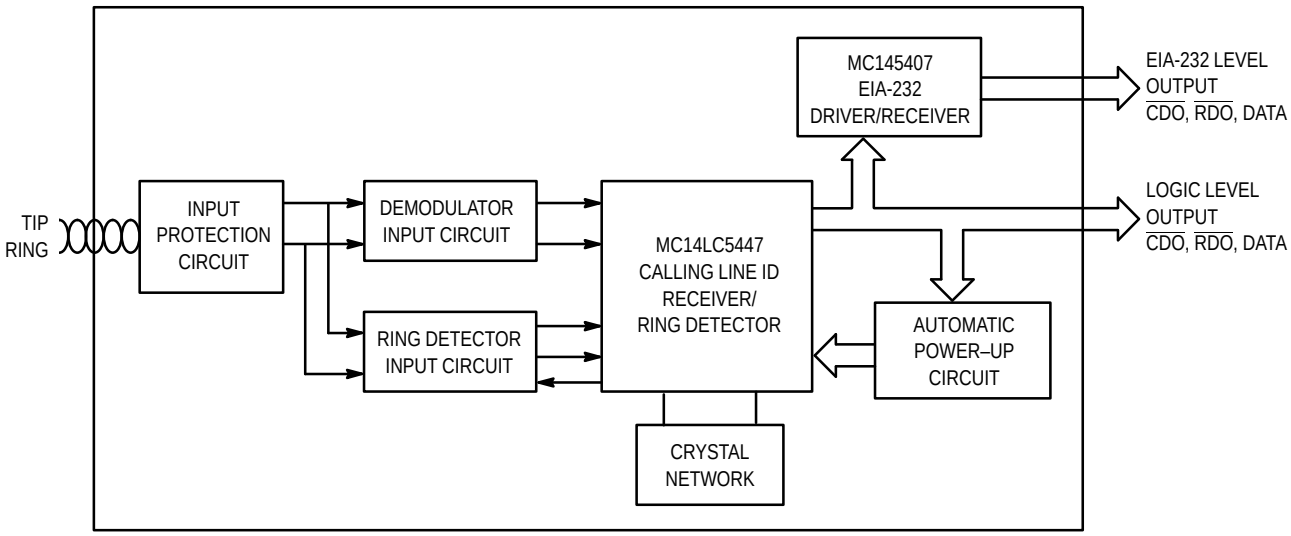
MC145460EVK

Calling Line Identification (CLID) Receiver Evaluation Kit User Guide

MC145460EVK BLOCK DIAGRAM



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SECTION 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The MC145460EVK is a low–cost evaluation platform for the MC14LC5447 Calling Line Identification (CLID) Receiver with Ring Detector. The MC145460EVK will facilitate development and testing of products that support the Bellcore Customer Premises Equipment (CPE) data interface, which enables services such as Calling Number Delivery (CND). The MC14LC5447 can be easily incorporated into any telephone, FAX, PBX, key system, answering machine, CND adjunct box, or other telephone equipment with the help of the MC145460EVK development kit.

1.2 ORGANIZATION OF USER GUIDE

This user guide is divided into six sections.

Section 1, General Description, introduces the MC145460EVK with a list of key features and a general hardware description.

Section 2, Getting Started, describes the MC145460EVK's initial configuration and explains how to set up automatic power–up mode and external clock sourcing. A simple test setup is also described.

Section 3, Connector Description, gives the pinout and function of each of the MC145460EVK's connectors.

Section 4, Jumper Description, explains the function of each jumper and how to configure them in different MC145460EVK operating modes.

Section 5, Parts List, includes the complete parts list for the evaluation board.

Section 6, Function Summary and Schematic, contains an operating mode summary and schematic.

1.3 FEATURES

- Easy Clip–On Access to Key MC14LC5447 Signals
- EIA–232 and Logic Level Ports for Connection to Any PC or MCU Development Platform
- Component Layout for Input Protection Circuit
- Carrier Detect, Ring Detect, and Data Status LEDs
- Generous Prototyping Area
- Large Pads and Wide Traces on Key Analog Line Interface Components for Easy Resoldering

1.4 GENERAL HARDWARE DESCRIPTION

Figure 1–1 shows the location of all important circuitry blocks, ICs, jumpers, and connectors on the MC145460EVK. Each of these components and circuit blocks perform a specific function which will be described in the following paragraphs. The jumper positions shown in Figure 1–1 will configure the MC14LC5447 for full–time power–up mode, which is described in Sections 4.4 and 2.1. The MC145460EVK is shipped with all the jumpers in the positions shown in Figure 1–1.

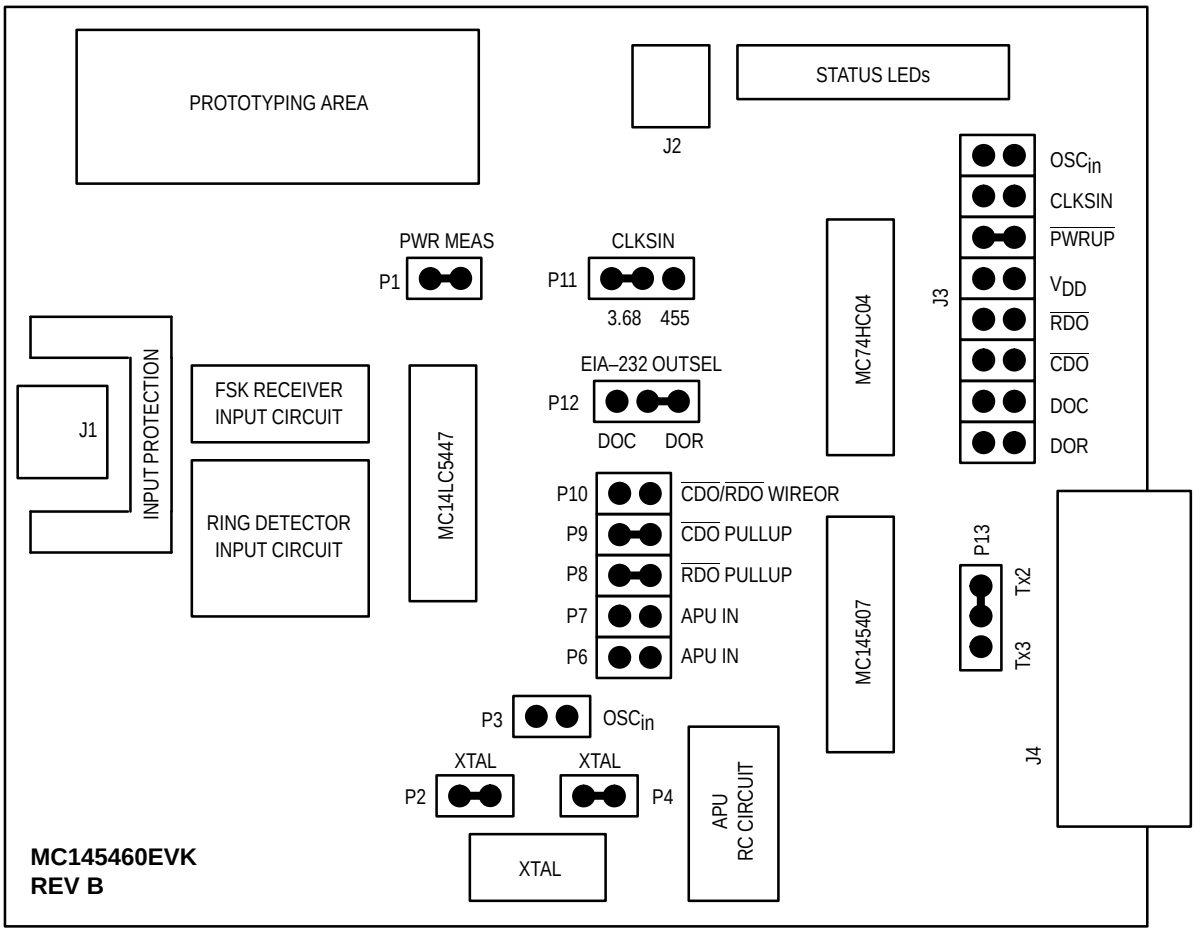

Figure 1–1. MC145460EVK Component Location

1.4.1 Circuit Blocks

The **INPUT PROTECTION** circuit components are not populated when the MC145460EVK is delivered, but component through holes are provided for two series current–limiting resistors and two back–to–back transient suppression devices of your choice. Before populating these resistors, cut the traces shorting R18 and R19 as shown in Figure 1–2. The schematic references for these components are R18, R19, D5, and D6.

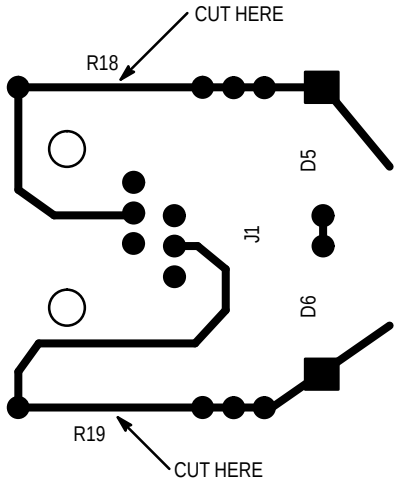

Figure 1–2. Bottom View of Printed Circuit Board Under J1

The **FSK RECEIVER INPUT CIRCUIT** provides the dc isolation necessary for proper operation of the MC14LC5447 FSK receiver. In addition, this circuit will provide some rejection of 60 Hz signals coupled in from power lines. Approximately 58 dB of 60 Hz rejection is included in the MC14LC5447 input bandpass filter. The schematic references for these components are R1, R2, C3, and C4.

The **RING DETECTOR INPUT CIRCUIT** is capacitively coupled to the telephone line (tip and ring) and includes a diode bridge rectifier and an attenuation network which is tuned for proper signal level input to the MC14LC5447 ring detector. For a more detailed description of this circuit and the MC14LC5447 ring detector, see the design information in the MC14LC5447 data sheet. The schematic references for these components are C1, C2, R3, R4, R5, R6, and D1 through D4.

The **STATUS LEDs** indicate the status of the MC14LC5447 digital output signals: Carrier Detect ($\overline{\text{CDO}}$), Ring Detect ($\overline{\text{RDO}}$), Raw Data (DOR), and Cooked Data (DOC), as well as the power supply (PWR) status. The schematic references for these components are D7, D9, D10, D11, and D12.

The **APU RC CIRCUIT** (automatic power–up circuit), is an RC network whose time constant is set to allow the MC14LC5447 to stay powered up from the end of a ring signal to the beginning of the FSK transmission (approximately 500 ms). The schematic references for these components are C6 and R17.

1.4.2 Integrated Circuits

There are three ICs on the MC145460EVK: MC14LC5447, MC145407, and MC74HC04. The schematic references for these ICs are U1, U2, and U3, respectively. The MC14LC5447 CLID receiver demodulates the 1200–baud FSK signal from tip and ring, and detects the power ring signal. The MC145407 EIA–232 driver/receiver is used to convert the MC14LC5447 digital outputs to EIA–232 levels, which are output on the DB–25 connector (J4). None of the MC145407 receivers are used. The MC74HC04 hex inverter IC is used to drive the status LEDs D9 through D12.

1.4.3 Connectors

There are four connectors on the MC145460EVK: J1, J2, J3, and J4. Tip and ring are brought on–board through J1, and power is brought in through J2. The $\overline{\text{CDO}}$, $\overline{\text{RDO}}$, and data (DOR or DOC) are output in EIA–232 format on the DB–25 connector referenced as J4. A straight post header (J3) can be used to clip–on to key digital signals.

1.4.4 Jumpers

The schematic references for the jumpers are P1, P2, P3, P4, P6, ... P13. Each jumper is labeled to indicate which function it performs. See Section 4 for more detail. The symbol used in this user guide for a shunted jumper is a line between two dots (see Figure 1–3). The symbol for an open jumper is shown in Figure 1–4.

Figure 1–3. Symbol for a Shunted Jumper

Figure 1–4. Symbol for an Open Jumper

SECTION 2
GETTING STARTED

This section describes the initial jumper settings on the MC145460EVK and explains how to configure the board for various MC14LC5447 operating modes. The last part of this section describes a simple test setup.

2.1 INITIAL JUMPER SETTINGS — FULL–TIME POWER–UP MODE

The MC145460EVK is shipped with the MC14LC5447 in full–time power–up mode. In this mode, the MC14LC5447 is ready to demodulate 1200 baud FSK data at all times. Shunts should be placed on jumpers P9 and P8, as well as across Pins 11 and 12 of J3. Jumpers P6, P7, and P10 should be left open. Jumpers P8 and P9 will connect a pull–up resistor to the Carrier Detect and Ring Detect open drain outputs of the MC14LC5447. The jumper across Pins 11 and 12 of J3 connects a power–on reset circuit to Pin 7 ($\overline{PWRUP}$) of the MC14LC5447.

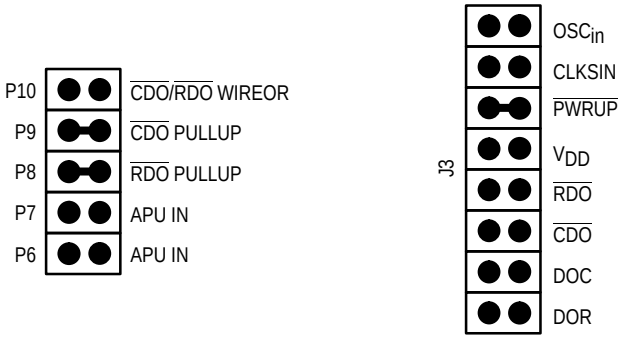

Figure 2–1. Full–Time Power–Up Mode

Since the MC145460EVK is shipped with a 3.68 MHz crystal oscillator, jumper P11 will be in the 3.68 position. This will put Pin 11 (CLKSIN) of the MC14LC5447 at V_{DD}.

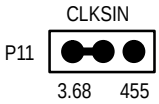

Figure 2–2. 3.68 MHz Operation

The MC145460EVK allows for use of either the on–board 3.68 MHz crystal or an external source for clocking of the MC14LC5447. When shipped, the MC145460EVK uses the on–board 3.68 MHz crystal, and as such, will have shunts in P2 and P4 to connect the crystal network to Pins 9 and 10 (OSC_{out} and OSC_{in}) of the MC14LC5447. P3 is left open, so as not to connect Pin 10 to the OSC_{in} input on J3.

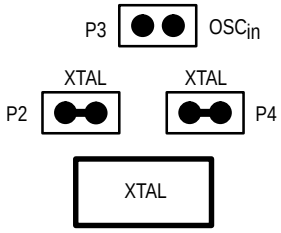

Figure 2–3. On–Board Crystal Operation

The EIA–232 port on the MC145460EVK allows data to be transmitted on Pins 2 or 3 of J4 to accommodate connections to DTE (e.g., a terminal) or DCE (e.g., a modem). Initially, the MC145460EVK is configured to transmit on Pin 2 of J4 by shunting P13 in the Tx2 position. To select the MC14LC5447 data output pin to be sent to the EIA–232 port, P12 needs to be shunted in the DOC or DOR position. Figure 2–4 shows the EIA–232 port initial configurations.

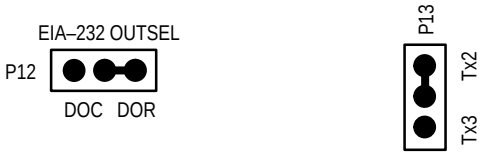

Figure 2–4. EIA–232 Port Configuration

2.2 AUTOMATIC POWER–UP MODE

In automatic power–up mode, the MC14LC5447 will power up only when a ring signal is detected. After the end of the power ring, an RC network will hold Pin 7 ($\overline{\text{PWRUP}}$) low until a sufficiently large carrier signal is present (approximately 500 ms). In this mode, Pins 12 ($\overline{\text{RDO}}$) and 13 ($\overline{\text{CDO}}$) are wire OR'd together by shunting P10 and leaving P9 and P8 open as shown in Figure 2–5. To connect the RC delay network into the circuit, P6 and P7 should be shunted as shown in Figure 2–5. The shunt across Pins 11 and 12 of J3 should be removed to disconnect the power–on reset circuit.

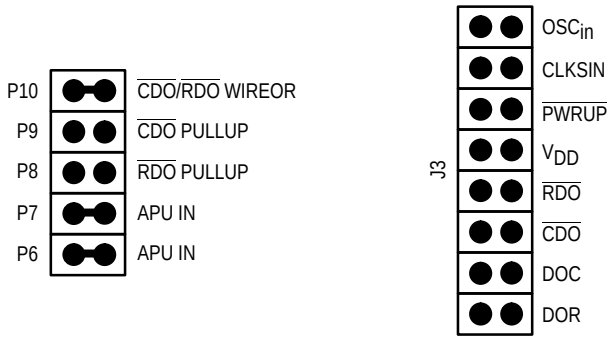

Figure 2–5. Automatic Power–Up Mode

2.3 EXTERNAL CLOCK SOURCING

To clock the MC14LC5447 externally, the on–board crystal network has to be disconnected by leaving P2 and P4 open. The external clock source should be connected to Pin 15 of J3, and P3 should be shunted to connect this source to Pin 10 (OSC_{in}) of the MC14LC5447, as shown in Figure 2–6.

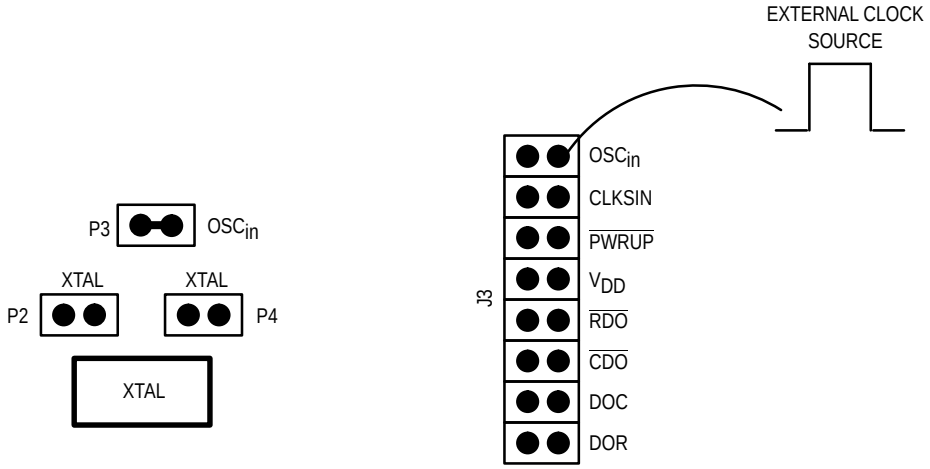

Figure 2–6. External Clock Sourcing

2.4 A SIMPLE TEST SETUP

The MC145460EVK is designed to provide an interface to software development platforms, to enable the developer to test the MC14LC5447 FSK receiver under worst case loop conditions, and to test the ring detector over a wide variety of ring signals. Even though the MC14LC5447 was designed to work well under these extreme conditions, the developer must ensure that the total system enables optimum performance to be achieved. Thus, the developer must be aware of the nature of these conditions and be able to test the system against them. To point the developer in the right direction, a simple test setup will be described.

Typical telephone line impairments include: attenuation, excessive noise, amplitude distortion, and envelope delay distortion. All of these factors contribute to degrade the quality of the FSK signal and ultimately add jitter and bit errors to the MC14LC5447 data output. In a minimal test setup, the ability to attenuate the FSK signal and generate random noise will be needed to produce small signal–to–noise ratios (SNR) at low amplitudes.

A versatile caller ID simulator, built by Rochelle Communications Inc., can reproduce these minimal conditions as well as generate standard power ring signals. To aid in software development, this simulator can also transmit single and multiple message format data as defined in the Bellcore TR–TSY–000030 specification. The PC–based Rochelle Caller ID Telephone Line Simulator can be easily connected to the MC145460EVK with a standard telephone cable. Connecting the EIA–232 port of the MC145460EVK to any terminal or terminal emulator, will allow the caller ID information to be displayed as it is received by the MC14LC5447. The MC145460EVK may be configured in the automatic or full–time power–up mode. This simple setup is shown in Figure 2–7.

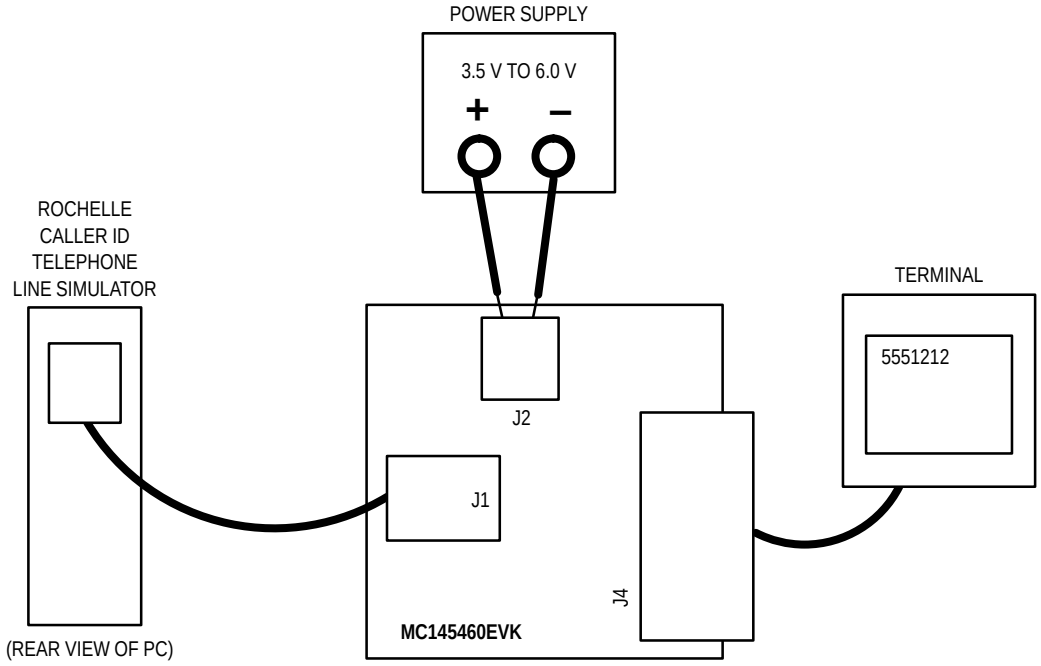

Figure 2–7. A Simple Test Setup

SECTION 3
CONNECTOR DESCRIPTION

3.1 CONNECTOR LIST

Table 3–1. Connector List

Connector	Schematic Reference	See User Guide Section
Power Supply	J2	3.2
Tip and RIng	J1	3.3
Logical Level Digital I/O	J3	3.4
EIA–232 Digital Output	J4	3.5

3.2 POWER SUPPLY — J2

The power supply connector is a snap–down type. D7 will light up when power is applied. Temporary overvoltage and reverse voltage protection is provided by a 7.5 V zener diode (D8) connected across Pins 1 and 2 of J2. A 47 µF (C7) capacitor decouples the power supply. The power supply voltage range is 3.5 to 6.0 V.

Table 3–2. Power Supply Connector Pins — J4

Pin	Signal
1	(+) Positive Power Supply — V_{DD}
2	(–) Negative Power Supply — GND

The power supply should be connected as shown in Figure 3–1, with the positive power supply lead connected to the terminal on J4 closest to the prototyping area.

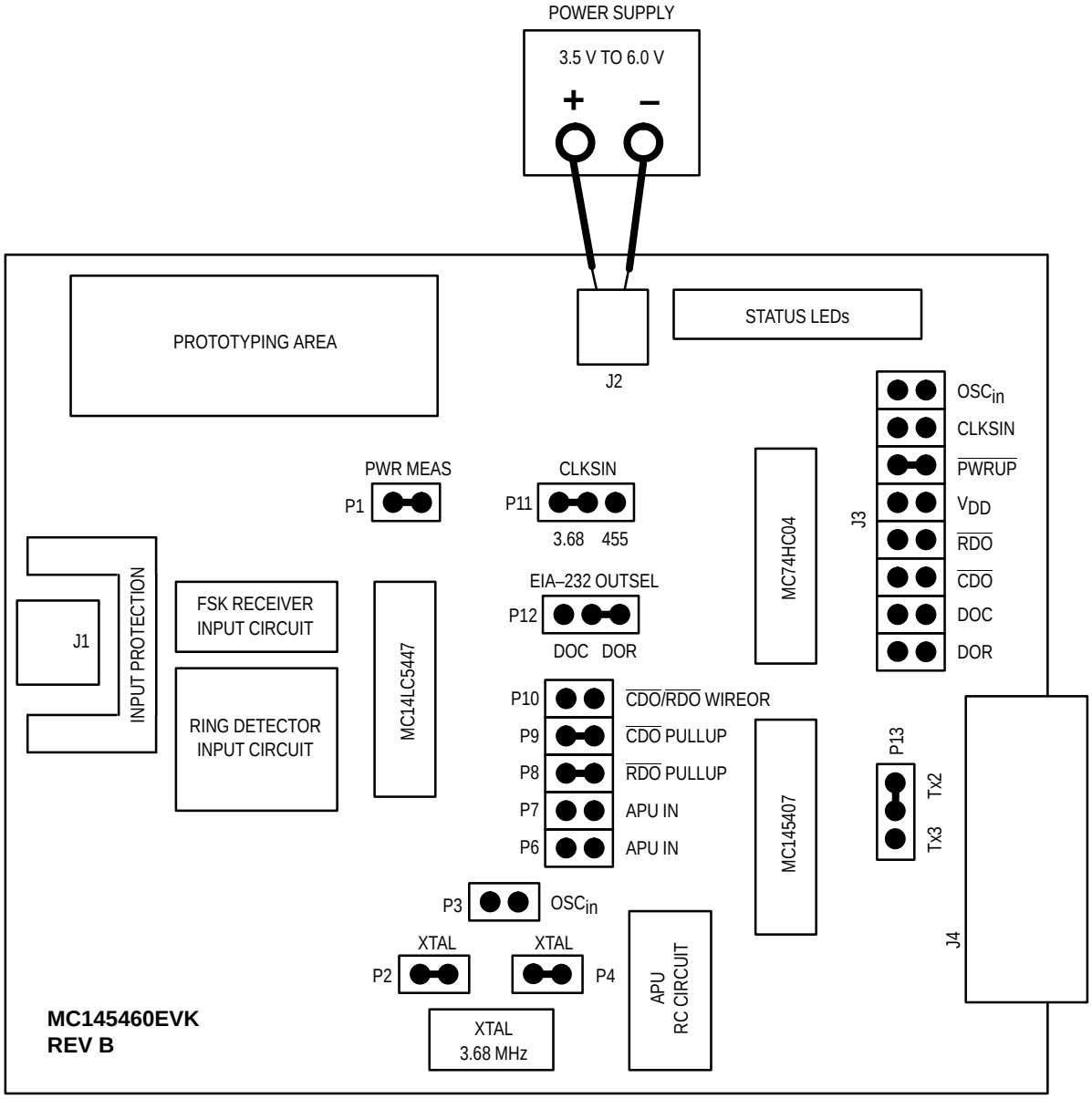

Figure 3–1. Power Supply Connection

3.3 TIP AND RING — J1

TIP and RING are input to the evaluation board through J1, a standard six–conductor RJ11 telephone jack.

Table 3–3. RJ11 Telephone Connector Pins — J1

Pin	Signal
1	NC
2	NC
3	RING
4	TIP
5	NC
6	NC

NOTE: NC = Not Connected.

3.4 LINE LEVEL DIGITAL I/O — J3

J3 is a 2X8 pin post header which provides easy access to the MC14LC5447 digital signals.

Table 3–4. Line Level Digital I/O Connector — J3

Pin	Signal	Remarks
1	DOR	Raw data output, connected to Pin 14 of MC14LC5447
3	DOC	Cooked data output, connected to Pin 15 of MC14LC5447
5	$\overline{\text{CDO}}$	Carrier detect output, connected to Pin 13 of MC14LC5447
7	$\overline{\text{RDO}}$	Raw data output, connected to Pin 12 of MC14LC5447
9	V_{DD}	Connected to positive power supply
11	$\overline{\text{PWRUP}}$	Power–up input, connected to Pin 7 of MC14LC5447
12	POWER–ON RESET	This pin is connected to an RC power–on reset circuit
13	CLKSIN	Oscillator frequency select input, connected to Pin 11 of MC14LC5447
15	OSC_{in}	Oscillator input, connected to Pin 10 of MC14LC5447 when jumper P3 is shunted
2, 4, 6, 8, 10, 14, 16	GROUND	All even–numbered pins are connected to ground, except Pin 12

3.5 EIA–232 DIGITAL OUTPUT — J4

J4 is a standard DB–25 female connector and provides the $\overline{\text{CDO}}$, $\overline{\text{RDO}}$, and DOR or DOC signals at EIA–232 levels. P12 is used to select the cooked data or raw data signals (Pins 15 and 14 of the MC14LC5447) to be output to J4. P13 selects the data output pin on J4. If J4 is to be configured as a DTE, then P13 should be shunted in the position marked Tx2; for a DCE, P13 should be shunted in the Tx3 position.

Table 3–5. EIA–232 Digital I/O Connector — J4

Pin	Signal	Remarks
2	DATA OUT	Data output for DTE with P13 in the Tx2 position
3	DATA OUT	Data output for DCE with P13 in the Tx3 position
7	GROUND	Signal ground
8	$\overline{\text{CDO}}$	Carrier detect output
22	$\overline{\text{RDO}}$	Ring detect output

SECTION 4
JUMPER DESCRIPTION

4.1 JUMPER LIST

Table 4–1. Jumper List

Schematic/ Silk Screen Reference	Jumper Function	See User Guide Section
P1 PWR MEAS	MC14LC5447 I_{DD} Current Monitor	4.2
P2 XTAL	Crystal Network Connect	4.3
P4 XTAL	Crystal Network Connect	4.3
P3 OSCIN	Oscillator Input Select	4.3
P6 APU IN	Automatic Power–Up	4.4
P7 APU IN	Automatic Power–Up	4.4
P8 RD PULLUP	$\overline{RDO}$ PULLUP Resistor Connect	4.4
P9 CD PULLUP	$\overline{CDO}$ PULLUP Resistor Connect	4.4
P10 CD/RD WIRE OR	$\overline{CDO}$ to $\overline{RDO}$ Shunt	4.4
P11 CLKSEL	Oscillator Frequency Select	4.5
P12 COOKD/RAWD	EIA–232 Data Output Select	4.6
P13 TX2/TX3	DB–25 Transmit Pin Select	4.7

4.2 MC14LC5447 I_{DD} CURRENT MONITORING — P1

During normal operation of the MC145460EVK, this jumper should be shunted so that a positive power supply connection is made to the MC14LC5447 CLID receiver. However, an ammeter may be connected across Pins 1 and 2 of P1 to measure the current delivered to the MC14LC5447.

4.3 OSCILLATOR SOURCE SELECT — P2, P3, P4

The MC14LC5447 oscillator may be driven by the on–board crystal network or an external clock source. To use the on–board crystal network, jumpers P2 and P4 should be shunted, and jumper P3 should be left open. If an external clock source is to be used, P2 and P4 should be left open and P3 shunted. The external clock source can be connected to J3 Pin 15, which is connected to the OSC_{in} (Pin 10) of the MC14LC5447.

4.4 POWER–UP CONTROL — P6, P7, P8, P9, P10

The MC14LC5447 power–up and standby states are controlled by Pin 7 on the MC14LC5447. When Pin 7 is low, the MC14LC5447 is powered up and ready to demodulate incoming FSK data; when high, the IC is powered down (standby mode). The MC145460EVK may be configured for the MC14LC5447 automatic power–up mode or full–time power–up mode. In full–time power–up mode, a shunt is put across J3 Pins 11 and 12. This will connect the power–on reset circuit to Pin 7 ($\overline{\text{PWRUP}}$). In automatic power–up mode, P8 and P9 should be open and P6, P7, and P10 shunted. There should not be a shunt across J3 Pins 11 and 12 in automatic power–up mode. If Pin 7 of the MC14LC5447 is to be driven externally, then P6 through P10 should be configured as in the full–time power–up mode, and the shunt across J3–11 and J3–12 left open. The power–up signal is then directly accessible on J3–11.

Table 4–2. Power–Up Control Jumper States

Function	Jumper State					
	P6	P7	P8	P9	P10	J3–10, J3–11
Automatic Power–Up Mode	Shunted	Shunted	Open	Open	Shunted	Open
Full–Time Power–Up Mode	Open	Open	Shunted	Shunted	Open	Shunted
External Power–Up	Open	Open	Shunted	Shunted	Open	Open

4.5 OSCILLATOR FREQUENCY SELECT — P11

This jumper controls the state of the MC14LC5447 Pin 11 (CLKSIN). With the jumper in the position marked 3.68, CLKSIN will be at the positive power supply (V_{DD}), and in the position marked 455, it will be at the negative power supply (GND).

4.6 EIA–232 DATA OUTPUT SELECT — P12

P12 will allow either DOC (COOKD) or DOR (RAWD) to be output to J4. With a shunt in the right position on P12, raw data from Pin 14 of the MC14LC5447 will be sent to J4. With a shunt in the left position, cooked data from Pin 15 will be sent to J4.

4.7 EIA–232 TRANSMIT PIN SELECT — P13

This option will allow the evaluation board to connect the DTEs or DCEs through the DB–25 connector J4. To connect to a DCE, put this jumper in the Tx2 position. Data will then be transmitted on J4–2. To connect to a DTE, put this jumper in the Tx3 position. Data will then be transmitted on J4–3. Since the MC14LC5447 has two data output pins, DOR (Pin 14) and DOC (Pin 15), another jumper, P12, will select which one of these signals is presented to J4.

SECTION 5
PARTS LIST

Table 5–1. MC145460EVK Evaluation Board Parts List

Item No.	Manufacturer	Part No.	Description	Quantity	Designators
1	Augat/RDI	2SV–02	Power Connector	1	J2
2	3M or equivalent	929836–01–36	2 Row Header 0.100″	1	J3
3	3M or equivalent	929834–01–36	1 Row Header 0.100″	3	P11, P12, P13
4	Mallory or equivalent	SKR470M1CD11	47 µF 16 V Electrolytic Cap	1	C7
5	Kemet or equivalent	C410C223K5R5CA	0.022 µF Cap	1	C5
6	Kemet or equivalent	C410C104M5U5CA	0.1 µF Cap	4	C14,jC15, C16, C17
7	Kemet or equivalent	C420C334M5U5CA	0.33 µF Cap	1	C6
8	Kemet or equivalent	C330C105K5R5CA	1 µF Cap	4	C10, C11, C12, C13
9	Kemet or equivalent	C410C330J1G5CA	33 pF Cap	2	C8, C9
10	Cornell Dubilier	DME2P22K	0.22 µF 250 V Cap	2	C1, C2
11	Philips or equivalent	DD–501	500 pF 250 V Cap	2	C3, C4
12	Amphenol	617–C025S–AJ120	DB25F Connector	1	J4
13	Motorola	1N4004	Diode, Axial Lead	4	D1, D2, D3, D4
14	Motorola	1N5922B	7.5 V Zener, Axial Lead	1	D8
15	Customer	Customer Determined	Diode	2	D5, D6
16	Motorola	MC74HC04AN	Hex Inverters 14–Pin DIP	1	U3
17	Motorola	MC14LC5447P	CLID 16–Pin DIP	1	U1
18	Motorola	MC145407P	5 V Driver/Receiver 20–Pin DIP	1	U2
19	Raltron or equivalent	A–3.6864–18	3.6864 MHz	1	Y1
20	3M or equivalent	929836–01–36	2–Pin Header, 0.100″	9	P1, P2, P3, P4, P6, P7, P8, P9, P10
21	Dialight or equivalent	521–9250	Green LED	3	D7, D9, D10
22	Dialight or equivalent	521–9240	Red LED	2	D11, D12
23	Dale or equivalent	CMF–551004GT–00	1M Resistor, 1/8 W Axial	1	R20
24	Dale or equivalent	CMF–552704GT–00	2.7M Resistor, 1/8 W Axial	1	R6
25	Dale or equivalent	CMF–554704GT–00	4.7M Resistor, 1/8 W Axial	1	R17
26	Dale or equivalent	CMF–551002GT–00	10K Resistor, 1/8 W Axial	4	R1, R2, R8, R9
27	Dale or equivalent	CMF–551005GT–00	10M Resistor, 1/8 W Axial	1	R7
28	Dale or equivalent	CMF–551502GT–00	15K Resistor, 1/8 W Axial	1	R5
29	Dale or equivalent	CMF–551802GT–00	18K Resistor, 1/8 W Axial	1	R4
30	Dale or equivalent	CMF–553300GT–00	330 Resistor, 1/8 W Axial	5	R12, R13, R14, R15, R16
31	Dale or equivalent	CMF–554703GT–00	470K Resistor, 1/8 W Axial	1	R3
32	Customer	Customer Determined	Customer Determined	2	R18, R19
33	AMP	520470–3	RJ11 Connector	1	J1
34	Augat	814–AG11D–ESL	14–Pin Socket	1	U3
35	Augat	816–AG11D–ESL	16–Pin Socket	1	U1
36	Augat	820–AG11D–ESL	20–Pin Socket	1	U2
37	3M	SJ5027SP	Bumper	4	

SECTION 6
FUNCTION SUMMARY AND SCHEMATIC

Table 6–1. Function Summary Matrix

Jumper	Full–Time Power–Up Mode	Automatic Power–Up Mode	On–Board 3.68 MHz XTAL Operation	External Clock Sourcing	See User Guide Section
P1 — MC14LC5447 I_{DD} Monitor	—	—	—	—	4.2
P2 — XTAL Connect	—	—	Shunted	Open	4.3
P3 — OSC_{in} Patch	—	—	Open	Shunted	4.3
P4 — XTAL Connect	—	—	Shunted	Open	4.3
P6 — Automatic Power–Up	Open	Shunted	—	—	4.4
P7 — Automatic Power–Up	Open	Shunted	—	—	4.4
P8 — $\overline{RDO}$ PULLUP	Shunted	Open	—	—	4.4
P9 — $\overline{CDO}$ PULLUP	Shunted	Open	—	—	4.4
P10 — $\overline{CDO}$/$\overline{RDO}$ WIREOR	Open	Shunted	—	—	4.4
P11 — CLKSIN	—	—	3.68 Position	—	4.5
P12 — EIA–232 Output Select	—	—	—	—	4.6
P13 — DB–25 Output Select	—	—	—	—	4.7
J3–11, J3–12 Power–On Reset	Shunted	Open	—	—	3.4

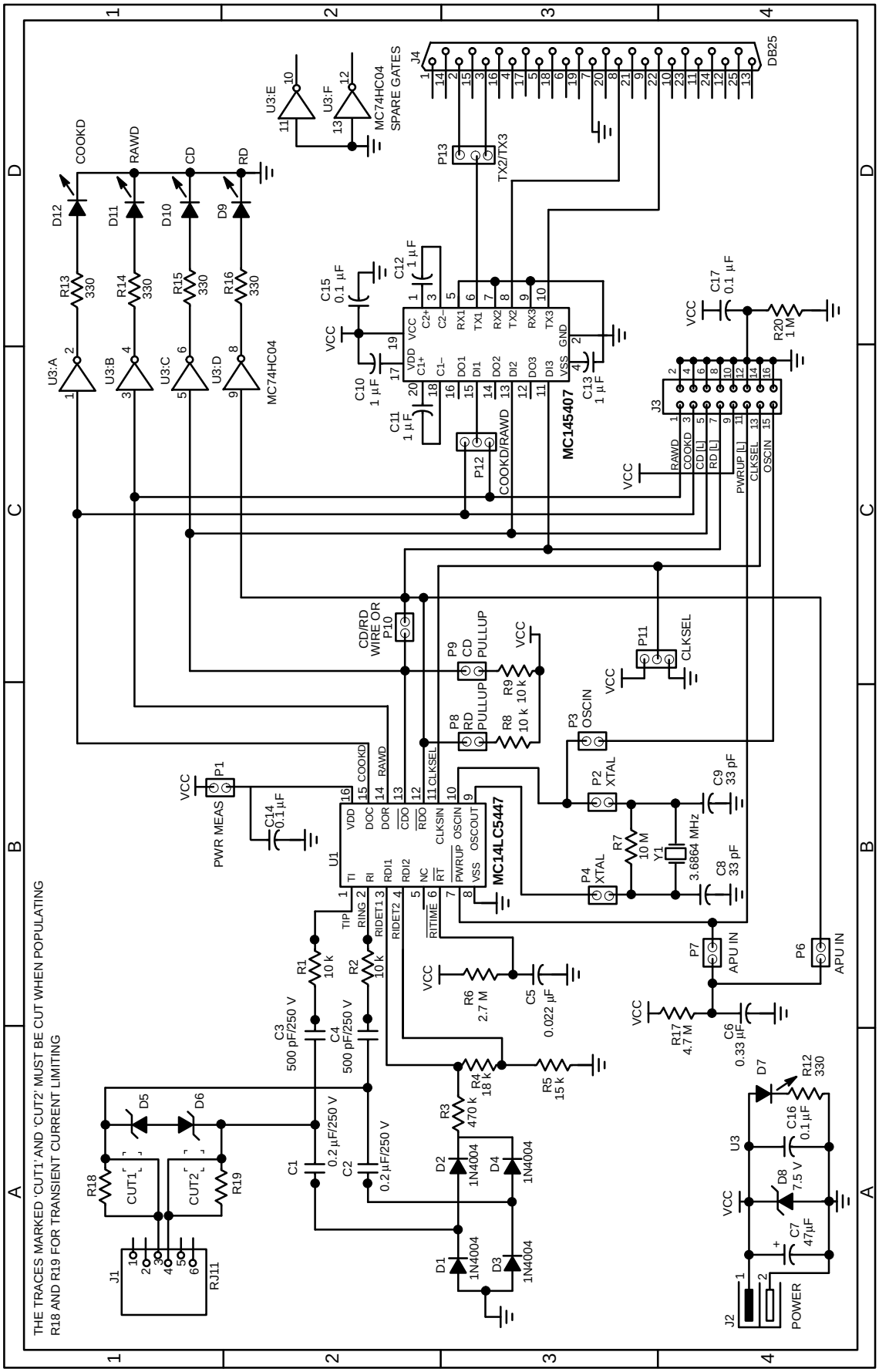

Figure 6–1. MC145460EVK Schematic

APPENDIX
CALLING LINE IDENTIFICATION SIMULATORS

Rochelle Caller ID Telephone Line Simulator

Rochelle Communications Inc.
P.O. Box 141189
Austin, TX 78714

Telephone: (800) 542–8808 (inside the USA)
(512) 794–0088 (outside the USA)

PC–based simulator with software.

Micro Seven Calling Number Delivery (Caller ID) Simulator

Micro Seven, Inc.
15100 S.W. Koll Parkway, Suite D
P.O. Box 5597
Beaverton, Oregon 97006

Telephone: (503) 626–7428
Fax: (503) 644–9458

Option for the standalone Micro Seven Mini–PBX Simulator.

NOTE: Motorola can not recommend one manufacturer over another and in no way implies that this is a complete listing.

ADDITIONAL DOCUMENTATION

More detailed documentation describing components is available from your local Motorola distributor or semiconductor sales office, or through a Motorola Literature Distribution Center.

Document Title	Order Number
MC14LC5447 Calling Line Identification (CLID) Receiver with Ring Detector	MC14LC5447/D
MC145407 5 V Only Driver/Receiver	MC145407/D

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ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

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