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Advance Information

FLEX™ Paging RF/IF Receiver Board

This document contains the information of a FLEX paging receiver reference prototype. This FLEX paging receiver board is a high performance RF/IF front–end for using in FLEX pager. This board employs Motorola's high frequency transistors MMBR941 as well as its M–ary FSK FM IF receiver MC2800 as the core. The whole board includes a LNA, an oscillator, a mixer and a FSK IF receiver.

Features:

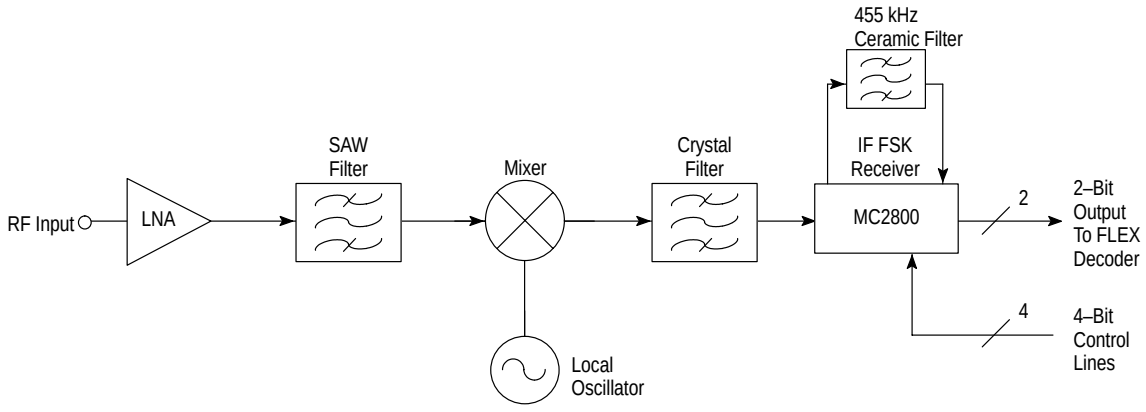
- Input RF Frequency: 284.14 MHz
- Excellent Sensitivity: –124 dBm
- Operating Voltage: V_{CC} = 1.1 to 1.7 V
- Total Current Consumption: 3.2 mA @ V_{CC} = 1.1 V
- Switchable Bit–Rate Filter to Support All Kinds of FLEX Data Rate
- Separate Interfacing Supply Voltage

ORDERING INFORMATION

Device	Description
MC2800EVK	FLEX Paging Receiver Board Evaluation Kit

FLEX is a trademark of Motorola, Inc.

Figure 1. System Block Diagram



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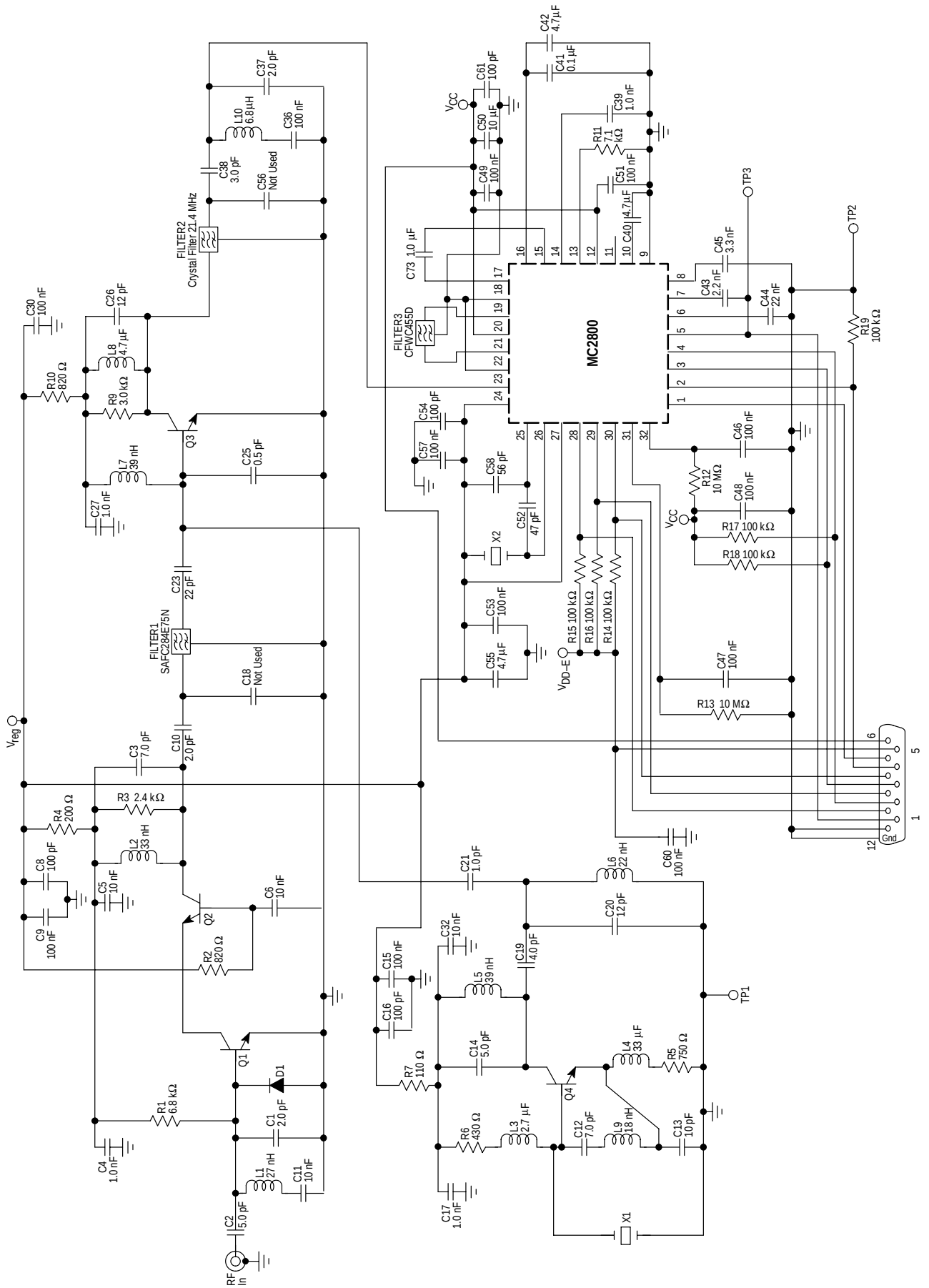

Figure 2. RF/IF Receiver Board Schematic

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{CC}	1.1	–	1.7	V
RF Input Frequency		284.135	–	284.145	MHz
FLEX Decoder Interface Voltage	$V_{DD–E}$	3.0	–	3.3	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 1.1 V, $V_{DD–E}$ = 3.3 V, V_{reg} = 0.960, f_{RF} = 284.140 MHz, unless otherwise noted.)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
LOW NOISE AMPLIFIER						
Power Gain [Note 1]	@ 284.140 MHz	G_P	–	20.6	–	dB
Input Return Loss [Note 1]		S_{11}	–	–4.2	–	dB
Output Impedance [Note 1]		Z_{out}	–	173 +j75	–	Ω
Noise Figure [Note 1]		NF	–	2.45	–	dB
Current Consumption	V_{reg} = 0.960 V	I	–	890	–	µA
SAW FILTER						
Insertion Loss	Terminating Impedance = 230 Ω		–	1.0	–	dB
FIRST LOCAL OSCILLATOR						
Crystal Frequency		f_C	–	65.681250	–	MHz
Desired Output Frequency	4th Harmonic	f_{LO1}	–	262.74194	–	MHz
Desired Output Power		P_{LO}	–	–23.9	–	dBm
3rd Harmonic Output Power	Referenced to 4th Harmonic	H3	–	–13.5	–	dBc
5th Harmonic Output Power		H5	–	–11.3	–	dBc
Startup Time	EN transits from '0' to '1'		–	<4.5	–	ms
Current Consumption	V_{reg} = 0.960 V	I	–	560	–	µA
LNA + SAW FILTER + MIXER						
Conversion Gain [Note 2]	Input @ 284.140 MHz Output @ 21.400 MHz	G_C	–	32.4	–	dB
Noise Figure [Note 2]		NF	–	2.69	–	dB
Output Impedance	@ 21.400 MHz	Z_{out}	–	1.13 – j1.16	–	kΩ
Current Consumption of Mixer	V_{reg} = 0.960 V	I	–	330	–	µA
CRYSTAL FILTER						
Insertion Loss	Terminating Impedance = 1.5 kΩ		–	0.9	–	dB
IF RECEIVER MC2800						
Input Impedance	@ 21.400 MHz	Z_{in}	–	770 – j550	–	Ω
Second Local Oscillator Frequency		f_{LO2}	–	20.94506	–	MHz
Startup Time of 2nd LO	EN transits from '0' to '1'		–	<1.0	–	ms

NOTES: 1. Output of the LNA is matched to 230 Ω by inserting a 180 Ω resistor in series with its output port.
2. Output of the Mixer is matched to 1.5050 kΩ by inserting a 1500 Ω resistor in series with its output port.
3. The circuit of this test board is the same as the schematic in Figure 2.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 1.1 V, $V_{DD–E}$ = 3.3 V, V_{reg} = 0.960, f_{RF} = 284.140 MHz, unless otherwise noted.)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
OVERALL RECEIVER PERFORMANCE						
(a) Phase A Characteristics [Note 3]						
Sensitivity						dBm
6400/4 Level FSK	@ 284.140 MHz R1 = '0' and R2 = '1'		–	–124	–	
1600/2 Level FSK	@ 284.140 MHz R1 = '1' and R2 = '0'		–	–125	–	
Co–channel Rejection	6400/4 Level FSK @ 284.140 MHz R1 = '0' and R2 = '1'		–	–6.0	–	dB
Adjacent Channel Rejection						dB
Low Side			–	71	–	
High Side			–	58	–	
Image Rejection						dB
First IF			–	62	–	
Second IF			–	65	–	
Intermodulation Rejection						dB
Low Side			–	48	–	
High Side			–	48	–	
Blocking Rejection						dB
@ 1.0 MHz			–	74	–	
@ 5.0 MHz			–	77	–	
Total Current Consumption		I_T				
Power Up	@ V_{CC} = 1.1 V EN = '1' and CL = '0'		–	3.18	–	mA
Power Down	@ V_{CC} = 1.1 V EN = '0' and CL = '0'		–	<30	–	µA
(b) Phase B Characteristics [Note 3]						
Sensitivity						dBm
6400/4 Level FSK	@ 284.140 MHz R1 = '0' and R2 = '1'		–	–120	–	
1600/2 Level FSK	@ 284.140 MHz R1 = '1' and R2 = '0'		–	–125	–	
Co–channel Rejection	6400/4 Level FSK @ 284.140 MHz R1 = '0' and R2 = '1'		–	–10	–	dB
Adjacent Channel Rejection						dB
Low Side			–	63	–	
High Side			–	55	–	
Image Rejection						dB
First IF			–	55	–	
Second IF			–	57	–	
Intermodulation Rejection						dB
Low Side			–	43	–	
High Side			–	42	–	
Blocking Rejection						dB
@ 1.0 MHz			–	69	–	
@ 5.0 MHz			–	75	–	
Total Current Consumption		I_T				
Power Up	@ V_{CC} = 1.1 V EN = '1' and CL = '0'		–	3.18	–	mA
Power Down	@ V_{CC} = 1.1 V EN = '0' and CL = '0'		–	<30	–	µA

NOTES: 1. Output of the LNA is matched to 230 Ω by inserting a 180 Ω resistor in series with its output port.
2. Output of the Mixer is matched to 1.5050 kΩ by inserting a 1500 Ω resistor in series with its output port.
3. The circuit of this test board is the same as the schematic in Figure 2.

APPLICATION NOTES

This FLEX paging receiver board uses Motorola's NPN silicon low–noise high–frequency transistors MMBR941 to construct the functional RF blocks, including a LNA, an oscillator and a mixer. The M–ary FSK IF receiver MC2800 performs the second down–conversion and demodulates the received FSK signal into two digital output bits.

The LNA employs cascode architecture (Q1 and Q2) with its output being matched to 230 Ω, the input impedance of the 284 MHz SAW filter. The input matching network should be changed when an antenna precedes the LNA. Special care must be taken in characterizing the LNA and antenna to acheive a good interface match.

The local oscillator (Q4) uses a Colpitts structure. Its output is bandpass filtered to obtain the 4^{th} harmonic. The values of C12 and C13 can be altered to fine tune the LO frequency. L9 is added in this capacitor network to increase the oscillator gain.

A common emitter circuit (Q3) is used as the mixer with both LO and RF being ac–coupled to its base. Its output is dc–coupled to the 21.4 MHz crystal filter. To minimize the distortion of the downconverted frequency spectrum, the filter output must be matched to MIX_IN of the MC2800.

For the characteristics of the MC2800 as well as its control (EN & CL pins) and bit–rate filter (R1 & R2 pins) setup, please refer to the MC2800 data sheet. It is recommended that a single ceramic filter configuration be used. That is, a 455 kHz 6–pole filter (FILTER3 in Figure 2) is inserted between the MIX_OUT and IF1_IN, and a 1.0 µF multi–layer ceramic chip capacitor (C73 in Figure 2) is connected between the IF1_OUT and IF2_IN. Although it is noted in the data sheet of MC2800 that 3.0 to 4.0 dB performance degradation is observed in the single ceramic filter application, this performance degradation does not occur in the overall RF/IF system performance. This is because the high gain and the low NF of the RF front end have effectively reduced the noise contribution of the MC2800 to the overall system.

FDB Interface

This pager board uses an 11–pin surface mount socket to interface with the pager baseband board or the FLEX Development Board (FDB). This interface provides 3 digital output pins (BDOut, D1 & D2), one audio output pin, 4 control pins (EN, CL, R1 & R2) and 3 supply pins (V_{CC}, $V_{DD–E}$ & Gnd). The pin descriptions are summarized in the following table and the footprint of this socket is depicted in Figure 3. In order to provide a default state for these input pins, pull up resistors (R17 & R18) are used at both R1 & R2 input pins whereas a pull down resistor (R19) is connected at the CL input pin.

Note: For general information regarding FLEX products, please contact the local Motorola SPS Sales Office or the web at **http://www.mot–sps.com**

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	Audio Output	Symbol rate filter output.
2	R2	Control bits of the MC2800 bit–rate filter. Default value = '1'.
3	R1	
4	CL	Pre–charge and reset of the MC2800. Default value = '0'.
5	$V_{DD–E}$	Operating voltage of FLEX decoder used.
6	V_{CC}	Battery supplies of MC2800.
7	EN	MC2800 enable pin.
8	D2	2–Bit digital outputs of the MC2800.
9	D1	
10	BD Out	Low battery detector output.
11	Gnd	Ground pin.

Figure 3. The Footprint of the 11 Pin Interface Socket

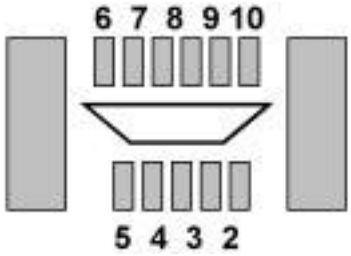

Figure 4. The PCB Layout of the Receiver Board (Top Layer)

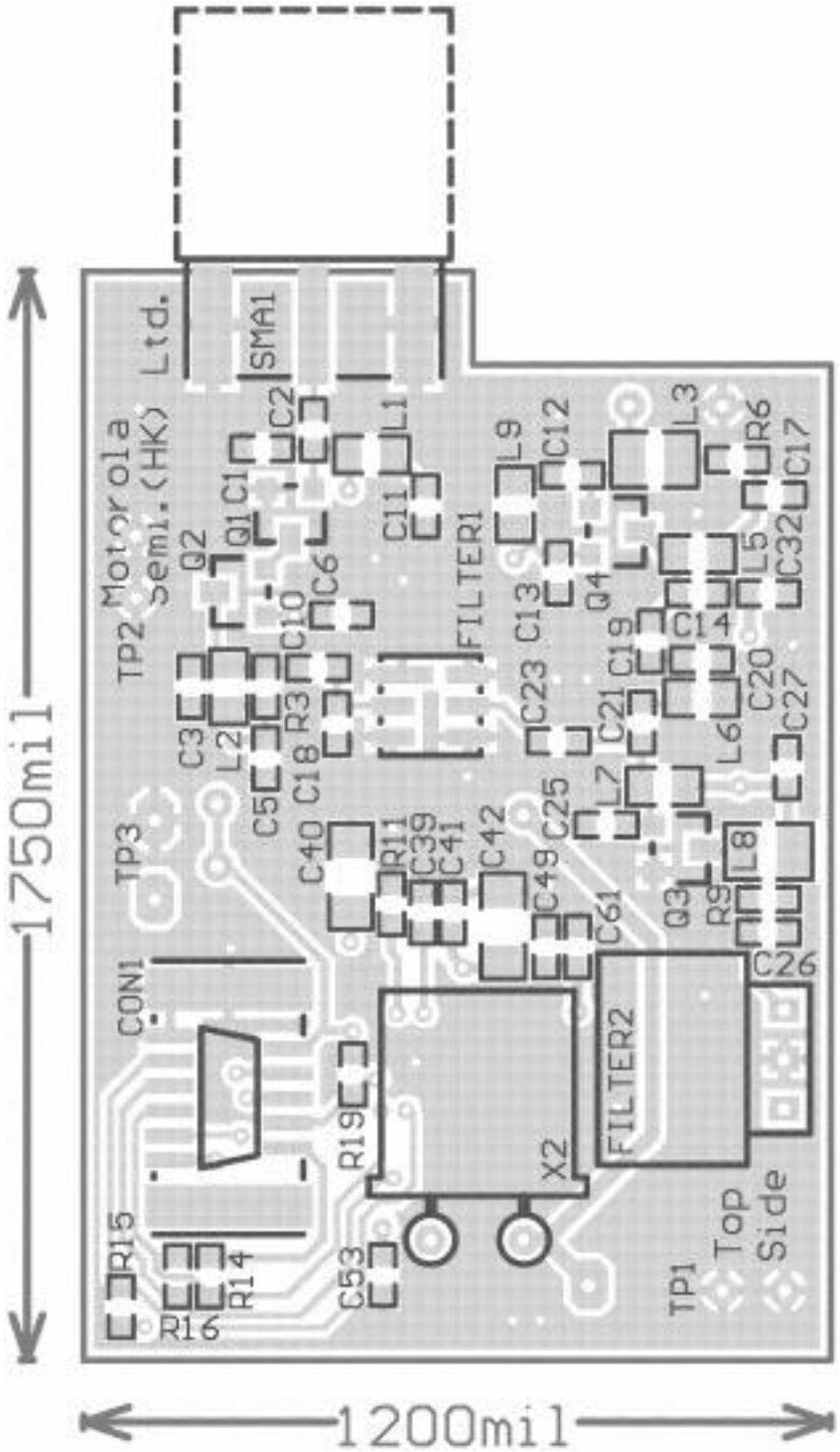

Figure 5. The PCB Layout of the Receiver Board (Bottom Layer)

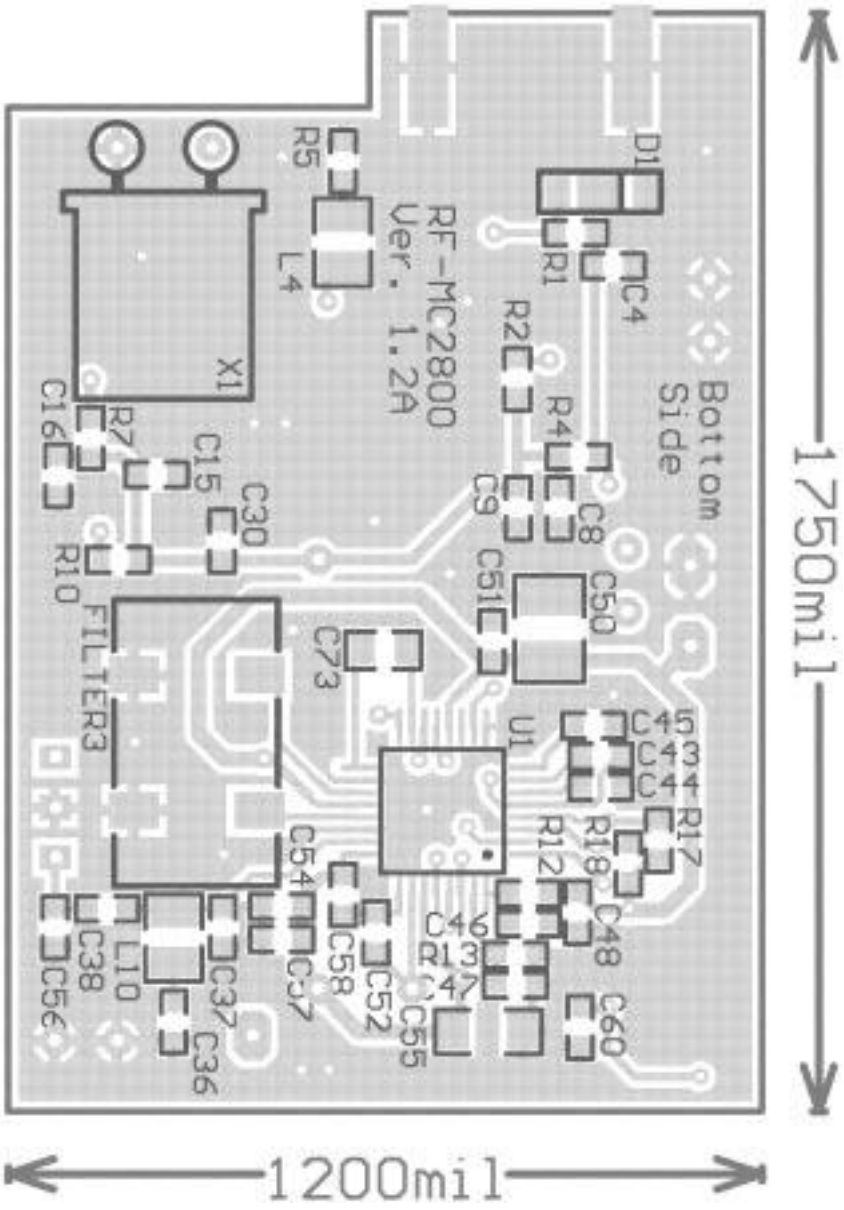

Table 1. Component List

Designator	Part No./Value	Designator	Part No./Value
C1 C10 C37	2.0 pF	L1	27 nH
C2 C14	5.0 pF	L2	33 nH
C3 C12	7.0 pF	L3	2.7 µH
C4 C17 C27 C39	1.0 nF	L4	3.3 µH
C5 C6 C11 C32	10 nF	L5 L7	39 nH
C8 C16 C54 C61	100 pF	L6	22 nH
C9 C15 C30 C36 C46 C47 C48 C49 C51 C53 C57 C60	100 nF	L8	4.7 µH
C13	10 pF	L9	18 nH
C18 C56	Not Used	L10	6.8 µH
C19	4.0 pF		
C20 C26	12 pF	R1	6.8 kΩ
C21	1.0 pF	R2 R10	820 Ω
C23	22 pF	R3	2.4 kΩ
C25	0.5 pF	R4	200 Ω
C38	3.0 pF	R5	750 Ω
C40 C42 C55	4.7 µF	R6	430 Ω
C41	0.1 µF	R7	110 Ω
C43	2.2 nF	R9	3.0 kΩ
C44	22 nF	R11	7.1 kΩ
C45	3.3 nF	R12 R13	10 MΩ
C50	10 µF	R14 R15 R16 R17 R18 R19	100 kΩ
C52	47 pF	D1	DIODE
C58	56 pF	U1	MC2800
C73	1.0 µF		
FILTER1	SAFC284E75N	X1	65.681250 MHz
FILTER2	Crystal Filter 21.4 MHz	X2	20.945000 MHz
FILTER3	CFWC455D	Q1 Q2 Q3 Q4	MMBR941LT1

Table 2. SAW Filter Specification

Part Number	SAFC284ME75N [Note]
Nominal Center Frequency, f_O	284.0 MHz
Insertion Loss	
f_O – 100 MHz to f_O – 37.5 MHz	48 dB min
f_O ± 4.0 MHz	4.5 dB max
f_O + 37.5 MHz to f_O + 100 MHz	40 dB min
Ripple within f_O ±4.0 MHz/dB	2.0 max
Nominal Input / Output impedance	230 Ω // – 0.2 pF

NOTE: SAW filter SAFC284ME75N is the product of muRata Manufacturing Co., Ltd. For further enquiry, please refer to the muRata's product catalog.

Table 3. Crystal Filter Specification

Nominal Center Frequency, f_O	21.400000 MHz ± 1.0 kHz
Number of Pole	2 poles
Pass Band Width	–3.0 dB / ±7.5 kHz min
Stop Band Width	–18 dB / ±25.0 kHz max
Pass Band Ripple	0.5 dB max
Insertion Loss	1.5 dB max
Nominal Input / Output impedance	1.5 kΩ // 2.0 pF

Table 4. Ceramic Filter Specification

Part Number	CFWC455D [Note]
Nominal Center Frequency, f_O	455 kHz
3.0 dB Bandwidth from f_O	±8.0 kHz
50 dB Bandwidth from f_O	±17.0 kHz
Stop Band Attenuation	
Within f_O ± 18 to 33 kHz	55 dB min
Within f_O ± 100 kHz	50 dB min
Spurious within 0.1 to 1.0 MHz	20 dB min
Ripple within f_O ± 7.5 kHz	2.0 dB max
Nominal Input/Output impedance	1.5 kΩ

NOTE: Ceramic filter CFWC455D is the product of muRata Manufacturing Co., Ltd. For further inquiry, please refer to muRata's product catalog.

Table 5. Quartz Crystal Specification

(a) 65.68125 MHz Quartz Crystal [Note]

Part Number	1U0656812D3035F0Z
Nominal Frequency, f_O	65.68125 MHz
Holder Type	UM–1
Resonance Mode	3rd Overtone
Operating Temperature	–30 to 80°C
Frequency Tolerance @ 25°C	±30 ppm
Load Capacitance	30 pF
Equivalent Series Resistance, ESR	60 Ω max
Shunt Capacitance C_0	7.0 pF
Drive Level	50 μW
Aging	±5.0 ppm/year

(b) 20.94500 MHz Quartz Crystal [Note]

Part Number	1U0209450D30F5D0Z
Nominal Frequency, f_O	20.945 MHz
Holder Type	UM–1
Resonance Mode	Fundamental
Operating Temperature	–30 to 80°C
Frequency Tolerance @ 25°C	±20 ppm
Load Capacitance	30 pF
Equivalent Series Resistance, ESR	30 Ω max
Shunt Capacitance C_0	7.0 pF
Drive Level	0.5 mW
Aging	±5.0 ppm/year

NOTE: The quartz crystals are the products of Hong Kong X'TALS Limited. For further inquiry, please refer to the product catalog of Hong Kong X'TALS Limited or **hkxtals@HongKongCrystal.com**.

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