MOTOROLA

MC33218A

Advance Information

Voice Switched Speakerphone with Microprocessor Interface

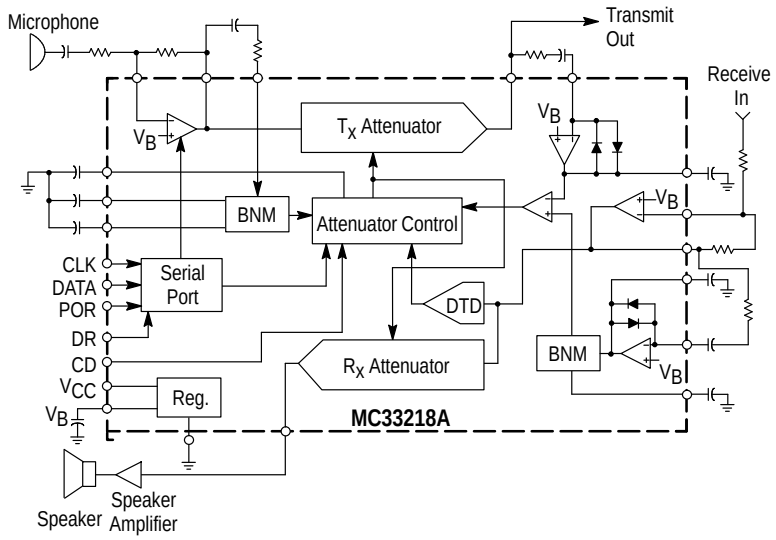
The Motorola MC33218A Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands–free speakerphone system. Included are a microphone amplifier with mute, transmit and receive attenuators, a background monitoring system for both the transmit and receive paths, and level detectors for each path. An AGC system reduces the receive gain on long lines where loop current and power are in short supply. A dial tone detector prevents fading of dial tone. A Chip Disable pin permits conserving power when the circuit is not in use.

Additionally, the MC33218A has a serial data port which permits microprocessor control of the receive volume level, microphone mute, attenuator range, and selection of transmit, receive, idle or normal modes. The data port can be operated at up to 1.0 MHz.

The MC33218A can be operated from a power supply, or from the telephone line, requiring typically 4.6 mA. It can be used in conjunction with a variety of speech networks. Applications include not only speakerphones, but intercoms and other voice switched devices.

- Supply Voltage Range: 2.7 to 6.5 V
- Attenuator Range: 53 or 27 dB (Selectable)
- 2 Point Sensing with Background Noise Monitor in Each Path
- Microprocessor Port for Control of:
  - Volume Control (40 dB Range over 16 Levels)
  - Mute Microphone Amplifier
  - Force to Receive, Transmit, or Idle Modes
  - Attenuator Range Selection (27 or 53 dB)
- Chip Disable Pin Powers Down the Entire IC
- 24 Pin Narrow Body (300 mil) DIP and 24 Pin SOIC

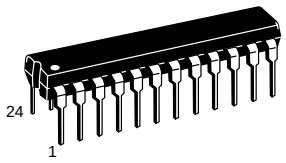
Simplified Block Diagram



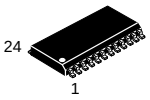
This device contains 610 active transistors.

VOICE SWITCHED SPEAKERPHONE WITH µPROCESSOR INTERFACE

SEMICONDUCTOR TECHNICAL DATA

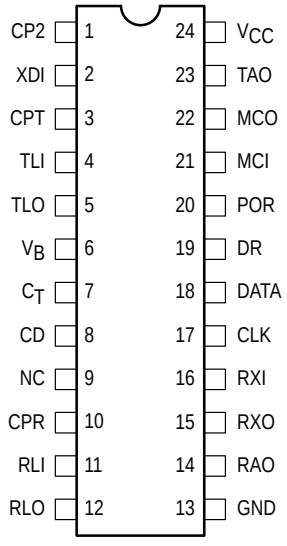


P SUFFIX
PLASTIC PACKAGE
CASE 724



DW SUFFIX
PLASTIC PACKAGE
CASE 751E

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33218ADW	T_A = – 40° to +85°C	SO–24L
MC33218AP		Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	–0.5	7.0	Vdc
Any Input	V_{in}	–0.4	V_{CC} + 0.4	Vdc
Maximum Junction Temperature	T_J	–	+150	°C
Storage Temperature Range	T_{stg}	–65	+150	°C

NOTE: Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage (Non–AGC Range) (AGC Range)	V_{CC}	3.5 2.7	– –	6.5 3.5	Vdc
Maximum Attenuator Input Signal	$V_{in(max)}$	–	–	300	mVrms
Logic Input Voltage (Pins 8, 17–19) Low High	V_{INL}	 0 2.0	 – –	 0.8 V_{CC}	Vdc
Clock and Data Rate (Serial Port)	F_{DATA}	0	–	1.0	MHz
V_B Output Current	I_{VB}	–	See Figure 14	–	mA
Operating Ambient Temperature Range	T_A	–40	–	+85	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted, see Figure 3.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Supply Current (Enabled, CD ≤ 0.8, V_B Open, See Figure 13) Idle Mode T_X Mode R_X Mode	I_{CCE}	 3.0 – –	 4.6 4.6 5.3	 6.0 – –	mA
Supply Current (Disabled, CD = 2.0 V, V_B Open) V_{CC} = 3.0 V V_{CC} = 5.0 V V_{CC} = 6.5 V	I_{CCD}	 – 50 –	 67 110 150	 – 170 –	µA
V_B Output Voltage (I_{VB} = 0, CD = 0) V_{CC} = 2.7 V V_{CC} = 5.0 V V_{CC} = 6.5 V	V_B	 – 2.1 –	 0.9 2.2 3.0	 – 2.3 –	Vdc
V_B Output Resistance (I_{VB} ≤ –1.0 mA)	R_{OVB}	–	600	–	Ω
PSRR @ V_B versus V_{CC}, f = 1.0 KHz, C_{VB} = 100 µF	PSRR	–	57	–	dB
ATTENUATOR CONTROL					
C_T Voltage (with Respect to V_B) (Full Range, B5 = 0) R_X Mode (Maximum Volume) Idle Mode T_X Mode (Half Range, B5 = 1) R_X Mode (Maximum Volume Idle Mode T_X Mode	$V_{CT} - V_B$	 – – – – – –	 +150 0 –100 +85 0 –35	 – – – – – –	mV
C_T Source Current (Switching to R_X Mode)	I_{CTR}	–55	–42	–33	µA
C_T Sink Current (Switching to T_X Mode)	I_{CTT}	33	42	55	µA
C_T Idle Current	I_{CTI}	–3.0	0	3.0	µA
Dial Tone Detector Threshold (with Respect to V_B at RXO)	V_{DT}	–40	–20	–8.0	mV

ELECTRICAL CHARACTERISTICS (continued) (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted, see Figure 3.)

Characteristic	Symbol	Min	Typ	Max	Unit
ATTENUATORS					
Receive Attenuator Gain (f = 1.0 kHz, Maximum Volume)					dB
Full Attenuation Range (B5 = 0)					
R_X Mode	G_{RXF}	3.0	6.7	9.0	
T_X Mode	G_{RXTF}	–49	–47	–43	
Idle Mode	G_{RXIF}	–28	–25	–22	
Range (R_X to T_X Mode)	ΔG_{RXF}	50	53	56	
Half Attenuation Range (B5 = 1)					
R_X Mode	G_{RXH}	–10	–7.0	–4.0	
T_X Mode	G_{RXTH}	–37	–34	–31	
Idle Mode	G_{RXIH}	–28	–25	–22	
Range (R_X to T_X Mode)	ΔG_{RXH}	23	27	29	
Volume Control Range (R_X Mode Only, B3–B0 Changed from 0000 to 1111, See Figures 6, 7)	V_{CR}				dB
Full Range		34	40	46	
Half Range		–	25	–	
AGC Attenuation Range (V_{CC} = 3.5 to 2.7 V, Receive Mode Only, B3–B0 = 0000, See Figure 8)	G_{AGC}				dB
Full Range		12	21	28	
Half Range		–	19	–	
Transmit Attenuator Gain (f = 1.0 kHz, Maximum Volume)					dB
Full Attenuation Range (B5 = 0)					
T_X Mode	G_{TXF}	3.0	6.7	9.0	
R_X Mode	G_{TXRF}	–49	–47	–43	
Idle Mode	G_{TXIF}	–19	–16	–13	
Range (T_X to R_X Mode)	ΔG_{TXF}	50	53	56	
Half Attenuation Range (B5 = 1)					
T_X Mode	G_{TXH}	–9.0	–6.5	–3.0	
R_X Mode	G_{TXRH}	–36	–34	–30	
Idle Mode	G_{TXIH}	–19	–16	–13	
Range (T_X to R_X Mode)	ΔG_{TXH}	23	27	29	
RAO, TAO Output Current Capability	I_{OATT}	–	2.0	–	mA
RAO Offset Voltage with Respect to V_B	V_{RAO}				mVdc
R_X Mode		–	–50	–	
Idle Mode		–	0	–	
T_X Mode		–	–2.0	–	
TAO Offset Voltage with Respect to V_B	V_{TAO}				mVdc
R_X Mode		–	–2.0	–	
Idle Mode		–	–5.0	–	
T_X Mode		–	–50	–	
MICROPHONE AMPLIFIER (Pins 21, 22)					
Output Offset with Respect to V_B (RF = 300 kΩ)	MCO_{VOS}	–	–10	–	mVdc
Input Bias Current (Pin 21)	I_{MBIAS}	–	–30	–	nA
Open Loop Gain (f < 100 Hz)	A_{VOLM}	–	80	–	dB
Gain Bandwidth	GBW_M	–	1.5	–	MHz
Maximum Output Voltage Swing (Note 1)	V_{OMAX}	–	350	–	mVrms
Maximum Output Current Capability	I_{OMCO}	–	2.0	–	mA
MUTING (Δ Gain)					
Microphone Amplifier Only (Measured at Pin 22)	AMT				dB
RF = 300 kΩ		–	73	–	
RF = 100 kΩ		–	64	–	
Microphone Amplifier + Transmit Attenuator in Receive Mode (Measured at Pin 23) RF = 300 kΩ	TMT	95	113	–	dB

NOTE: 1. Output swing is limited by the capability of the transmit attenuator input. See Figure 16.

ELECTRICAL CHARACTERISTICS (continued) (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted, see Figure 3.)

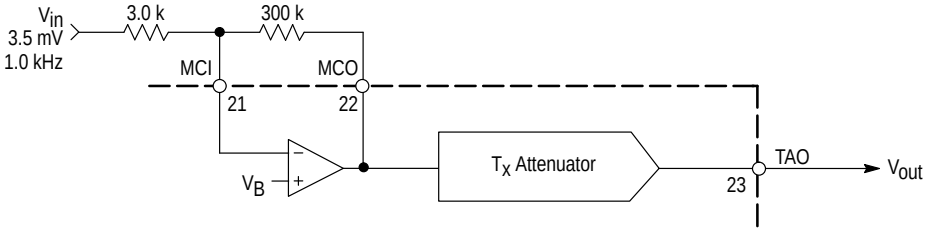
Characteristic	Symbol	Min	Typ	Max	Unit
MUTING (Δ Gain)					
Timing from Data Ready Lo–to–Hi (See Figure 27)					µs
To Mute	t_{MM}	–	2.0	–	
To Enable	t_{ENM}	–	1.0	–	
RECEIVE AMPLIFIER (Pins 15, 16)					
Output Offset with Respect to V_B (RF = 10 kΩ)	RXO_{VOS}	–	–1.3	–	mVdc
Input Bias Current (Pin 16)	I_{RBIAS}	–	–30	–	nA
Open Loop Gain (f < 100 Hz)	A_{VOLR}	–	80	–	dB
Gain Bandwidth	G_{BWR}	–	1.5	–	MHz
Maximum Output Voltage Swing (Note 2)	V_{OMAX}	–	350	–	mVrms
Maximum Output Current Capability	I_{ORXO}	–	2.0	–	mA
LEVEL DETECTORS AND BACKGROUND NOISE MONITORS					
T_X–R_X Switching Threshold (Pins 4, 11)	I_{TH}	0.8	1.0	1.2	µA/µA
CPR, CPT Output Resistance (for Pulldown)	R_{CP}	–	5.0	–	Ω
CPR, CPT Leakage Current	I_{CPLK}	–	–0.2	–	µA
CPR, CPT Nominal DC Voltage (No Signal)	V_{CP}	–	1.9	–	Vdc
TLO, RLO, CP2 Source Current (@ V_B – 1.0 V)	I_{LDOH}	–	–2.0	–	mA
TLO, RLO, CP2 Output Resistance	R_{LD}	–	500	–	Ω
TLO, RLO, CP2 Sink Current (@ V_B + 1.0 V)	I_{LDOL}	–	2.0	–	µA
CD INPUT (Pin 8)					
Switching Threshold	V_{THCD}	–	1.5	–	Vdc
Input Resistance (V_{in} = 0.8 V)	R_{CD}	170	235	300	kΩ
Input Current (V_{in} = 5.0 V)	I_{CD}	–	40	–	µA
Timing					µs
To Disable	t_{CD}	–	3.0	–	
To Enable	t_{ENC}	–	See Figure 26	–	
POR INPUT (Pin 20)					
Switching Threshold (2.7 V ≤ V_{CC} ≤ 6.5 V)	V_{THPOR}	–	1.2	–	Vdc
Nominal DC Voltage (2.7 V ≤ V_{CC} ≤ 6.5 V)	V_{POR}	–	1.5	–	Vdc
Effective Resistance (0 V < V_{in} < 0.5 V)	R_{POR}	70	115	160	kΩ
Input Current	I_{POR}				µA
V_{in} = 0 V		–	–40	–	
V_{in} = 5.0 V		–	630	–	
Timing to Reset (Pin 20 Taken to < 1.2 V)	t_{POR}	–	30	–	µs
Minimum Power On Reset Time (See Figure 20)	T_{MPOR}				ms
C = 0.1 µF V_{CC} = 6.5 V		–	2.7	–	
V_{CC} = 5.0 V		–	3.7	–	
V_{CC} = 2.7 V		–	10.6	–	

NOTE: 2. Output swing is limited by the capability of the receive attenuator input. See Figure 16.

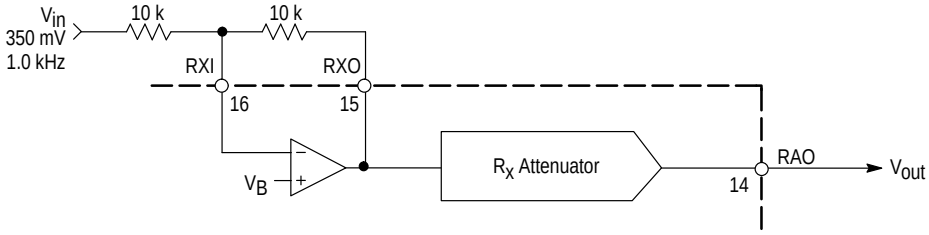
ELECTRICAL CHARACTERISTICS (continued) (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted, see Figure 3.)

Characteristic	Symbol	Min	Typ	Max	Unit
SERIAL PORT (Pins 17–19)					
Switching Threshold	V_{THSP}	–	1.3	–	Vdc
Clock Input Current (Pin 17)	I_{INCK}				µA
DR ≤ 0.8 V V_{in} = 0.9 V		5.6	7.5	12.8	
V_{in} = 5.0 V		–	75	–	
DR ≥ 2.0 V V_{in} = 0.6 V		5.2	7.9	13.3	
V_{in} = 5.0 V		–	84	–	
Data Input Current (Pin 18)	I_{INDA}				µA
V_{in} = 0.9 V		5.6	7.5	12.8	
V_{in} = 5.0 V		–	75	–	
Data Ready Input Current (Pin 19)	I_{INDR}				µA
V_{in} = 0.9 V		13.8	20	36	
V_{in} = 5.0 V		–	200	–	
Timing (Minimum Requirements) (See Figure 2)					ns
Data Ready Falling Edge to Clock	t_1	–	200	–	
8th Clock Rising Edge to DR Rising Edge	t_2	–	100	–	
Data Setup Time	t_3	–	100	–	
Data Hold Time	t_4	–	100	–	
Clock High Time	t_5	–	200	–	
SYSTEM DISTORTION (See Figure 1)					
Microphone Amplifier + T_X Attenuator Distortion	THD_T	–	0.2	3.0	%
Receive Amplifier + R_X Attenuator Distortion	THD_R	–	0.2	3.0	%

Figure 1. System Distortion Test



NOTE: T_X Attenuator forced to transmit mode.



NOTE: R_X Attenuator forced to receive mode.

TYPICAL TEMPERATURE PERFORMANCE

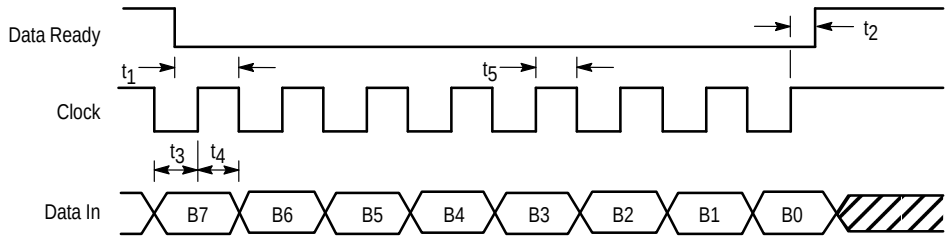
Characteristics	–40°C	0°C	+25°C	+85°C	Unit
Power Supply Current Enabled, V_B Open Disabled, V_B Open	 5.4 129	 4.9 118	 4.6 110	 4.2 125	 mA µA
V_B Output Voltage (I_{VB} = 0)	2.0	2.15	2.2	2.3	Vdc
C_T Source Current (Switching to R_X Mode)	–37	–41	–42	–42	µA
C_T Sink Current (Switching to T_X Mode)	36	41	42	43	µA
Attenuator “On” Gain (Full Range)	6.7	6.7	6.7	6.4	dB
Attenuator Range (Full Range)	53	53	53	53	dB
Volume Control Range (R_X Mode Only, B3–B0 Changed from 0000 to 1111)	36	39	40	42	dB
AGC Attenuation Range	38	20	21	22	dB

NOTE: Temperature data is typical performance only, based on sample characterization, and does not provide guaranteed limits over temperature.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	CP2	A capacitor at this pin stores voltage representing the transmit background noise and speech levels for the background noise monitor.
2	XDI	Input to the transmit background noise monitor.
3	CPT	An RC sets the time constant for the transmit background noise monitor.
4	TLI	Input to the transmit level detector.
5	TLO	Output of the transmit level detector.
6	V_B	A mid–supply reference voltage, and analog ground for the amplifiers. This must be well bypassed for proper power supply rejection.
7	C_T	An RC sets the switching time between transmit, receive and idle modes.
8	CD	Chip Disable (Logic Input). When low, the IC is active. When high, the entire IC is powered down and non–functional, except for V_B. Input impedance is nominally 235 kΩ.
9	NC	No internal connection.
10	CPR	An RC sets the time constant for the receive background noise monitor.
11	RLI	Input to the receive level detector.
12	RLO	Output of the receive level detector.
13	GND	Ground pin for the entire IC.
14	RAO	Output of the receive attenuator.
15	RXO	Output of the receive path input amplifier, and input of the receive attenuator and the dial tone detector.
16	RXI	Inverting input of the receive amplifier. Bias current flows out of the pin.
17	CLK	Serial Port Clock. 1.0 MHz maximum. Data is entered on clock’s rising edge.
18	DATA	Serial Port Data Input. Data consists of an 8 bit word, B7 first, B0 last.
19	DR	Serial Port Data Ready. Taking this line high latches new data into the registers.
20	POR	Power On Reset for the serial port. Upon power up, or when CD is active, all internal registers are set to logic 0. This logic input may be taken low to reset the registers.
21	MCI	Inverting input of the microphone amplifier. Bias current flows out of the pin.
22	MCO	Output of the microphone amplifier, and input of the transmit attenuator.
23	TAO	Output of the transmit attenuator.
24	V_{CC}	Power Supply Pin. Operating Range is 2.7 V to 6.5 Vdc. Bypassing is requried.

Figure 2. Serial Port Timing Diagram



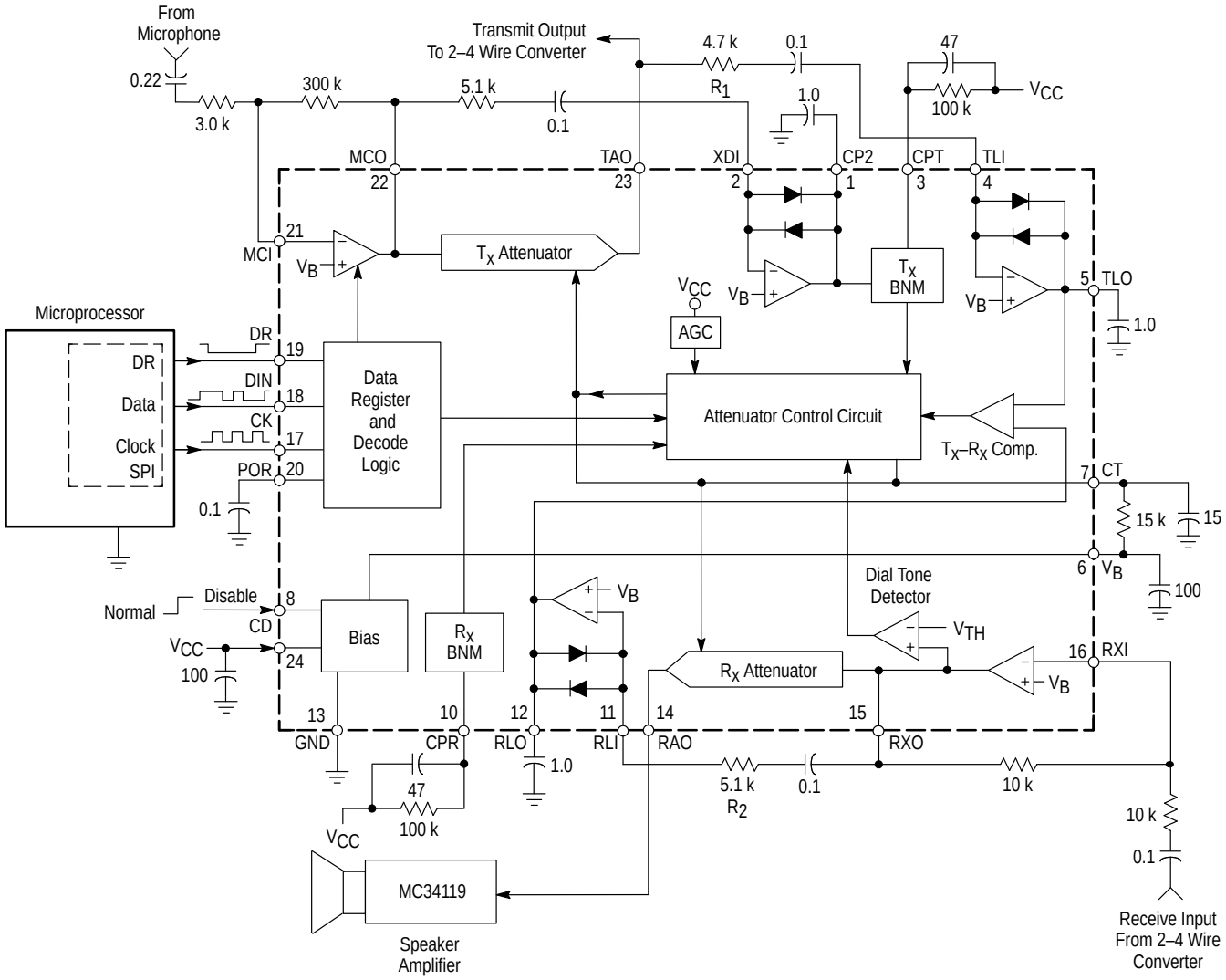
NOTES: 1. Maximum clock and data rate is 1.0 MHz. There is no required minimum rate.
2. B7 is to be entered first, B0 last.
3. Data is entered on the clock rising edge.
4. Clock can continue to toggle after B0 is entered if Data Ready goes high before the clock's next rising edge. This is not recommended due to possible noise problems.
5. Upon power up, all bits are internally set to logic 0, by the POR pin.
6. Data Ready must go low before the first falling clock edge after the clock rising edge associated with B7. See text for additional information.

SERIAL PORT CONTROL BITS

Bits	Code	Function
B7, B6	00 01 10 11	Normal voice switched operation Force to receive mode Force to idle mode Force to transmit mode
B5	0 1	Attenuator range is 53 dB Attenuator range is 27 dB
B4	0 1	Microphone amplifier is active Microphone amplifier is muted
B3–B0 (Note 1)	0000 1111	Maximum receive volume Minimum receive volume

NOTE: 1. Bit B0 is the LSB for the volume control.

Figure 3. MC33218A Block Diagram and Test Circuit



NOTES: 1. All capacitors are in µF unless otherwise noted.
2. Values shown are suggested initial values only. See Applications Information for circuit adjustments.

Figure 4. Attenuator Gain versus V_{CT} (Pin 7)
(Full Attenuator Range)

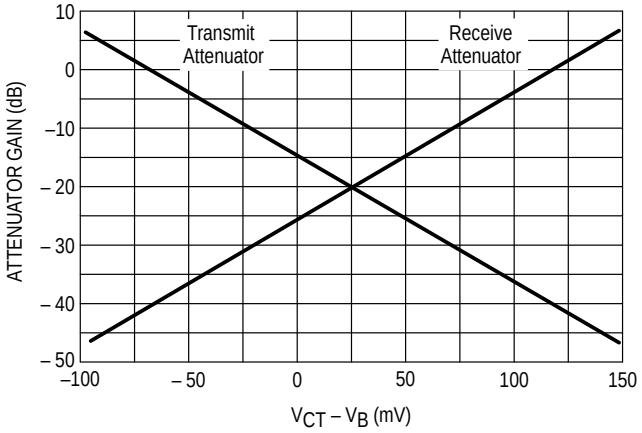


Figure 5. Attenuator Gain versus V_{CT}
(Half Attenuation Range)

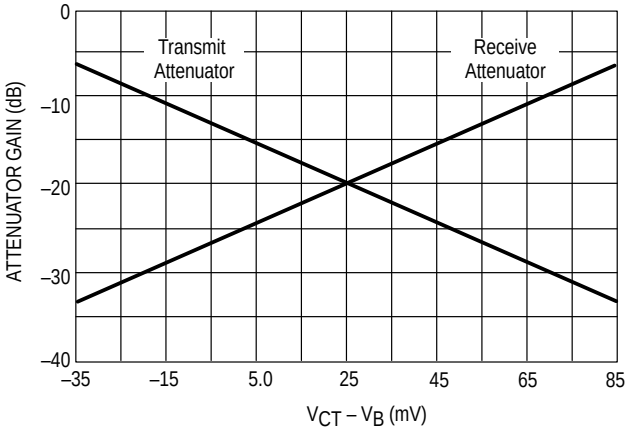


Figure 6. Receive Gain versus Volume Control Levels (Full Attenuation Range)

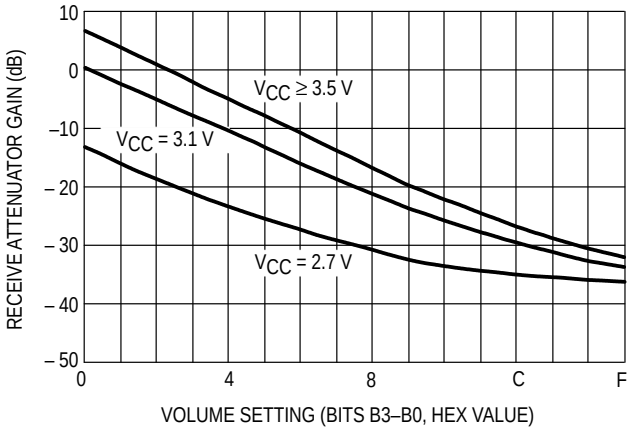


Figure 7. Receive Gain versus Volume Control Levels (Half Attenuation Range)

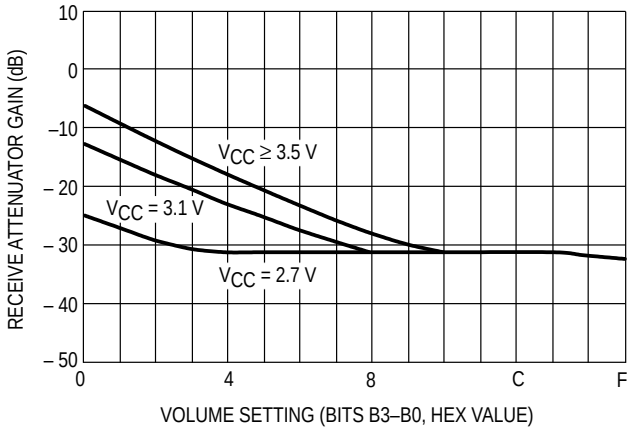


Figure 8. Receive Gain versus V_{CC}

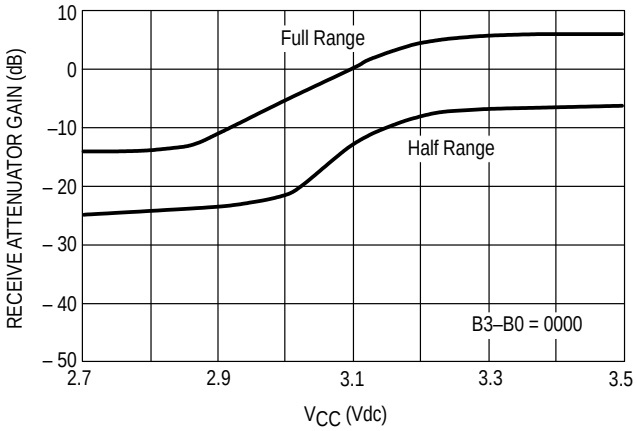


Figure 9. Level Detector AC Transfer Characteristics

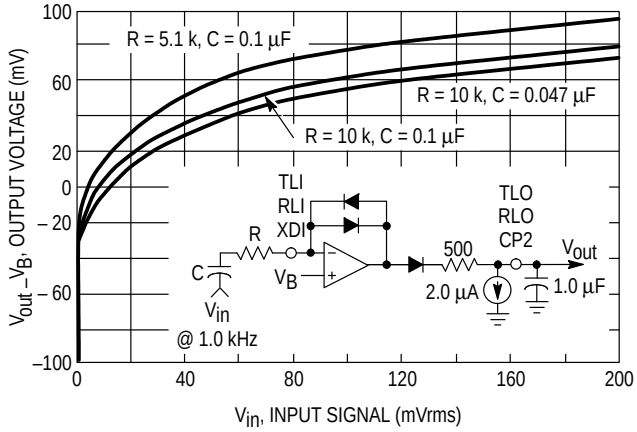


Figure 10. Level Detector AC Transfer Characteristics versus Frequency

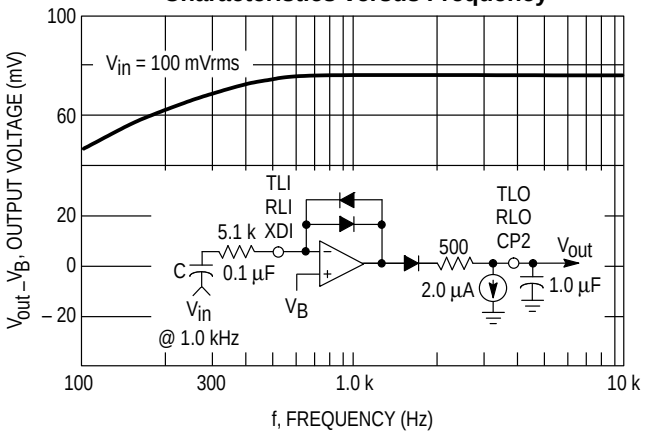


Figure 11. Level Detector DC Transfer Characteristics

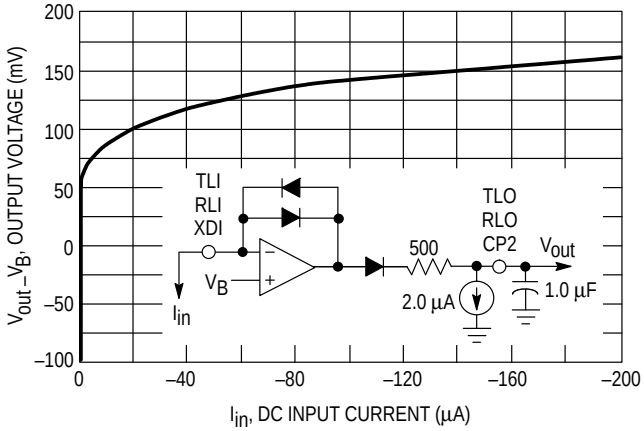


Figure 12. CD Input Characteristics (Pin 8)

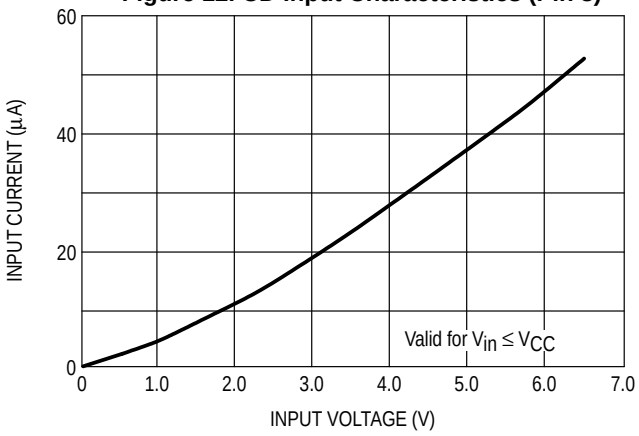


Figure 13. Power Supply Current

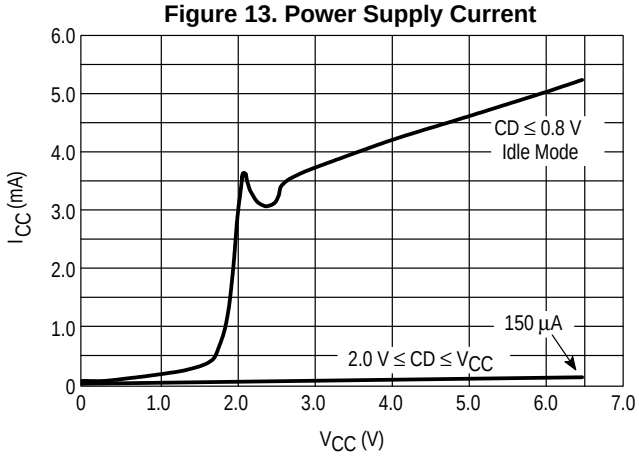


Figure 14. V_B Output Characteristics

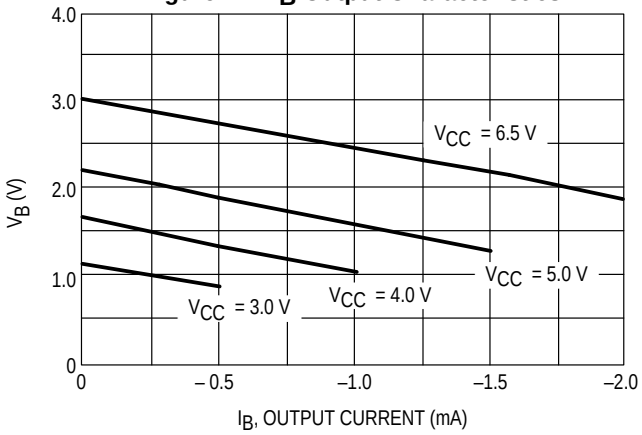


Figure 15. V_B Power Supply Rejection versus Frequency and V_B Capacitor

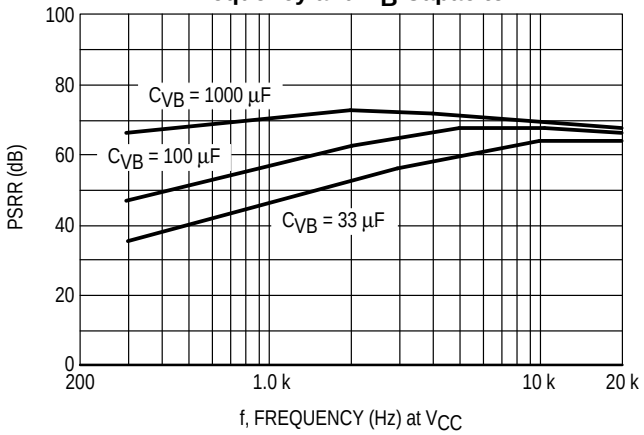


Figure 16. Receive Amp and Microphone Amp Output Swing

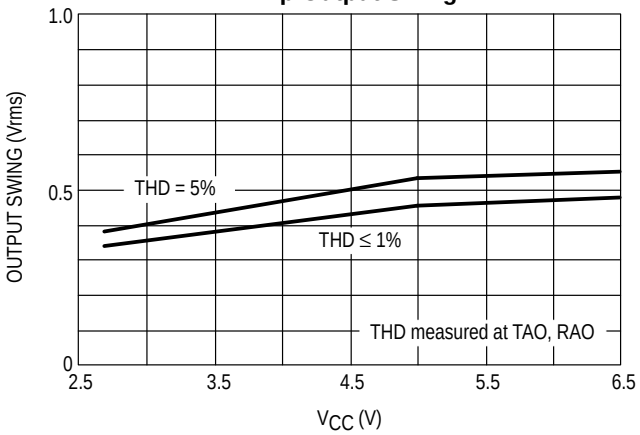


Figure 17. Microphone Amplifier Muting versus Feedback Resistor

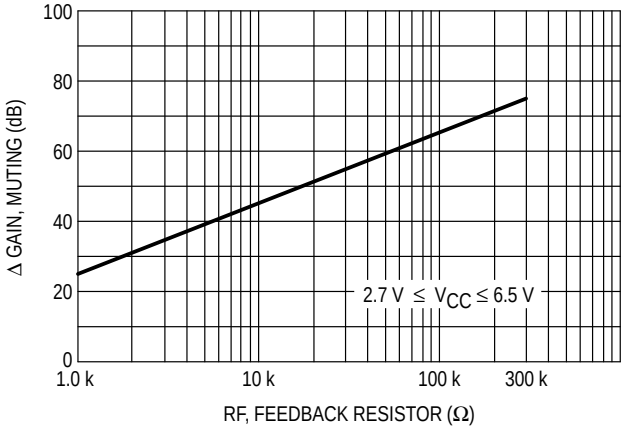


Figure 18. Serial Port Input Characteristics (Pins 17, 18, 19)

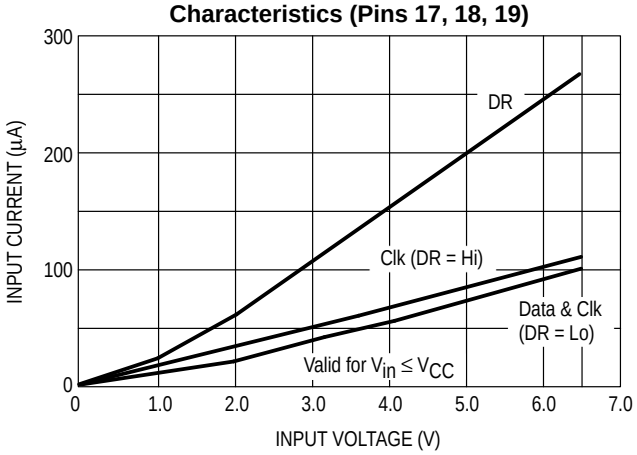


Figure 19. POR Input Characteristics (Pin 20)

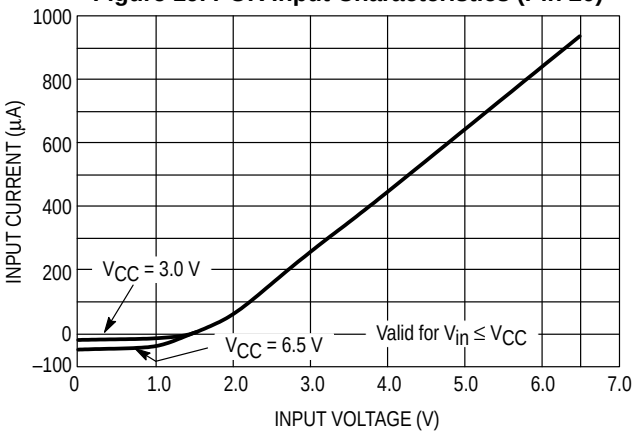


Figure 20. Minimum Reset Time versus V_{CC} and Pin 20 Capacitor

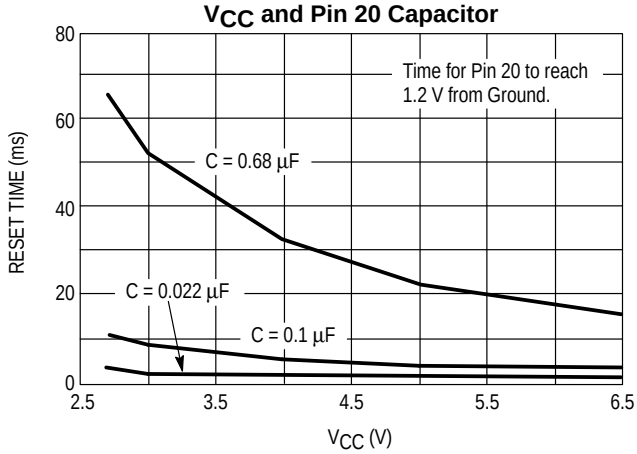


Figure 21. Idle ⟷ Transmit Timing

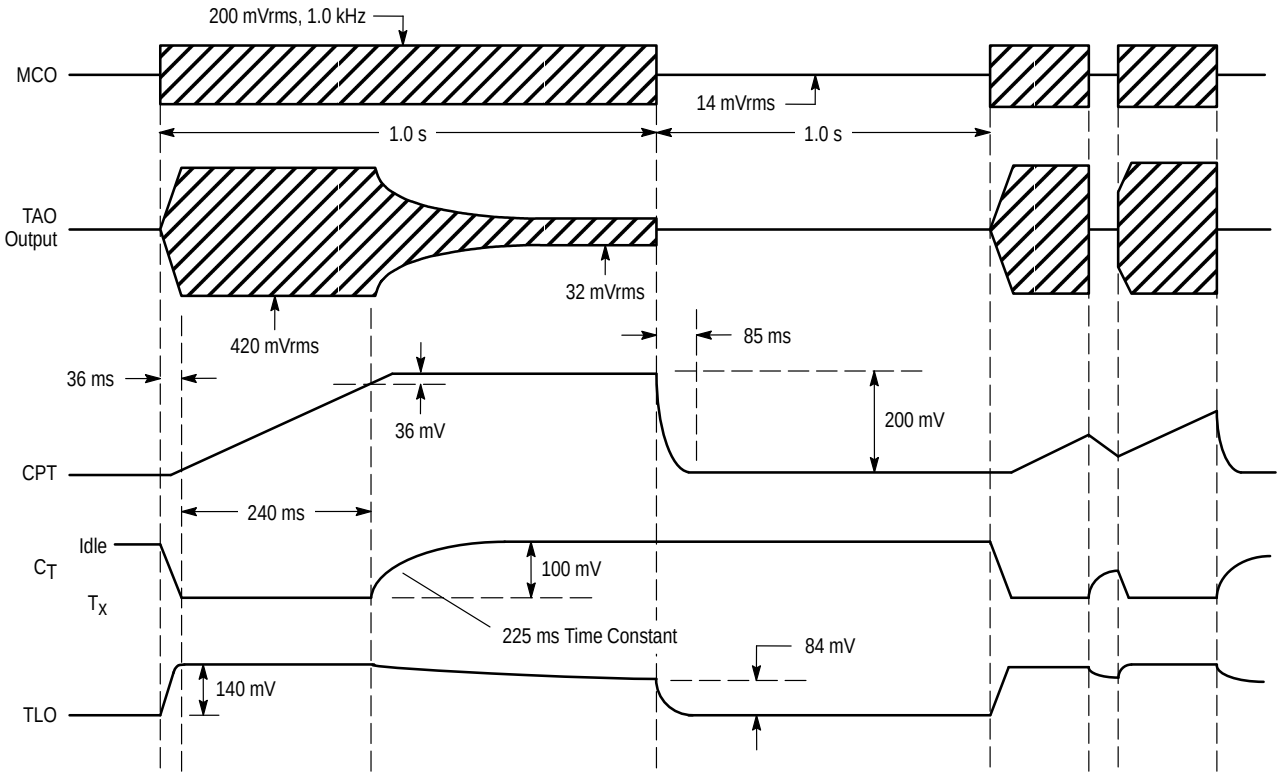
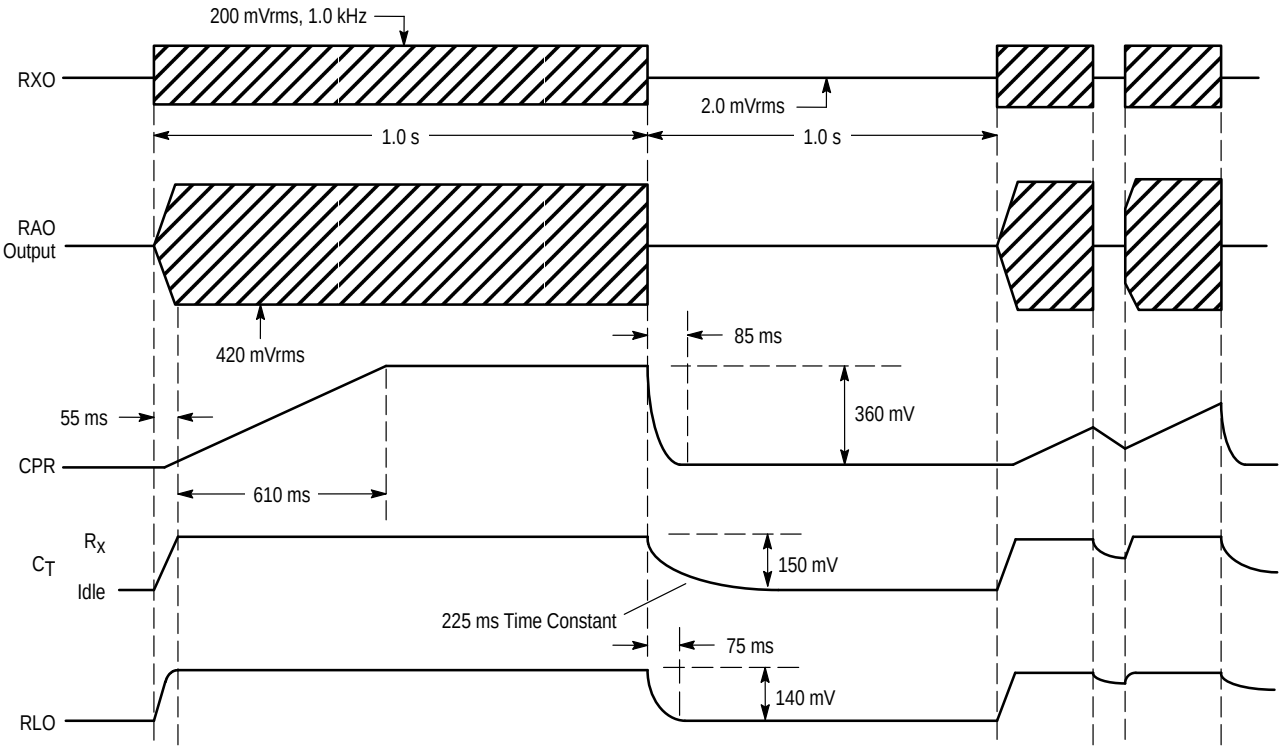
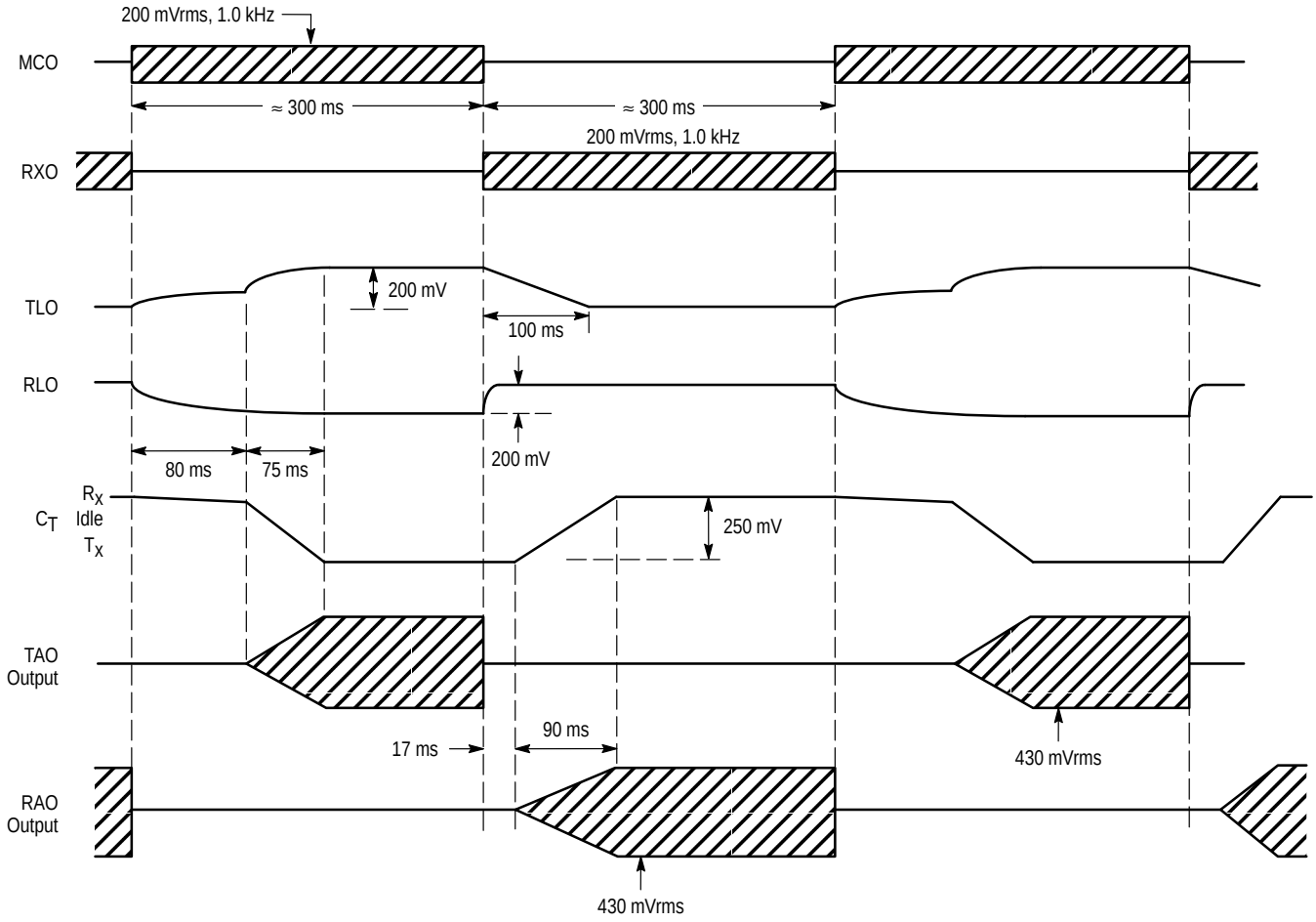


Figure 22. Idle ⟷ Receive Timing



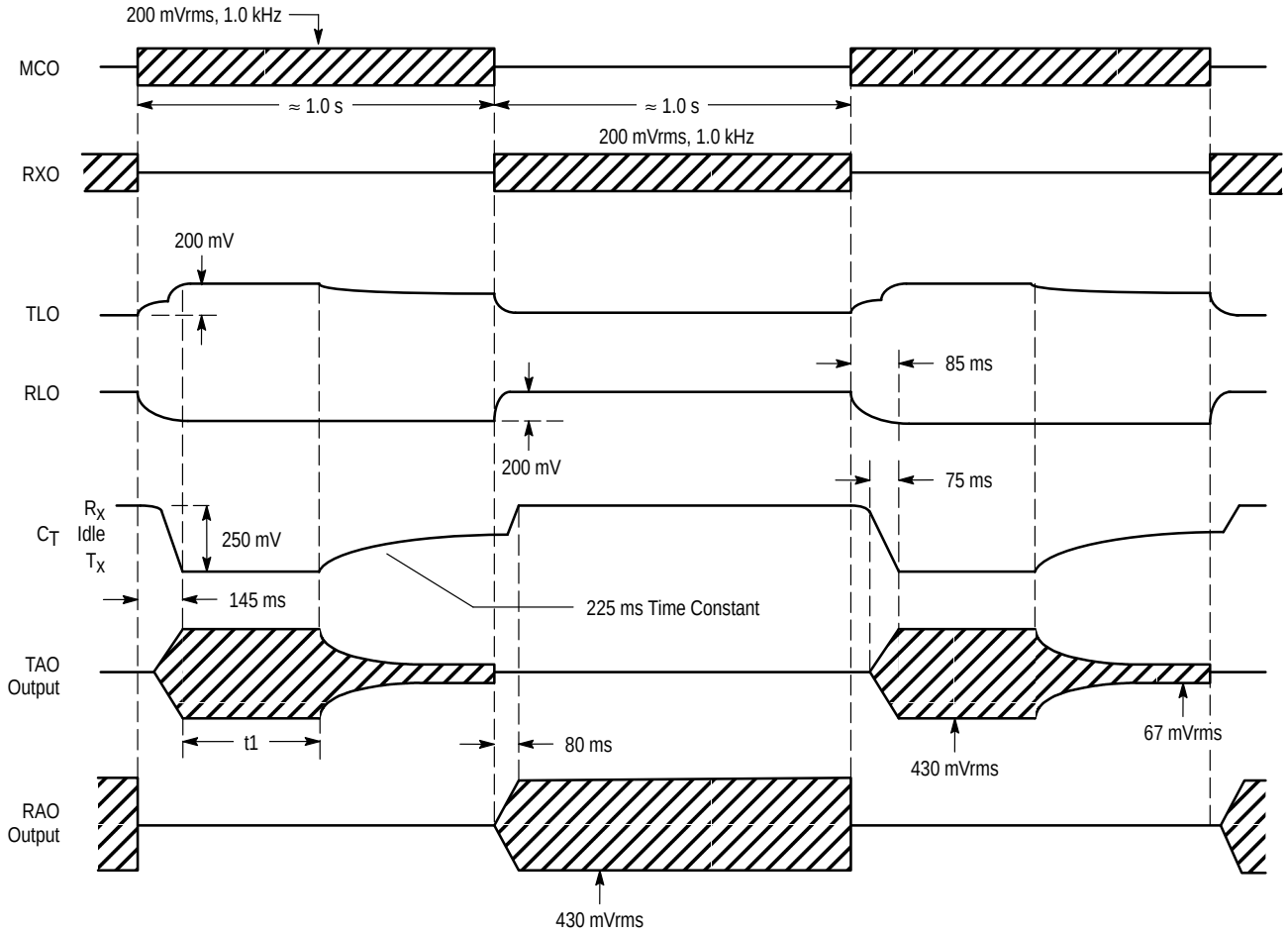
NOTE: Refer to Figure 3 for component values. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application. Bits B7, B6 = 00.

Figure 23. Transmit ⟷ Receive Timing (Short Cycle Timing)



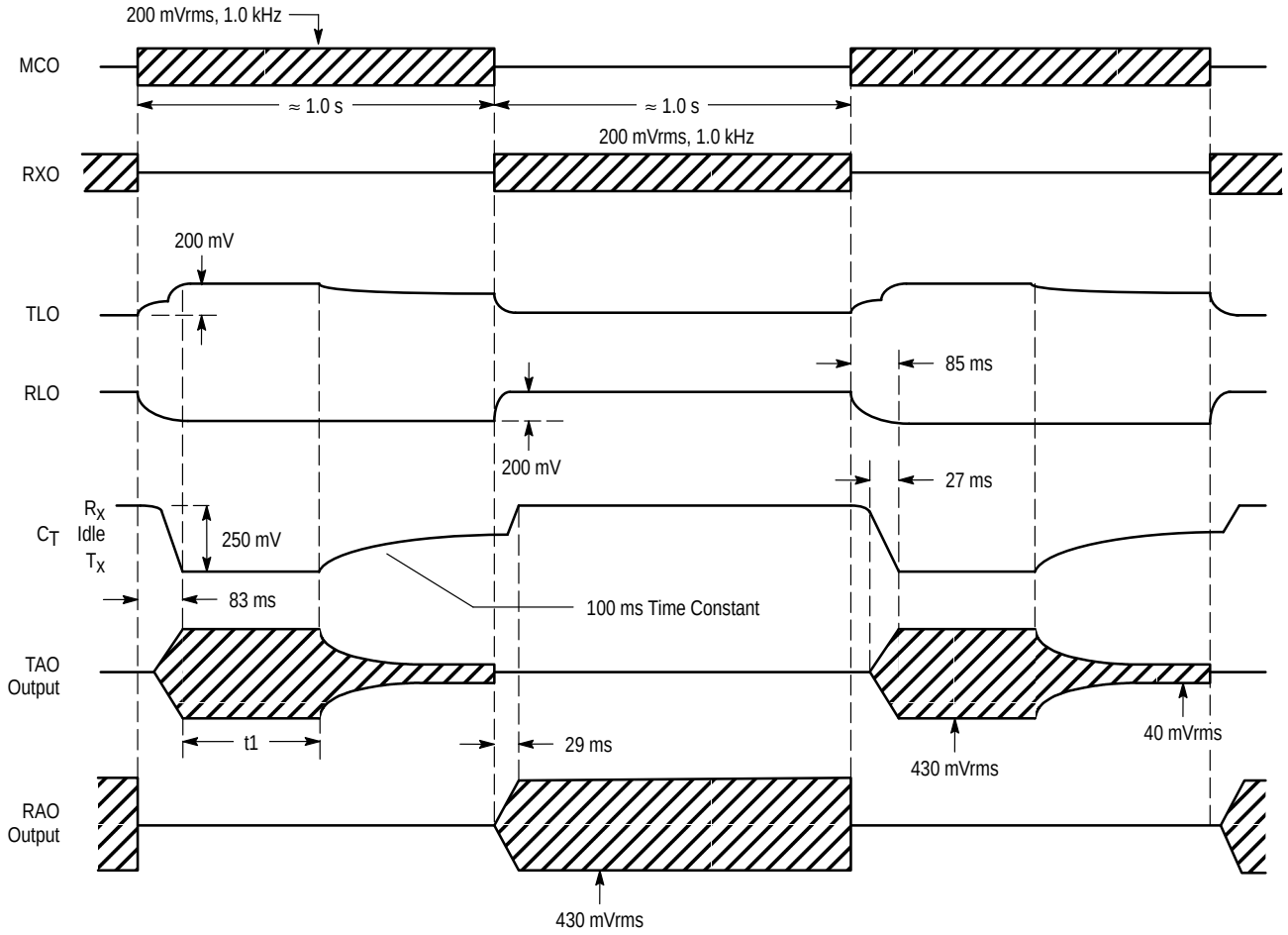
NOTE: External component values are those shown in Figure 3. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application. Bits B7, B6 = 00.

Figure 24. Transmit ⟷ Receive Timing (Long Cycle Timing)



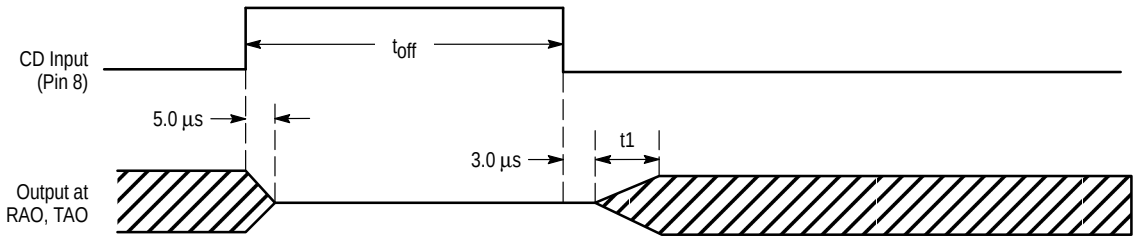
NOTE: External component values are those shown in Figure 3. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application. Time t1 depends on the ratio of the "on"/"off" amplitude of the signal at MCO. Bits B7, B6 = 00.

Figure 25. Transmit ⟷ Receive Timing (Long Cycle Timing)



NOTE: External component values are those shown in Figure 3, except the capacitor at C_T is 6.8 µF. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application. Time t1 depends on the ratio of the "on"/"off" amplitude of the signal at MCO. Bits B7, B6 = 00.

Figure 26. Chip Disable Timing



NOTE: Enable time t1 depends on the length of t_{off} according to the following chart:

t_{off}	t1
10 ms	25 ms
20 ms	45 ms
≥ 50 ms	60 ms

Figure 27. Mute Timing

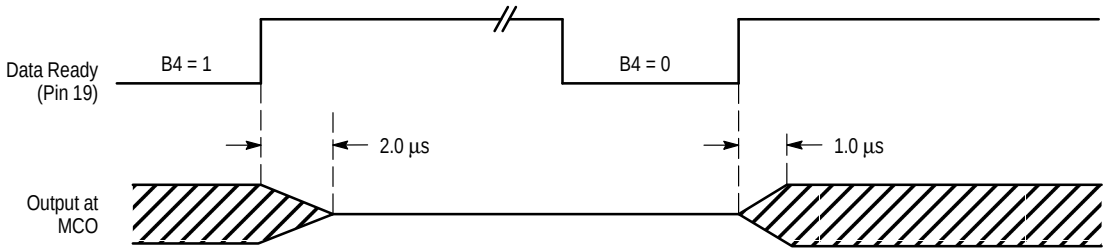
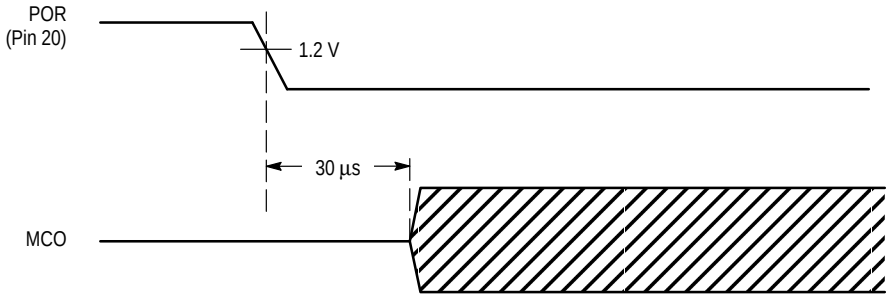


Figure 28. POR Timing



NOTE: Above time established by first muting the microphone amplifier (B4 = 1). Then the POR pin is taken low. The 30 µs is representative if the internal delay for the internal registers to be reset to 0, and the associated function change. The registers will remain set to 0 when POR goes high, until new data is written.

FUNCTIONAL DESCRIPTION

Introduction

The fundamental difference between the operation of a speakerphone and a telephone handset is that of half–duplex versus full–duplex. The handset is full duplex, meaning conversation can occur in both directions (transmit and receive) simultaneously. This is possible due to both the low sound level at the receiver, and the fact that the acoustic coupling from the earpiece to the mouthpiece is almost non–existent (the receiver is normally held against a person's ear). The loop gain from the receiver to the microphone and through the circuit is well below that needed to sustain oscillations.

A speakerphone, on the other hand, has higher gain levels in both the transmit and receive paths, and attempting to converse full duplex results in oscillatory problems due to the loop that exists within the speakerphone circuit. The loop is formed by the hybrid, the acoustic coupling (speaker to microphone), and the transmit and receive paths (between the hybrid and the speaker/microphone). The only practical and economical method used to date is to design the speakerphone to function in a half duplex mode – i.e., only one person speaks at a time, while the other listens. To achieve this requires a circuit which can detect who is talking (in reality, who is talking louder), switch "on" the appropriate path (transmit or receive), and switch "off" (attenuate) the other path. In this way, the loop gain is maintained less than unity. When the talkers exchange function, the circuit must quickly detect this, and switch the circuit appropriately. By providing speech level detectors, the circuit operates in a "hands–free" mode, eliminating the need for a "push–to–talk" switch.

The MC33218A provides the necessary circuitry to perform a voice switched, half duplex, speakerphone function. The IC includes transmit and receive attenuators, pre–amplifiers, and level detectors and background noise monitors for each path. An attenuator control circuit automatically adjusts the gain of the transmit and receive attenuators based on the relative strengths of the voice signals present, the volume control, and the supply voltage (when low). The detection sensitivity and timing are externally controllable.

The MC33218A is unique compared to most speakerphone integrated circuits in that it has a microprocessor serial port for control of various functions. Those functions are:

– Volume level (15 steps of ≈ 3.0 dB each)
– Microphone amplifier mute
– Attenuator range selection (53 dB or 27 dB)
– Force to receive, idle, or transmit to override the automatic switching.

Please refer to the Block Diagram (Figure 3) when reading the following sections.

Transmit and Receive Attenuators (Full Range B5 = 0)

The transmit and receive attenuators are complementary, performing a log–antilog function. When one is at maximum gain (≈ 6.7 dB), the other is at maximum attenuation (–47 dB) – they are never both fully "on" or fully "off". Both attenuators are controlled by a single output from the Attenuator Control Circuit which ensures the sum of their gains will remain constant at a typical value of –40 dB. Their purpose is to provide the half–duplex operation required in a speakerphone.

The attenuators are non–inverting, and have a usable bandwidth of 50 kHz. Their input signal (at MCO and RXO) should be limited to 300 mVrms (850 mVp–p) to prevent distortion. That maximum recommended input signal is independent of the volume control setting. Both the inputs and outputs are biased at ≈ V_B. The output impedance is <10 Ω until the output current limit (typically 2.0 mA peak) is reached.

The attenuators are controlled by the single output of the Attenuator Control Circuit, which is measurable at C_T (Pin 7). When the circuit detects speech signals directing it to the receive mode (by means of the level detectors described below), an internal current source of 42 μA will charge the C_T capacitor to a voltage positive with respect to V_B (see Figure 29). At the maximum volume control setting, this voltage will be approximately +150 mV, and the receive attenuator will have a gain of +6.7 dB. When the circuit detects speech signals directing it to the transmit mode, an internal current source of 42 μA will take the capacitor to approximately –100 mV with respect to V_B (the transmit attenuator will have a gain of +6.7 dB). When there is no speech present in either path, the current sources are shut off, and the voltage at C_T will decay to be equal to V_B. This is the idle mode, and the attenuators' gains are nearly half–way between their fully "on" and fully "off" positions (–25 dB for the R_X attenuator, –16 dB for the T_X attenuator). Monitoring the C_T voltage (with respect to V_B) is the most direct method of monitoring the circuit's mode, and its response.

Transmit and Receive Attenuators (Half Range B5 = 1)

With the attenuators set to the half range, the attenuator which is "on" will have a gain of ≈ –7.0 dB, while the "off" attenuator will have a gain of ≈ –34 dB. The idle mode is the same as for the full range (–25 dB for the R_X attenuator, –16 dB for the T_X attenuator). The voltage at the C_T pin, with respect to V_B, will be –35 mV for the transmit mode, and +85 mV for the receive mode.

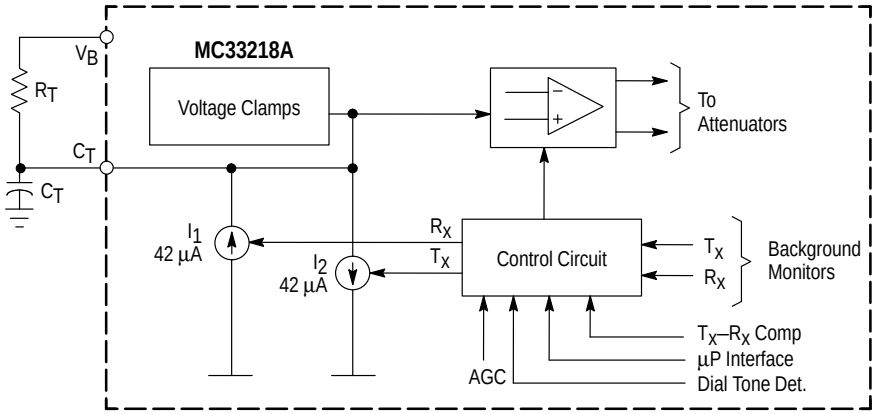
Attenuator Control Circuit

The inputs to the Attenuator Control Section (Figure 29) are six: The T_X–R_X comparator operated by the level detectors, two background noise monitors, the AGC circuit, the dial–tone detector, and the microprocessor interface. These six functions are described as follows.

Level Detectors, T_X–R_X Comparator

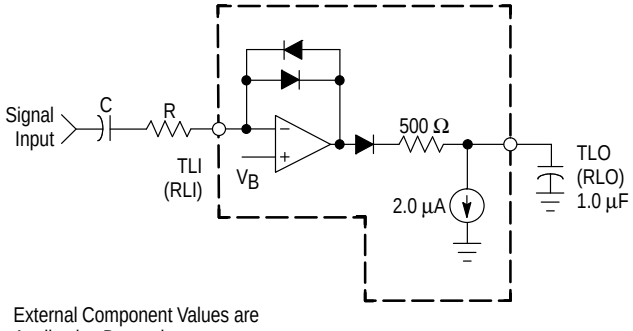
There are two identical level detectors – one on the receive side and one on the transmit side (refer to Figure 30). Each level detector is a high gain amplifier with back–to–back diodes in the feedback path, resulting in non–linear gain, which permits operation over a wide dynamic range of speech levels. Refer to the graphs of Figures 9, 10, and 11 for their DC and AC transfer characteristics. The sensitivity of each level detector is determined by the external resistor and capacitor at their input (TLI and RLI). The output charges an external capacitor through a diode and limiting resistor, thus providing a DC representation of the input AC signal level. The outputs have a quick rise time (determined by the capacitor and an internal 500 Ω resistor), and a slow decay time set by an internal current source and the capacitor. The capacitors at RLO and TLO should have the same value (±10%) to prevent timing problems.

Figure 29. C_T Attenuator Control Circuit



Referring to Figure 3, the outputs of the two level detectors drive the T_X–R_X comparator. The comparator's output state depends on whether the transmit or receive speech signal is stronger, as sensed by the level detectors. The Attenuator Control Circuit uses this signal, along with the background noise monitors, to determine which mode to set.

Figure 30. Level Detector



External Component Values are Application Dependent.

Background Noise Monitors

The purpose of a background noise monitor is to distinguish speech (which consists of bursts) from background noise (a relatively constant signal). There are two background noise monitors – one for the receive path and one for the transmit path. Referring to Figure 32, each is operated on by a level detector, which provides a dc voltage representative of the combined speech and noise level. The peaks, valleys, and bursts, which are characteristic of speech, will cause that DC voltage (at CP2 or RLO) to increase relatively quickly, causing the output of the next amplifier to also rise quickly. If that increase exceeds the 36 mV offset, at a speed faster than the time constant at CPT (CPR), the output of the last comparator will change, indicating the presence of speech to the attenuator control circuit. This will keep the circuit in either the transmit or the receive mode, depending on which side has the stronger signals. Whenever a new continuous signal is applied, the time constant at CPT (CPR) determines how long it takes the circuit to decide that the new sound is continuous, and therefore background noise. The system requires that the average speech signal be stronger than the background noise level (by 6.0–7.0 dB) for proper speech detection to occur.

When only background noise is present in both paths, the output of the monitors will indicate the absence of speech, allowing the circuit to go to the idle mode.

AGC Circuit

In the receive mode only, the AGC circuit decreases the gain of the receive attenuator when the supply voltage at V_{CC} falls below 3.5 V, according to the graph of Figure 8. The gain of the transmit path changes in a complementary manner.

The purpose of this feature is to reduce the power (and current) used by the speaker when the speakerphone is powered by the phone line, and is connected to a long telephone line, where the available power is limited. Reducing the speaker power controls the voltage sag at V_{CC}, reduces clipping and distortion at the speaker output, and prevents possible erratic operation.

Dial Tone Detector

When a speakerphone is initially taken off–hook, the dial tone signal will switch the circuit to the receive mode. However, since the dial tone is a continuous signal, the MC33218A will consider it as background noise, rather than speech, and would switch from receive to idle, causing the dial tone sound to fade. The dial tone detector prevents the fading by disabling the receive background noise monitor.

The dial tone detector is a comparator with one side connected to the receive attenuator input (RXO), and the other input connected to V_B with a –20 mV offset (see Figure 31). If the circuit is in the receive mode, and the incoming signal has peaks greater than 20 mV (14 mV rms), the comparator's output will change, keeping the circuit from switching to the idle mode. The receive attenuator will then be at a gain determined solely by the volume control. **NOTE:** The dial tone detector is **not** a frequency discriminating circuit.

Figure 31. Dial Tone Detector

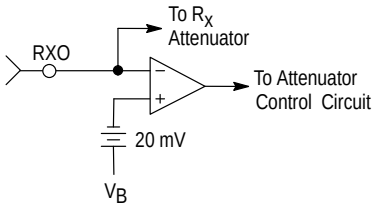
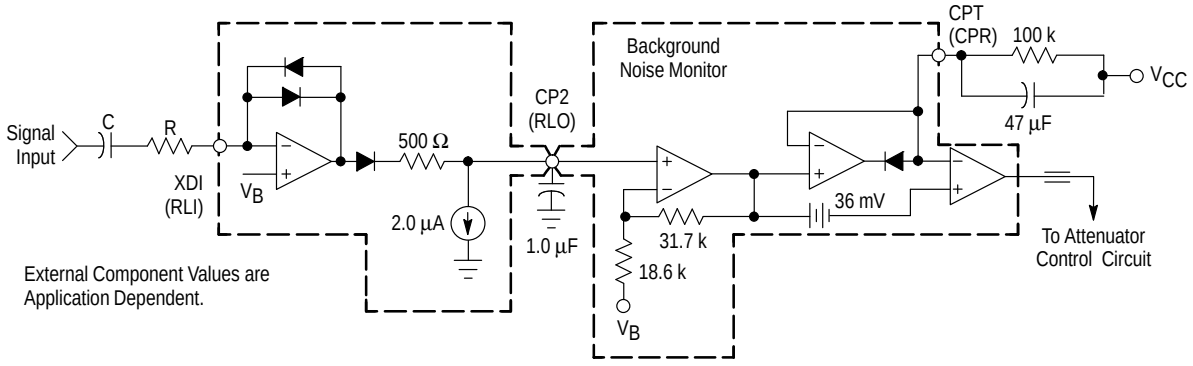


Figure 32. Background Noise Monitor



Microprocessor Interface

The three line SPI port (Pins 17–19) is used for setting various functions with a single 8 bit word. The functions are as follows:

– Volume Control: Bits B0–B3 control the gain of the attenuators only when in the receive mode. Setting B3–B0 = 0000 sets the receive attenuator to its maximum gain (+6.7 dB in full range, –7.0 dB in half range), and therefore maximum volume at the speaker. Setting B3–B0 = 1111 sets the receive attenuator to a minimum gain level (≈ –32 dB), and is the minimum volume setting. B0 is the LSB for this function, and each step changes the gain by ≈ 3.0 dB at the high volume end (see Figure 6 and 7). The transmit attenuator gain is varied in a complementary manner. These bits have no effect in the idle or transmit modes.

– Muting of the Microphone Amplifier: Bit B4 is used to set the microphone amplifier to the normal or the muted mode. When this bit is a 1, the amplifier is muted. See the paragraph entitled “Microphone Amplifier, Mute” elsewhere in this document.

– Attenuator Range: Bit B5 is used to select the attenuator range. When it is a 0, the range is 53 dB (from full “on” to full “off”). When it is a 1, the range is 27 dB. The 53 dB range is used for the majority of applications, such as desktop speakerphones (home or office use), intercom units, and any application where the speaker and microphone are in close proximity. The 27 dB range is commonly used in European speakerphone applications, where the typical design involves using the handset for the microphone function, and is therefore somewhat separated from the speaker.

– Operating Mode: Bits B7 and B6 set the circuit operating mode. When 00, the normal voice activated switching is enabled, and the circuit responds to the speech levels as described elsewhere in this document. When 01, the circuit is forced to the receive mode in that the receive attenuator is “on” and the transmit attenuator is “off”. The volume control (Bits B3–B0) is effective in this mode. When 10, the circuit is forced to the idle mode. When 11, the circuit is forced to the transmit mode. The volume control bits have no effect in the idle or transmit modes.

The eight bits are entered serially, B7 first and B0 last. Each bit is entered on a clock rising edge. The maximum clock and data rate is 1.0 MHz, and there is no minimum required speed. Data Ready, which is normally high, is to be held low while the eight bits are clocked in. The eight bits take effect when Data Ready is taken high. There is no chip address, or other protocol or handshaking required. See Figure 2 for a timing diagram. Note that Data Ready need not be taken low before the first clock rising edge. It must be taken low before the first clock falling edge which follows the first clock rising edge. This allows Data Ready to be taken low coincident with the first clock rising edge, if desired, as well as before that.

It is recommended that DR be kept high when not entering data, to prevent disruption of the circuit by transients or glitches on the clock or data lines. This is not required, and DR may be taken low after latching in data, if desired.

The clock input can be stopped after B0 is entered, or it may continue to run as long as Data Ready is taken high before the next clock rising edge. It is recommended that the clock not be continued to prevent possible noise problems.

The three inputs must be kept within the range of V_{CC} and GND. If an input is taken more than 0.5 V above V_{CC} or below GND excessive currents will flow, and the device’s operation will be distorted. See Figure 18 for input current requirements at these pins.

Power On Reset

The Power On Reset, when at a logic low (below its threshold of 1.2 V) resets the internal registers to a logic 0, independent of the Clock, Data, or Data Ready position. A capacitor on this pin provides a power up time delay to allow V_{CC} to stabilize before the registers can accept data. Alternately, Pin 20 can be driven directly from a logic source if desired. The POR input must be kept within the range of V_{CC} and GND. If the input is taken more than 0.5 V above V_{CC} or below GND excessive currents will flow, and the device’s operation will be distorted. The configuration of this pin is shown in Figure 33.

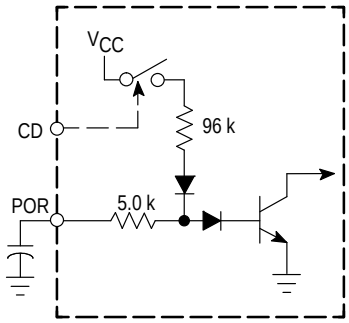
When V_{CC} is applied to the MC33218A, the registers will be enabled when the voltage at POR exceeds 1.2 V. The time to reach this level depends on the capacitor at POR, and V_{CC}, and will not be less than the time shown in Figure 20. The actual reset time is affected by the rise time of V_{CC}. Any data written to the registers while POR is below 1.2 V will not be stored or effective.

The nominal DC voltage at POR is ≈ 1.5 V.

The registers may be intentionally reset by external control by pulling POR to ground with (for example) an open collector NPN transistor. The time to reset is shown in Figure 28. When POR once again goes high, the registers’ data will remain at 0 until new data is entered. Old data is not retained. The time required to release the registers after releasing POR (by turning “off” the NPN transistor) is shown in Figure 20.

If POR is driven by an external logic output, its input current requirement is shown in Figure 19.

Figure 33. Power On Reset Pin

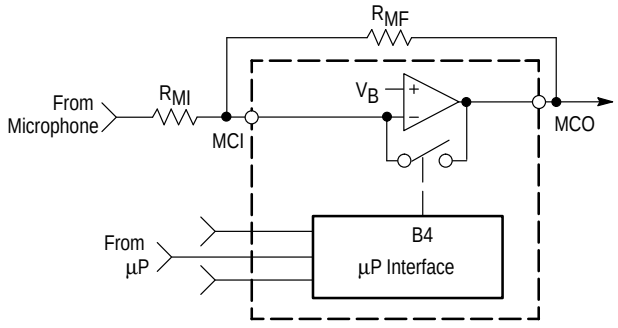


Microphone Amplifier, Mute

The microphone amplifier (Pins 21, 22) has the non–inverting input internally connected to V_B, while the inverting input and the output are pinned out. Unlike most op–amps, the amplifier has an all–NPN output stage, which maximizes phase margin and gain–bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain is typically 80 dB (f <100 Hz), and the gain–bandwidth is typically 1.5 MHz. The maximum output swing, for 1.0% or less distortion, is determined by the input capability of the transmit attenuator (300–350 mVrms), and by V_{CC} at low supply voltages (see Figure 16). The output impedance is <10 Ω until current limiting is reached (typically 2.0 mA peak). The input bias current at MCI is typically 30 nA out of the pin.

The mute function, when activated, will reduce the gain of the amplifier by shorting the external feedback resistor (RMF Figure 34). The amplifier is not disabled in this mode – MCO remains a low impedance output, and MCI remains a virtual ground at V_B. The amount of muting (the **change** in gain) depends on the value of the external feedback resistor, according to the graph of Figure 17. Muting is enabled by setting bit B4 to a logic 1.

Figure 34. Microphone Amplifier and Mute



Receive Amplifier

The receive amplifier (Pins 15, 16) has the non–inverting input internally connected to V_B, while the inverting input and the output are pinned out. Unlike most op–amps, the amplifier has an all–NPN output stage, which maximizes phase margin and gain–bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain is typically 80 dB (f <100 Hz), and the gain–bandwidth is typically 1.5 MHz. The maximum p–p output swing, for 1.0% or less distortion, is determined by the input capability of the receive attenuator (300–350 mVrms), and by V_{CC} at low supply voltages (see Figure 16). The output impedance is <10 Ω until current limiting is reached (typically 2.0 mA peak). The input bias current at RXI is typically 30 nA out of the pin.

Power Supply, V_B and Chip Disable

The power supply voltage at Pin 24 is to be between 3.5 and 6.5 V for normal operation, and down to 2.7 V with the AGC in effect (see AGC section). The supply current required is typically 4.6 mA in the idle and transmit modes (at 5.0 V), and slightly more in the receive mode. Figure 13 shows the supply current for both the normal and disabled modes.

The output voltage at V_B (Pin 6) is approximately equal to (V_{CC} – 0.7)/2, and provides an ac ground for the internal amplifiers, and the system. The output impedance at V_B is approximately 600 Ω, and in conjunction with the external capacitor at V_B, forms a low pass filter for power supply noise rejection. The choice of the V_B capacitor size is application dependent based on whether the circuit is powered by the telephone line or a regulated supply. See Figure 15 for PSRR data from V_{CC} to V_B. Since V_B biases the microphone and receive amplifiers, the amount of supply rejection at their outputs is a function of the rejection at V_B, as well as the gains of the amplifiers.

The amount of current which can be sourced out of the V_B pin depends on the V_{CC} voltage (see Figure 14). Drawing current in excess of that shown in Figure 14 will cause V_B to drop low enough to disrupt the circuit's operation. This pin can sink ≈ 100 µA when enabled, and 0 µA when disabled.

The Chip Disable (Pin 8) permits powering down the IC for power conservation. With CD between 0 and 0.8 V, normal operation is in effect. With CD between 2.0 V and V_{CC}, the IC is powered down, and the supply current drops to ≈ 110 µA (at V_{CC} = 5.0 V, see Figure 13). When CD is high, the microphone and receive amplifiers, the level detectors, and the two attenuators are disabled (their outputs go to a high impedance). The background noise monitors are disabled, and Pins 3 and 10 will go to V_{CC}. The V_B output, however, remains active, except that it cannot sink any current. The serial port is disabled so that new data may not be entered. Upon re–enabling the circuit, the 8 internal registers will be set to 0, regardless of their previous contents. Figure 26 indicates the disable and enable timing.

The CD input must be kept within the range of V_{CC} and GND. See Figure 12 for input current requirements. If the input is taken more than 0.5 V above V_{CC} or below GND, excessive currents will flow, and the device's operation will be distorted. If the disable function is not used, the pin should be connected to ground.

APPLICATIONS INFORMATION

Switching and Response Time Theory

The switching time of the MC33218A circuit is dominated by the components at C_T (Pin 7, refer to Figure 3), and second by the capacitors at the level detector outputs (RLO, TLO).

The transition time to receive or to transmit mode from idle, or from the other mode, is determined by the capacitor at C_T, together with the internal current sources (refer to Figure 29). The switching time is:

$$\Delta T = \frac{\Delta V \times C_T}{I}$$

When switching from idle to receive, ΔV = 150 mV, I = 42 μA, the C_T capacitor is 15 μF, and ΔT calculates to ≈ 53 ms. When switching from idle to transmit, ΔV = 100 mV, I = 42 μA, the C_T capacitor is 15 μF, and ΔT calculates to ≈ 36 ms.

When the circuit switches to idle, the internal current sources are shut "off", and the time constant is determined by the C_T capacitor and RT, the external resistor (see Figure 29). With C_T = 15 μF, and RT = 15 kΩ, the time constant is ≈ 225 ms, giving a total switching time of ≈ 0.68 s (for 95% change). The switching period to idle begins when both speakers have stopped talking. The switching time back to the original mode will depend on how soon that speaker begins speaking again. The sooner the speaking starts during the "decay to idle" period, the quicker the switching time since a smaller voltage excursion is required. That switching time is determined by the internal current sources as described above.

When the circuit switches directly from receive to transmit (or vice–versa), the total switching time depends not only on the components and currents at the C_T pin, but also on the response of the level detectors, the relative amplitude of the two speech signals, and the mode of the circuit, since the two level detectors are connected differently to the two attenuators.

The rise time of the level detector's outputs (RLO, TLO) is not significant since it is so short. The decay time, however, provides a significant part of the "hold time" necessary to hold the circuit (in transmit or receive) during the normal pauses in speech. The capacitors at the two outputs must be equal value (±10%) to prevent problems in timing and signal response.

The components at the inputs of the level detectors (RLI, TLI) do not affect the switching time, but rather affect the relative signal levels required to switch the circuit, as well as the frequency response of the detectors. They must be adjusted for proper switching response as described later in this document.

Switching and Response Time Measurements

Using burst of 1.0 kHz sine waves to force the circuit to switch among its modes, the timing results were measured and are indicated in Figures 21–25.

a) In Figure 21, when a signal is applied to the transmit attenuator only (normally via the microphone and the microphone amplifier), the transmit background noise monitor immediately indicates the "presence of speech" as evidenced by the fact that CPT begins rising. The slope of the rising CPT signal is determined by the external resistor and capacitor on that pin. Even though the transmit attenuator is initially in the idle mode (–16 dB), there is sufficient signal at its output to cause TLO to increase. The attenuator control circuit then forces the circuit to the transmit mode, evidenced by the change at the C_T pin. The attenuator output signal is then 6.7 dB above the input.

With the steady sine wave applied to the transmit input, the circuit will stay in the transmit mode until the CPT pin gets to within 36 mV of its final value. At that point the internal comparator (see Figure 32) switches, indicating to the attenuator control circuit that the signal is not speech, but rather it is background noise. The circuit now begins to decay to idle, as evidenced by the change at C_T and TLO, and the change in amplitude at TAO.

When the transmit signal at MCO is removed (or reduced), the CPT pin drops quickly, allowing the CPT to quickly respond to any new speech which may appear afterwards. The voltage at C_T decays according to the time constant of its external components, if not already at idle.

The voltage change at CP2, CPT, and TAO depend on the input signal's amplitude, and the components at XDI and TLI. The change at C_T is internally fixed at the level shown. The timing numbers shown depend both on the signal amplitudes and the components at the C_T and CPT pins.

b) Figure 22 indicates what happens when the same signal is applied to the receive side only. RLO and CPR react similarly to TLO and CPT. However, the circuit does not switch to idle when CPR finishes transitioning since the dial tone detector disables the background noise monitor, allowing the circuit to stay in the receive mode as long as there is a signal present. If the input signal amplitude had been less than the dial tone detector's threshold, the circuit response would have been similar to that shown in Figure 21. The voltage change at C_T depends on the setting of the volume control (bits B3–B0). The +150 mV represent maximum volume.

c) Figure 23 indicates the circuit response when transmit and receive signals are alternately applied, with relatively short cycle times (300 ms each) so that neither attenuator will begin to go to idle during its "on" time. Figure 24 indicates the circuit response with longer cycle times (1 s each), where the transmit side is allowed to go to idle. Figure 25 is the same as Figure 24, except the capacitor at CT has been reduced from 15 μF to 6.8 μF, providing a quicker switching time. The reactions at the various pins are shown. The response times at TAO and RAO are different, and typically slightly longer than what is shown in Figures 21 and 22 due to:

– The larger transition required at CT pin,

– The greater difference in the levels at RLO and TLO due to the positions of the attenuators, as well as their decay time, and

– Response time of background noise monitors.

The timing responses shown in these three figures are representative for those input signal amplitudes, and burst durations. Actual response time will vary for different signal conditions.

NOTE: While it may seem desirable to decrease the switching time between modes by reducing the capacitor at CT, this should be done with caution for two reasons:

1) If the switching time is too short, the circuit response may appear to be "too quick" to the user, who may consider its operation erratic. The recommended values in this data sheet, along with the accompanying timings, provide what

experience has shown to be a “comfortable response“ by the circuit.

2) The distortion in the receive attenuator will increase as the CT capacitor value is decreased. The extra THD will be most noticeable at the lower frequencies, and at the lower amplitudes. Table 1 provides a guideline for this issue.

Table 1. THD versus CT Capacitor

CT Capacitor	Idle–R_X Transition	Input @ RAI	Freq.	THD @ RAO
15 µF	53 ms	20 mVrms	300 Hz	1.5%
			1.0 kHz	0.3%
		100 mVrms	300 Hz	0.6%
			1.0 kHz	0.12%
6.8 µF	24 ms	20 mVrms	300 Hz	3.6%
			1.0 kHz	1.0%
		100 mVrms	300 Hz	1.4%
			1.0 kHz	0.4%
3.3 µF	12 ms	20 mVrms	300 Hz	7.0%
			1.0 kHz	1.9%
		100 mVrms	300 Hz	2.8%
			1.0 kHz	0.7%

Considerations in the Design of a Speakerphone

The design and adjustment of a speakerphone involves human interfaces issues, as well as proper signal levels. Because of this fact, it is not practical to do all of the design mathematically. Certain parts of the design must be done by trial and error, most notably the switching response and the “How does it sound?” part of the testing. Among the recommendations for a successful design are:

1) Design the enclosure **concurrently** with the electronics. Do not leave the case design to the end as its properties are just as important (just as *equally* important) as the electronics. One of the major issues involved in a speakerphone design is the acoustic coupling of the speaker to the microphone, which must be minimized. This parameter is dependent entirely on the design of the enclosure, the mounting of the speaker and the microphone, and their characteristics.

2) Ensure the speaker is optimally mounted. This fact alone can make a difference of several dB in the sound level from the speaker, as well as the sound quality. The speaker manufacturer should be consulted for this information.

3) Do not breadboard the circuit with the microphone and speaker hanging out in midair. It will not work. The speaker and microphone must be in a suitable enclosure, preferably one resembling the end product. If this is not feasible, temporarily use some other properly designed enclosure, such as one of the many speakerphones on the market.

4) Do not breadboard the circuit on a wirewrapped board or a plug–in prototyping board. Use a PC board, preferably with a ground plane. Proper filtering of the supply voltage, at the V_{CC} pin, is essential.

5) The speakerphone must be tested with the intended hybrid, and connected to a phone line, or phone line simulator. The performance of the hybrid is just as important as the enclosure and the speakerphone IC.

6) When testing the speakerphone, be conscious of the environment. If the speakerphone is in a room with large windows and tile floors, it will sound different than if it is in a carpeted room with drapes. Additionally, be conscious of the background noise in a room.

7) When testing the speakerphone on a phone line, make sure the person at the other end of the phone line is **not** in the same room as the speakerphone.

Design and Adjustment Procedure

Assuming the end product enclosure is available, with the intended production microphone and speaker installed, and the PC boards installed (or temporary substitutes for the PC boards) a recommended sequence is as follows (refer to Figure 35):

1) Design the hybrid, ensuring it interfaces properly with the phone line for both DC and AC characteristics. The return loss must be adjusted so as to comply with the appropriate regulatory agency. The sidetone should then be adjusted according to the intent of the product. If the product is a speakerphone only, without a handset, the sidetone gain (GST) should be adjusted for maximum loss. If a handset is part of the end product, the sidetone must be adjusted for the minimum acceptable sidetone levels in the handset. Generally, for the speakerphone, 10–20 dB sidetone loss is preferred for GST.

2) Check the acoustic coupling of the enclosure (GAC in Figure 35). With a steady sound coming out of the speaker, measure the rms voltage on the speaker terminals, and the rms voltage out of the microphone. Experience has shown that the loss should be at least 40 dB, preferably 50 dB. This should be checked over the frequency range of 20 Hz to 10 kHz.

3) Adjust the transmit path for proper signal levels, based on the lowest speech levels as well as the loudest. Based on the typical levels from commonly available microphones, a gain of about 35–45 dB is required from the microphone terminals to Tip and Ring. Most of that gain should be in the microphone amplifier so as to make best use of the transmit attenuator, but make sure the maximum attenuator input level at MCO is not exceeded. If a signal generator is used instead of a microphone for testing, the circuit can be locked into the transmit mode by grounding CPT (Pin 3), or using bits B7 and B6 (set to 11). Frequency response can generally be tailored with capacitors at the microphone amplifier.

4) Adjust the receive path for proper signal levels, based on the lowest speech levels as well as the loudest. A gain of about 30 dB is required from Tip and Ring to the speaker terminals for most applications (at max. volume). Most of that gain should be in the receive amplifier (at RXI, RXO) so as to make best use of the receive attenuator, but make sure the max. attenuator input level at RXO is not exceeded. If a signal generator is used for signal injection during testing, the circuit can be locked into the receive mode by grounding CPR (Pin 10), although this is usually not necessary since the dial tone detector will keep the circuit in the receive mode. As an alternate, bits B7 and B6 can be set to 01. Frequency response can generally be tailored with capacitors at the receive amplifier.

5) Check that the loop gain (i.e., the receive path gain + acoustic coupling gain + transmit path gain + sidetone gain) is less than 0 dB over all frequencies. If not, “singing” will occur – a steady oscillation at some audible frequency.

6) a) The final step is to adjust the resistors at the level detector inputs (RLI and TLI) for proper switching response

(the switchpoint occurs when $I_1 = I_2$). This has to be the last step as the resistor values depend on all of the above adjustments, which are based on the mechanical, as well as the electrical, characteristics of the system. **NOTE:** An extreme case of level detector misadjustment can result in “motorboating”. In this condition, with a receive signal applied, sound from the speaker enters the microphone, and causes the circuit to switch to the transmit mode. This causes the speaker sound to stop (as well as the sound into the microphone), allowing the circuit to switch back to the receive mode. This sequence is then repeated, usually, at a rate of a few Hz. The first thing to check is the acoustic coupling, and then the level detector input resistors.

b) Starting with the recommended values for R_1 and R_2 (in Figure 3), hold a normal conversation with someone on another phone. If the resistor values are not optimum, one of the talkers will dominate, and the other will have difficulty getting through. If, for example, the person at the speakerphone is dominant, the transmit path is overly sensitive, and the receive path is not sensitive enough. In this case, R_1 should be increased, or R_2 decreased, or both. Their exact value is not critical at this point, only their relative value. Keeping R_1 and R_2 in the range of 2.0–20 K, adjust them until a suitable switching response is obtained.

c) Then have the person at the other end of the phone line speak continuously loudly, or connect to a recording which is somewhat strong. Monitor the state of the circuit (by measuring the C_T versus V_B pins, and by listening carefully to the speaker) to check that the sound out of the speaker is not attempting to switch the circuit to the transmit side (through acoustic coupling). If it is, increase R_1 (at TLI) in small steps just enough to stop the switching (this de–sensitizes the transmit side). If R_1 has been changed a large amount, it may be necessary to readjust R_2. If this cannot be achieved in a reasonable manner, the acoustic coupling is too strong.

d) Then have the person at the speakerphone speak somewhat loudly, and again monitor the state of the circuit, primarily by having the person at the other end listen carefully for fading. If there is obvious fading of the sound, increase R_2 so as to de–sensitize the receive side. Increase R_2 just enough to stop the fading. If this cannot be achieved in a reasonable manner, the sidetone coupling is too strong.

e) If necessary, readjust R_1 and R_2, relative to each other, a small amount to further optimize the switching response.

Microprocessor Interface

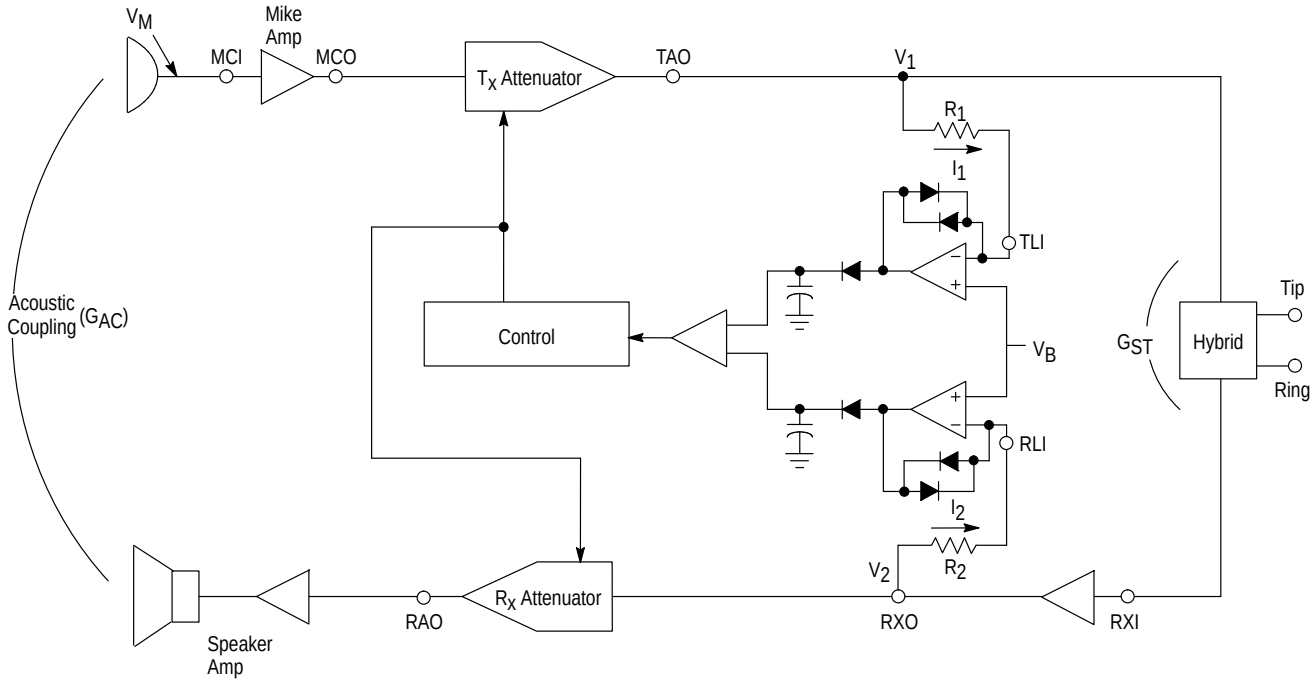
The microprocessor interface (Pins 17–19) can be controlled by any microprocessor with an SPI port, or from a general purpose port which can be configured to provide the correct signals. The MC33218A requires one 8–bit word to set the various parameters – there is no chip address, or other protocol or handshaking required. See Figure 2 for a timing diagram. The function of each of the bits is described in the Functional Description, as well as in a table near the beginning of this document. The pin’s functions are as follows:

– DATA: Bit B7 is entered first, and B0 last, and each bit is entered on a clock rising edge. The minimum setup and hold times indicated in the Electrical Characteristics must be adhered to. If more than 8 bits are entered, the last 8 bits to be entered will be stored in the registers.

– CLOCK: The clock enters the data on each rising edge. There is no minimum required frequency, and the maximum frequency is 1.0 MHz. It is recommended that the clock be stopped when data is not being entered to minimize the possibility of creating audible noise in the speech paths. This input is disabled when Data Ready is high.

– DATA READY: This input must be held low while data is being entered, and then taken high to latch in the new data. The new data will not affect the MC33218A until Data Ready is taken high. It is recommended that Data Ready be kept high at all times except when entering data, although this is not required for the IC to function correctly.

Figure 35. Basic Block Diagram for Design Purposes



Upon powering up the MC33218A, or when the IC is disabled by means of the CD pin (Pin 8), the eight registers are internally set to a logic 0, regardless of their previous contents. This default condition corresponds to normal voice switched operation, 53 dB attenuator range, active microphone amplifier, and maximum receive volume level.

The amplitude of the three inputs must be less than 0.8 V for a logic 0, and between 2.0 V and V_{CC} for a logic 1. The three inputs must be kept within the range of V_{CC} and GND. If any input is taken more than 0.5 V above V_{CC} or below GND excessive currents will flow, and the device's operation will be distorted.

Power On Reset

The Power On Reset function sets the 8 internal registers to logic 0's whenever the MC33218A is powered up, or whenever the Chip Disable pin (Pin 8) is taken high. A capacitor on Pin 20 (POR) creates a time delay, allowing V_{CC} to stabilize before the registers can accept data. The effective resistance at this pin, for timing purposes, is ≈ 115 kΩ. A 0.1 µF capacitor, for example, provides a time delay of ≈ 3.7 ms (at V_{CC} = 5.0 V).

Alternately, Pin 20 can be driven directly from a logic source if desired, – the switching threshold is ≈ 1.2 V. When taken low, the registers are reset to 0, independent of the Clock or Data Ready position. The POR input must be kept within the range of V_{CC} and GND. If the input is taken more than 0.5 V above V_{CC} or below GND excessive currents will flow, and the device's operation will be distorted. See Figure 33 for the circuit configuration.

Transmit/Receive Detection Priority

Although the MC33218A was designed to have an idle mode such that the transmit side has a small priority (the idle mode position is closer to the full transmit side than the receive side), the idle mode position can be moved with respect to the transmit or the receive side. With this done, the ability to gain control of the circuit by each talker will be changed.

By connecting a resistor from C_T (Pin 7) to ground, the circuit will be biased more towards the transmit side. The resistor value is calculated from:

$$R = R_T \left[\frac{V_B}{\Delta V} - 1 \right]$$

where R is the added resistor, R_T is the resistor normally between Pins 6 and 7 (typically 15 kΩ), and ΔV is the desired change in the C_T voltage at idle. V_B is the voltage at Pin 6.

By connecting a resistor from C_T (Pin 7) to V_{CC}, the circuit will be biased towards the receive side. The resistor value is calculated from:

$$R = R_T \left[\frac{V_{CC} - V_B}{\Delta V} - 1 \right]$$

R, R_T, ΔV, and V_B are the same as above. Switching response and the switching time will be somewhat affected in each case due to the different voltage excursions required to get to transmit and receive from idle. For practical considerations, the ΔV shift should not exceed 50 mV.

Disabling the Idle Mode

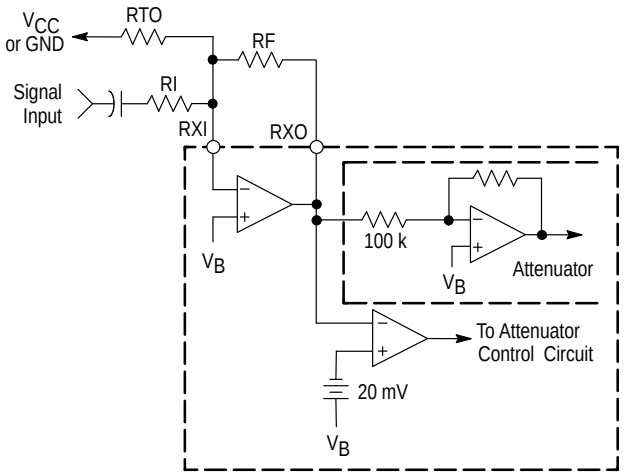
In order to test the gain, and performance, of the transmit path and the receive path, they can each be set to their full "on" positions using bits B7 and B6 of the serial port. However, if it is desired to tests these paths with the IC in the normal voice switched mode (B7, 6 = 00), the transmit or receive attenuator can be set to the "on" position, even with steady signals applied, by disabling the background noise monitors. Grounding the CPT pin will disable the transmit background noise monitor, causing the circuit to stay in the full transmit mode, even with a low level continuous signal applied to the transmit path. Grounding CPR does the same for the receive path. Additionally, the receive background noise monitor is automatically disabled by the dial tone detector whenever the receive signal exceeds that detector's threshold.

Dial Tone Detector Threshold

The threshold for the dial tone detector is internally set at ≈ 20 mV (14 mVrms) below V_B (see Figure 31). That threshold can be changed if desired by changing the DC bias level at RXO.

Since the attenuator input is DC coupled to the receive amplifier, the threshold is changed by forcing an offset through the receive amplifier. As shown in Figure 36, connect a resistor (RTO) from the summing node to either ground or V_{CC}, depending on whether the dial tone detector threshold is to be increased or decreased. RF and RI are the resistors normally used to set the receive audio gain.

Figure 36. Adjusting Dial Tone Detector Threshold



Adding RTO, and connecting it to ground will shift RXO up, thereby increasing the dial tone detector threshold. In this case, RTO is calculated from:

$$RTO = \frac{V_B \times RF}{\Delta V}$$

V_B is the voltage at Pin 6, and ΔV is the amount that the detector's threshold is to be increased. For example, if V_B = 2.2 V, RF = 10 K, and ΔV = 20 mV, RTO calculates to 1.1 MΩ.

Connecting RTO to V_{CC} will shift RXO down, thereby decreasing the dial tone detector threshold. In this case, RTO is calculated from:

$$RTO = \frac{(V_{CC} - V_B) \times RF}{\Delta V}$$

For example, if V_{CC} = 5.0 V, V_B = 2.2 V, RF = 10 K, and ΔV = 10 mV, RTO calculates to 2.8 MΩ.

Board Layout, RFI Interference

Although the MC33218A is meant to be used at audio frequencies, the various amplifiers within have bandwidths exceeding 1.0 MHz, and can therefore oscillate due to stray capacitance and other parasitics if care is not taken in the board layout. A PC board, with a ground plane, is recommended for breadboarding as well as production. Factors to keep in mind are:

– The heavy current draw in a speakerphone type product is in the speaker, and consequently, in the speaker amplifier. The power supply and ground connection to the speaker amplifier must be done with care so as to not create significant ripple, or ground noise, for the remaining circuitry.

– The power supply bypass for the MC33218A should be 100 μF if powered by a regulated power supply, and 1000 μF if powered by the phone line. The bypass capacitor must be physically close to the IC – preferably within one inch. This is particularly important in a circuit powered by the phone line. Oscillations, or instabilities, can result if this guideline is not followed.

– As with any circuit which involves mixing analog and digital circuitry, care must be taken in the layout to prevent digital noise from getting into the analog speech paths. As a general rule, all the analog circuitry (phone line interface, speech network, speakerphone, and speaker amplifier) should be “in its own area”. Mixing of the analog and digital circuits can result in the high speed logic transitions creating frequencies in the audible range.

– Generally it is not necessary to have a separate analog and digital ground. With many mixed mode devices (such as the MC33218A), this is impractical since there is only one ground pin on the IC. The significant factors here are that the ground plane be continuous, the various circuit sections be arranged logically, and that the V_{CC} distribution be done so as to not distribute noise to the analog circuits.

– Potential radio frequency interference (RFI) problems should be addressed early in the electrical and mechanical design of the speakerphone. RFI may enter the circuit through Tip and Ring, through the microphone wiring to the microphone amplifier (this wiring should be short), or through any of the PC board traces. The most sensitive pins on the MC33218A are the inputs to the level detectors (RLI, TLI, XDI) since, when there is no speech present, the inputs are high impedance and these op amps are in a near open loop condition. The board traces to these pins should be kept short, and the resistor and capacitor for each of these pins should be physically close to the pins. All other input pins should also be considered sensitive to RFI signals.

In The Final Analysis ...

Proper operation of a speakerphone is a combination of proper mechanical (acoustic) design as well as proper electronic design. The acoustics of the enclosure must be considered early in the design of a speakerphone. In general, electronics cannot compensate for poor acoustics, low speaker quality, low microphone quality, or any combination of these items. Proper acoustic separation of the speaker and microphone is essential. The physical location of the microphone, along with the characteristics of the selected microphone, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

In the final analysis, the circuit will have to be fine tuned to match the acoustics of the enclosure, the specific hybrid, and the specific speaker and microphone selected. The components shown in this data sheet should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at the microphone and receive amplifiers, respectively. The switching response can then be fine tuned by varying (in small steps) the components at the level detector inputs (TLI, RLI) until satisfactory operation is obtained for both long and short lines.

For additional information on speakerphone design please refer to The Bell System Technical Journal, Volume XXXIX (March 1960, No. 2).

DEFINITIONS

Attenuation – A decrease in magnitude of a communication signal, usually expressed in dB.

Bandwidth – The range of information carrying frequencies of a communication system.

Battery – The voltage which provides the loop current to the telephone from the CO. The name derives from the fact that COs have always used batteries, in conjunction with AC power, to provide this voltage.

C–Message Filter – A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

Central Office – Abbreviated CO, it is a main telephone office, usually within of a few miles of its subscribers, that houses switching gear for interconnection within its exchange area, and to the rest of the telephone system. A CO can handle up to 10,000 subscriber numbers.

CO – See Central Office.

CODEC – Coder/Decoder – In the Central Office, it converts the transmit signal to digital, and converts the digital receive signal to analog.

dB – A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

$$10 \times \log (P_1/P_2)$$

for power measurements, and

$$20 \times \log (V_1/V_2)$$

for voltage measurements.

dBm – An indication of signal power. 1.0 mW across 600 Ω, or 0.775 Vrms, is defined as 0 dBm. Any other voltage level is converted to dBm by:

dBm = 20 x log (Vrms/0.775), or
dBm = [20 x log (Vrms)] + 2.22.

dBmp – Indicates dBm measurement using a psophometric weighting filter.

dBrn – Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = –90 dBm.

dBrnC – Indicates a dBrn measurement using a C–message weighting filter.

DTMF – Dual Tone MultiFrequency. It is the "tone dialing" system based on outputting two non–harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a keypad.

Four Wire Circuit – The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the Transmit path, and one pair is for the Receive path.

Full Duplex – A transmission system which permits communication in both directions simultaneously. The standard handset telephone system is full duplex.

Gain – The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

Half Duplex – A transmission system which permits communication in one direction at a time. CB radios, with "push–to–talk" switches, and voice activated speakerphones, are half duplex.

Hookswitch – A switch, within the telephone, which connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Hybrid – A two–to–four wire converter.

Idle Channel Noise – Residual background noise when transmit and receive signals are absent.

Line Card – The pc board, and circuitry, in the CO or PBX which connects to the subscriber's phone line. A line card may hold circuitry for one subscriber, or a number of subscribers.

Longitudinal Balance – The ability of the telephone circuit to reject longitudinal signals on Tip and Ring.

Longitudinal Signals – Common mode signals.

Loop – The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or AC power.

Loop Current – The DC current which flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20–120 mA.

Mute – Reducing the level of an audio signal, generally so that it is inaudible. Partial muting is used in some applications.

Off Hook – The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the DC current as an indication that the phone is busy.

On Hook – The condition when the telephone is disconnected from the phone system, and no DC loop current flows. The central office regards an on hook phone as available for ringing.

PABX – Private Automatic Branch Exchange. In effect, a miniature central office, it is a customer owned switching system servicing the phones within a facility, such as an office building. A portion of the PABX connects to the Bell (or other local) telephone system.

Power Supply Rejection Ratio – The ability of a circuit to reject outputting noise, or ripple, which is present on the power supply lines. PSRR is usually expressed in dB.

Protection, Primary – Usually consisting of carbon blocks or gas discharge tubes, it absorbs the bulk of a lightning induced transient on the phone line by clamping the voltages to less than ±1500 V.

Protection, Secondary – Usually located within the telephone, it protects the phone circuit from transient surges. Typically, it must be capable of clamping a ±1.5 kV surge of 1.0 ms duration.

Pulse Dialing – A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed, and the interruption rate is typically 10 per second. The old rotary phones, and many new pushbutton phones, use pulse dialing.

Receive Path – Within the telephone it is the speech path from the phone line (Tip and Ring) towards the receiver or speaker.

REN – Ringer Equivalence Number. An indication of the impedance, or loading factor, of a telephone bell or ringer circuit. An REN of 1.0 equals ≈ 8.0 kΩ. The Bell system typically permits a maximum of 5.0 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

Return Loss – Expressed in dB, it is a measure of how well the telephone's AC impedance matches the line's AC characteristic impedance. With a perfect match, there is no reflected signal, and therefore infinite return loss. It is calculated from:

$$RL = 20 \times \log \frac{(Z_{LINE} + Z_{CKT})}{(Z_{LINE} - Z_{CKT})}$$

Ring – One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

SPI – Serial Port Interface. A three line microprocessor interface port which is used to clock in data serially. The three lines are clock, data, and a control line which enables entry of the data. Some serial ports are bidirectional.

Sidetone Rejection – The rejection (in dB) of the reflected signal in the receive path resulting from a transmit signal applied to the phone, and phone line.

SLIC – Subscriber Line Interface Circuit. It is the circuitry within the CO or PBX which connects to the user's phone line.

Subscriber – The customer at the telephone end of the line.

Subscriber Line – The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

Tip – One of the two wires connecting the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

Transmit Path – Within the telephone it is the speech path from the microphone towards the phone line (Tip and Ring).

Two Wire Circuit – Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

Two–to–Four Wire Converter – A circuit which has four wires (on one side) – two (signal and ground) for the outgoing signal, and two for the incoming signal. The outgoing signal is sent out differentially on the two wire side, and incoming differential signals received on the two wire side are directed to the receive path of the four wire side. Additional circuit within cancels the reflected outgoing signal to keep it separate from the incoming signal.

Voiceband – That portion of the audio frequency range used for transmission across the telephone system. Typically it is 300–3400 Hz.

Suggested Vendors

Microphones

Primo Microphones Inc.
Bensenville, IL 60106
1–800–76–PRIMO

Telecom Transformers

Microtran Co., Inc.
Valley Stream, NY 11528
516–561–6050
(Ask for Application Bulletin F232)

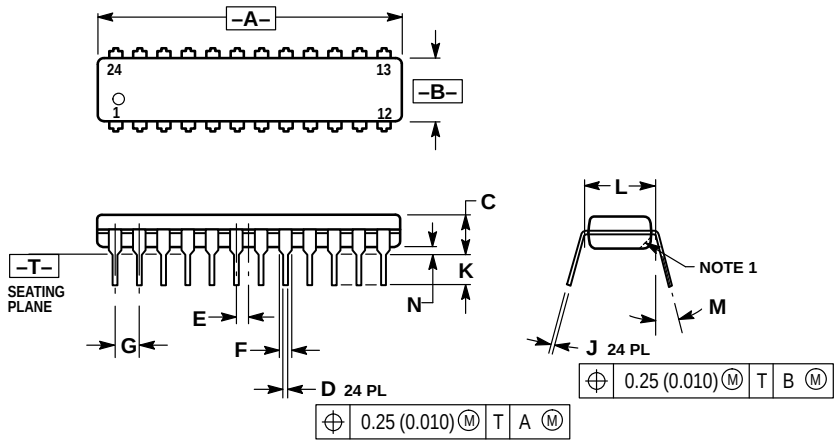
PREM Magnetics, Inc.
McHenry, IL 60050
815–385–2700

Stancor Products
Logansport, IN 46947
219–722–2244

Motorola does not endorse or warrant the suppliers referenced.

OUTLINE DIMENSIONS

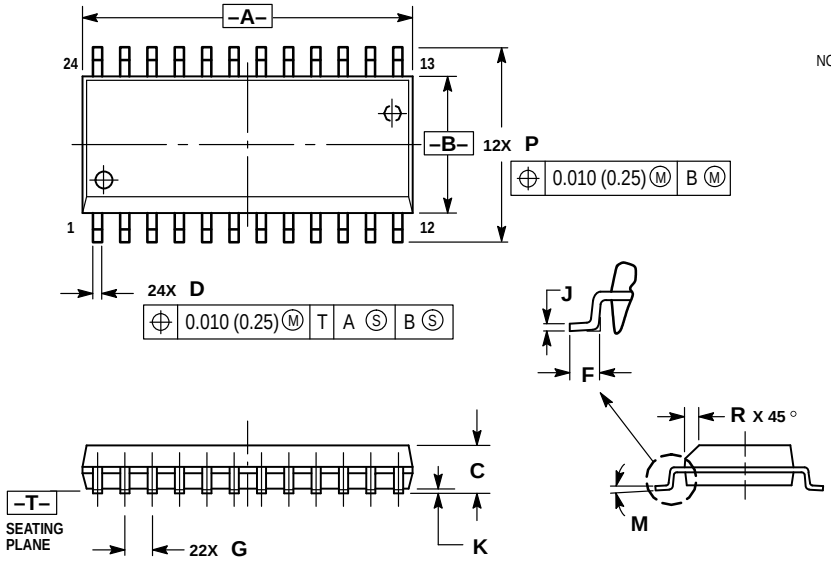
P SUFFIX
PLASTIC PACKAGE
CASE 724–03
ISSUE D



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC PACKAGE
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
– US & Canada ONLY 1–800–774–1848

INTERNET: http://motorola.com/sps

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 4–32–1,
Nishi–Gotanda, Shinagawa–ku, Tokyo 141, Japan. 81–3–5487–8488

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298