Order Number: MC33253/D
Rev 3, 03/2001

MOTOROLA

Advance Information

Full Bridge Pre-Driver

MC33253

55 VOLTS

SEMICONDUCTOR TECHNICAL DATA

The MC33253 is a full bridge driver including integrated charge pump, two independent high and low side driver channels.

The high and low side drivers include a cross conduction suppression circuit, which, if enabled, prevents the external power FETs from being on at the same time.

The drive outputs are capable to source and sink 1 A pulse peak current. The low side channel is referenced to ground, the high side channel is floating above ground.

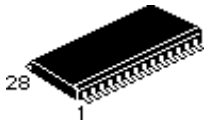
A linear regulator provides a maximum of 15.5V to supply the low side gate driver stages. The high side driver stages are supplied with a 10V charge pump voltage. Such built-in feature, associated to external capacitor provides a full floating high side drive.

An under- and over-voltage protection prevents erratic system operation at abnormal supply voltages. Under fault, these functions force the driver stages into off state.

The logic inputs are compatible with standard CMOS or LSTTL outputs. The input hysteresis makes the output switching time independent of the input transition time.

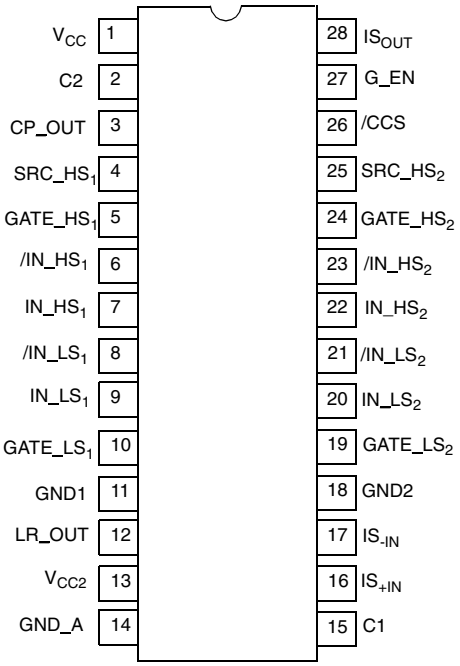
The global enable logic signal can be used to disable the charge pump and all the bias circuit. The net advantage is the reduction of the quiescent supply current to under 10µA. To wake up the circuit, 5 V has to be provided at G_EN. A built-in single supply operational amplifier could be used to feedback information from the output load to the external MCU.

- V_{CC} Operating Voltage Range from 5.5 V up to 55 V
- V_{CC2} Operating Voltage Range from 5.5 V up to 28 V
- Automotive Temperature Range -40°C to 125°C
- 1A Pulse Current Output Driver
- Fast PWM Capability
- Built-In Charge Pump
- Cross Conduction Suppression Circuit



DW SUFFIX
PLASTIC PACKAGE
CASE 751F-05

PIN CONNECTIONS
(TOP VIEW)
CASE 751F-05

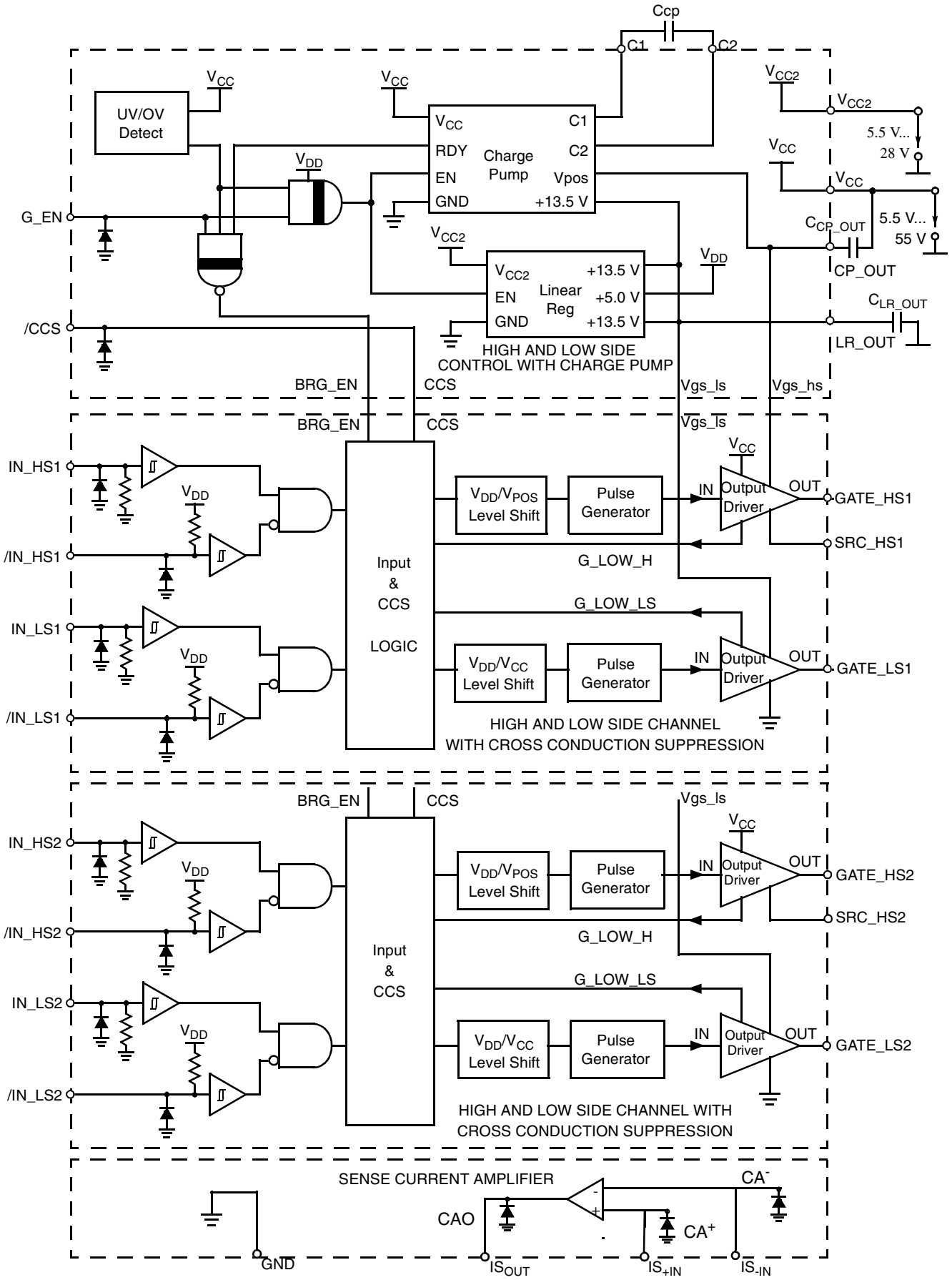


ORDERING INFORMATION

Device	Temperature Range	Package
PC33253DW	-40°C to +125°C	SOIC28

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Figure 1. Principal Building Blocks



JTE MAXIMUM RATINGS Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND.

Rating	Symbol	Min	Max	Unit
Supply Voltage1	V_{CC}	-0.3	65	V
Supply Voltage2 (NOTE 1)	V_{CC2}	-0.3	35	V
Linear Regulator Output Voltage	V_{LR_out}	-0.3	18	V
High Side Floating Supply Absolute Voltage	V_{CP_OUT}	-0.3	65	V
High Side Floating Source Voltage	V_{SRC_HS}	-0.3	65	V
High Side Gate Voltage	V_{GATE_HS}	-0.3	65	V
High Side Gate Source Voltage	V_{GATE_HS} - V_{SRC_HS}	-0.3	20	V
High Side Source Current from Cpout in Switch On State	I_S		250	mA
High Side Floating Supply Gate Voltage	V_{CP_OUT} - V_{GATE_HS}	-0.3	65	V
Low Side Output Voltage	V_{GATE_LS}	-0.3	17	V
Wake up Voltage	V_{G_EN}	-0.3	35	V
Logic Input Voltage	V_{IN}	-0.3	10	V
Charge Pump Capacitor Voltage	V_{C1}	-0.3	V_{LR_OUT}	V
Charge Pump Capacitor Voltage	V_{C2}	-0.3	65	V
Operational Amplifier Output Voltage	V_{CAO}	-0.3	7	V
Operational Amplifier Inverting Input Voltage	V_{CA}^-	-0.3	7	V
Operational Amplifier Non Inverting Input Voltage	V_{CA}^+	-0.3	7	V
ESD Voltage on any Pins (HBM, 100pF, 1.5kOhms)	V_{ESD}	-2.0	2.0	kV
Power Dissipation and Thermal Characteristics				
Maximum Power Dissipation@25°C	P_D		2	W
Thermal Resistance Junction-to-Air	$R_{\theta JA}$		60	°C/W
Operating Junction Temperature	T_J	-40	+150	°C
Storage Temperature	T_{stg}	-65	+150	°C

OPERATING CONDITIONS Typical values for T_A = 25°C, Min/Max values for T_A = -40°C to +125°C

Rating	Symbol	Min	Max	Unit
Supply Voltage1	V_{CC}	5.5	55	V
Supply Voltage2	V_{CC2}	5.5	28	V
High Side Floating Supply Absolute Voltage	V_{CP_OUT}	V_{CC}+4	V_{CC}+11but<65	V

NOTE1: VCC can sustain load dump pulse 40V, 400ms, 2Ohms

ELECTRICAL CHARACTERISTICS V_{CC} = 12 V, V_{CC2} = 12 V, C_{CP} = 33 nF, G_EN = 4.5 V unless otherwise specified.
Typical values for TA = 25°C, Min/Max values for TA = -40°C to +125°C, unless otherwise specified.

Characteristics	Pin #	Symbol	Min	Typ	Max	Unit
LOGIC SECTION						
Logic "1" Input Voltage (IN_LS & IN_HS)	7, 9, 20, 22	V_{IH}	2.0		10	V
Logic "0" Input Voltage (IN_LS & IN_HS)		V_{IL}			0.8	V
Logic "1" Input Current Vin=5V	7, 9, 20, 22	I_{in+}	200		1000	uA
Logic "0" Input Current Vin=0V		I_{in-}	200		1000	uA
Logic "0" Input Voltage (/IN_LS & /IN_HS&/CCS)	6, 8, 21, 23, 26	V_{IH}	2.0		10	V
Logic "1" Input Voltage (/IN_LS & /IN_HS&/CCS)		V_{IL}			0.8	V
Logic "0" Input Current Vin=5V	6, 8, 21, 23, 26	I_{in+}	TBD		TBD	uA
Logic "1" Input Current Vin=0V		I_{in-}	TBD		TBD	uA
Wake Up Input Voltage (G_EN)	27	V_{G_EN}	4.5	5.0	V_{CC2}	V
Wake Up Current (G_EN) VG_EN = 14 V	27	I_{G_EN}		200	500	uA
LINEAR REGULATOR SECTION						
Linear Regulator V_{LR_OUT} @ V_{CC2} from 16.5 to 28 V, I_{LOAD} from 0mA to 20mA	12	V_{LR_OUT}	13.5		16.5	V
Linear Regulator V_{LR_OUT} @ V_{CC2} =12 V, I_{LOAD} = 20mA	12	V_{LR_OUT}	V_{CC2} - 1.5			V
V_{LR_OUT} @ V_{CC2} =5.5V, I_{LOAD} =TBD, V_{CC} = 5.5V	12			TBD		V
CHARGE PUMP SECTION						
Charge Pump Output Voltage, referenced to V_{CC} I_{LOAD} = 0mA, C_{Cpout}=1uF	3	V_{CP_OUT}	V_{LR_OUT} - 2			V
Charge Pump Output Voltage, referenced to V_{CC} I_{LOAD} = 7mA, C_{Cpout}=1uF	3	V_{CP_OUT}	V_{LR_OUT} -3			V
Charge Pump Output Voltage, referenced to V_{CC} V_{CC2} = V_{CC}=5.5V I_{LOAD} = 0mA, C_{Cpout}=1uF	3	V_{CP_OUT}	V_{LR_OUT} - TBD			V
Charge Pump Output Voltage, referenced to V_{CC} V_{CC2} = V_{CC}=5.5V I_{LOAD} = 7mA, C_{Cpout}=1uF	3	V_{CP_OUT}	V_{LR_OUT}- -TBD			V
Peak current through pin 15under rapid changing Vcc voltages (see Figure 6)	15	I_{C1}	-2.0		2.0	A
Minimum peak voltage at pin 15under rapid changing Vcc voltages (see Figure 6)	15	V_{C1}min	-1.5			V
SUPPLY VOLTAGE SECTION						
Quiescent Vcc Supply Current V_{G_EN}=0V	1				TBD	uA
Operating Vcc Supply Current (@V_{CC}=55V and V_{CC2}=28V) (@V_{CC}=12V and V_{CC2}=12V)	1 1				TBD TBD	mA mA
Quiescent Vcc2 Supply Current V_{G_EN}=0V	13				TBD	uA

Characteristics	Pin #	Symbol	Min	Typ	Max	Unit
Operating Vcc2 Supply Current (@V_{CC}=55V and V_{CC2}=28V) (@V_{CC}=12V and V_{CC2}=12V) Logic pin inactive (high impedance)	13 13				10 8	mA
Under Voltage Shutdown V_{CC2} (Note2)	13	UV2	4.6	5.1	5.5	V
Under Voltage Shutdown V_{CC}	1	UV	4.6	5.1	5.5	V
Over Voltage Shutdown V_{CC}	1	OV	57	61	64	V
Over Voltage Shutdown V_{CC2}	13	OV2	29.5	31	32.5	V
OUTPUT SECTION						
Output Sink Resistance (Turned off) V_{GATE_HS} - V_{SRC_HS} =1V	3, 4, 5, 10, 19, 24, 25	R_{DS}			22.0	Ohms
Output Source Resistance (Turned on) V_{CP_OUT} - V_{GATE_HS} =0.1V		R_{DS}			22.0	Ohms
High Side Source Current from Cpout in Switch On State	4, 25	$I_S$max			200	mA
Max Voltage (V_{GATE_HS} - V_{SRC_HS}), INH=1, I_{Smax}=200mA	4, 5, 24, 25				18	V
SENSE CURRENT AMPLIFIER SECTION (Internal VCC supply @ 12V)						
Output Dynamic Range ($I_{sink/source}$ = 200µA)	28	V_{OH} V_{OL}	4.7	5.0	 300	V mV
Open Loop Gain (at 25°C)		A		50		dB
Input Bias Current	16, 17	I_{IB}			1.0	uA
Input Offset Voltage (at 25°C)		V_{io}	-5.0	2.0	5.0	mV
Input Common Mode Voltage Range		ICMR	0		5	V
Common Mode Rejection Ratio		CMRR		70		dB
Sink Capability (Vo>1.1V) (Note 3)	28	I_{sink}	2.0	3.0		mA
Source Capability (Vo<5V) (Note 3)	28	I_{source}	2.0	3.0		mA
Gain Bandwidth Product		GBW		1.8		MHz
Operational Amplifier Output Voltage, $I_{sink=500uA}$	28	V_{CAO}			0.5	V
Operational Amplifier Output Voltage, $I_{source=500uA}$	28	V_{CAO}	5			V
Operational Amplifier Slew Rate (+)		SR+		1		V/us
Operational Amplifier Slew Rate (-)		SR-		1		V/us

DYNAMIC ELECTRICAL CHARACTERISTICS V_{CC} = 12 V, V_{CC2} = 12 V, C_{CP} = 33 nF, G_EN = 4.5 V unless otherwise specified.
Typical values for TA = 25°C, Min/Max values for TA = -40°C to +125°C, unless otherwise specified.

Characteristics	Pin #	Symbol	Min	Typ	Max	Unit
Prop. Delay HS and LS, C_{load}=5nF; Between 50% Input to 50% Output (see Figure 2)	5, 6, 7, 8, 9, 20, 21, 22, 23	t_{PD}		200	300	ns
Turn On Rise Time, C_{load}=5nF ; 10% to 90% (NOTE 4) (see Figure 2)	5, 10, 19, 24	t_r		80	180	ns
Turn Off Fall Time, C_{load}=5nF ; 10% to 90% (NOTE 4) (see Figure 2)		t_f		80	180	ns

NOTE 2: Between 4.6V and 5.5V, the device has been a non erroneous behaviour.
NOTE 3: Input overdrive 1V
NOTE 4: Rise time is given by time needed to charge the gate from 1V to 10V (Vice versa for fall time)

NOTE : C_{load} corresponds to a capacitor between GATE_HS and SRC_HS for the high side and between GATE_LS and ground for low side.

N.B.

In some applications a large dV/dt at Pin 2 (C2) due to sudden changes at V_{CC} can cause a large peak currents flowing through Pin15 (C1).

Positive transitions at Pin2 (C2) ;mimimum peak current :
I_{c1}min = 2.0A
t_{c1}min = 600ns (see for peak description)

Negative transitions at Pin2 (C2); maximum peak current :
I_{c1}max = 2.0A
t_{c1}max = 600ns (see for peak description)

Current sourced by Pin 15 (C1) during a large dV/dt will result in a negative voltage at Pin 15; negative transitions at Pin2(C2); minimum peak voltage:

V_{c1}min = -1.5V
t_{c1}max = 600ns (see for peak description)

Figure 2. Limits of C1 Current&Voltage with Large ValuesdV/dt of Vcc

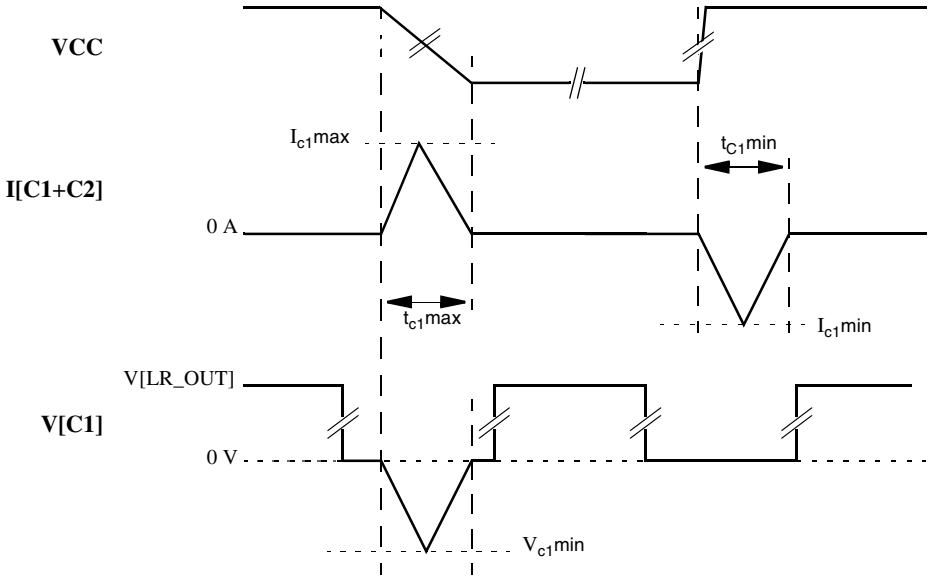
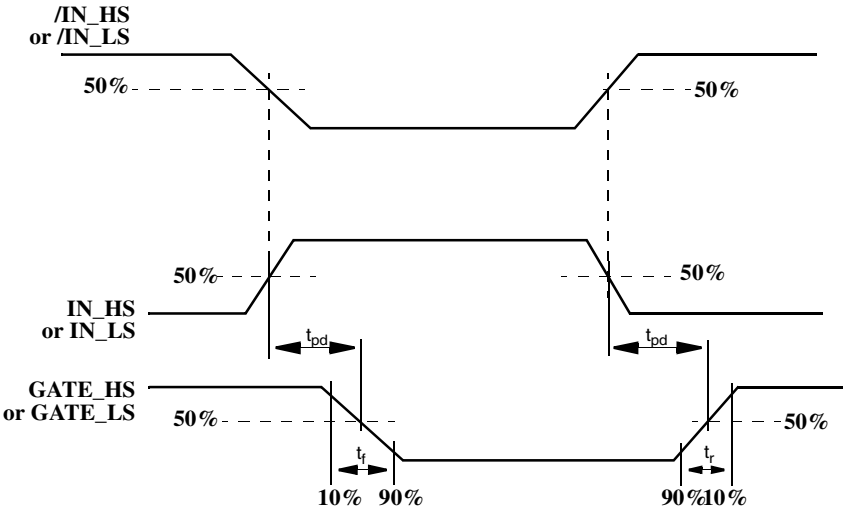


Figure 3. Dynamic Characteristics



Driver Characteristics

Turn-On

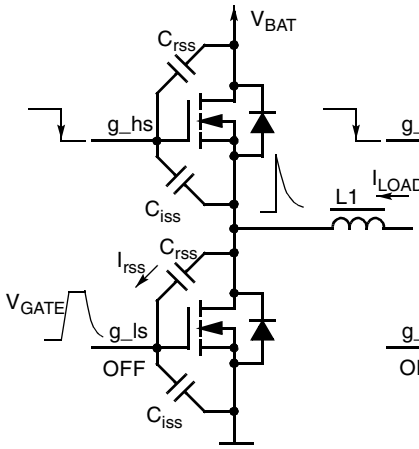
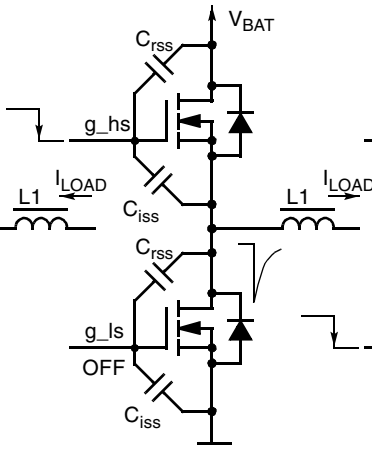
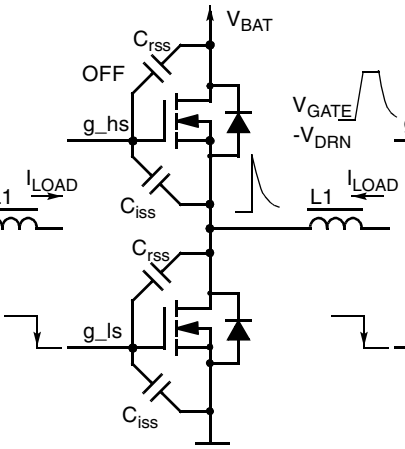
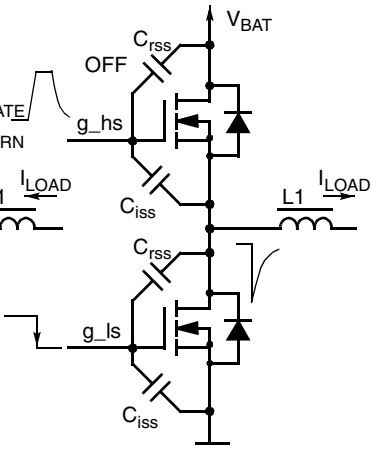
For turn-on the current required to charge the gate source capacitor Ciss in the specified time can be calculated as follows: Peak Current for Rise/Fall Time (tr) and a typical PowerMosFET Gate Charge Qg. IP = Qg/tr = 75 nC/80 ns ª 1.0 A

Turn-Off

The peak current for turn-off can be obtained in the same way as for turn-on. In addition to the dynamic current, required to turn-off or turn-on the FET, various application related switching scenarios have to be considered:

The output driver sources a peak current of up to 1A for 200 ns to turn on the gate. After 200 ns 100 mA are provided continuously to maintain the gate charged. The output driver sinks a peak current of up to 1A for 200 ns to turn off the gate. After 200 ns 100 mA are sinked continuously to maintain the gate discharged. In order to withstand high dV/dt spikes a low resistive path between gate and source is implemented during the off state.

Figure 4. OFF-State Driver Requirement

Flyback Spike charge LS-Gate via C_{rss} Charge Current I_{rss} up to 2.0 A! Uncontrolled Turn-On of Low Side FET	Flyback Spike pull down HS-Drain V_{GS} Increase Delayed Turn-Off of High Side FET	Flyback Spike charge LS-Gate via C_{rss} Charge Current I_{rss} up to 2.0 A! Delayed Turn-Off of Low Side FET	Flyback Spike pull down HS-Drain V_{GS} Increase Uncontrolled Turn-On of High Side FET
			
Driver Requirement: Low Resistive Gate-Source Path during OFF-State	Driver Requirement: Low Resistive Gate Source Path during OFF-State. High Peak Sink Current Capab.	Driver Requirement: High Peak Sink Current Capab.	Driver Requirement: Low Resistive Gate-Source Path during OFF-State

Driver Supply

The High Side Driver is supplied from the internal charge pump buffered at CP_OUT. The low-drop regulator provides approx. 3.5 mA (f_{PWM} = 50kHz) per gate. In case of the full bridge that means approximately. 14 mA; 7.0 mA for the high side and 7.0 mA for the low side. (Note: The average current required to switch a gate with a frequency of 100kHz is: Average Current (Charge Pump) for PWM Frq. (f_{PWM}) and $I_{CP} = Q_g * f_{PWM} = 75\,nC * 100\,kHz = 7.5mA$. A full bridge application switch only one high side and one low side at the same time.)

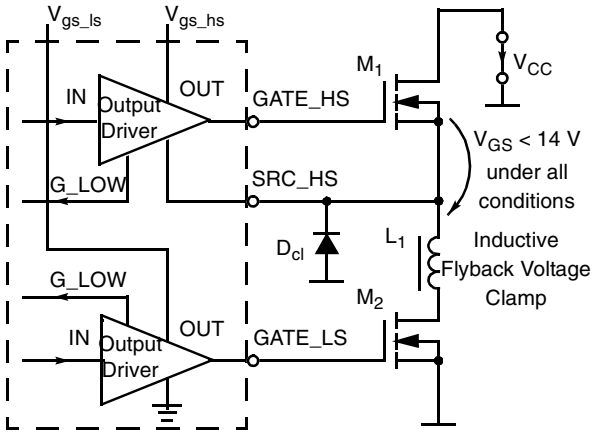
External capacitors on Charge Pump and on Linear Regulator are necessary to supply high peak current absorbed during switching. The Low Side Driver is supplied from built in low drop regulator.

Gate Protection

The low side gate is protected by the internal linear regulator, which guarantees that V_{GATE_LS} does not exceed the maximum V_{GS}. Especially when working with the charge pump the voltage at POS_HS can be up to 65V. The high side gate is clamped internally, in order to avoid a V_{GS} exceeding 14V.

The Gate protection does not include a Flyback Voltage Clamp that protects the driver and the external FET from a Flyback voltage that can appear when driving inductive load.This Flyback voltage can reach high negative voltage values and needs to be clamped externally.

Figure 5. Gate Protection and Flyback Voltage Clamp



TMOS Failure Protection

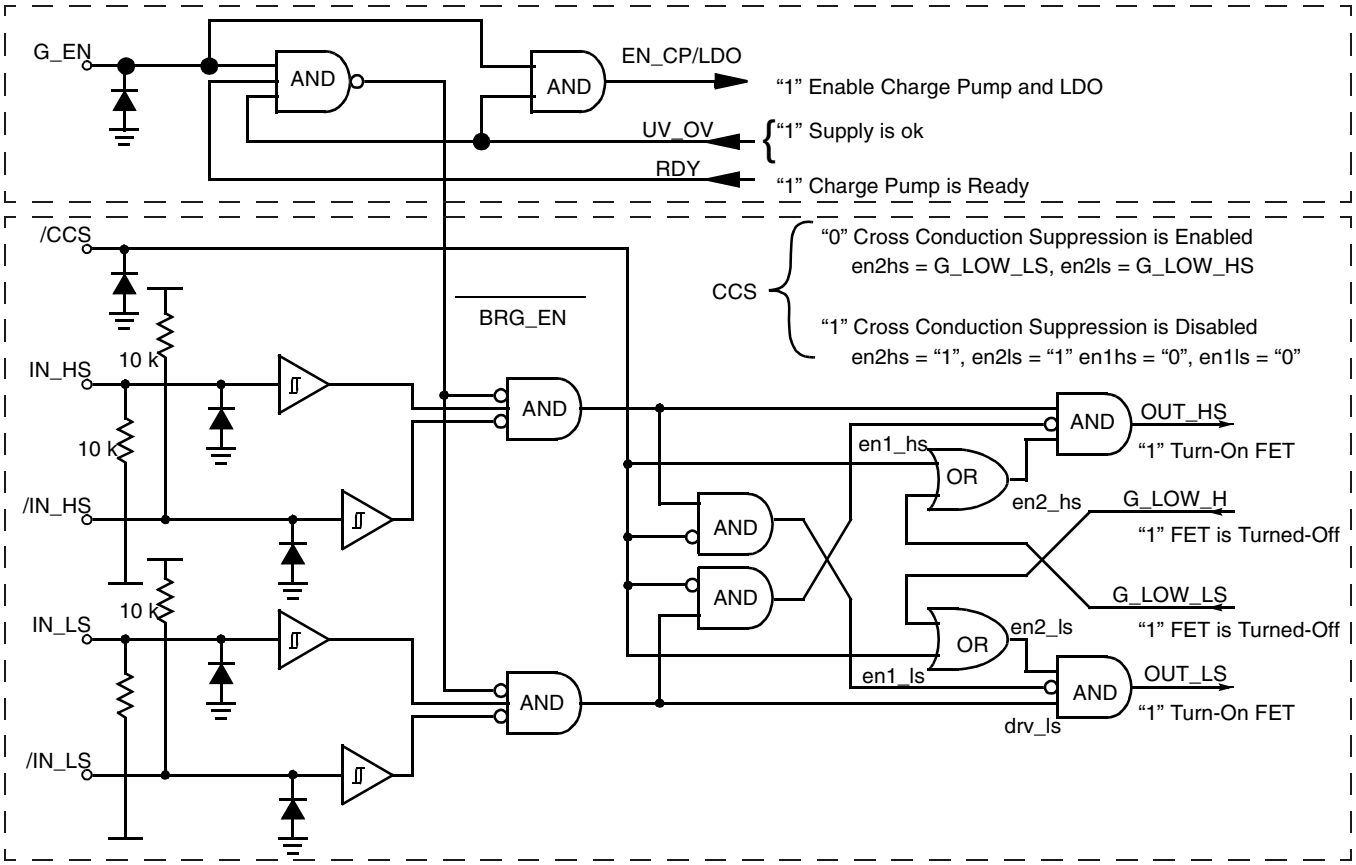
All output driver stages are protected against TMOS failure conditions. If one of the external power FETs is destroyed (Gate = V_{CC}, or Gate = Gnd) the function of the remaining output driver stages is not affected. All output drivers are short circuit protected against short circuits to ground.

Cross Conduction Suppression

The purpose of the cross conduction suppression is to avoid that high and low side FET are turned on at the same time, which prevents the half bridge power FETs of a shoot-through condition. The CCS can be disabled / enabled by an external signal (/CCS).

- /CCS=0, the cross conduction is not allowed.
- /CCS=1, the cross conduction is allowed.

Figure 6. Input Logic and Cross Conduction Suppression



Logic Inputs

Logic Input Voltage Range:
Absolute Max :
-0.3 V ... 10 V
Wake Up Function:
(G_EN)
4.5 V ... V_{CC2}
During Wake-Up the logic is supplied from the G_EN pin.

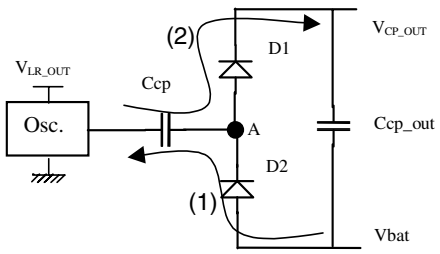
Low Drop Linear Regulator

The low drop linear regulator provides the 5.0 V for the logic section of the driver, the V_{gs_ls} buffered at LR_OUT and the +13.5 V for the charge pump, which generates the V_{gs_hs}. The low drop linear regulator provides 3.5 mA average current per driver stage. If typically V_{CC2} exceeds 14.5V the output is limited to 14V.

Charge Pump

The charge pump generates the high side driver supply voltage (V_{gs_hs}), buffered at C_{CP_OUT}. The basic circuit (Fig 7), shows charge pump without load:

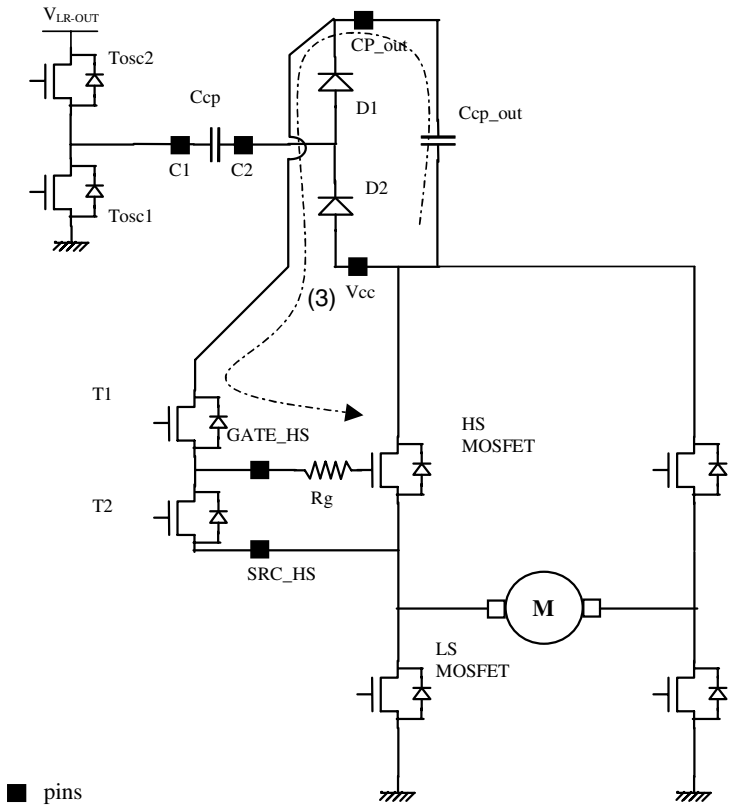
Figure 7. Charge Pump Basic Circuit



When the oscillator is in low state (1), C_{cp} is charged through D2 until its voltage reaches V_{bat}-V_{d2}. When the oscillator is in high state (2), C_{cp} is discharged though D1 in C_{cp_out}, and final voltage of the charge pump, V_{cp_out} is V_{bat}+V_{LR_OUT} - 2V_d. The frequency of the MC33253 oscillator is about 330 kHz.

The Figure 8 represents a simplified circuitry of the high side gate driver.

Figure 8. High Side Gate Driver

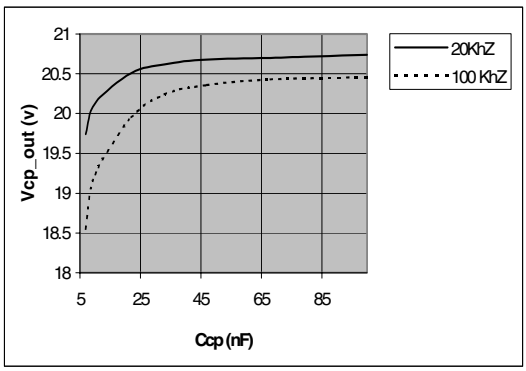


The transistors Tosc1 and Tosc2 are the oscillator switching MOSFETs. When Tosc1 is on, the oscillator is at low level. When Tosc2 is on, the oscillator is at high level. The high side MOSFET predriver is composed of two transistors T1 and T2. When T1 is on the HS MOSFET is turn on, when T2 is on the HS MOSFET is off. The capacitor C_{cp_out} provides peak current to the HS MOSFET through T1 during turn on (3) as shown in figure 11.

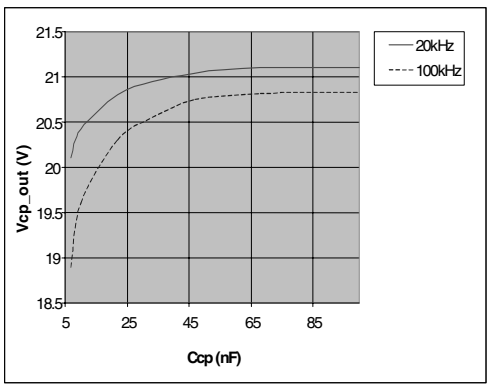
C_{cp}

C_{cp} choice depends on Power MOSFET characteristics and the working switching frequency. The following diagrams show the influence of C_{cp} value on V_{cp_out} average voltage level. The diagrams are given at two different frequencies for two power MOSFETs (MTP60N06HD and MPT36N06V).

Figure 9. V_{cp_out} Versus C_{cp}



MTP60N06HD (Q_g=50nC)



MTP36N06V (Q_g=40nC)

Figure 10.

The smaller C_{cp} value is, the smaller V_{cp_out} value is. Moreover, for a same C_{cp} value, when the switching frequency increases, the average V_{cp_out} level decreases. For most of the applications a typical value of 33nF is recommended.

C_{cp_out}

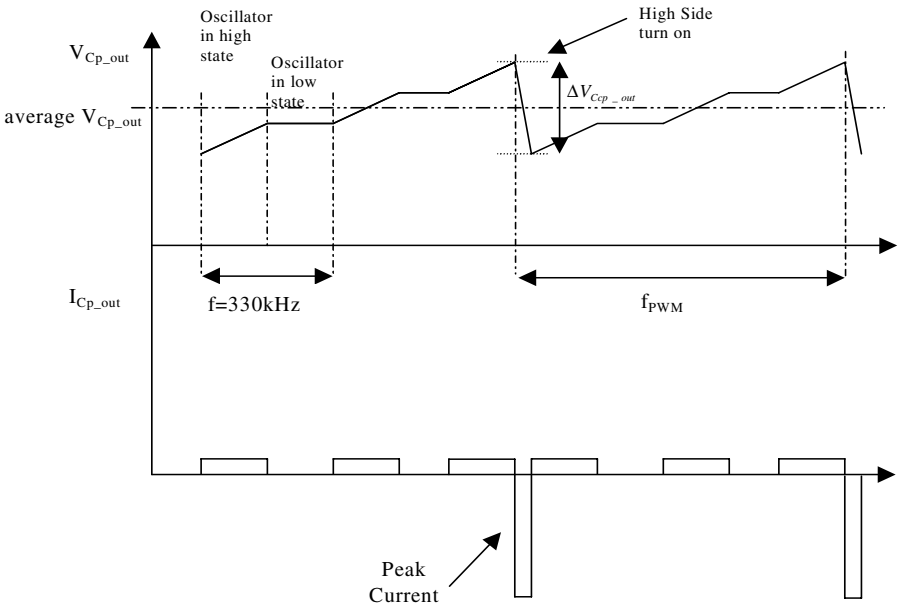
As shown in figure 11, at high side MOSFET turn on, V_{cp_out} voltage decreases. This decrease can be calculated according to C_{cp_out} value as following :

$$\Delta V_{Ccp\_out} = \frac{Q_g}{C_{cp\_out}}$$

Q_g : Power MosFET Gate Charge

The following figure is the simplified C_{cp_out} current and voltage waveforms.
f_{pwm} : working switching frequency

Figure 11. Simplified C_{cp_out} Current and Voltage Waveforms



C_{LR_OUT}

C_{LR_OUT} provides peak current needed by the low side MOSFET turn on. V_{LR_OUT} decreasing is as follow:

$$\Delta V_{LR\_out} = \frac{Q_g}{C_{LR\_out}}$$

Capacitors typical values

In most working cases the following typical values are advised for a good charge pump performing:
C_{cp}=33nF, C_{cp_out}=470nF and C_{LR_OUT}=470nF.
These values give a typical 100mV voltage ripple on V_{cp_out} and V_{LR_OUT} with Q_g=50nC.

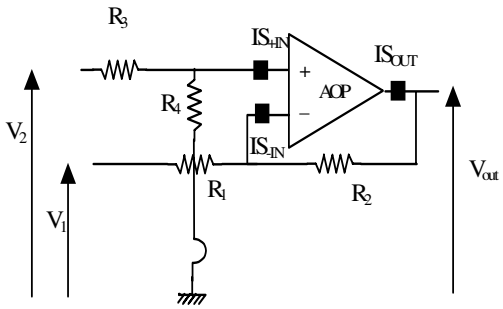
OP-Amp

The built-in A.O.P. available in the MC33253 allows to get a voltage image of the H-bridge current. This voltage can be provided by a shunt resistor, as shown in figure 13.

Typically shunt resistivity is dimensioned as low as possible (25mOhm/10A). The maximum A.O.P output voltage is 5V. Therefore a gain of 10 sets the maximum drop voltage on the sensing resistance at 500mV.

A differential mode is advised as shown in fig 12:

Figure 12. : Differential A.O.P



with R2=R4 and R1=R3, $V_{out} = \frac{R2}{R1}(V2 - V1)$

A gain of 10 gives $\frac{R2}{R1} = 10$ (a)

To minimize the perturbations, impedance seen by the A.O.P inputs may be as low as possible.
Knowing the maximum output current (2mA), the minimum value of (R1+R2) can be deduced when V_{OUT} maximum is 5V:

$$(R_1 + R_2)_{\min} = \frac{5V}{2mA} = 2{,}5k \quad (b)$$

with (a) and (b), the minimum values of R1, R2, R3 and R4 can be calculated.

R1=R3=227 Ohms and R2=R4=2.27 kOhms

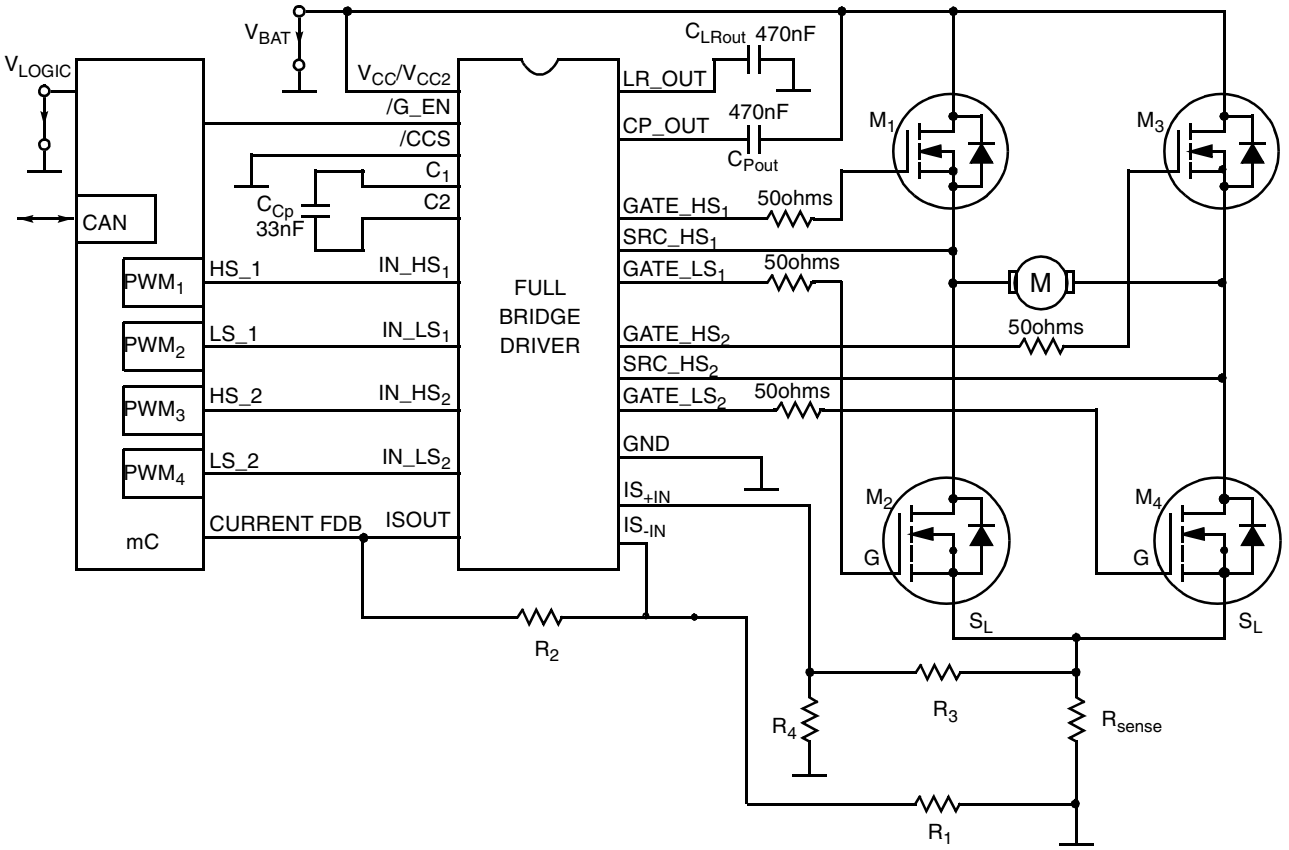
Over/Under Voltage Shutdown

The under voltage protection becomes active at V_{CC} below 5.5 V and the overvoltage protection is activated at V_{CC} above 55 V or at V_{CC2} above 28 V. If the O/UV protection is activated the outputs are driven low, in order to switch off the FETs.

Protection

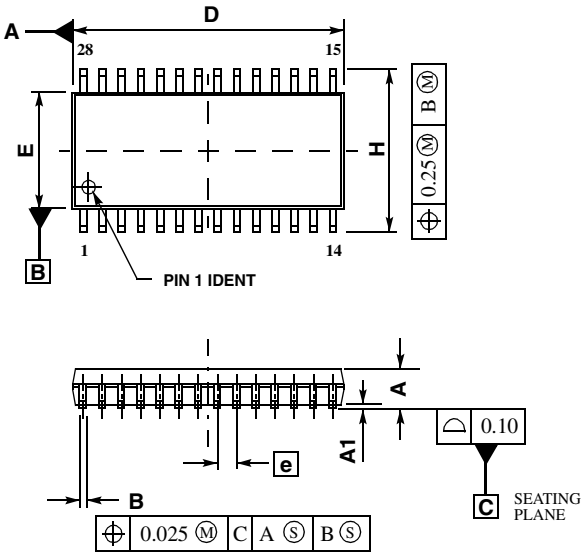
A protection against double battery and load dump spikes up to 55 V is given by V_{CC} = 55 V. A protection against reverse polarity is given by the external power FET with the free wheeling diodes, forming a conducting pass from ground to V_{CC}. An additional protection is not provided within the circuit. There is a temperature shut down protection per each half bridge. It protects the circuitry against temperature damage by blocking the output drives.

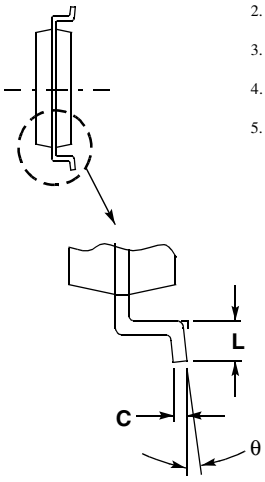
Figure 13. DC Motor Control with Microcontroller



This application use the internal charge pump to provide the high side floating voltage. This voltage can be provided by an external source also.

Pin	Symbol	Pin Description
1	V_{CC}	Supply1
2	C2	Charge Pump Capacitor
3	CP_OUT	Charge Pump Out
4	SRC_HS1	Source 1 Output High Side
5	GATE_HS1	Gate 1 Output High Side
6	/IN_HS1	Neg. Input High Side 1
7	IN_HS1	Pos. Input High Side 1
8	/IN_LS1	Neg. Input Low Side 1
9	IN_LS1	Pos. Input Low Side 1
10	GATE_LS1	Gate 1 Output Low Side
11	GND1	Power Ground
12	LR_OUT	Linear Regulator Output
13	V_{CC2}	Supply 2
14	GND_A	Analog Ground (A.O.P)
15	C1	Charge Pump Capacitor
16	IS+	Sense OpAmp Pos. Input
17	IS-	Sense OpAmp Neg. Input
18	GND2	Logic Ground 2
19	GATE_LS2	Gate 2 Output Low Side
20	IN_LS2	Pos. Input Low Side 2
21	/IN_LS2	Neg. Input Low Side 2
22	IN_HS2	Pos. Input High Side 2
23	/IN_HS2	Neg. Input High Side 2
24	GATE_HS2	Gate 2 Output High Side
25	SRC_HS2	Source 2 Output High Side
26	/CCS	Enable Cross Conduction Suppression
27	G_EN	Global Enable
28	IS_OUT	Sense Current OpAmp Output





NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
4. MAXIMUM MOLD PROTRUSION 0.015 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
θ	0°	8°

CASE 751F-05
ISSUE F

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