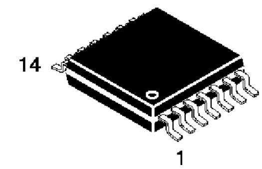
Order Number: MC33492/D
Rev. 3.3, 06/2001

Preliminary

PLL Tuned UHF Transmitter for Data Transfer Applications

- Switchable frequency bands 315-434MHz and 868MHz
- OOK modulation
- Adjustable output power range
- Fully integrated VCO
- Supply voltage range: 1.9-3.6V
- Very low standby current: 0.1nA @ T_A=25°C
- Low supply voltage shutdown
- Data clock output for microcontroller
- Extended temperature range: -40°C to 125°C
- Low external component count
- Typical application compliant with ETSI standard

TANGO3
MC33492



TSSOP–14
DTB SUFFIX
CASE 948G

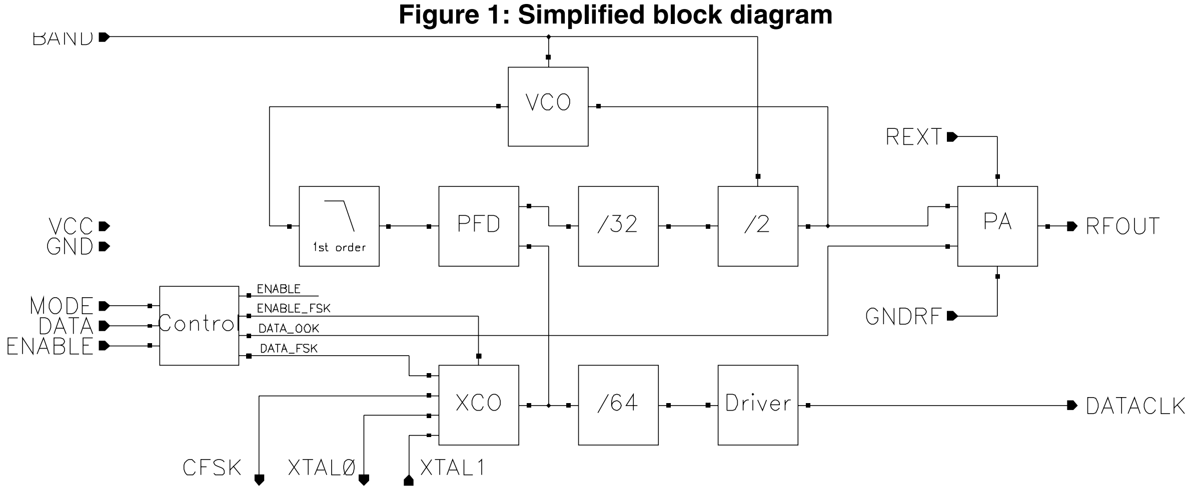
PIN CONNECTIONS

DATACLK	1	14	MODE
DATA	2	13	ENABLE
BAND	3	12	VCC
GND	4	11	GNDRF
XTAL1	5	10	RFOUT
XTAL0	6	9	VCC
REXT	7	8	CFSK

Ordering Information

Device	Ambiant Temperature Range	Package
MC33492 DTB	-40°C to 125°C	TSSOP14

Figure 1: Simplified block diagram



This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	DATACLK	Clock output to the microcontroller
2	DATA	Data input
3	BAND	Frequency band selection
4	GND	Ground
5	XTAL1	Reference oscillator input
6	XTAL0	Reference oscillator output
7	REXT	Power amplifier output current setting input
8	CFSK	Non connected
9	VCC	Power supply
10	RFOUT	Power amplifier output
11	GNDRF	Power amplifier ground
12	VCC	Power supply
13	ENABLE	Enable input
14	MODE	Modulation type selection input

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	V_{GND} - 0.3 to 3.7	V
Voltage Allowed on Each Pin		V_{GND} - 0.3 to V_{CC} + 0.3	V
ESD HBM Voltage Capability on Each Pin (note 1)		±2000	V
ESD MM Voltage Capability on Each Pin (note 2)		±150	V
Solder Heat Resistance Test (10 s)		260	°C
Storage Temperature	Ts	-65 to +150	°C
Junction Temperature	Tj	+150	°C

Notes:
1 Human Body model, AEC-Q100-002 Rev. C.
2 Machine Model, AEC-Q100-003 Rev. D.

TRANSMITTER FUNCTIONAL DESCRIPTION

MC33492 is a PLL tuned low power UHF transmitter. The different modes of operation are controlled by the microcontroller through several digital input pins. The power supply voltage ranges from 1.9V to 3.6V allowing operation with a single lithium cell.

PHASE LOCKED LOOP AND LOCAL OSCILLATOR

The VCO is a completely integrated relaxation oscillator. The Phase Frequency Detector (PFD) and the loop filter are fully integrated. The exact output frequency is equal to: $f_{RFOUT} = f_{XTAL}$ x PLL divider ratio. The frequency band of operation is selected through the BAND pin.

Table 1 provides details for each frequency band selection.

Table 1: Frequency band selection and associated divider ratios

BAND input level	Frequency band (MHz)	PLL divider ratio	Crystal oscillator frequency (MHz)
High	315	32	9.84
	434		13.56
Low	868	64	

An out-of-lock function is performed by monitoring the PFD output voltage. When it exceeds its limits, the RF output stage is disabled.

RF OUTPUT STAGE

The output stage is a single ended square wave switched current source. Harmonics will be present in the output current drive. Their radiated absolute level depends on the antenna characteristics and output power. Typical application demonstrates compliance to ETSI standard.

A resistor R_{ext} connected to the REXT pin controls the output power allowing a tradeoff between radiated power and current consumption.

The output voltage is internally clamped to $V_{cc} \pm 2V_{be}$ (typ. $V_{cc} \pm 1.5V$ @ T_A=25°C).

MODULATION

A low logic level has to be applied on pin MODE, to select the On Off Keying (OOK) modulation. This modulation is performed by switching on/off the RF output stage. The logic level applied on pin DATA controls the output stage state:

DATA=0 -> output stage off

DATA=1 -> output stage on

MICROCONTROLLER INTERFACE

Four digital input pins (ENABLE, DATA, BAND and MODE) enable the circuit to be controlled by a microcontroller. It is recommended to configure the band frequency and the modulation type before enabling the circuit. In a typical application the input pin MODE is hardwired to ground. To reduce total current consumption, it is recommended to connect pin BAND according to the following table 2.

Table 2: Digital pins connecting recommendation

434MHz Frequency band	BAND = I/O or ENABLE
868MHz Frequency band	BAND = GND

One digital output (DATACLK) provides to the microcontroller a reference frequency for data clocking. This frequency is equal to the crystal oscillator frequency divided by 64 (see table 3).

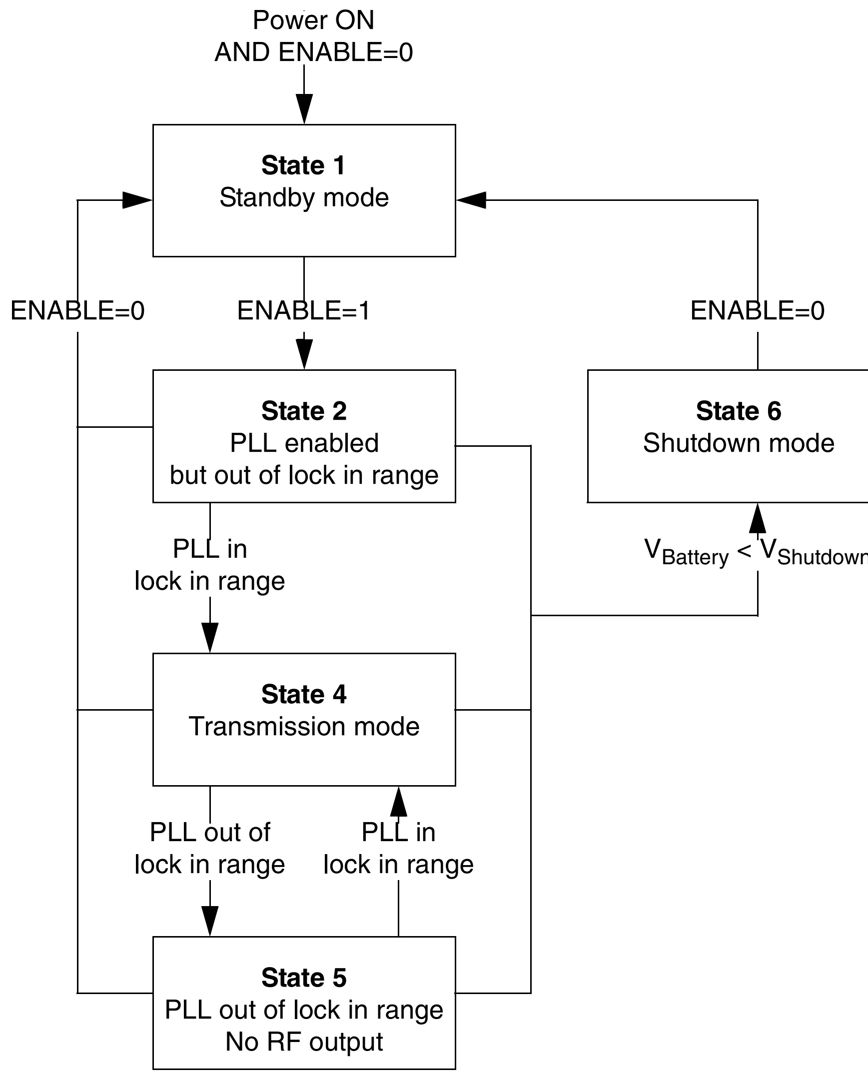
Table 3: DATACLK frequency versus crystal oscillator frequency

Crystal oscillator frequency (MHz)	DATACLK frequency (kHz)
9.84	154
13.56	212

STATE MACHINE

Figure 2 details the main state machine.

Figure 2: Main state machine



State 1:

The circuit is in standby mode and draws only a leakage current from the power supply.

State 2:

In this state, the PLL is enabled but out of the lock in range. Therefore the RF output stage is switched off preventing any data transmission. Data clock is available on pin DATACLK. In normal operation, this state is transitional.

State 4:

In this state, the PLL is within the lock in range.

If $t<t_{PLL\_lock\_in}$ then the PLL can still be in acquisition mode.

If $t \geq t_{PLL\_lock\_in}$ then the PLL is locked.

Data entered on pin DATA is output on pin RFOUT.

State 5:

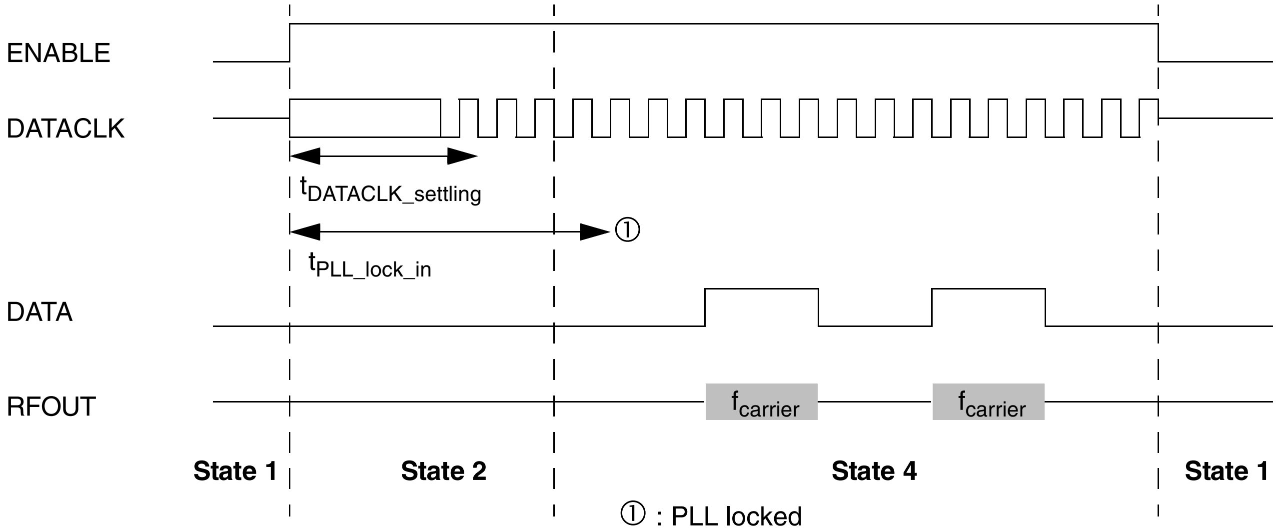
An out-of-lock condition has been detected. The RF output stage is switched off preventing any data transmission. Data clock is still available on pin DATACLK.

State 6:

When the supply voltage falls below the shutdown voltage threshold (V_{SDWN}), the whole circuit is switched off. Applying a low level on pin ENABLE is the only condition to get out of this state.

Figure 3 shows the waveforms of the main signals for a typical application cycle

Figure 3: Signals waveforms and timings definition



POWER MANAGEMENT

When the battery voltage falls below the shutdown voltage threshold (V_{SDWN}) the whole circuit is switched off. It has to be noted that after this shutdown, the circuit is latched until a low level is applied on pin ENABLE (see state 6 of the state machine).

DATA CLOCK

At start-up data clock timing is valid after the data clock settling time. As clock is switched off asynchronously the last period length cannot be guaranteed.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: V_{cc}=3V, R_{ext}=12kΩ, operating temperature range T_A=-40°C to +125°C, RF output frequency $f_{carrier}$=433.92MHz, reference frequency $f_{reference}$=13.56MHz, output load = 50Ω resistor (see figure 7). Values refer to the circuit shown in the recommended application schematic (see figure 10).
Typical values reflect average measurement at V_{CC}=3V and T_A=25°C.

	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	
1	**General Parameters**					
1.1	Supply Current in Standby Mode	T_A≤25°C	-	0.1	5	nA
1.2		T_A=60°C	-	7	30	nA
1.3		T_A=85°C	-	40	100	nA
1.4		T_A=125°C	-	800	1700	nA
1.7	Supply Current in Transmission Mode	315 & 434 bands, continuous wave, T_A=25°C	-	11.6	13.5	mA
1.5		315 & 434 bands, DATA=0, -40°C≤T_A≤125°C	-	4.4	6.0	mA
1.6		868MHz band, DATA=0, -40°C≤T_A≤125°C	-	4.6	6.2	mA
1.8		315 & 434 bands, continuous wave, -40°C≤T_A≤125°C	-	11.6	14.9	mA
1.9		868MHz band, continuous wave, -40°C≤T_A≤125°C	-	11.8	15.1	mA
1.10	Supply Voltage		-	3	3.6	V
1.11	Shutdown Voltage Threshold	T_A=-40°C	-	2.04	2.11	V
1.12		T_A=-20°C	-	1.99	2.06	V
1.13		T_A=25°C	-	1.86	1.95	V
1.14		T_A=60°C	-	1.76	1.84	V
1.15		T_A=85°C	-	1.68	1.78	V
1.16		T_A=125°C	-	1.56	1.67	V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: V_{cc}=3V, R_{ext}=12kΩ, operating temperature range T_A=-40°C to +125°C, RF output frequency $f_{carrier}$=433.92MHz, reference frequency $f_{reference}$=13.56MHz, output load = 50Ω resistor (see figure 7).
Values refer to the circuit shown in the recommended application schematic (see figure 10).
Typical values reflect average measurement at V_{CC}=3V and T_A=25°C.

	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	
2	**RF Parameters**					
2.1	R_{ext} value		12	-	21	kΩ
2.2	Output Power	315 & 434MHz bands, with 50Ω matching network	-	5	-	dBm
2.3		868MHz band, with 50Ω matching network	-	1	-	dBm
2.4		315 & 434MHz bands, -40°C≤T_A≤125°C	-3	0	3	dBm
2.8		868MHz band, -40°C≤T_A≤125°C	-7	-3	0	dBm
2.12	Current & Output Power Variation vs R_{ext} value	315 & 434MHz bands, with 50Ω matching network	-	-0.35	-	dB/kΩ mA/kΩ
2.13	Harmonic 2 Level	315 & 434MHz bands, with 50Ω matching network	-	-34	-	dBc
2.14		868MHz band, with 50Ω matching network	-	-49	-	dBc
2.15		315 & 434MHz bands	-	-23	-17	dBc
2.16		868MHz band	-	-38	-27	dBc
2.17	Harmonic 3 Level	315 & 434MHz bands, with 50Ω matching network	-	-32	-	dBc
2.18		868MHz band, with 50Ω matching network	-	-57	-	dBc
2.19		315 & 434MHz bands	-	-21	-15	dBc
2.20		868MHz band	-	-48	-39	dBc
2.21	Spurious Level @ $f_{carrier} \pm f_{DATACLK}$	315 & 434MHz bands	-	-36	-24	dBc
2.22		868MHz band	-	-29	-17	dBc
2.23	Spurious Level @ $f_{carrier} \pm f_{reference}$	315 MHz band	-	-37	-30	dBc
2.24		434MHz band	-	-44	-34	dBc
2.25		868MHz band	-	-37	-27	dBc
2.41	Spurious Level @ $f_{carrier}/2$	315MHz band	-	-62	-53	dBc
2.26		434MHz band	-	-80	-60	dBc
2.27		868MHz band	-	-45	-39	dBc
2.30	Phase Noise	315 & 434MHz bands, ±175kHz from $f_{carrier}$	-	-75	-68	dBc/Hz
2.31		868MHz band, ±175kHz from $f_{carrier}$	-	-73	-66	dBc/Hz
2.32	PLL Lock in Time, $t_{PLL\_lock\_in}$	$f_{carrier}$ within 30kHz from the final value, crystal series resistor=150Ω	-	350	1500	µs

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: V_{cc}=3V, R_{ext}=12kΩ, operating temperature range T_A=-40°C to +125°C, RF output frequency $f_{carrier}$=433.92MHz, reference frequency $f_{reference}$=13.56MHz, output load = 50Ω resistor (see figure 7).
Values refer to the circuit shown in the recommended application schematic (see figure 10).
Typical values reflect average measurement at V_{CC}=3V and T_A=25°C.

	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	
2.33	XTAL1 Input Capacitance		-	1	-	pF
2.34	Crystal Resistance		-	20	200	Ω
2.35	Modulation Depth		75	90	-	dBc
2.40	Data Rate	Manchester coded	-	-	10	kBd
2.41	Data to RF delay difference between falling and rising edges	From 50% of data edge to corresponding RF signal enveloppe edge (see note 1)	3	5	8	µs
Note 1: This parameter can have a slight impact on data duty cycle.						
3	**Microcontroller Interfaces**					
3.1	Input Low Voltage	Pins BAND, MODE, ENABLE, DATA	0	-	0.3 x V_{CC}	V
3.2	Input High Voltage	Pins BAND, MODE, ENABLE, DATA	0.7 x V_{CC}	-	V_{CC}	V
3.3	Input Hysteresis Voltage	Pins BAND, MODE, ENABLE, DATA	-	-	150	mV
3.4	Input Current	Pins BAND, MODE, DATA = 1	-	-	100	nA
3.5	ENABLE Pull Down Resistor		-	180	-	kΩ
3.6	DATACLK Output Low Voltage	C_{load} = 2pF	0	-	0.25 x V_{CC}	V
3.7	DATACLK Output High Voltage	C_{load} = 2pF	0.75 x V_{CC}	-	V_{CC}	V
3.8	DATACLK Rising Time	C_{load} = 2pF, measured from 20% to 80% of the voltage swing	-	250	500	ns
3.9	DATACLK Falling Time	C_{load} = 2pF, measured from 20% to 80% of the voltage swing	-	150	400	ns
3.10	DATACLK Settling Time, $t_{DATACLK\_settling}$	45% < Duty Cycle $f_{DATACLK}$ < 55%	-	800	1800	µs

RF OUTPUT SPECTRUM

Following are spectrums of transmitter carrier, measured in conduction. Three different spans have been used. The 5MHz span spectrum (figure 4) shows phase noise response close to the RF carrier, and the noise suppression within the PLL loop bandwidth. The 50MHz span spectrum (figure 5) shows both phase noise and reference spurious. Finally figure 6 shows second and third harmonics of carrier.

All these spectrums are measured in OOK modulation, at DATA=1.

Figure 4: RF spectrum at 434MHz frequency band displayed with a 5MHz span

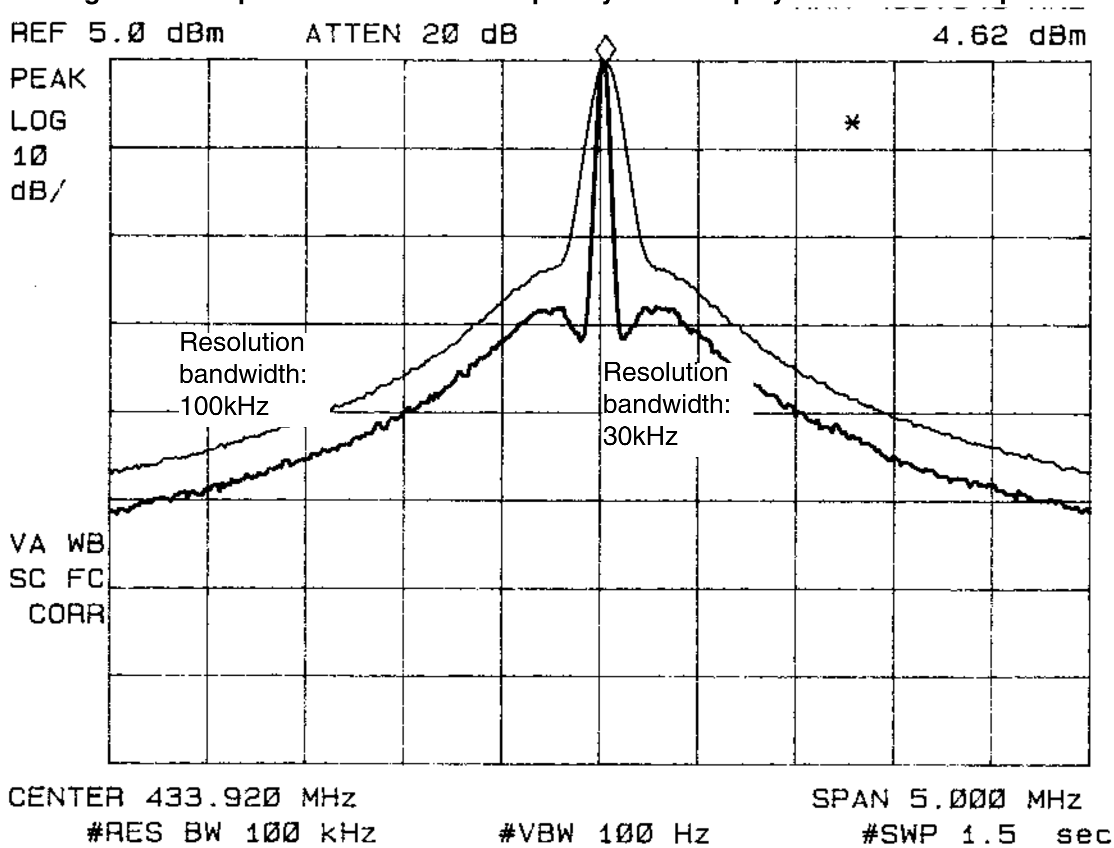


Figure 5: RF spectrum at 434MHz frequency band displayed with a 50MHz span

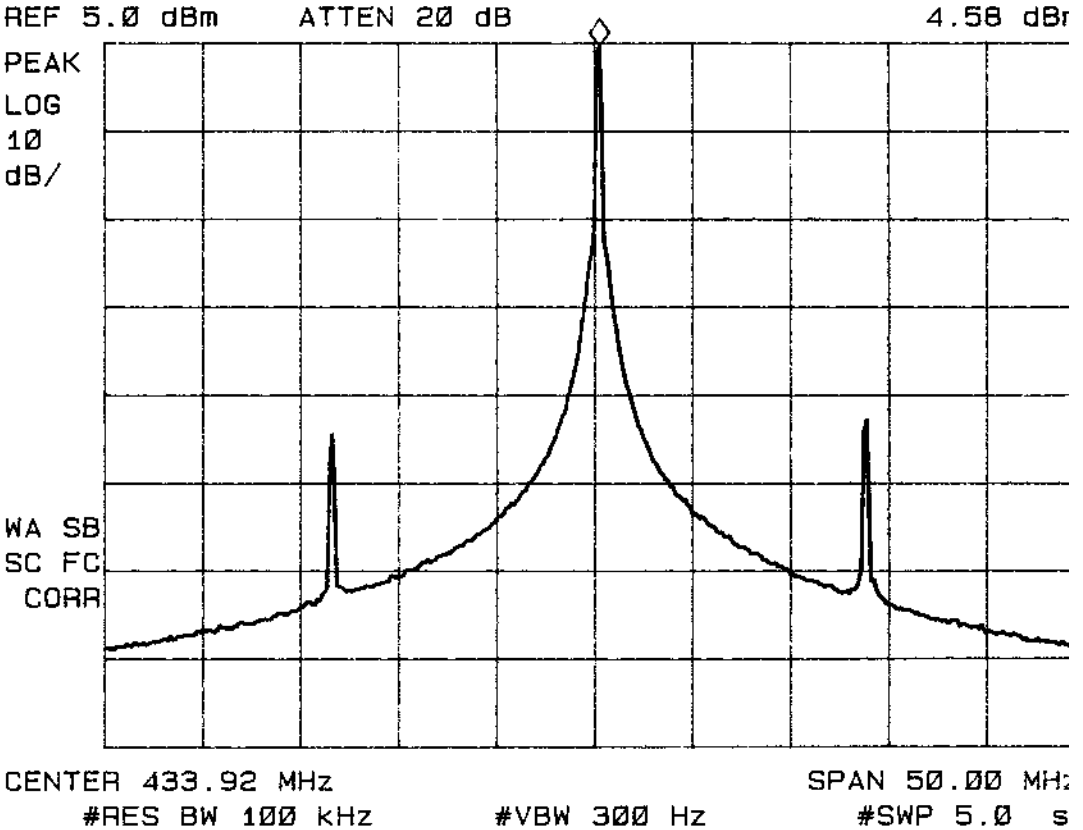
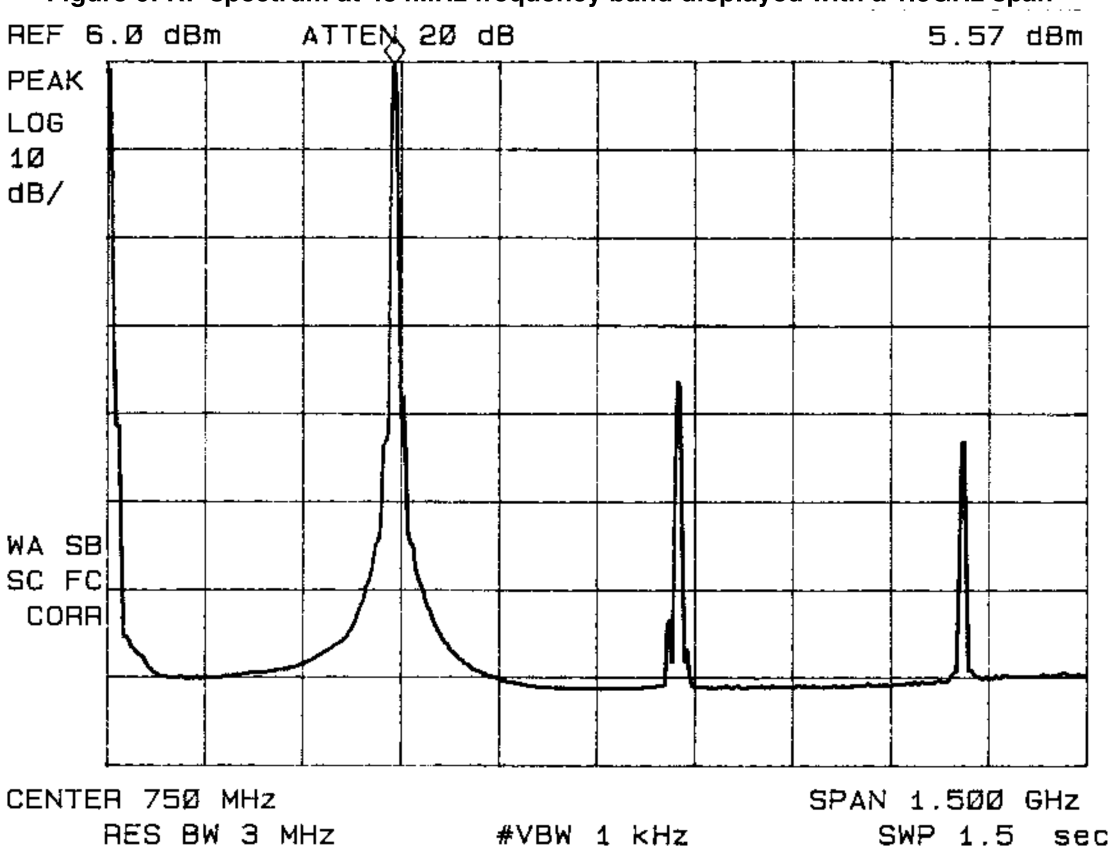


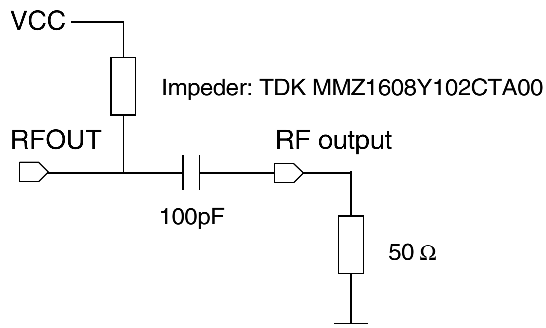
Figure 6: RF spectrum at 434MHz frequency band displayed with a 1.5GHz span



OUTPUT POWER MEASUREMENT

The RF output levels given in the electrical characteristics section are measured whith a 50Ω load directly connected to the pin RFOUT as shown below in figure 7. This wideband coupling method gives results independant of the application.

Figure 7: Output power measurement configurations



The configuration shown in figure 8-a provides a better efficiency in terms of output power and harmonics rejection. Schematic on figure 8-b gives the equivalent circuit of the pin RFOUT and impeder as well as the matching network components for 434MHz frequency band. Note that the impeder is moved to the load side to decrease its influence (similar to DC bias through the antenna).

Figure 8: Ouput characteristic and matching network for 434MHz frequency band

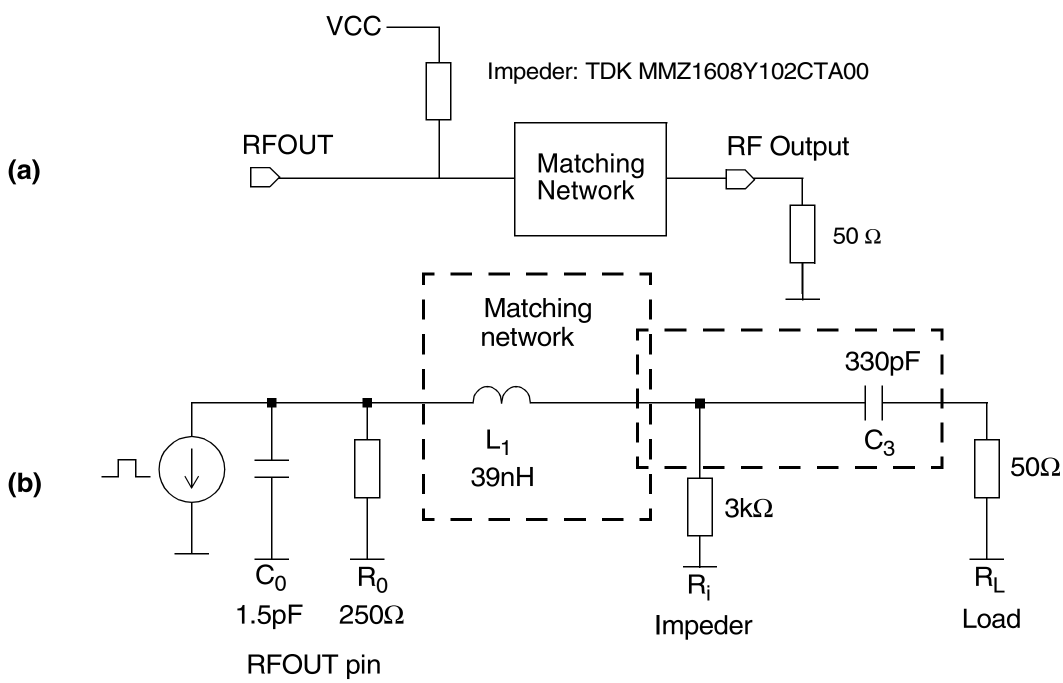
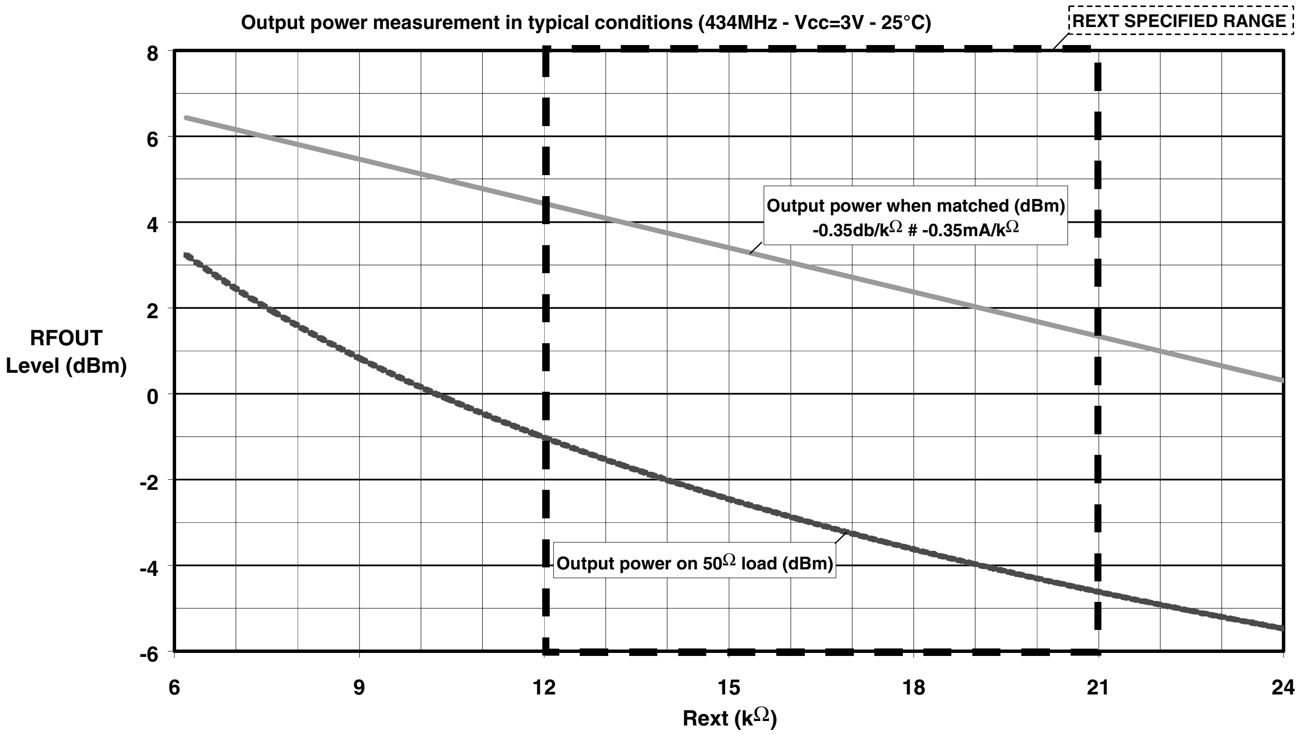


Figure 9 gives the output power versus the Rext resistor value with 50Ω load and with matching network.

Figure 9: Output power at 434MHz frequency band versus Rext value



The 50Ω matching network used for the 868MHz band is similar to the 434MHz, except components values:

L1 is changed to 8.2nH and C3 to 470pF

The expected gain of this 868MHz matching network is 4dB (typical) compared to unmatched boards.

APPLICATION SCHEMATIC

Figures 10 show application schematic for the 315 & 434MHz frequency bands. For 868MHz band application, the input pin BAND must be wired to ground. See component description on table 4.

Figure 10: Application schematic for 315 & 434MHz frequency bands

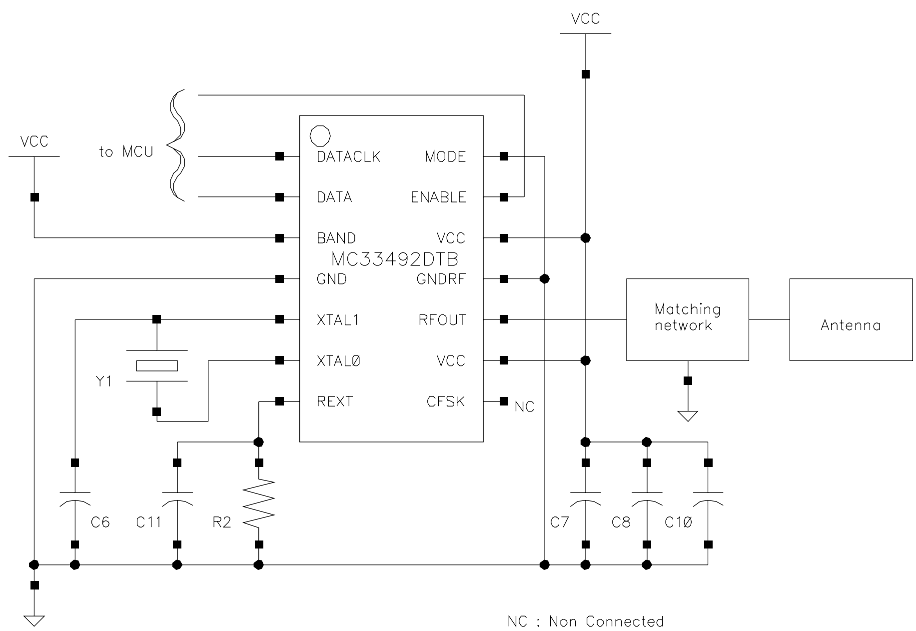


Table 4: External components description

Component	Function	Value	Unit
Y1	Crystal	For 315MHz band: 9.84, see table 5	MHz
		For 434MHz band: 13.56, see table 5	MHz
		For 868MHz band: 13.56, see table 5	MHz
R2	RF output level setting resistor (R_{ext})	12	kΩ
C6	Crystal load capacitor	8.2	pF
C10	Power supply decoupling capacitor	4.7	µF
C7		22	nF
C8		100	pF
C11	Low pass filter capacitor for spurious reduction at $\pm f_{reference}$	47	pF

Examples of crystal reference are given below (see characteristics on table 5) for different application bands:
- at 315MHz band ($f_{reference}$ = 9.84375MHz, -40°C≤T_A≤85°C): NDK LN-G102-950,
- at 434/868MHz bands ($f_{reference}$ = 13.56MHz, -40°C≤T_A≤125°C): NDK NX8045GA S1-40125-8050-12

Table 5: Recommended crystal characteristics (SMD ceramic package)

Parameter	NDK LN-G102-950 (315MHz)	NDK S1-40125-8050-12 (434 & 868MHz)	Unit
Load capacitance	12	12	pF
Motional capacitance	3.33	4.4	fF
Static capacitance	1.05	1.5	pF
Loss resistance	28	18.5	Ω

COMPLETE APPLICATION SCHEMATIC WITH PCB

Figure 11 gives a complete application schematic using a Motorola MC68HC908RK2 microcontroller. $f_{carrier}$= 433.92MHz. C_2 to C_5 capacitors can be removed if switches debounce is done by software.

Figure 11: Complete application schematic for 434MHz frequency band

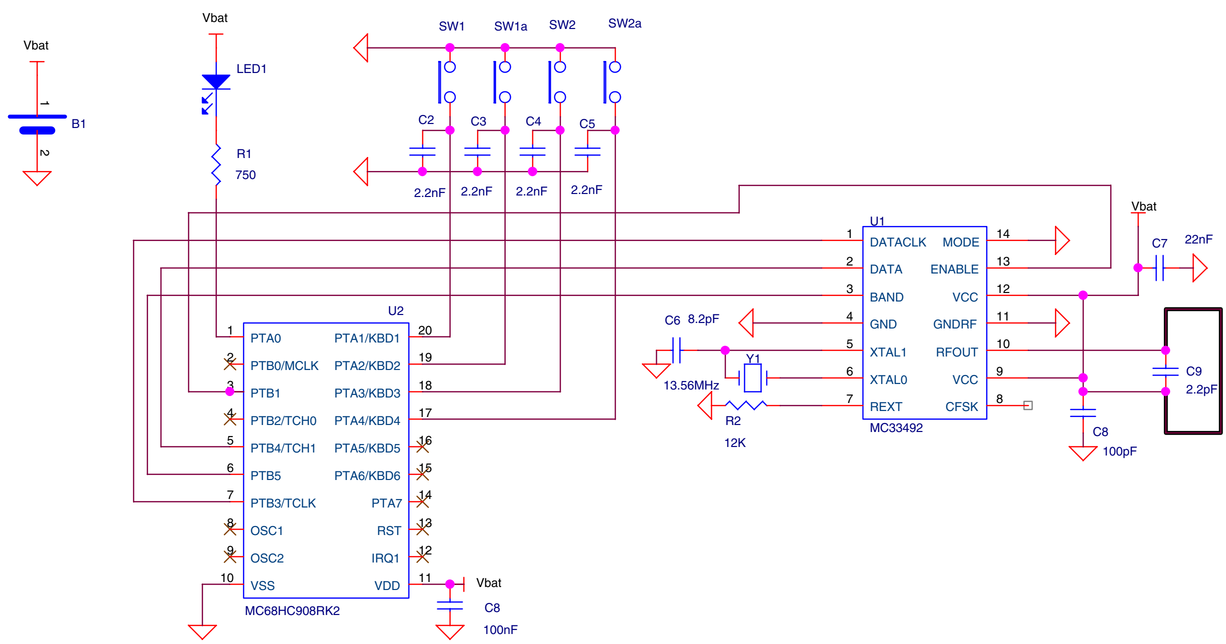
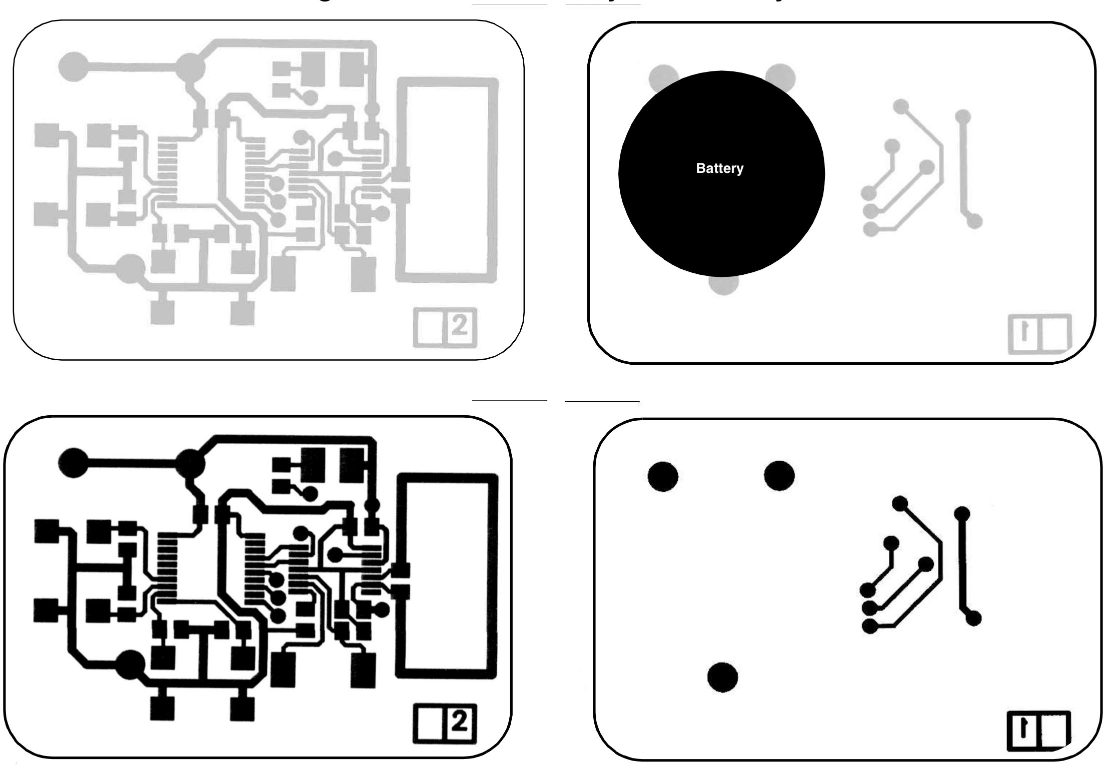
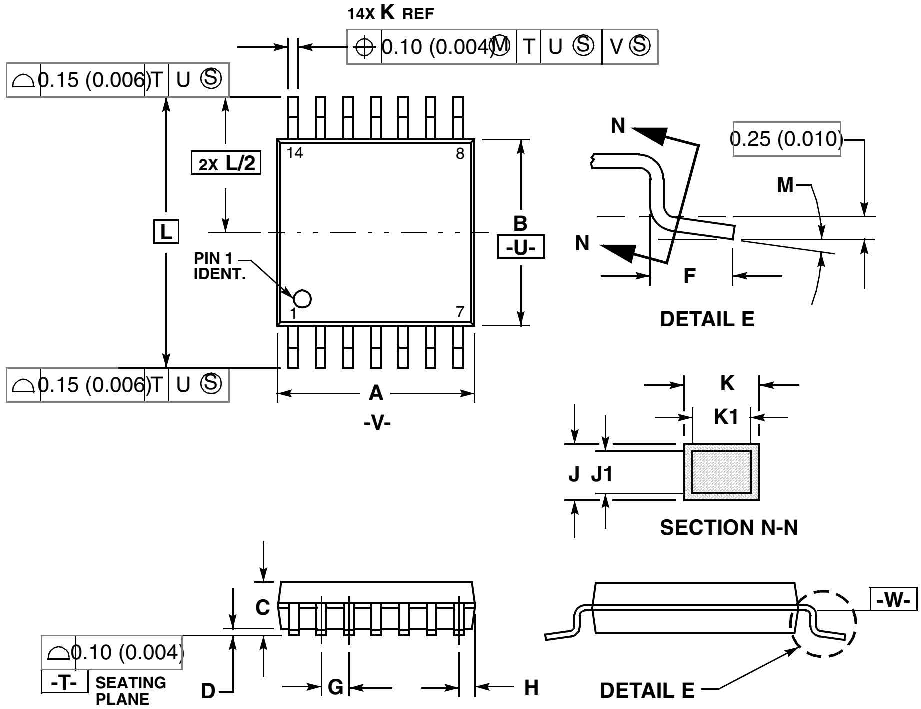


Figure 12 shows a two buttons keyfob board. Real size is 30 x 45 millimeters.

Figure 12: Two button keyfob board layout



CASE OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

CASE 948G-01
ISSUE O

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