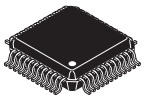
Document Number: MC33909
Rev. 4.0, 8/2016

System basis chip with DC/DC and multiple switch-to-ground interface

33909

SYSTEM BASIS CHIP



AD SUFFIX (PB-FREE)
48 PIN LQFP-EP
98ASA00737D

This SMARTMOS IC integrates the common functionality of system basis chips with switch detection inputs. The device works as an advanced power management unit for the MCU and additional integrated circuits such as sensors, CAN transceivers, and eXtreme switches. It has one built-in enhanced high-speed CAN interface (ISO 11898-2 and -5), with local and bus failure diagnostics, protection and fail-safe operation mode, and includes four LINs, compatible with specification 2.1 and SAEJ2602-2.

The IC starts operating when the VBATP (reverse battery protected) pin reaches 5.3 V maximum. The device requires a reverse blocking ultrafast or Schottky diode for operation. The VPRE supply operating in Buck/Boost mode allows functional operation of the IC from 2.5 V to 35 V on VBATP. The VPRE pin supplies the source voltage for the VDD, VAUX, CAN5V, and SG power rails.

Switch-to-ground inputs are available for switch detection and supply configurable pulsed wetting current, with low sustain current levels for improved thermal and power management. The IC can be programmed to wake-up when a change of state is detected on any input. The device also implements an innovative and advanced fail-safe state machine and concept solution.

Features

- VDD rail (3.3 V or 5.0 V) operates down to 2.5 V on VBATP (provided by V_{PRE} Buck/Boost)
- VAUX rail (3.3 V or 5.0 V) capable of surviving short-to-battery (40 V) conditions
- Low Q current operation for low-power sleep mode, typ. 125 µA
- Secured SPI and advanced watchdog
- SAFE_B pin for limp home mode
- Six switch to GND inputs with selectable wake-up in change of state
- Analog multiplexer

Applications

- Front/rear body controllers
- Gateway modules
- Electric power steering
- Power train

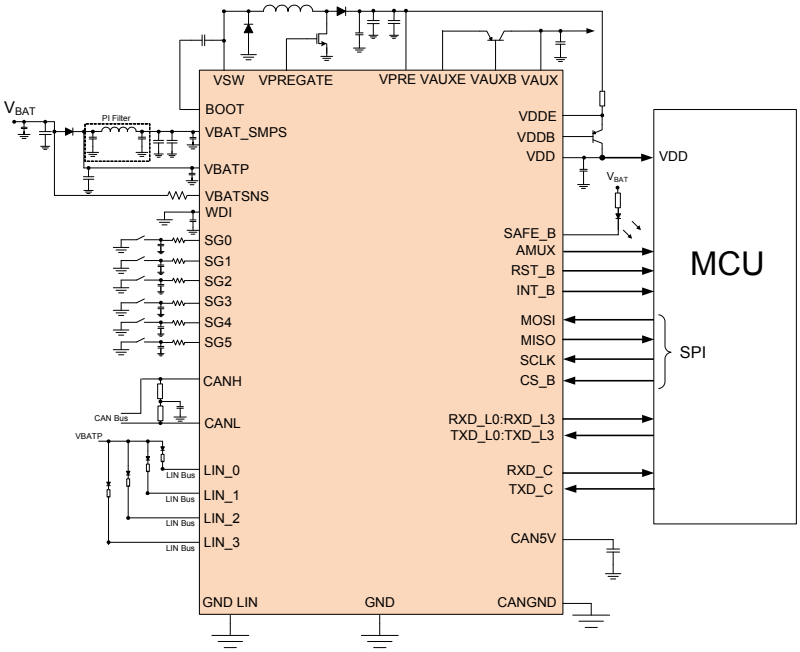


Figure 1. 33909AD simplified application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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1 Orderable parts

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.freescale.com and perform a part number search for the following device numbers.

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package	VDD output voltage	CAN interface(s)	LIN interface(s)	Switch to GND inputs	Notes
MC33909N5AD	-40 °C to 125 °C	7.0 x 7.0, 48 LQFP exposed pad	5.0 V	1	0	6	(1)
MC33909L5AD					1		
MC33909D5AD					2		
MC33909Q5AD					4		
MC33909N3AD			3.3 V		0		
MC33909L3AD					1		
MC33909D3AD					2		
MC33909Q3AD					4		

Notes
1. To order parts in Tape & Reel, add the R2 suffix to the part number.

2 Internal block diagram

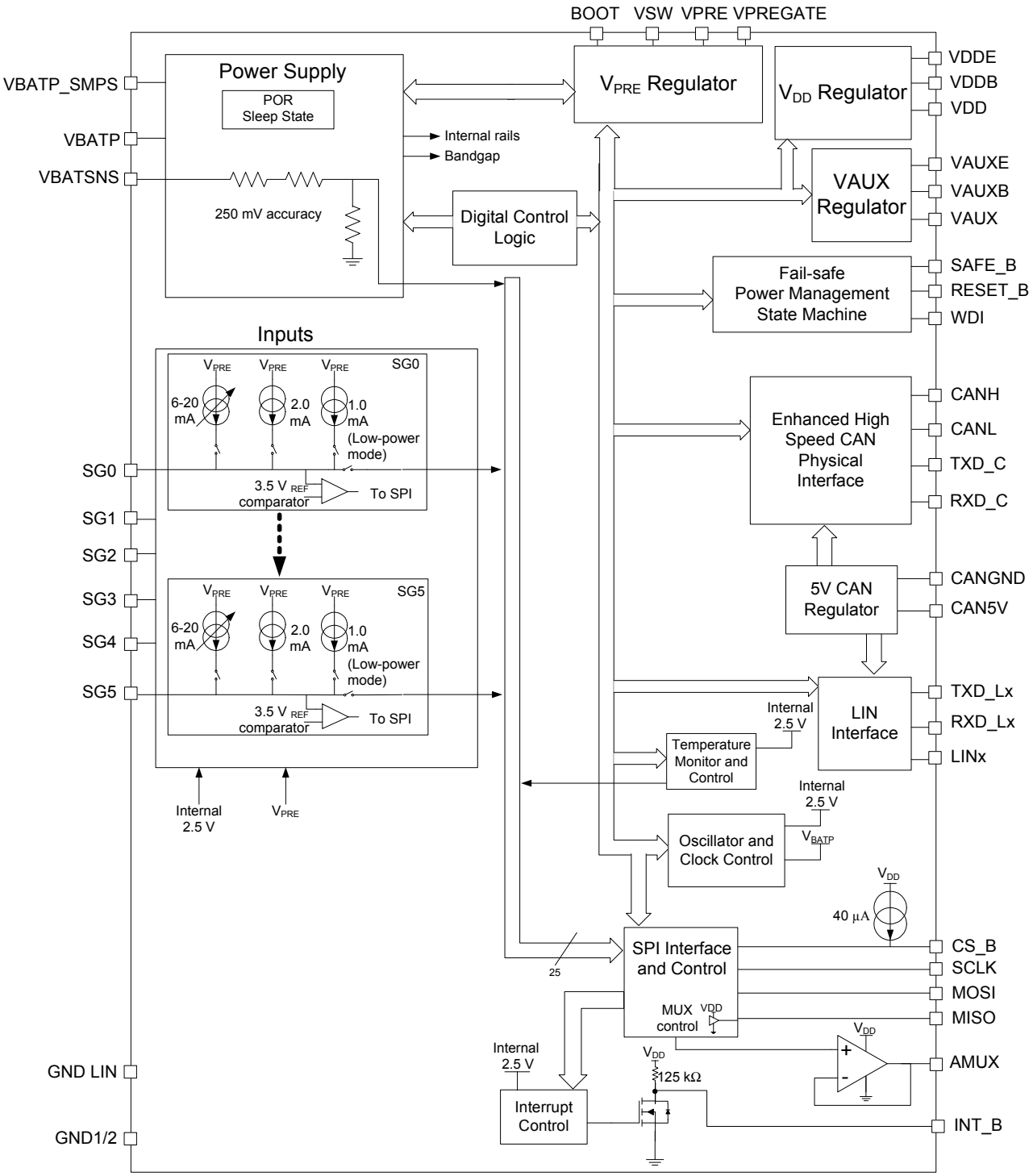


Figure 2. 33909AD simplified internal block diagram

2.1 Pin connections

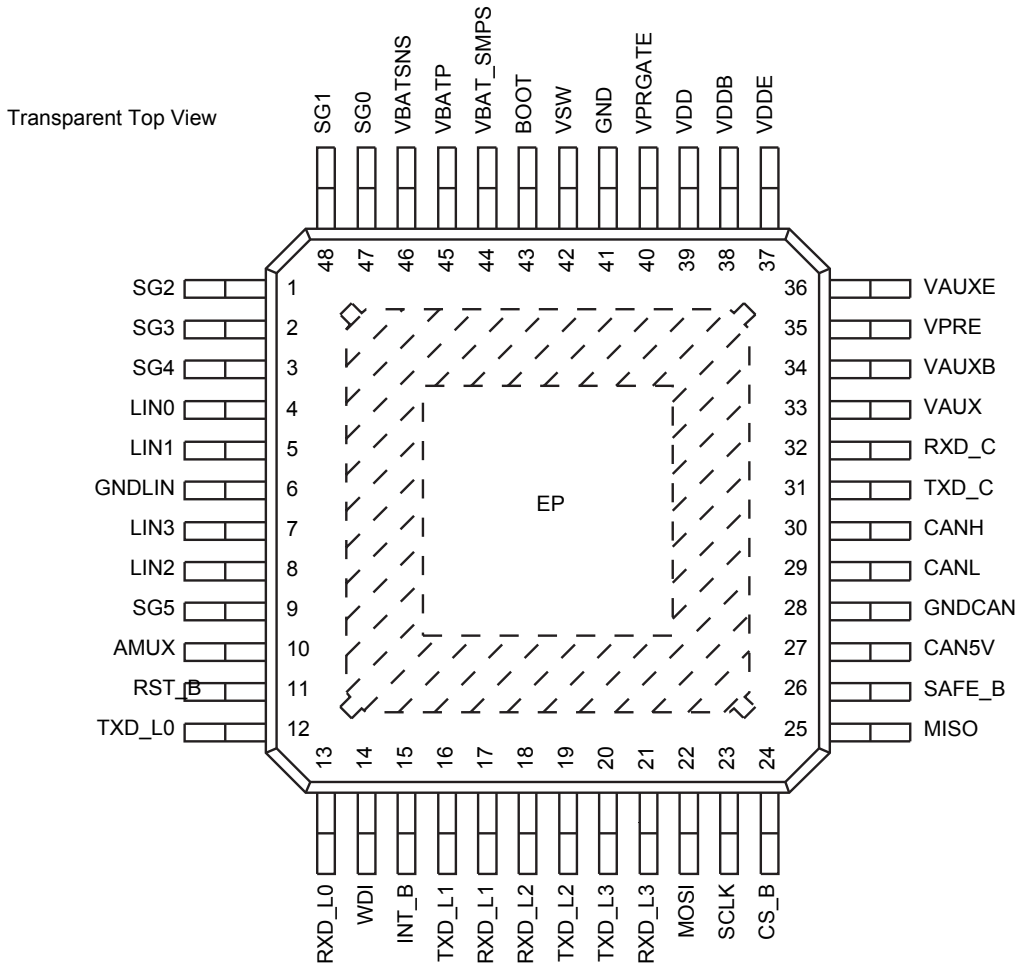


Figure 3. 33909AD pin connections

A functional description of each pin can be found in the Functional device operation section.

Table 2. 33909 pin definitions

Pin number	Pin name	Pin function	Definition
–	EP	Ground	Exposed pad – connect to the ground plane
1-3, 9, 47, 48	SG0 - SG5	Input	Switch to Ground inputs
4	LIN0	Input/Output	LIN0 bus input/output connected to the LIN bus
5	LIN1	Input/Output	LIN1 bus input/output connected to the LIN bus
6	GND LIN	Ground	Ground for LIN 0 - 3 bus
7	LIN3	Input/Output	LIN3 bus input/output connected to the LIN bus
8	LIN2	Input/Output	LIN2 bus input/output connected to the LIN bus
11	RST_B	Input/Output	This is the device reset output whose main function is to reset the MCU. This pin has an internal pull-up to VDD. RESET_B input voltage is also monitored in order to detect external reset and safe conditions.
10	AMUX	Output	Analog multiplex output
12	TXD_L0	Input	LIN0 bus transmit data input. Includes an internal pull-up resistor to VDD

Table 2. 33909 pin definitions (continued)

Pin number	Pin name	Pin function	Definition
13	RXD_L0	Output	LIN0 bus receive data output
14	WDI	Input	Watchdog inhibit
15	INT_B	Output	Open drain output to the MCU is used to indicate an input switch change of state.
16	TXD_L1	Input	LIN1 bus transmit data input. Includes an internal pull-up resistor to VDD
17	RXD_L1	Output	LIN1 bus receive data output
18	RXD_L2	Output	LIN2 bus receive data output
19	TXD_L2	Input	LIN2 bus transmit data input. Includes an internal pull-up resistor to VDD
20	TXD_L3	Input	LIN3 bus transmit data input. Includes an internal pull-up resistor to VDD
21	RXD_L3	Output	LIN3 bus receive data output
22	MOSI	Input / SPI	SPI control data input pin from the MCU
23	SCLK	Input / SPI	SPI control clock input pin
24	CS_B	Input / SPI	SPI control chip select bar input pin. Logic [0] allows data to be transferred in.
25	MISO	Output / SPI	Provides digital data from 33909 to the MCU
26	SAFE_B	Output	Output of the safe circuitry. The pin is asserted LOW in case a safe condition is detected (e.g.: software watchdog is not triggered, V_{DD} low, issue on reset pin, etc.). Open drain structure.
27	CAN5V	Output	Output voltage for the embedded CAN interface. A capacitor must be connected to this pin.
28	GNDCAN	Ground	Power ground for the embedded CAN interface
29	CANL	Output	CAN low output
30	CANH	Output	CAN high output
31	TXD_C	Input	CAN bus transmit data input. Internal pull-up to V_{DD}
32	RXD_C	Output	CAN bus receive data output
33	VAUX	Input	Output pin for the auxiliary voltage
34	VAUXB	Output	Base connection for the external PNP transistor
35	VPRE	Input	Supply for VDD, VAUX, CAN5V, and SG Inputs
36	VAUXE	Input	Collector connection for the external PNP transistor
37	VDDE	Input	Emitter connection for the external LDO
38	VDDB	Output	Base connection for the external LDO
39	VDD	Input	V_{DD} supply voltage
40	VPREGATE	Output	Gate control for low-side FET
41	GND	Ground	Ground for logic and analog (GND1 and GND2)
42	VSW	Output	Switching output
43	BOOT	Input	Boot capacitor to VSW
44	VBATP_SMPS	Power	Supply for SMPS power rail. This pin requires external reverse battery protection.
45	VBATP	Power	Battery supply input pin. This pin requires external reverse battery protection. Supplies internal voltage except SMPS.
46	VBATSNS	Input	Battery sense input. A 1.0 kΩ external resistor required to pass battery transients.

3 Electrical characteristics

3.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
V_{BATP}/V_{BATP_SMPS}	DC Voltage at Power Supply Pins	-0.3 to 40	V	
V_{BATSNS}	DC Voltage at Battery Sense Pin	-14.0 to 41	V	
V_{DIG}	DC Voltage at INT_B, RST_B, MISO, MOSI, CS_B, SCLK, AMUX	-0.3 to 7.0	V	
V_{SAFE_B}	DC Voltage at SAFE_B Pin	-0.3 to 40	V	
V_{WDI}	DC Voltage at WDI Pin	-0.3 to 18	V	
V_{SG}	DC Voltage at SG0, 1, 2, 3, 4, 5	-14 to 40	V	
V_{CAN_5V}	DC Voltage on CAN_5V pin	-0.3 to 7.0	V	
V_{BUS_CAN}	DC Voltage on CANL, CANH	-32 to 40	V	
V_{BUS_DIG}	DC Voltage on TXD_C, RXD_C, TXD_Lx, RXD_Lx	-0.3 to $_{VDD}$ +0.3	V	
V_{BUS_LIN}	DC Voltage on LINx	-27 to 40	V	
V_{PRE}	DC Voltage at VPRE Pin	-0.3 to8.0	V	
V_{PRE_GATE}	DC Voltage at VPRE_GATE Pin	-0.3 to 8.0	V	
V_{SW}	DC Voltage at VSW Pin	-0.3 to 40	V	
V_{BOOT}	DC Voltage at BOOT Pin	-0.3 to 45	V	
V_{DD}	DC Voltage at VDD Pin	-0.3 to 7.0	V	
$V_{DD\_E,B}$	DC Voltage at VDDE, VDDB Pin	-0.3 to 8.0	V	
V_{AUX}	DC Voltage at VAUX Pin	-2.0 to 40	V	
$V_{AUX\_E,B}$	DC Voltage at VAUXE, VAUXB Pin	-0.3 to 40	V	
I_{BUS_CAN}	Continuous Current Capability of CANL, CANH	200	mA	

Table 3. Maximum ratings *(continued)*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
ESD ratings				
V_{ESD1-1} V_{ESD1-2} V_{ESD1-3} V_{ESD1-4} V_{ESD2-1} V_{ESD2-2}	AEC Q100 • LINx pins versus GND • VBAT_SMPS, VBATSNS pins versus GND • VBATP pin versus GND • all other pins Charge Device Model • Corner pins (pins 1, 12, 24, 25, 36, 37, and 48) • All other pins (pins 2-11, 14-23, 26-35, 38-47)	 ±8000 ±4000 ±3000 ±2000 ±750 ±500	V	(2)
V_{ESD4-1} V_{ESD4-2} V_{ESD4-3} V_{ESD4-4} V_{ESD4-5}	Contact Discharge, Unpowered • LIN0, LIN1, LIN2, and LIN3 pin with 220 pF • LIN0, LIN1, LIN2, and LIN3 pin without capacitor • CANH and CANL • SGx - pins with 47-100 nF capacitor • VBATP, VBAT_SMPS, VBATSNS	 ±6000 ±6000 ±6000 ±6000 ±6000	V	(3)
V_{ESD5-1} V_{ESD5-2} V_{ESD5-3} V_{ESD5-4}	Unpowered • LIN0, LIN1, LIN2, and LIN3 pin with 220 pF and without capacitor • CANH, CANL pin without capacitor • VBATP (100 nF to GND) • VBATSNS (1.0 kΩ series resistance)	 ±15000 ±15000 ±8000 ±8000	V	(3)
V_{ESD6-1} V_{ESD6-2}	SGx pins with 47 nF to 100 nF capacitor • Air discharge - unpowered and powered • Contact discharge - unpowered and powered	 ±15000 ±8000	V	(3)
V_{ESD7-1}	Contact Discharge, Unpowered, GND connected to ESD gun GND • CANH, CANL without capacitor	 ±7000	V	(3)
Thermal ratings				
T_A	Ambient Temperature	-40 to 125	°C	
T_J	Junction Temperature	-40 to 150	°C	
T_{STORE}	Storage Temperature	-55 to 150	°C	

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) JESD22/A114 (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
3. According to Hardware requirements for LIN, CAN, and Flexray Interfaces in Automotive Applications, Revision 1.0, 2008-12-10 (IEC 61000-4-2: C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω.

Table 4. Table of thermal resistance data

Symbol	Ratings	Value	Unit	Notes
$R_{\Theta JA}$	Junction to Ambient, Natural Convection, Single Layer board (1s)	72	°C/W	(4),(5)
$R_{\Theta JA}$	Junction to Ambient, Natural Convection, Four layer board (2s2p)	31	°C/W	(4),(5)
$R_{\Theta JCTOP}$	Junction to Case Top	23	°C/W	(6)
$R_{\Theta JCBOTTOM}$	Junction to Case Bottom	1.2	°C/W	(7)

Notes

4. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
5. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
6. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
7. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.

3.2 Static electrical characteristics

Table 5. Static electrical characteristics

Characteristics noted under conditions T_{CASE} = -40 °C to 125 °C, Battery Voltage = 3.5 V to 28 V DC (VBATP = 2.5 V DC to 27 V DC), unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power input						
V_{BATP}	Full DC voltage Range Typical DC Operating Range	2.5 7.0	– –	35 27	V	
V_{BATUV}	VBATP Undervoltage • VBAT Power Down Range, POR occurs	2.3	–	2.5	V	
V_{S_HIGH}	VBATP Overvoltage Detector Thresholds, at VBATP Pin • Not active in Low-power modes	35	–	40	V	
I_{VBATP}	Total Supply Current, in Normal Mode, CAN in Recessive Mode, SGx is open switch, 5.0 V CAN and VAUX ON, LINx in Recessive Mode	–	7.0	14	mA	
I_{LPM_OFF}	Low-power Mode V_{DD} Off. Wake-up from CAN, SGx inputs at T_{SCAN} = 64 ms, LIN • VBATP = 18 V and 8.0 V	–	100	190	µA	
I_{LPM_ON}	Low-power Mode V_{DD}ON (5.0 V) with V_{DD} Undervoltage and V_{DD} Overcurrent Monitoring, Wake-up from CAN, SGx Inputs at T_{SCAN} = 64 m and LIN • VBATP = 18 V and 8.0 V	–	125	200	µA	
I_{OSC}	Low-power Mode V_{DD} OFF (no wake-up) • VBATP = 18 V and 8.0 V	–	90	170	µA	
VPRE buck boost converter						
$V_{BAT\_MIN\_SU}$	Minimum Start Up Voltage • VBAT Power Up Range, V_{DD} is not Operating (VBATP < $V_{BAT\_MIN\_SU}$)	4.5	5.0	5.3	V	
$V_{BATPTHD}$	Buck to Boost Mode Threshold Voltage	6.2	6.6	7.0	V	
$V_{BATPTHU}$	Boost to Buck Mode Threshold Voltage	6.8	7.25	7.8	V	
I_{PRE_LIM}	Peak Input Current Limit	3.5	4.0	–	A	(8)
I_{LOAD}	Transient Load Current Change	–	–	500	mA	(8)
$I_{PRE/DT}$	V_{PRE} Load regulation Variation	–	–	25	A/ms	(8)
f_{SW}	Switching Frequency	418	440	462	kHz	(8),(9)
I_{LOAD_BUCK} I_{LOAD_BOOST}	Continuous Output Load Current • Buck mode • Boost mode (VBATP = 2.5 V)	3.0 –	– –	– 0.5	A	(8)
t_{ILIM_BT}	Current Limit Blanking Time	200	–	600	ns	
I_{LPM_LOAD}	Continuous Output Load Current During Low-power Mode	25	40	–	mA	

Notes
8. Guaranteed by design.
9. Fixed frequency.

Table 5. Static electrical characteristics (continued)

Characteristics noted under conditions T_{CASE} = -40 °C to 125 °C, Battery Voltage = 3.5 V to 28 V DC (VBATP = 2.5 V DC to 27 V DC), unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
VPRE buck boost converter						
V_{PREOV}	V_{PRE} Overvoltage	7.2	–	8.0	V	
$V_{PREOVHYST}$	V_{PRE} Overvoltage Hysteresis	0.05	–	0.2	V	
V_{PREUV}	V_{PRE} Undervoltage	5.5	–	6.0	V	
$V_{PREUVHYST}$	V_{PRE} Undervoltage Hysteresis	0.05	–	0.2	V	
V_{SUP_IPFF}	I_{PFF}: Input Voltage Detection	19	–	24	V	
$V_{SUP\_IPFF\_HYST}$	I_{PFF}: Input Voltage Hysteresis	0.2	–	–	V	
$t_{\_VSUP\_IPFF}$	I_{PFF}: Input Voltage Filter Time	1.0	–	4.0	µs	
$I_{PRE\_IPFF\_PK}$	I_{PFF}: HS Peak Current Detection	2.2	–	–	A	
$t\_I_{PRE\_IPFF}$	I_{PFF}: HS Peak Current Filter Time	100	–	300	ns	
T_{PRE_TWARN}	V_{PRE} Thermal Warning Threshold	–	125	–	°C	(10)
T_{PRE_TSD}	V_{PRE} Thermal Shutdown Threshold	160	–	–	°C	(10)
$T_{PRE\_TSD\_HYS}$	V_{PRE} Thermal Shutdown Hysteresis	10	–	–	°C	(10)
C_{VPRE}	VPRE External Capacitor	–	47	–	µF	(10)
R_{VPRE}	VPRE External Capacitor ESR	–	–	100	mΩ	(10)
Buck converter						
$VPRE_{BUCK}$	Output Voltage VPRE • VBATP = $VBATP_{(THD\ or\ THU)}$ to 36 V	6.3	6.5	6.7	V	
$R_{DS(on)}$	VSW Drain-source On-resistance • I_D = 500 mA, VBATP = 9.0 V	–	–	300	mΩ	
Boost converter						
$VPRE_{BST}$	Output Voltage V_{PRE} in Boost Mode • VBATP = 2.5 V to $V_{BATP\ (THD\ or\ THU)}$, I_{VPRE} = -550 mA	6.0	6.3	7.0	V	
V_G	VPREGATE Output Voltage, Power MOSFET ON	3.5	4.0	V_{PRE}	V	
I_{SOURCE}	VPREGATE Source Continuous Current	–	350	–	mA	(10)
I_{SINK}	VPREGATE Sink Continuous Current	200	350	500	mA	(10)

Notes

10. Guaranteed by design.

Table 5. Static electrical characteristics (continued)

Characteristics noted under conditions T_{CASE} = -40 °C to 125 °C, Battery Voltage = 3.5 V to 28 V DC (VBATP = 2.5 V DC to 27 V DC), unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
VDD voltage regulator, VDD pin						
V_{OUT5}	Output voltage (5.0 V device) • VBATP = 2.5 V to 35 V, I_{OUT} = 0 mA to 500 mA, Normal mode	4.9	5.0	5.1	V	
V_{OUT3}	Output voltage (3.3 V device) • VBATP = 2.5 V to 35 V, I_{OUT} = 0 mA to 500 mA, Normal mode	3.23	3.3	3.367	V	
I_{SCVDD}	VDD Short-circuit Current • V_{DD} = 1.65 V, $V_{SCFDIFF} = V_{PRE}-V_{DDE}$	-90	–	-60	mA	
I_{VDD_FBILIM}	VDD Foldback Current Limit • V_{DD} = 0.5 V, $V_{SCFDIFF} = V_{PRE}-V_{DDE}$	-60	–	-30	mA	
V_{DD_FB}	VDD Foldback Current Limit Threshold (VDD voltage when foldback current kicks in)	0.5	1.075	1.65	V	
I_{VDDBC}	VDD Base Current Capability	25	–	–	mA	
$PSRR_{VDD}$	PSRR (Power supply rejection ratio) • f = 350 kHz to 500 kHz	40	–	–	dB	(11)
C_{EXT}	Range of Decoupling Capacitor	4.7	–	100	µF	(11)
$R_{3CAPESR}$	External capacitor ESR	10	–	100	mΩ	(11)
V_{DDLP5}	Low-power Mode V_{DDON}, output voltage (5.0 V device) • $I_{OUT} \leq$ 40 mA (time limited), VBATP ≥ 8.5 V • $I_{OUT} \leq$ 20 mA (time limited), VBATP ≥ 5.5 V	4.7	5.0	5.25	V	
V_{DDLP3}	Low-power Mode V_{DDON}, output voltage (3.3 V device) • $I_{OUT} \leq$ 40 mA (time limited), VBATP ≥ 8.5 V • $I_{OUT} \leq$ 20 mA (time limited), VBATP ≥ 5.5 V	3.135	3.3	3.465	V	
I_{LP-ITH}	Low-power Wake-up Current Threshold, VBATP ≥ 6.0 V	2.0	5.0	9.0	mA	
Voltage regulator for CAN interface supply, CAN5V pin						
$5V_{CANOUT}$	Output Voltage • I_{OUT} = 0 mA to 200 mA, VBATP = 5.5 V to 40 V	4.75	5.0	5.25	V	
$5V_{CANILIM}$	Output Current Limitation	200	–	–	mA	
$5V_{CANUV}$	Undervoltage Threshold Falling	4.0	–	4.7	V	
$5V_{CANUV}$	Undervoltage Threshold Rising	4.0	–	4.75	V	
$5V_{CANUV}$	Undervoltage Hysteresis	0.05	0.1	0.3	V	
$5V_{CANTS}$	Thermal Shutdown	160	–	–	°C	(11)
$C_{EXT-CAN}$	External Capacitance	1.0	–	100	µF	(11)

Notes
11. Guaranteed by design.

Table 5. Static electrical characteristics (continued)

Characteristics noted under conditions T_{CASE} = -40 °C to 125 °C, Battery Voltage = 3.5 V to 28 V DC (VBATP = 2.5 V DC to 27 V DC), unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
V Auxiliary output, 5.0 V and 3.3 V selectable VB-AUX, VAUX pin						
V_{AUX5}	VAUX Output Voltage 5.0 V • I_{OUT} = 0 mA to 200 mA	4.85	5.0	5.15	V	
V_{AUX3}	VAUX Output Voltage 3.3 V • I_{OUT} = 0 mA to 200 mA	3.2	3.3	3.4	V	
$V_{AUX-UVTH5}$	VAUX Undervoltage Detector 5.0 V	4.2	4.5	4.75	V	
$V_{AUX-UVTH3}$	VAUX Undervoltage Detector 3.3 V	2.75	3.0	3.1	V	
$V_{AUX-OVTH}$ $V_{AUX-SBDL}$	VAUX Overvoltage • VAUX Short to Battery Detection Level	5.6	6.0	7.0	V	
V_{AUX_TRACK}	VAUX Tracking Supply • V_{DD} = 5.0 V only, I_{AUX} = 100 mA	V_{DD}-15 mV	V_{DD}	V_{DD}+15 mv	V	
$I_{AUX-ILIM}$	VAUX Current Limit • V_{AUX} = 1.65 V	200	–	360	mA	
$I_{AUX-FBILIM}$	VAUX Fold-back Current Limit • $V_{AUX} < V_{AUX-FB}$	120	–	230	mA	
V_{AUX-FB}	VAUXE Fold-back Current Limit Threshold - VAUX level at which Fold-back Current Kicks In	0.5	1.075	1.65	V	
$I_{AUX-SBLK}$	VAUX Short to Battery Leakage	0.0	–	15	µA	
I_{VAUXBC}	VAUX Base Current Capability	10	–	–	mA	
C_{3CAP}	External Capacitance	2.2	–	100	µF	(12)
$R_{3CAPESR}$	External Capacitor ESR - Includes PCB Impedance	10	–	100	mΩ	(12)
Undervoltage reset and reset function, RST_B pin						
$V_{ST-TH5H}$	VDD Undervoltage Threshold 5H, 5.0 V device (falling)	4.25	4.5	4.75	V	
$V_{ST-TH5L}$	VDD Undervoltage Reset Threshold 5L,5.0 V device (falling)	2.75	3.3	3.4	V	
$V_{ST-TH3L}$	VDD Undervoltage Threshold 3L, 3.3 V device (falling)	1.85	–	2.05	V	
$V_{ST-TH3H}$	VDD Undervoltage 3H 3.3 V device (falling)	2.75	–	3.15	V	
$V_{ST-HYST}$	VDD Undervoltage Hysteresis, 5.0 V device	50	100	500	mV	
$V_{ST-TH3L}$	VDD Undervoltage Hysteresis, 3.3 V device	40	100	500	mV	
$V_{SVDD-OV}$	VDD Overvoltage	5.5	–	6.0	V	
V_{OL}	RST_B VOL at 1.5 mA, V_{BATP} = 2.5 V to 35 V	–	–	500	mV	
$I_{SINKRESET}$	RST_B Sink Current - VRESET Driven Low (25 °C Only)	5.0	7.0	25	mA	
$R_{PULL-UP}$	Pull-up Resistor (to VDD pin)	10	20	–	kΩ	
V_{ST-VTH}	RST_B input Threshold	–	0.4	–	V	
$V_{RST-HYST}$	RST_B Input Hysteresis	450	–	950	mV	

Notes

12. Guaranteed by design.

Table 5. Static electrical characteristics (continued)

Characteristics noted under conditions T_{CASE} = -40 °C to 125 °C, Battery Voltage = 3.5 V to 28 V DC (VBATP = 2.5 V DC to 27 V DC), unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
VBATSNS input						
V_{ACC5} V_{ACC3}	VBATSNS Resistor Divider (VBATP = 27 V) • 5.0 V device, Divider 1/5.94 • 3.3 V device, Divider 1/8.9	 – –	 – –	 5.0 5.0	%	
$R_{VBATSNS}$	Input Resistor to GND. In all modes except in Low-power modes	50	–	–	kΩ	
Analog MUX output						
C_{MUX}	External Capacitor at AMUX Output	–	–	1.0	nF	(13)
TEMP-COEFF	Chip Temperature Sensor Coefficient	–	4.0	–	mV/°C	(13)
V_{OFFSET}	Input Offset Voltage when Selected as Analog	-10	–	10	mV	
V_{OL}	Analog Operational Amplifier Output Voltage • Sink 250 µA	–	–	50	mV	
V_{OH}	Analog Operational Amplifier Output Voltage • Source 250 µA	V_{DD} -0.1	–	V_{DD} +0.1	V	
Temperature limit						
T_{LIM}	Temperature monitor	155	–	185	°C	(13)
$T_{LIM(HYS)}$	Temperature Monitor Hysteresis	5.0	–	15	°C	(13)
WDI input						
R_{WDIA}	SAFE_B Mode A • External Resistor to GND on WDI pin	–	–	2.5	kΩ	
R_{WDIB1}	SAFE_B Mode B1 • External Resistor to GND on WDI pin	7.0	–	14	kΩ	
R_{WDIB2}	SAFE_B Mode B2 • External Resistor to GND on WDI pin	29	–	40	kΩ	
R_{WDIB3}	SAFE_B Mode B3 • External Resistor to GND on WDI pin	80	–	–	kΩ	
V_{WDIT}	Watchdog Inhibit for Debug • For Watchdog inhibit mode	8.0	–	–	V	
SAFE output						
$I_{SINKSAFE\_B}$	SAFE_B Sink Current • SAFE_B driven low (25 °C only)	2.5	–	–	mA	
V_{OLSAFE}	SAFE_B Low Level • I = 500 µA	0.0	–	1.0	V	
$I_{SAFE\_B\text{-}IN}$	SAFE_B Leakage Current (VDD_{LOW}, or device unpowered) • V_{SAFE_B} = 35 V	-1.0	0.0	1.0	µA	

Notes

13. Guaranteed by design.

Table 5. Static electrical characteristics (continued)

Characteristics noted under conditions T_{CASE} = -40 °C to 125 °C, Battery Voltage = 3.5 V to 28 V DC (VBATP = 2.5 V DC to 27 V DC), unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Interrupt						
V_{OLINT}	Output Low Voltage - I_{OUT} = 1.5 mA	–	0.2	1.0	V	
V_{OHINT}	INT_B Voltage High - INT_B = Open circuit	V_{DD} -0.5	–	V_{DD} +0.1	V	
R_{PU}	Pull-up Resistor	10	20	25	kΩ	
$I_{SINKINT}$	Sink Current - V_{INT} > 5.0 V, INT Driven Low (25 °C only)	2.5	7.5	25	mA	
CAN logic input pins (TXD)						
V_{IH}	High Level Input Voltage	0.7 x V_{DD}	–		V	
V_{IL}	Low Level Input Voltage		–	0.3 x V_{DD}	V	
R_{PUCAN}	Pull-up resistor - V_{IN} = 0 V	22	33	66	kΩ	
CAN data output pins (RXD)						
$VOUT_{LOW}$	Low Level Output Voltage - I_{RXD} = 5.0 mA	0.0	–	0.3 x V_{DD}	V	
$VOUT_{HIGH}$	High Level Output Voltage - I_{RXD} = -3.0 mA	0.7 x V_{DD}	–	V_{DD}	V	
$IOUT_{HIGH}$	High Level Output Current - V_{RXD} = V_{IO} - 0.4 V	-6.0	-3.0	-1.0	mA	
$IOUT_{LOW}$	Low Level Output Current - V_{RXD} = 0.4 V	2.0	5.0	12	mA	
CAN output pins (CANH, CANL) - RBUS = 60 Ω for product test						
V_{COM}	Bus Pins Common Mode Voltage for Full Functionality (voltage range for CAN test)	-15	–	20	V	
$V_{CANH-VCANL}$	Differential Input Voltage Threshold	500	–	900	mV	
$V_{DIFF-HYST}$	Differential Input Hysteresis	100	–	-	mV	
R_{IN}	Input Resistance	5.0	–	50	kΩ	
$R_{IN-DIFF}$	Differential Input Resistance	10	–	100	kΩ	
$R_{IN-MATCH}$	Input Resistance Matching	-3.0	0.0	3.0	%	
V_{CANH}	CANH Output Voltage (45 Ω < R_{BUS} < 65 Ω) • TX dominant state • TX recessive state	 2.75 2.0	 3.5 2.5	 4.5 3.0	V	
V_{CANL}	CANL Output Voltage (45 Ω < R_{BUS} < 65 Ω) • TX dominant state • TX recessive state	 0.5 2.0	 1.5 2.5	 2.25 3.0	V	
V_{OH-VOL}	Differential Output Voltage (45 Ω < R_{BUS} < 65 Ω) • TX dominant state • TX recessive state	 1.5 -0.5	 2.0 0.0	 3.0 0.05	V	
I_{CANH}	CANH Output Current Capability - Dominant state	–	–	-35	mA	
I_{CANL}	CANL Output Current Capability - Dominant state	35	–	–	mA	
$I_{CANL-OC}$	CANL Overcurrent Detection - Error reported in register	-100	-85	-70	mA	
$I_{CANH-OC}$	CANH Overcurrent Detection - Error reported in register	70	85	100	mA	
$R_{INSLEEP}$	CANH, CANL Input Resistance Device Supplied and in CAN Sleep Mode, V_CANH, V_CANL from 0 V to 5.0 V	5.0	–	50	kΩ	

Table 5. Static electrical characteristics (continued)

Characteristics noted under conditions T_{CASE} = -40 °C to 125 °C, Battery Voltage = 3.5 V to 28 V DC (VBATP = 2.5 V DC to 27 V DC), unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
CAN output pins (CANH, CANL) - RBUS = 60 Ω for product test (continued)						
V_{CANLP}	CANL, CANH Output Voltage in Sleep and Standby Modes (45 Ω < R_{BUS} < 65 Ω)	-0.1	0.0	0.1	V	
I_{CAN}	CANH, CANL Input Current, Device Unsupplied, VBATP connected to GND • V_{CANH}, V_{CANL} = 5.0 V • V_{CANH}, V_{CANL} = -2.0 V to + 7.0 V	 – –	 5.0 –	 250 –	µA	
$I_{LEAKGND}$	Loss of Ground Leakage Current (GB CZ) • VBATP = 12 V	–	250	–	µA	(14)
CANH and CANL diagnostic information						
V_{LG} V_{HG}	GND Detection Threshold • CANL • CANH	-200	250	900	mV	
V_{LVB} V_{HVB}	VBATP Detection Threshold • CANL • CANH	4.7	5.1	5.7	V	
LIN 0-3 pin (parameters guaranteed for 7.0 V < VBATP < 17 V)						
$V_{BATTERY}$	Operating Voltage Range (voltage range for LIN testing)	8.0	–	18	V	
V_{BATP}	Supply Voltage Range (voltage range for LIN testing)	7.0	–	18	V	
$V_{BATP\_NON\_OP}$	Voltage Range within which the Device is Not Destroyed	-0.3	–	40	V	
I_{BUS_LIM}	Current Limitation for Driver Dominant State Driver ON, V_{BUS} = 18 V	40	90	200	mA	
$I_{BUS\_PAS\_DOM}$	Input Leakage Current at the Receiver Driver OFF; V_{BUS} = 0 V; V_{BATP} = 12 V	-1.0	–	–	mA	
$I_{BUS\_PAS\_REC}$	Leakage Output Current to GND Driver OFF; 7.0 V < V_{BATP} < 17 V; 8.0 V < V_{BUS} < 18 V	–	–	20	µA	
$I_{BUS\_NO\_GND}$	Control Unit Disconnected from GND (Loss of local ground must not affect communication in the residual network) GNDDEVICE = V_{BATP}, V_{BATP} = 12 V, 0 < V_{BUS} < 18 V	-1.0	–	1.0	mA	(14)
I_{BUSNO_BAT}	VBATP Disconnected, V_{BATP_DEVICE} = GND, 0 < V_{BUS} < 18 V (Node has to sustain the current which can flow under this condition. Bus must remain operational under this condition)	–	–	100	µA	
V_{BUSDOM}	Receiver Dominant State	–	–	0.4	V_{BATP}	
V_{BUSREC}	Receiver Recessive State	0.6	–	–	V_{BATP}	
V_{BUS_CNT}	Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2	0.475	0.5	0.525	V_{BATP}	
V_{HYS}	Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	–	–	0.175	V_{BATP}	

Notes

14. Guaranteed by CZ. Parameter not tested in production.

Table 5. Static electrical characteristics (continued)

Characteristics noted under conditions T_{CASE} = -40 °C to 125 °C, Battery Voltage = 3.5 V to 28 V DC (VBATP = 2.5 V DC to 27 V DC), unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
LIN 0-3 pin (parameters guaranteed for 7.0 V < VBATP < 17 V) (continued)						
$V_{SERDIODE}$	Voltage Drop at the Serial Diode in Pull-up Path - High Z State at LINx	0.4	–	1.0	V	
V_{SHIFT_BAT}	VBATP_SHIFT (GBD)	0.0	–	11.5%	V_{BATP}	(15)
V_{SHIFT_GND}	GND_SHIFT (GBD)	0.0	–	11.5%	V_{BATP}	(15)
V_{BUSWU}	LIN Wake-up Threshold from Stop or Sleep Mode	3.2	3.5	3.8	V	
R_{SLAVE}	LIN Pull-up Resistor to V_{BATP}	20	30	60	kΩ	
V_{UVR}, V_{UVF}	LIN Undervoltage Threshold (rising and falling) (J2602)	5.9	6.2	6.85	V	
V_{UVHSY}	LIN Undervoltage Hysteresis (V_{UVR} – V_{UVF}) (J2602)	–	100	–	mV	
T_{LINSD}	Overtemperature Shutdown	150	160	180	°C	(15)
T_{LINSD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	(15)
LIN RXD output pins						
V_{OL_RXDL}	Low Level Output Voltage - $I_{IN} \leq$ 1.5 mA	–	–	0.9	V	
V_{OH_RXDL5}	High Level Output Voltage (VDD = 5.0 V) - $I_{OUT} \leq$ 250 µA	4.25	–	5.25	V	
V_{OH_RXDL3}	High Level Output Voltage (VDD = 3.3 V) - $I_{OUT} \leq$ 250 µA	3.0	–	3.5	V	
LIN TXD input pins						
V_{IL_TXDL}	Low Level Input Voltage	–	–	0.3 x V_{DD}	V	
V_{IH_TXDL}	High Level Input Voltage	0.7 x V_{DD}	–	–	V	
$V_{INHYSTL}$	Input Threshold Voltage Hysteresis	450	–	950	mV	
R_{PULLIN}	Pull-up Resistor - VIN = 0.0 V	22	33	66	kΩ	
Switch input						
I_{LEAKSG_GND}	Leakage (SGx pins) to GND • Inputs tristated, analog mux selected for each input, voltage at SGx = GND	–	–	2.0	µA	
I_{LEAKSG_BAT}	Leakage (SGx pins) to Battery • Inputs tristated, analog mux selected for each input, voltage at SGx = VBATP	–	–	2.0	µA	
I_{LEAKSG_WE}	Leakage (SGx pins) Voltage at SGx = 36 V, VBATP and VPRE = 0 V	–	–	2.0	µA	
I_{WET1}	Pulse Wetting Current 1 - Mode 1 I_{PULSE1} = 6.0 mA	5.4	–	6.6	mA	
I_{WET2}	Pulse Wetting Current 2 - Mode 2 I_{PULSE2} = 8.0 mA	7.2	–	8.8	mA	
I_{WET3}	Pulse Wetting Current 3 - Mode 3 I_{PULSE1} = 10 mA	9.0	–	11	mA	

Notes

15. Guaranteed by design.

Table 5. Static electrical characteristics (continued)

Characteristics noted under conditions T_{CASE} = -40 °C to 125 °C, Battery Voltage = 3.5 V to 28 V DC (VBATP = 2.5 V DC to 27 V DC), unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Switch input (continued)						
I_{WET4}	Pulse Wetting Current 4 - Mode 4 I_{PULSE2} = 12 mA	10.8	–	13.2	mA	
I_{WET5}	Pulse Wetting Current 5 - Mode 5 I_{PULSE3} = 14 mA	12.6	–	15.4	mA	
I_{WET6}	Pulse Wetting Current 6 - Mode 6 I_{PULSE4} = 16 mA	14.4	–	17.6	mA	
I_{WET7}	Pulse Wetting Current 7 - Mode 7 I_{PULSE5} = 20 mA	18	–	22	mA	
$I_{SUSTAIN}$	Sustain Current	1.60	–	2.40	mA	
$I_{MATCH(SUS)}$	Matching Between SG Channels (2.0 mA) $\frac{I_{SUS(MAX)} - I_{SUS(MIN)} \text{ X } 100}{I_{SUS(AVG)}}$	-10	–	10	%	
$I_{MATCH(WET)}$	Matching Between SG Channels (6, 8, 10, 12, 14, 16, and 20 mA) $\frac{I_{WET(MAX)} - I_{WET(MIN)} \text{ X } 100}{I_{WET(AVG)}}$	-5.0	–	5.0	%	
V_{ICTHR}	Switch Detection Threshold - Normal mode	3.20	–	3.8	V	
$I_{SUSTAINLP}$	Low-power Polling Current	0.850	1.1	1.35	mA	
$V_{LPICTHR}$	Low-power Switch Detection Threshold	100	210	350	mV	
Digital interface						
V_{IH}	Input Logic High Voltage Thresholds (MISO, MOSI, SCLK, CS_B)	0.7 X V_{DD}	–	–	V	
V_{IL}	Input Logic Low Voltage Thresholds (MISO, MOSI, SCLK, CS_B)	–	–	0.2 X V_{DD}	V	
I_{HZ}	Tri-state Leakage Current (MISO) - V_{DD} = 0.0 V to V_{DD}	-2.0	–	2.0	µA	
I_{SCLK}, I_{MOSI}	SCLK/MOSI Input Current - SCLK/MOSI = 0.0 V	-3.0	–	3.0	µA	
I_{SCLK}, I_{MOSI}	SCLK/MOSI Pull-down Current - SCLK/MOSI = V_{DD}	-5.0	–	-15	µA	
I_{CS_B}	CS_B Input Current - $\overline{CS}$ = V_{DD}	-10	–	10	µA	
I_{CS_B}	CS_B Pull-up Current- $\overline{CS}$ = 0.0 V	30	–	100	µA	
$V_{SO(HIGH)}$	MISO High-side Output Voltage - $I_{SO(HIGH)}$ = -200 µA	V_{DD} – 0.8	–	V_{DD} + 0.3	V	
$V_{SO(LOW)}$	MISO Low-side Output Voltage - $I_{SO(LOW)}$ = 1.6 mA	–	–	0.40	V	
C_{IN}	Input Capacitance on SCLK, MOSI, Tri-state MISO	–	–	20	pF	(16)

Notes

16. Guaranteed by characterization in the development phase, parameter not tested.

3.3 Dynamic electrical characteristics

Table 6. Dynamic electrical characteristics

Characteristics noted under conditions T_{CASE} = -40 °C to 125 °C, Battery Voltage = 3.5 V to 28 V DC (VBATP = 2.5 V to 27 V DC), unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Switch input						
$t_{PULSE(ON)}$	Pulse Wetting Current Timer - Normal Mode	18	–	22	ms	(17)
$t_{INT-DLY}$	Interrupt Delay Time - Normal Mode	–	–	16	µs	(17)
$t_{SCAN\ TIMER}$	Scan Timer Accuracy - Low-power Mode	–	–	20	%	(17)
$t_{INT\ TIMER}$	Interrupt Timer Accuracy - Low-power Mode	–	–	20	%	(17)
$t_{TSCAN\ TIME}$	Tscan Timer (time actual polling takes place) - Low-power Mode	44	55	66	µs	(17)
$t_{GLITCH\ TIMER}$	Glitch Filter Timer - Normal Mode	–	–	9.1	µs	(18)
Digital interface timing						
f_{OP}	Transfer Frequency	–	–	6.25	MHz	(18)
t_{SCK}	SCLK Period - 1	160	–	–	ns	(17)
t_{LEAD}	Enable Lead Time - 2	140	–	–	ns	(17)
t_{LAG}	Enable Lag Time - 3	50	–	–	ns	(17)
t_{SCKHS}	SCLK High Time - 4	56	–	–	ns	(17)
t_{SCKLS}	SCLK Low Time - 5	56	–	–	ns	(17)
t_{SUS}	MOSI Input Setup Time - 6	16	–	–	ns	(17)
t_{HS}	MOSI Input Hold Time - 7	20	–	–	ns	(17)
t_A	MISO Access Time - 8	–	–	116	ns	(17)
t_{DIS}	MISO Disable Time - 9	–	–	100	ns	(17)
t_{VS}	MISO Output Valid Time - 10	–	–	116	ns	(17)
t_{HO}	MISO Output Hold Time (No cap on MISO) - 11	20	–	–	ns	(17)
t_{RO}	Rise Time (Design Information) - 12	–	–	30	ns	(17)
t_{FO}	Fall Time (Design Information) - 13	–	–	30	ns	(17)
t_{CSN}	CS_B Negated Time - 14	500	–	–	ns	(17)
Supply, voltage regulator, reset						
$t_{S\_LOW1/2\ DGLT}$	VBATP Undervoltage Detector Threshold Deglitcher	30	50	100	µs	(17)
$t_{RST-DGLT}$	Deglitcher Time to Set Reset Pin Low	–	10	20	µs	(18)
VPREGATE						
$t_{VPREMST}$	VPREGATE (mode select) Time	–	150	–	µs	(17)

Notes

17. Guaranteed by CZ. Parameter not tested in production. All SPI timing is performed with a 100 pF load on MISO, unless otherwise noted.
18. Guaranteed by design.

Table 6. Dynamic electrical characteristics (continued)

Characteristics noted under conditions T_{CASE} = -40 °C to 125 °C, Battery Voltage = 3.5 V to 28 V DC (VBATP = 2.5 V to 27 V DC), unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
VPRE						
V_{PRESS}	VPRE Soft start Ramp cap. = 57 µF	5.0	12	25	V/ms	
VDD regulator						
V_{DD_SS}	VDD Soft Start Ramp - C_{VDD} = 10 µF; I = 10 mA	5.0	12	25	V/ms	
VAUX regulator						
V_{AUX_SS}	VAUX Soft Start Ramp (non-tracking mode) - C_{VAUX} = 10 µF; I = 10 mA	5.0	12	25	V/ms	
V_{AUX_SSTR}	VAUX Soft Start Ramp (tracking mode) - C_{VAUX} = 10 µF; I = 10 mA	5.0	–	25	V/ms	
Reset pulse duration						
$t_{RST-PULSE}$	V_{DD} Undervoltage (SPI selectable) • Short, default at power ON when BATFAIL bit set • Medium • Medium long • Long	 – – – –	 1.0 5.0 10 20	 – – – –	ms	(19)
t_{RST-WD}	Watchdog Reset	–	1.0	–	ms	(19)
AMUX output						
$t_{AMUX-VALID}$	AMUX Access Time (Selected output to selected output) • CMUX = 1.0 nF Rising edge of CS_B to selected	–	20	–	µs	(20)
$t_{AMUX-VALID}$	AMUX Access Time (Tri-state to ON) • CMUX = 1.0 nF Rising edge of CS_B to selected	–	–	20	µs	
Oscillator						
$t_{OSC-TOL}$	Oscillator Tolerance	-5.0	–	5.0	µs	
Interrupt						
$t_{INT-PULSE}$	INT pulse duration (refer to SPI) • Short • Medium	 – –	 25 100	 – –	µs	(19)

Notes

19. Guaranteed by design.
20. AMUX settling time to be within 10 mV accuracy. $AMUX_{VALID}$ is dependent of the voltage step applied on the source SGx pin, or the difference between the first and second channel selected as the multiplexed analog output. See Figure 10 for a typical AMUX access time versus voltage step waveform.

Table 6. Dynamic electrical characteristics (continued)

Characteristics noted under conditions T_{CASE} = -40 °C to 125 °C, Battery Voltage = 3.5 V to 28 V DC (VBATP = 2.5 V to 27 V DC), unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
CAN dynamic characteristics						
t_{DOUT}	TXD Dominant State Timeout	0.8	1.8	2.8	ms	
t_{DOM}	Bus Dominant Clamping Detection	0.8	1.6	2.8	ms	
t_{LRD}	Propagation Loop Delay TXD to RXD, recessive to dominant (Slew rate 0)	60	120	210	ns	
t_{TRD}	Propagation Delay TXD to CAN, recessive to dominant	–	70	110	ns	
t_{RRD}	Propagation Delay CAN to RXD, recessive to dominant	–	45	140	ns	
t_{LDR}	Propagation Loop Delay TXD to RXD, dominant to recessive	100	120	255	ns	
t_{TDR}	Propagation Delay TXD to CAN, dominant to recessive	–	75	150	ns	
t_{RDR}	Propagation Delay CAN to RXD, dominant to recessive	–	50	140	ns	
LIN 1-4 physical layer: driver characteristics for normal slew rate - 20.0 kBit/sec according to lin physical layer specification bus load R_{BUS} and C_{BUS} 1.0 nF/1.0 k, 6. nF/660, 10 nF/500. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. (21)						
D1	Duty Cycle 1: • THREC (max) = 0.744 * V_{BATP} • THDOM (max) = 0.581 * V_{BATP} • D1 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 50 µs, 7.0 V ≤ VBATP ≤ 18 V	0.396	–	–		
D2	Duty Cycle 2: • THREC (min.) = 0.422 * V_{BATP} • THDOM (min.) = 0.284 * V_{BATP} • D2 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 50 µs, 7.6 V ≤ VBATP ≤ 18 V	–	–	0.581		
LIN physical layer: driver characteristics for slow slew rate - 10.4 kBit/sec according to lin physical layer specification (48), (50) bus load R_{BUS} and C_{BUS} 1.0 nF/1.0 k, 6.8 nF/660, 10 nF/500. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. (22)						
D3	Duty Cycle 3: • THREC (max) = 0.778 * V_{BATP} • THDOM (max) = 0.616 * V_{BATP} • D3 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.0 V ≤ VBATP ≤ 18 V	0.417	–	–		
D4	Duty Cycle 4: • THREC (min.) = 0.389 * V_{BATP} • THDOM (min.) = 0.251 * V_{BATP} • D4 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.6 V ≤ VBATP ≤ 18 V	–	–	0.59		
LIN physical layer: driver characteristics for fast slew rate						
BR_{FAST}	LIN Fast Slew Rate (Programming mode)	–	20	100	kBits/s	

Notes
21. See Figure 4.
22. See Figure 5.

Table 6. Dynamic electrical characteristics (continued)

Characteristics noted under conditions T_{CASE} = -40 °C to 125 °C, Battery Voltage = 3.5 V to 28 V DC (VBATP = 2.5 V to 27 V DC), unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
LIN physical layer: characteristics and wake-up timings, VBATP from 7.0 V to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF/1.0 k, 6.8 nF/660, 10 nF/500. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. (23)						
t_{REC_PD}	Propagation Delay of Receiver, t_{REC_PD} = MAX (t_{REC_PDR}, t_{REC_PDF})	–	4.2	6.0	µs	
t_{REC_SYM}	Symmetry of Receiver Propagation Delay, t_{REC_PDF} - t_{REC_PDR}	-2.0	–	2.0	µs	
t_{PROPWL}	Bus Wake-up Deglitcher (Sleep and Stop modes) (See Figure 9 for Sleep and Figure 11 for Low-power mode.)	42	70	95	µs	(24)
t_{WAKE_SLEEP} t_{WAKE_STOP}	Bus Wake-up Event Reported • From Sleep Mode • From Stop Mode	 – 9.0	 250 27	 – 35	µs	(24)
t_{TXDDOM}	TXD Permanent Dominant State Delay	0.65	1.0	1.35	s	(24)

Notes
23. See Figure 6 and Figure 7.
24. Guaranteed by characterization.

3.4 Timing diagrams

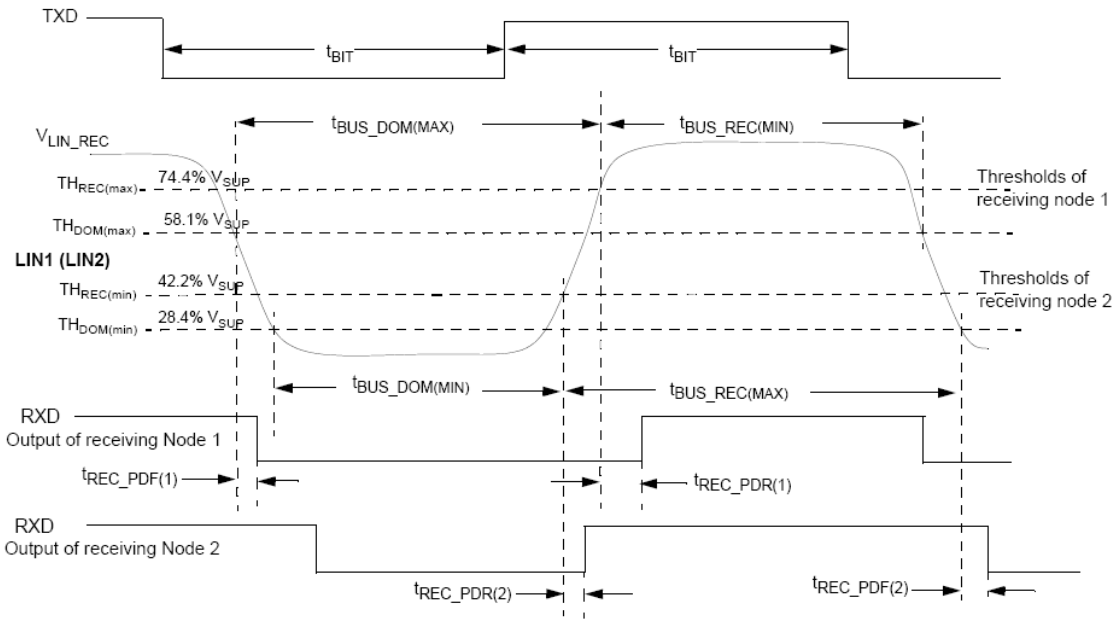


Figure 4. LIN timing measurements for normal slew rate

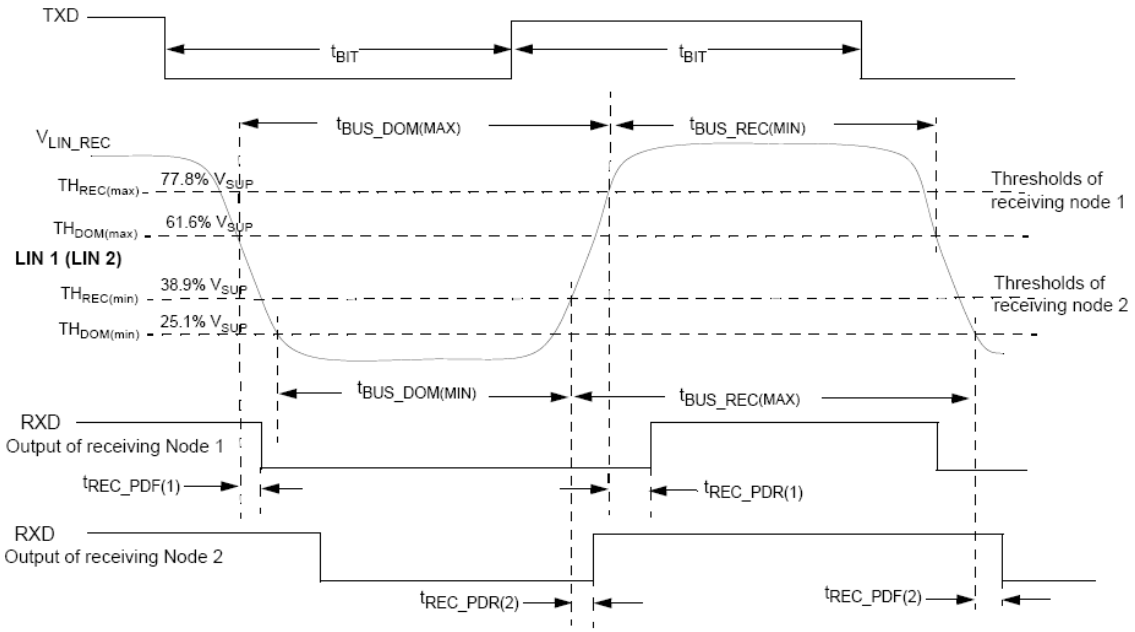


Figure 5. LIN timing measurements for slow slew rate

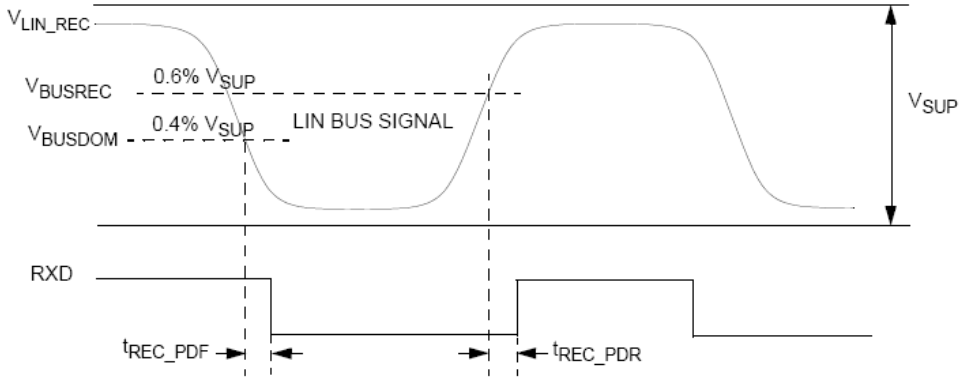


Figure 6. LIN receiver timing

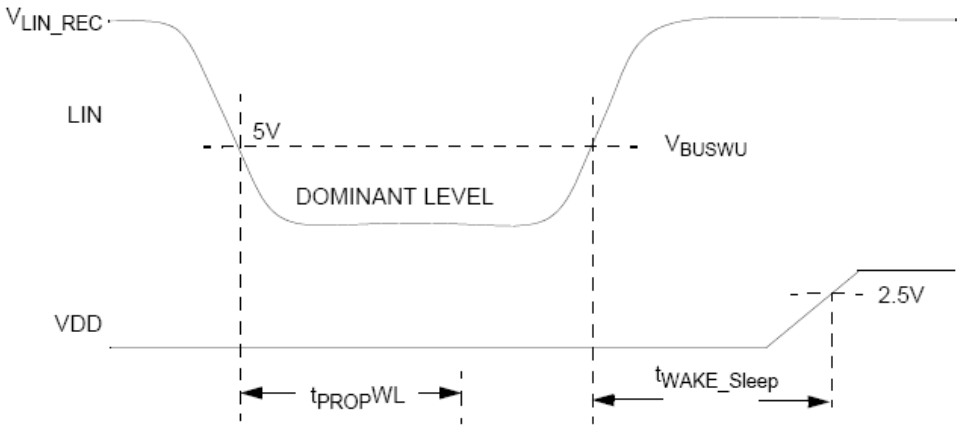


Figure 7. LIN wake-up timing from low-power V_{DD} off mode

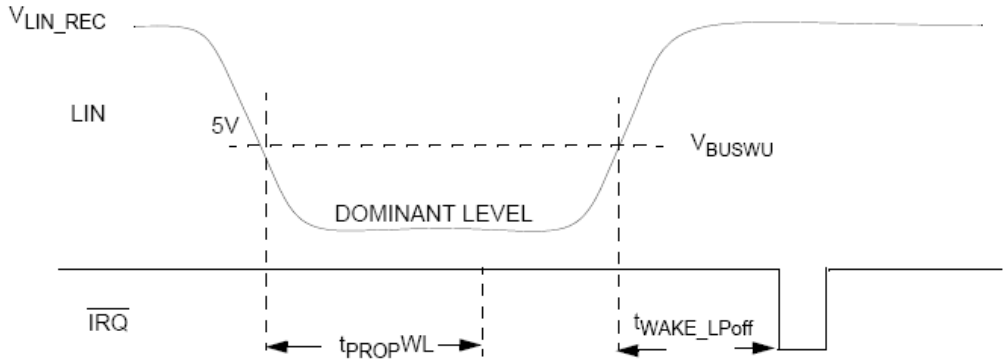


Figure 8. LIN wake-up timing from low-power V_{DD} on mode

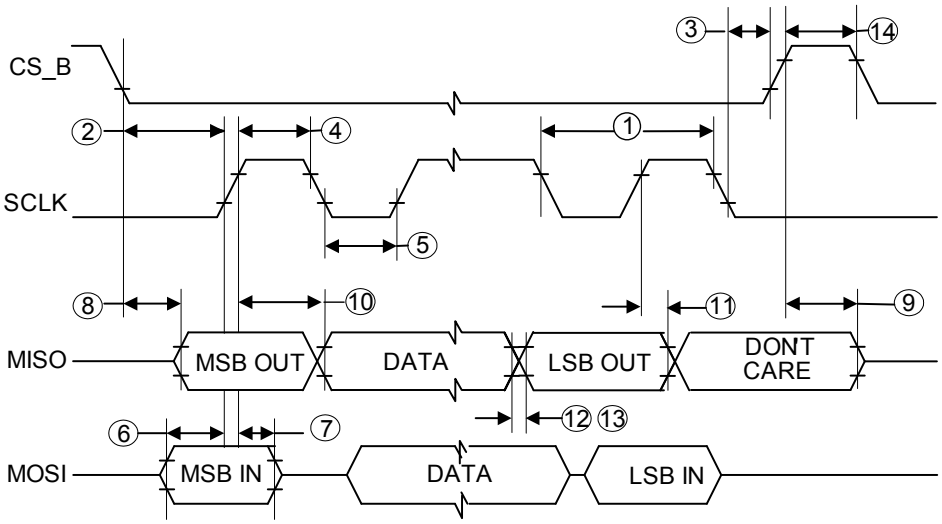


Figure 9. SPI timing diagram

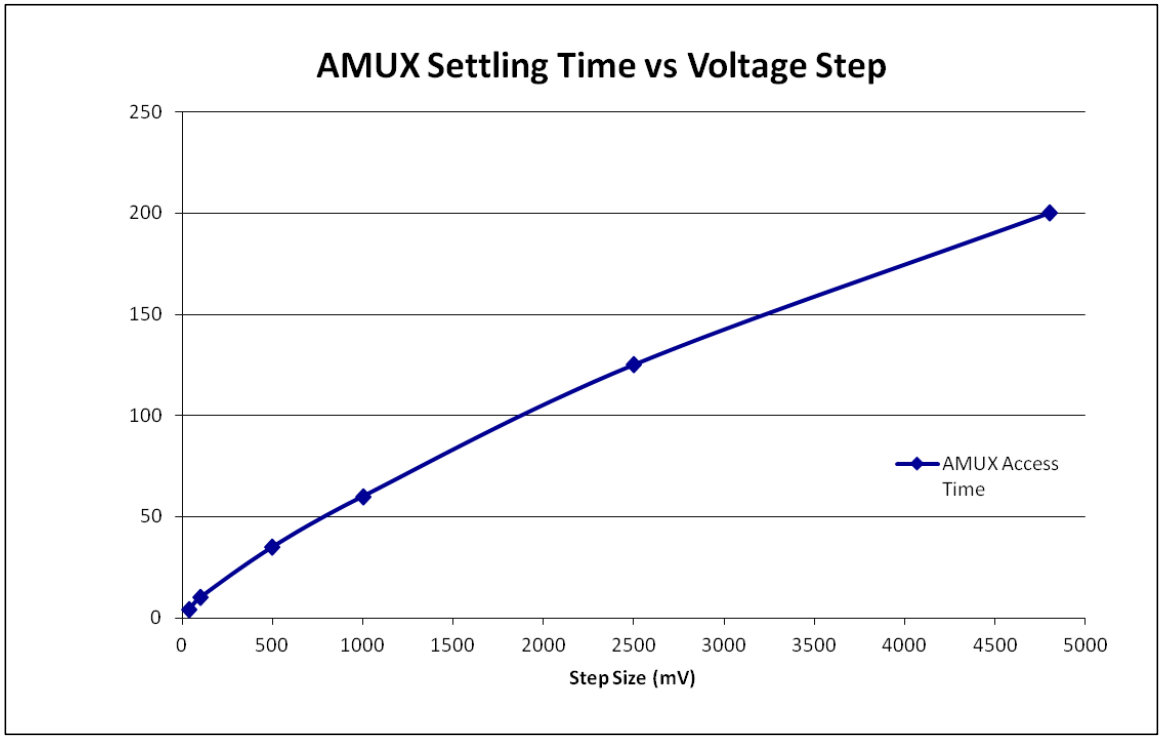


Figure 10. AMUX access time

4 Functional device operation

4.1 Battery voltage ranges

The 33909 device operates from 3.5 V ≤ Battery ≤ 36 V (2.5 V ≤ VBATP ≤ 35 V) and can survive to 41 V Battery. Overvoltage kicks in at VBATP > 35 V and shuts down main functions of the IC. Battery voltages in excess of 41 V must be clamped externally in order to protect the IC from destruction. The VBATP pin must be isolated from the main battery node by a diode.

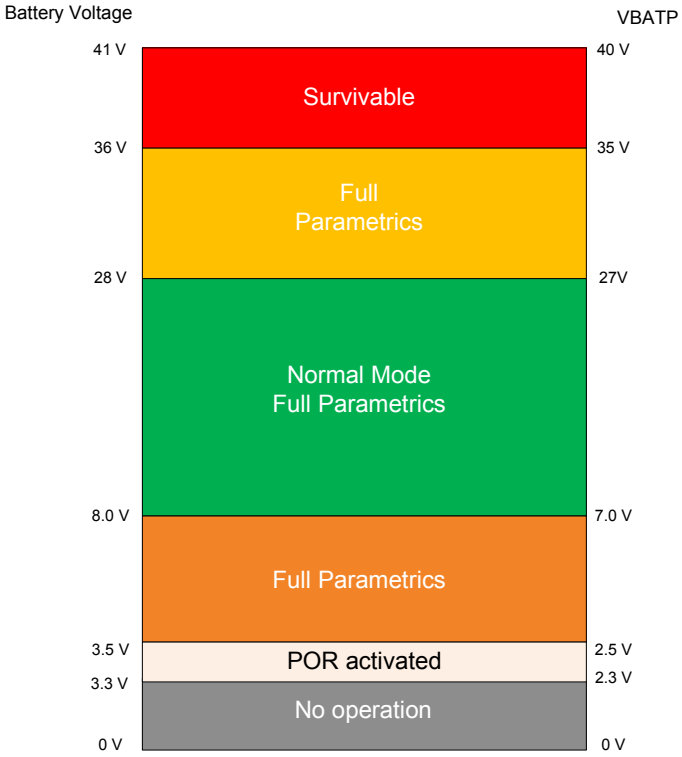


Figure 11. 33909 (buck - boost mode) battery diagram

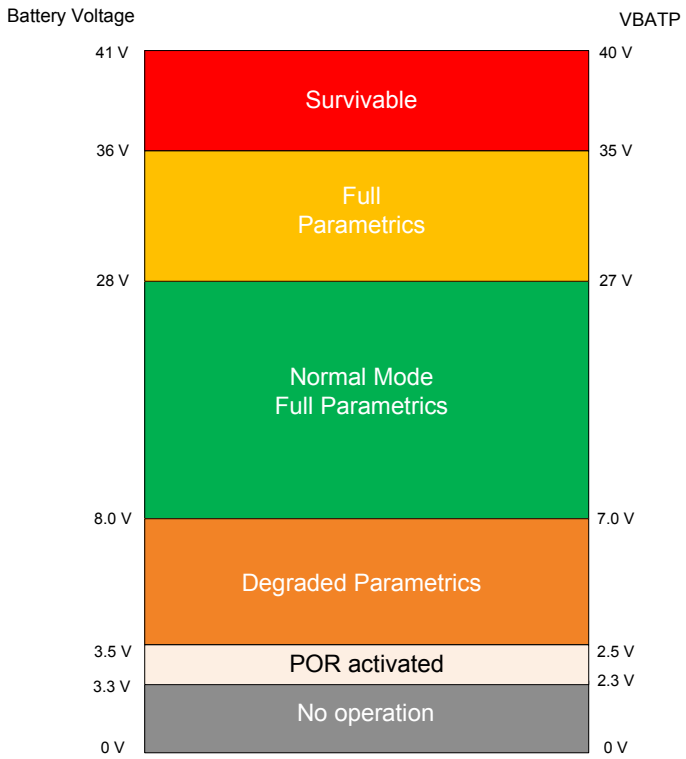


Figure 12. 33909 (buck only mode) battery diagram

4.1.1 POR

A Power On Reset occurs between 2.3 V < VBATP < 2.5 V. The 33909 is held in reset when V_{BATP} < PORFALLING. The 33909 re-initializes after the POR is de-asserted (VBATP_MIN_SU).

4.1.2 No operation

No operation in this range. The device does not send or receive SPI commands, and must reset properly upon leaving this range (when battery is supplied). No unintended leakage currents flows causing undesired effects.

4.1.3 Start-up requirements

Upon application of voltage to the VBATP node, the IC does not supply the VDD and VAUX voltage rails until all parameters can be guaranteed. Internal circuitry can power up and begin to function, but the supply rails remain OFF until a stable output voltage (VDD and VAUX) can be supplied. A typical voltage of 7.2 V on VBATP is expected to be the value where V_{DD} and V_{AUX} would be able to regulate within specified range (another voltage may be determined to be the correct value, 7.0 V is a guide). This allows the micro to power up in a known state with no glitches due to the power supply.

Upon startup of the VDD and VAUX rails, a soft start circuit limits the turn ON time of the rails (15 V/ms typical - d_{VDD}/dt), to reduce the overshoot of the regulated voltages. Figure 13 shows the desired waveform for the startup of the V_{DD} and V_{AUX} supplies.

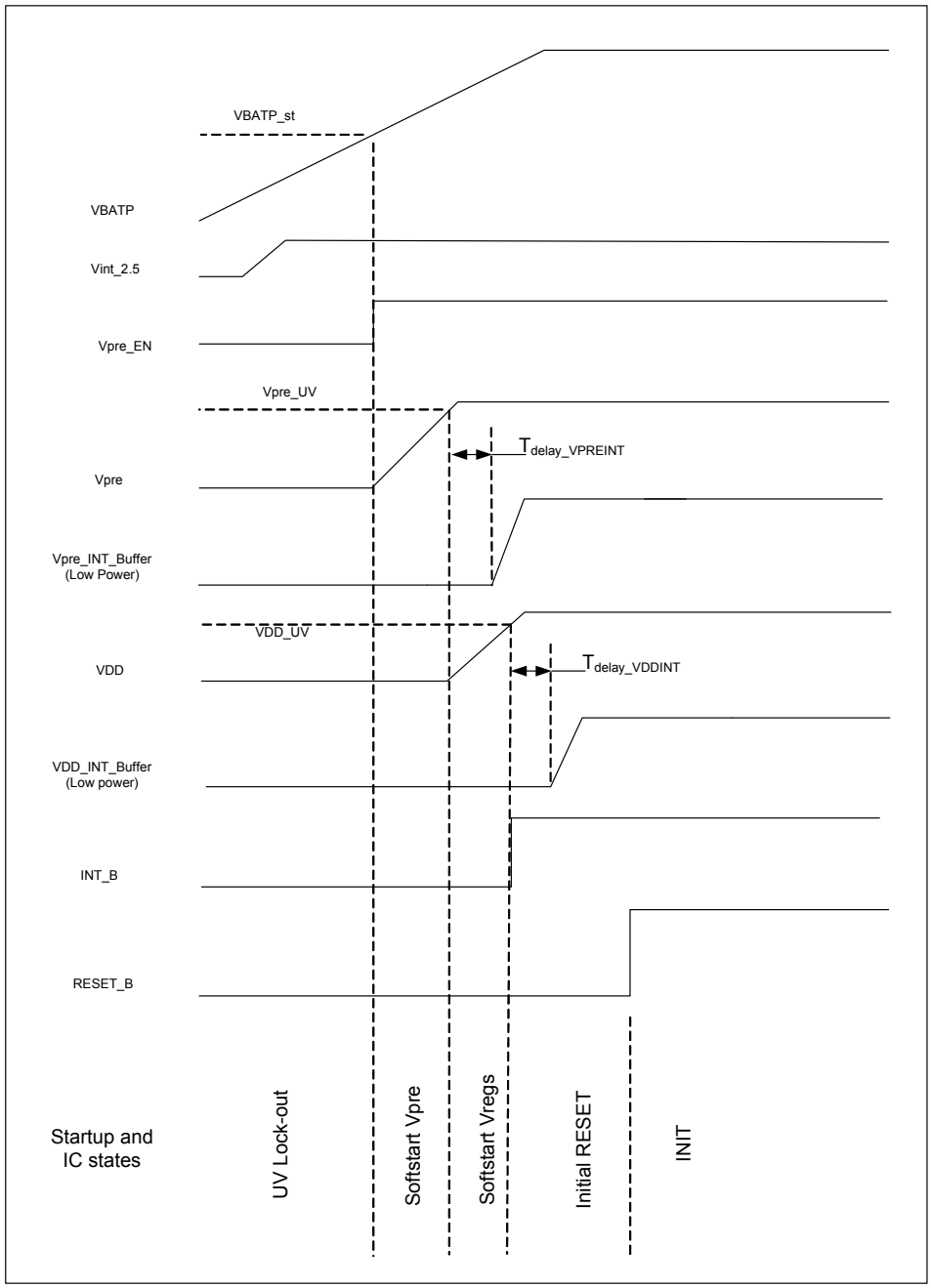


Figure 13. Power up sequencing

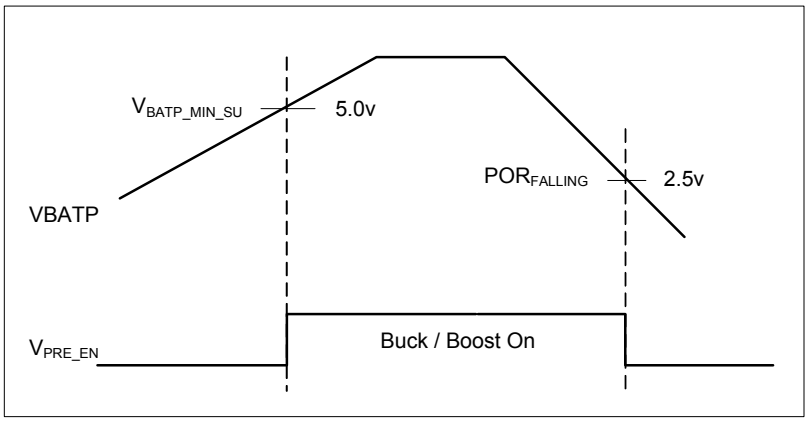


Figure 14. VBATP start-up and POR

4.1.4 Power supply functional block

This block has the V_{BATP} supply and V_{PRE} supply as an input. The internal 2.5 V rail is generated in this block. Power On Reset (POR), Sleep mode power, and the Bandgap reference are controlled here as well.

4.2 Input functional block

There are six Switch-to-Ground inputs used to detect switch closures and provide wetting current. The main functions of this block is to detect a change of state at the input via a 3.5 V (typical) comparator, provide a signal to the main logic to issue an interrupt signal, and also provide wetting/sustain current for the switch. A SPI read allows the micro to know the status of all the inputs.

4.2.1 SG inputs

The SG inputs are switch to ground detect inputs with a comparator threshold (VICTHR - 3.5 V typical). A closed switch is a switch shorted to ground (or otherwise below the VICTHR value) and is reported via the SPI as a logic 1. An open switch is any condition causing the input voltage to rise above the VICTHR value, and is reported via the SPI as a logic 0. In the case where the user needs a Switch to Battery, the user must take note that the IC reports a logic 1 when the input voltage is less then VICTHR. The inputs also provide a wetting current output with selectable values ranging from 6.0 to 20 mA (I_{WETX}) in steps of 2.0 mA. A sustain ($I_{SUSTAIN}$) current level is used to decrease power consumption in the IC. The current sources are pull-up sources with a reference of V_{PRE}. A blocking diode is in series with the current source to block voltages at the input greater than the V_{PRE} from back feeding into the IC. Due to this diode, the maximum voltage the SGx pins can pull up to is ~ 6.5 V (V_{PRE}) - 1 diode drop (~0.7 V) for a final value of ~5.7 V. This use greatly benefits the power consumption of the input current sources, but does limit headroom when using the current sources to drive external loads. V_{PRE} voltage is supplied during Normal (via the SMPS) and Low-power modes (via internal linear). Battery voltages below 7.0 V are not supported in Low-power mode.

All register settings programmed in Normal mode are remembered in Sleep mode. The current used to detect open switches in Low-power mode is ~1.0 mA. Upon leaving Low-power mode the programmed settings are used.

In Low-power mode, the inputs do not use the typical 3.5 V switch threshold. Rather a comparison threshold is used to measure the beginning of the t_{SCAN} time (before the LPM current source is turned on) and after the t_{SCAN} timer (typical 55 µs) has completed. If this voltage has passed the low-power switch detection threshold (typ 210 mV), the IC detects an open switch and compares to the internal logic to determine if a change of state has occurred.

Figure 16 describes the state diagram for the SGx inputs and how they move from state to state. Of note is the three times retry of the wetting current (I_{PRGM} in this notation) in case of a t_{LIM}. This allows for one time thermal events to be dealt with and still operate normally when able. After three times t_{LIM}, the input goes to tri-state and wait for the user to clear the t_{LIM} fault via the SPI word.

In the case where a SAFE mode operation would like to sense the key OFF condition of the module, SG0 is used in conjunction with the WDI pin to facilitate the SAFE operation and turn OFF the V_{DD} supply.

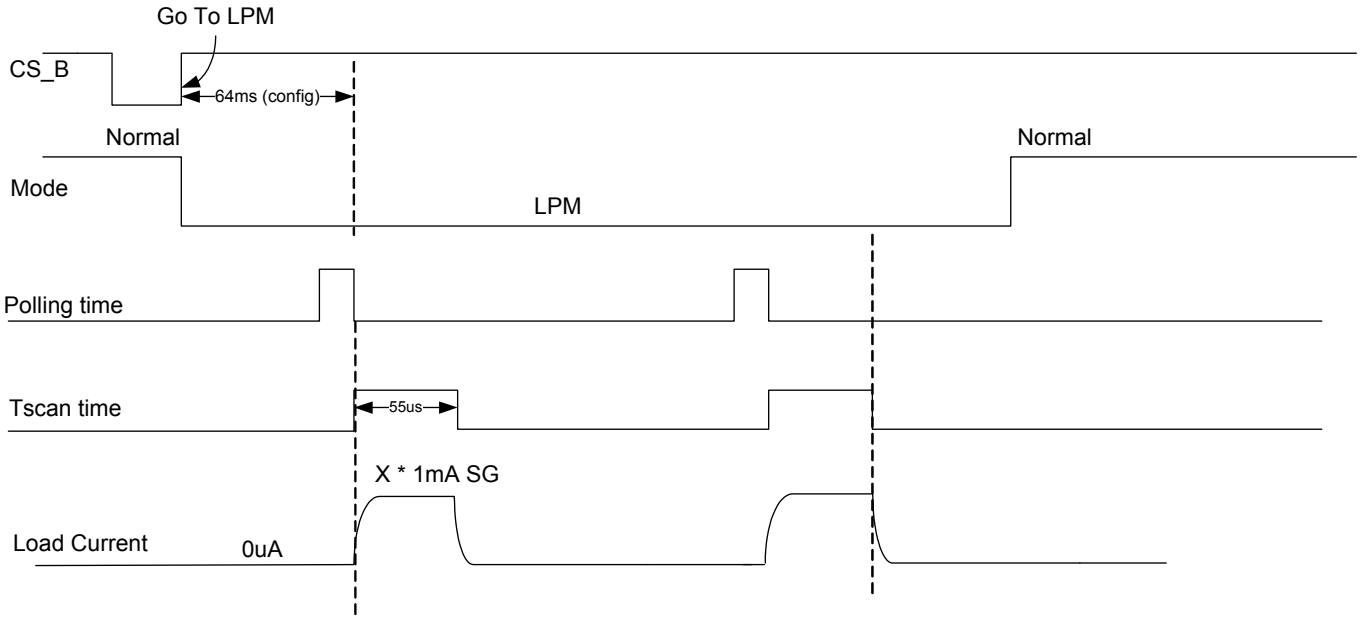
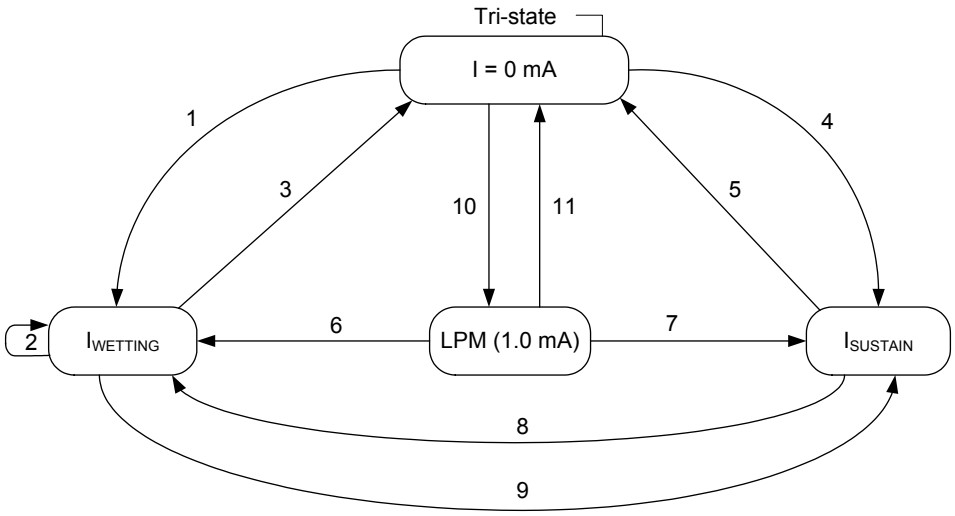


Figure 15. Low-power mode typical timing diagram



1) Change from 0 mA to Wetting current value: Wetting current programmed to all time or Pulsed Mode and untristate the input.
2) Maintain Wetting current: When switch is closed to ground and 20 ms timer not expired (wetting current timer enabled).
3) Change from Wetting Current to 0 mA: Go to Low Power mode (LPM) or Tri-state command sent.
4) Change from 0 mA to Sustain current (2.0 mA): Wetting current off command sent and untri-state.
5) Change from Sustain current to 0 mA: Go to LPM or Tri-state command
6) Change from LPM to Wetting current: Wake-up and not in Wetting current off mode.
7) Change from LPM to Sustain current: Wake-up and in Wetting current off mode.
8) Change from Sustain to Wetting current: Switch opens and wetting current timer on or a SPI message to turn Wetting current on.
9) Change from Wetting current to Sustain: Closed switch and timer expired or a SPI message turning Wetting current off.
10) Change from 0 mA to LPM current: During active scan timer (100 us long) in LPM (Periodic sense).
11) Change from LPM current to 0 mA: During inactive scan timer in LPM.

Note 1. Three Tlim instances on the SG sensor puts the device into Sustain only mode for the SGs. A SPI read clears the function and allows wetting current to be active again.
Note 2. Overvoltage on the VBATP pin causes the SG inputs to switch to Sustain only until the overvoltage condition is gone.
Note 3. A POR results in the IC resetting and the SG inputs back in the Tri-state condition.

Figure 16. 33909 SG state diagram

4.2.1.1 Alternative functions of the SG0 pin

There are some additional functions for SG0. These functions are described in the block most closely associated with their additional functions.

1. SG0 can be used in conjunction with the SAFE mode to determine how the IC should operate when a SAFE condition is detected. See Table 7 for information on SAFE mode operation.

4.2.2 SG input pin functions: SGx

Each input pin is the connection used by the user to determine the state of the switch, and source the wetting and sustain currents. A capacitor is required on the input with a minimum value of 47 nF (CAPSG) and a maximum capacitance of 100 nF. Characterization of the input defines the available capacitor range.

4.2.3 Oscillator and timer control functional block

The oscillator is generated in this block. All timers are generated from the reference oscillator. The oscillator is trimmed to ±5.0%. There is no external pin for the oscillator and timer control block. The 5.0% oscillator is turned OFF in Low-power mode to reduce quiescent current.

A second oscillator is used in Low-power mode. The oscillator operates at 200 kHz and is accurate to 20%. All of the Low-power mode timers are based on this Low-power oscillator.

4.2.4 TLIM functional block

The device has multiple tlim cells to detect thermal excursions. An independent t_{LIM} cell exists for multiple circuit blocks including:

1. CAN regulator
2. VPRE circuitry
3. SG inputs
4. LIN cells

The corresponding block contains the description of what occurs when t_{LIM} is seen by the related circuitry. Hysteresis for each cell is used to keep the device from cycling. There is no external pin connection for the t_{LIM} functional block.

4.2.4.1 INT_B functional block

This block is used to alert the micro to a change of state on an input. The INT_B pin is an interrupt output from the 33909 device. The INT_B pin is an open-drain output with an internal pull-up to V_{DD}. In Normal mode, a switch state change triggers the INT_B pin (when enabled). The INT_B pin and INT_B bit in the SPI register are latched on the falling edge of CS_B. This permits the MCU to determine the origin of the interrupt. The INT_B pin is cleared on the rising edge of CS_B. The INT_B pin does not clear with rising edge of CS_B if a switch contact change has occurred while CS_B was LOW.

4.2.5 INT_B pin functions: INT_B

The INT_B output is asserted low or drives a pulse when an interrupt condition occurs. The INT condition is enabled in the INT register. The INT_B operation (assertion of a low level or a pulse) is defined by the SPI.

4.2.6 SAFE_B functional block

This mode is entered when specific fail conditions occur. The “Safe state” condition defaults to condition A in Table 7. A SPI word can then be used to modify the operation as found in Table 7. Safe mode is entered after additional event or conditions are met: timeout for CAN communication. Exit of the Safe state is always possible by a wake-up event: in the safe state the device is automatically wakeable CAN. Upon wake-up, the device operation is resumed: enter in Reset mode.

4.2.6.1 Debug detect

The operation of the SAFE_B block is determined by the state of the WDI pin and the associated resistance to ground is supplied external to the IC. The IC is put into watchdog inhibit mode when the voltage at the WDI pin is > 10 V. This results in a SAFE mode A, but no watchdog refresh is needed.

The debug detect circuit measures an external pull-down resistor on the WDI. Three thresholds exist (excluding the Test mode) and outputs to the logic block, in which mode the SAFE_B block should operate (Mode<B3:A>). The mode is read in by determining the resistor value on the WDI pin at power ON only (during the INIT RESET node), and remains in this state until a new power ON sequence is detected.

4.2.6.2 Fail-safe operation

4.2.6.2.1 Fail-safe functionality

Upon a dedicated event or issue, detected at a device pin (i.e RESET), the Safe mode can be entered. In this mode, the SAFE_B pin is active low.

4.2.6.2.2 Description

Upon activation of the SAFE_B pin, and if the failure condition which caused the activation of SAFE_B has not recovered, the device can help to reduce ECU consumption, assuming the MCU is not able to set the whole ECU in Low-power mode.

Two main cases are available:

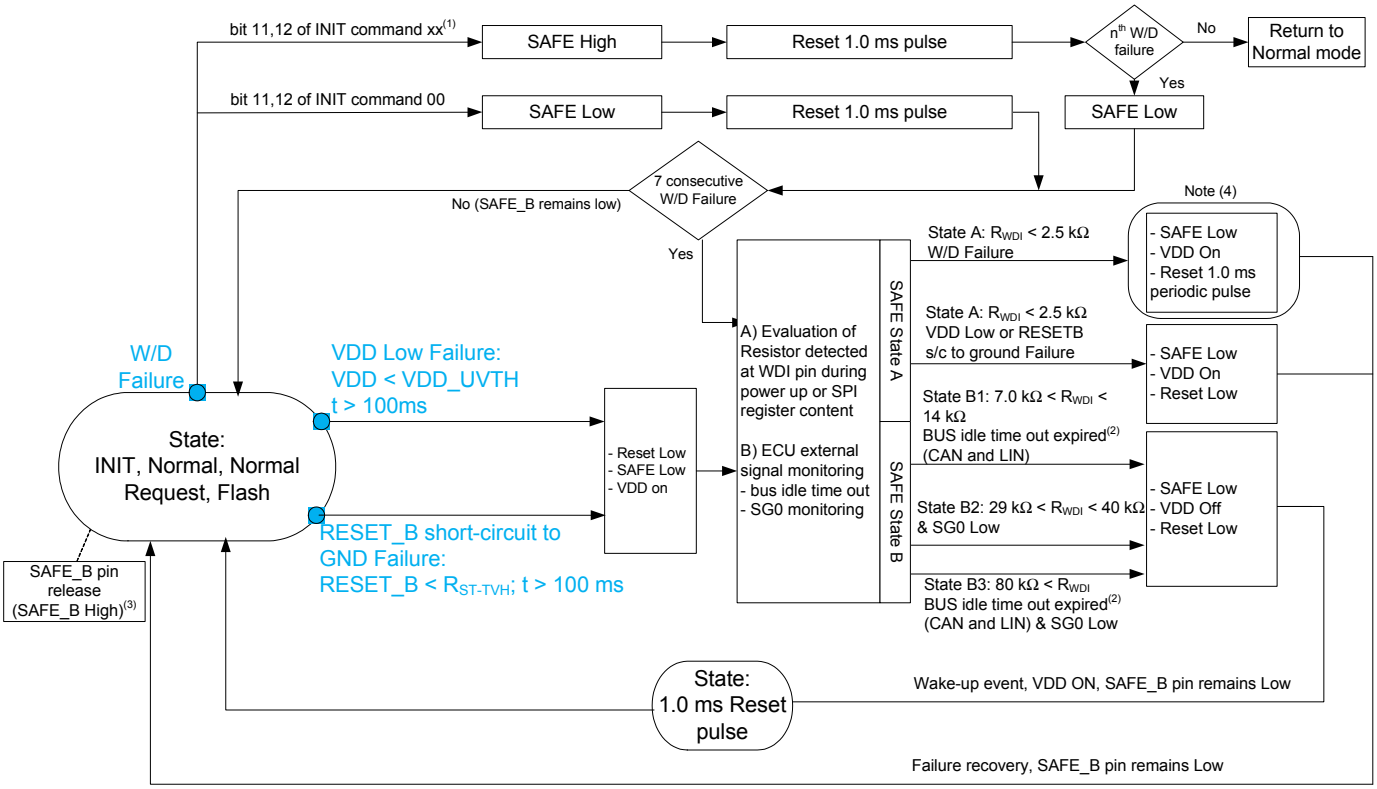
- Upon SAFE_B activation, the MCU remains powered (V_{DD} stays ON), until the failure condition recovers (i.e S/W is able to properly control the device and properly refresh the W/D).
- Upon SAFE_B activation, the system continues to monitor external events, and disable the MCU supply (turn V_{DD} off). The external events monitored are: SG0 switch to ground and CAN and LIN traffic. For this condition, three sub cases exist: B1,B2, B3.

Note: CAN and LIN traffic bus idle indicates the ECU of the vehicle is no longer active, thus the car is being parked and stopped.

SAFE_B mode code	V_{DD} status
A	Remains ON
B1	Turn OFF 8 sec. after CAN and LIN traffic bus idle detection.
B2	Turn OFF when the SG0 switch is closed to ground.
B3	Turn OFF 8 sec. after CAN and LIN traffic bus idle detection when SG0 low level is detected.

Exit of the safe state with V_{DD} OFF is always possible by a wake-up event: in this Safe state the device is automatically wakeable with CAN and the SG0 input. Upon wake-up, the device operation is resumed: enter in Reset mode. The SAFE_B pin remains active, until a proper read and clear of the SPI flags reporting the SAFE_B conditions.

Figure 17 illustrates the SAFE_B mode activation and the power consumption reduction after CAN traffic idle time.



Notes:
1) Bits 11 and 12 of the INIT command control the number of times a reset / Watchdog failure should occur nth time: 00 = 1st time, 01 = 2nd time, 10 = 3rd time, 11 = 5th time.
2) 8 second timer for bus idle time out.
3) SPI command to release SAFE_B pin after recovery from failure (5F000000).
4) Dynamic behavior: 1.0 ms reset pulse every 256 ms due to no watchdog refresh SPI command and the device state transitions between RESET and Normal Request or INIT RESET and INIT modes.

Figure 17. SAFE operation flow chart

Table 7. SAFE mode operation

State	VDD	CAN5V	VAUX	LINx	SGx	CAN0
Power down	OFF	OFF	OFF	High-impedance	High-impedance	High-impedance
Init Reset	ON	OFF	OFF	OFF: internal 30 kΩ pull-up active. Transmitter: receiver/ wake-up OFF.	High-impedance	OFF: CAN termination 25k to GND Transmitter/receiver /wake-up OFF
INIT	ON	OFF	OFF	OFF	High-impedance	OFF
Reset	ON	Keep SPI configuration	OFF	OFF	SPI configuration	OFF
Normal Request	ON	Keep SPI configuration	OFF	OFF	SPI configuration	OFF
Normal	ON	SPI configuration	SPI configuration	SPI configuration	SPI configuration	SPI configuration
Low-power VDDOFF	OFF	OFF	OFF	OFF + wake-up enable/disable	SPI configuration	OFF + wake-up enable/disable
Low-power VDDON	ON	OFF	OFF	OFF + wake-up enable/disable	SPI configuration	OFF + wake-up enable/disable
SAFE_B output low: SAFE_B case A	safe case A: ON safe case B: OFF	A: Keep SPI configuration, B: OFF	OFF	OFF + wake-up enable	SPI configuration	OFF + wake-up en
FLASH	ON	SPI configuration	SPI configuration	OFF	SPI configuration	SPI configuration

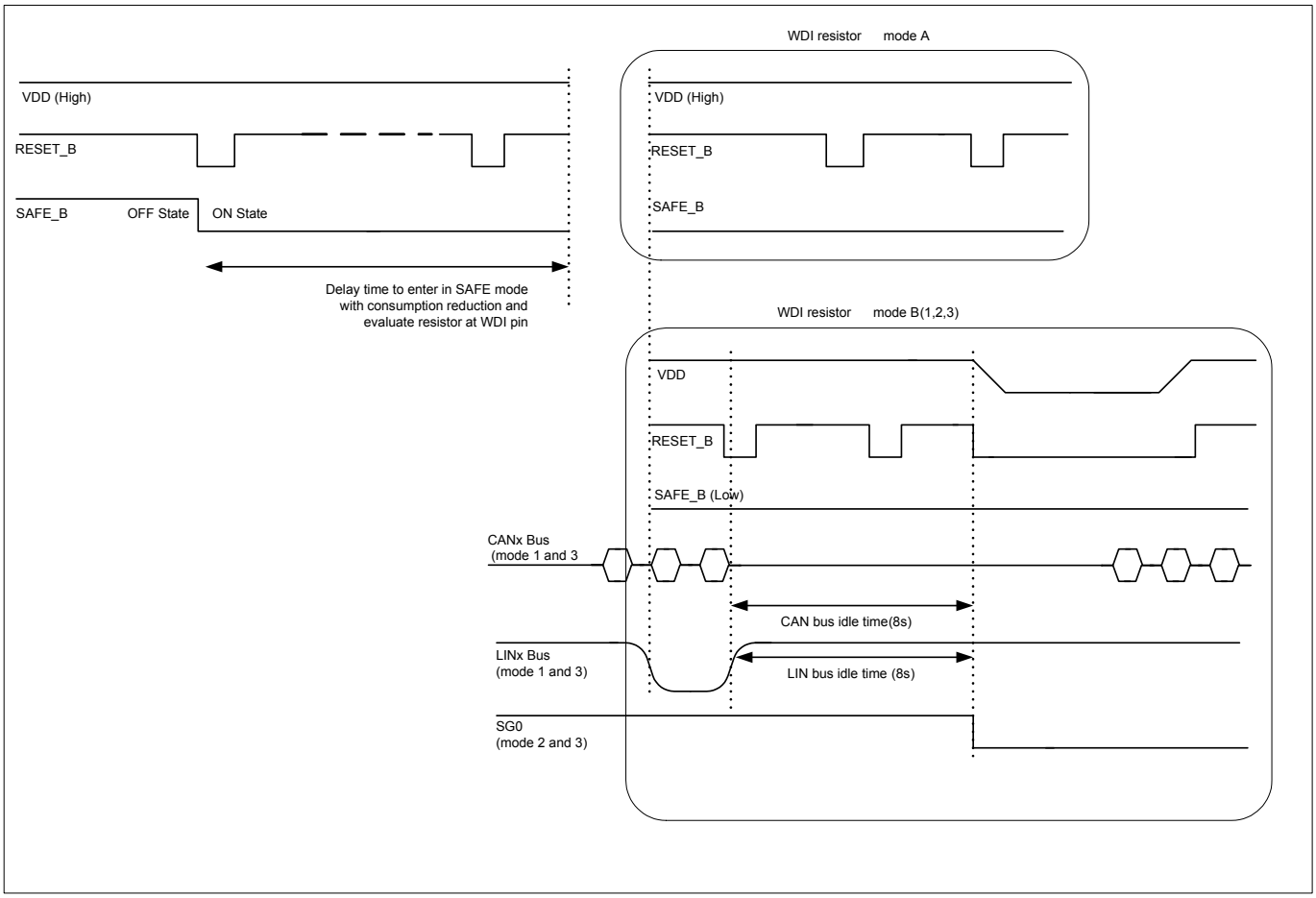


Figure 18. SAFE mode A and B (1, 2, 3)

4.2.6.3 SAFE_B pin functions: SAFE_B

This pin is an output which is asserted low in case a fault event occurs. The objective is to drive electrical safe circuitry outside the MCU and the SBC. This safe circuitry activates the default function of the ECU, independent of the MCU and SBC.

Flexibility is provided to the user to select SAFE output operation via a resistor at the WDI pin. The SAFE output is an open drain structure.

4.2.6.4 SAFE_B pin functions: WDI

This pin is an input used to set the device in Debug mode. When the device is powered up with a voltage at the WDI pin > 10 V, the device enters into Debug mode. In this mode, only a single WD refresh command (SPI 0x47000000) is necessary to put the device in Normal Mode. This allows for easy debugging of the software routine controlling the device.

In addition, a resistor can be connected from the WDI pin to GND to select Fail-safe mode operation.

4.2.7 Watchdog functional block

4.2.7.1 In normal request mode

In Normal Request mode, the device expects to receive a watchdog configuration before the end of the normal request timeout period. This period is reset to a long (256 ms) after power-on and when BATFAIL is set. In Normal Request mode the watchdog operation is “timeout” only and can be triggered/served any time within the period.

4.2.7.2 Watchdog type selection

Two different watchdog modes are implemented: Window or Advance. The selection of “Window” or “Advance” is done in INIT mode, after device power up when the Batfail flag is set. Configuration is done via the SPI. Then the watchdog mode selection content is locked and can be changed only via a secured SPI procedure.

4.2.7.3 Window watchdog operation

The window watchdog is available in Normal mode only. The watchdog period selection can be kept (SPI is selectable in INIT Mode), while the device enters into Low-power Stop mode. The watchdog period is reset to the default long period after BATFAIL.

The period and the refresh of watchdog are done by the SPI. A refresh must be done in the open window of the period, which starts at 50% of the selected period and ends at the end of the period. If the watchdog is triggered before 50%, or not triggered before end of period, a reset has occurred. The device enters into Reset mode.

4.2.7.4 Watchdog in debug mode

When the device is in Debug mode (entered after a POR when the WDI is > 10.0 V), the watchdog continues to operate, but does not affect the device operation by asserting a reset. A single WD refresh command (SPI 0x47000000) is necessary to put the device in Normal Mode. For the user, operation appears without the watchdog once Normal Mode is entered. When Debug is left by software (SPI mode reg.), the watchdog period starts at the end of the SPI command. When Debug mode is left by hardware, when the voltage on the WDI drops below 8.9 V, the device enters into an INIT Reset mode. The WDI pin is discussed in the SAFE_B functional block section.

4.2.7.5 Watchdog in flash mode

During Flash mode operation, the watchdog can be selected to a long timeout period. Watchdog is timeout only and an INT pulse can be generated at 50% of the time window.

4.2.7.6 Advance watchdog operation

When the Advance watchdog is selected (at INIT mode), the refresh of the watchdog must be done using a random number and with 1, 2, or 4 SPI commands. The software must read a random byte from the SBC, then it must return the random byte inverted to clear the watchdog. The random byte write can be done in 1, 2, or 4 different SPI commands.

If 1 command is selected, all 8 bits are written at once.

If 2 commands are selected, first write command must include 4 of the 8 bits of the inverted random byte. The second command must include the next 4 bits. This completes the watchdog refresh.

If 4 commands are selected, the first write command must include 2 of the 8 bits of the inverted random byte. The second command must include the next 2 bits, the 3rd command the next 2, and the last command, the last 2. This completes the watchdog refresh.

When multiple writes are used, the most significant bits are sent first. The latest SPI command needs to be done inside the open window time frame.

4.2.7.7 Detail SPI operation and SPI commands for all watchdog types

In INIT mode, the W/D type is selected using register Init W/D, bits 1, 2, and 3. The W/D period is selected via TIM_A register. The W/D period selection can also be done in Normal mode or in Normal Request mode.

Transition from INIT mode to Normal mode, or from Normal Request mode to Normal mode is done via a single W/D refresh command (SPI 0x47000000).

While in Normal mode, the W/D refresh command depends upon the W/D type selected in INIT mode. These are detailed in the following paragraph:

Simple W/D: refresh commands is 0x47000000. It can be sent any time within the W/D period if the timeout W/D operation is selected (INIT-W/D register, bit 1 WD N/Win = 0). It must be sent in the open window (second half of the period) if the Window Watchdog operation was selected (INIT-W/D register, bit 1 WD N/Win = 1).

4.2.7.8 Advance watchdog

The first time device enters into Normal mode (entry on Normal mode using the 0x47000000 command), the RND code must be read using SPI command 0x0B000000. Device returns on the MISO fourth byte of the RND code. The full 32 bit MISO response is 0xXX0000RD.

Advance Watchdog, refresh by 1 SPI command:

The refresh command is 0x4B0000RD. During each refresh command device returns a new Random Code on MISO. This new random code must be inverted and sent along with the next refresh command, and so on.

It must be done in the open window if the Window operation was selected.

Advance Watchdog, refresh by 2 SPI commands:

The refresh command is split in 2 SPI commands.

The first partial refresh command is 0x4B0000w1, and the second is 0x4B0000w2. Byte w1 contains the first 4 inverted bits of the RD byte plus the last 4 bits equal to zero. Byte w2 contains 4 bits equal to zero plus the last 4 inverted bits of the RD byte.

During this second refresh command, the device returns a new Random Code on MISO. This new random code must be inverted and send along with the next 2 refresh commands and so on.

The second command must be done in the open window if the Window operation was selected.

Advance Watchdog, refresh by 4 SPI commands:

The refresh command is split in 4 SPI commands.

The first partial refresh command is 0x4B0000w1, the second is 0x4B0000w2, the third is 0x4B0000w3 and the last is 0x5Aw4.

Byte w1 contains the first 2 inverted bits of the RD byte plus the last 6 bits equal to zero.

Byte w2 contains 2 bits equal to zero plus the next 2 inverted bits of the RD byte plus 4 bits equal to zero.

Byte w3 contains 4 bits equal to zero plus the next 2 inverted bits of the RD byte plus 2 bits equal to zero.

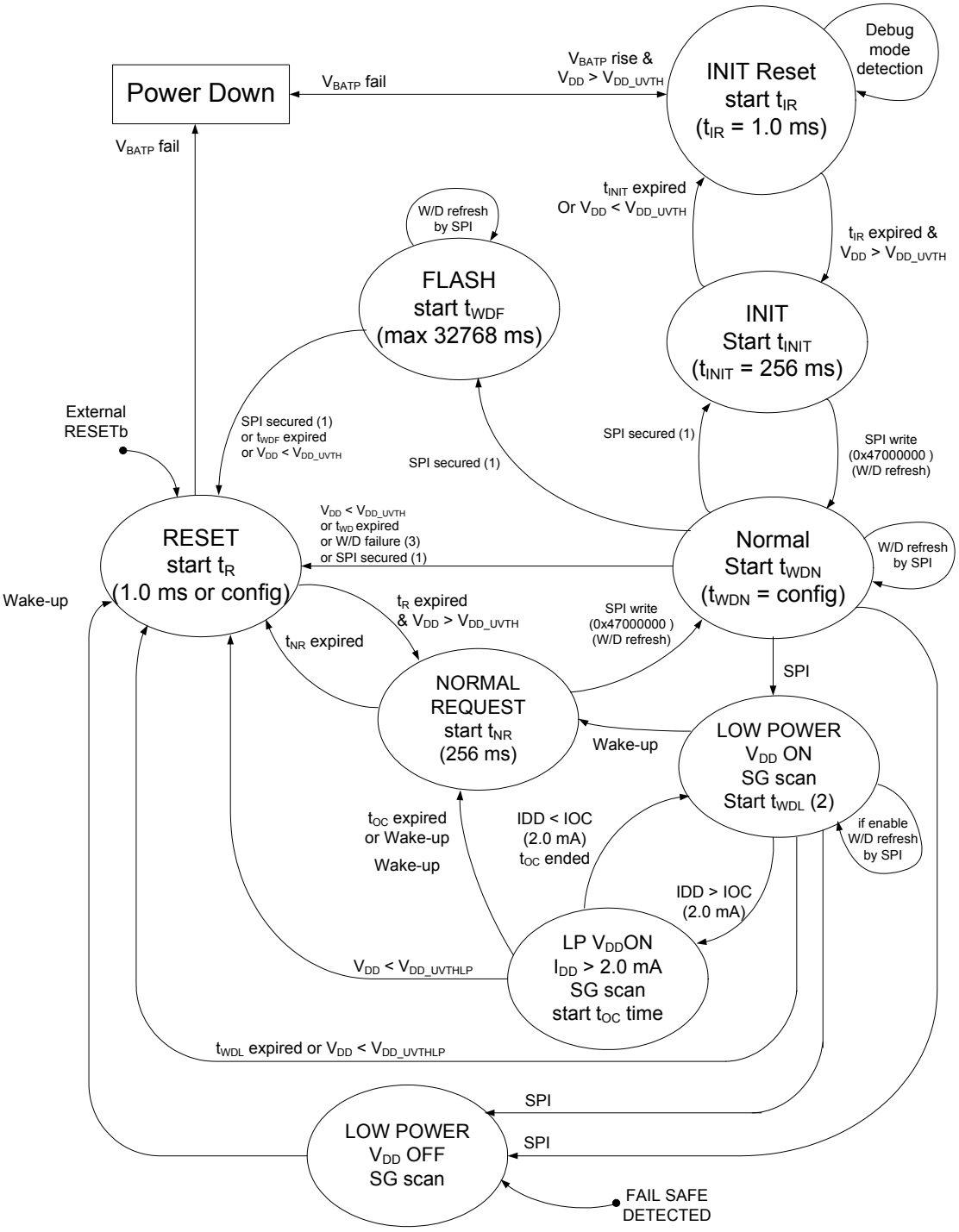
Byte w4 contains 6 bits equal to zero plus the next 2 inverted bits of the RD byte.

During this fourth refresh command, the device returns on MISO a new Random Code. This new random code must be inverted and sent along with the next 4 refresh commands. The fourth command must be done in the open window, if the Window operation was selected.

4.3 Operational modes

4.3.1 Introduction

The device has several operation modes. The transitions and conditions to enter or leave each mode are described in Figure 19.



(1) Refer to “SPI secured” description.
(2) If enabled by SPI prior to entering LP V_{DD} ON mode.
(3) W/D refresh in closed window or enhanced W/D refresh failure.

Figure 19. State diagram

4.3.1.1 INIT reset

This mode is automatically entered after device “power ON”. In this mode, the RST_B pin is asserted low, for a duration of typically 1.0 ms. Control bits and flags are “set” to their default reset condition. The BATFAIL is set to indicate the device is coming from an unpowered condition, and all previous device configurations are lost and “reset” is the default value. The duration of the INIT reset is typically 1.0 ms. INIT reset mode is also entered from INIT mode, if the expected SPI command does not occur in due time (ref. INIT mode)

4.3.1.1.1 INIT

This mode is automatically entered from “INIT reset” mode. In this mode, the device must be configured via the SPI within a time of 256 ms max. One SPI word to configure the INIT registers (three registers called Watchdog, REG, and MISC) must be configured during INIT mode.

Once the INIT registers configuration is done, a SPI Watchdog Refresh command must be sent in order to set the device into Normal mode. If the SPI W/D refresh does not occur within the 256 ms period, the device returns into INIT reset mode for a typical 1.0 ms, and then reenter into INIT mode.

Register read operation is allowed in INIT mode, to collect device status or to read back the INIT register configuration. When INIT mode is left by a SPI Watchdog refresh command, it is possible to reenter the INIT mode only by a secured SPI command.

4.3.1.1.2 Reset

In this mode, the RST_B pin is asserted low. Some bits and flags are reset. Reset mode is entered from Normal mode, from Normal Request mode, from LP V_{DD} ON mode and from Flash mode, when the watchdog is not triggered, or a V_{DD} low condition is detected.

The duration of reset is typically 1.0 ms by default. The user can define a longer Reset pulse activation, only when the Reset mode is entered, following a V_{DD} low condition. Reset pulse is always 1.0 ms, in case the Reset mode is entered due to a wrong watchdog refresh command.

4.3.1.2 Normal request

This mode is automatically entered from Reset mode, or after a wake-up from Low-power V_{DD} ON mode. A watchdog refresh SPI command is necessary to allow a transition to Normal mode. The duration of the Normal request mode is 256 ms maximum duration when Normal Request mode is entered after Reset or when entered from the LP V_{DD} ON mode. If the watchdog refresh SPI command does not occur within the 256 ms, the device enters into Reset mode for a duration of typically 1.0 ms.

4.3.1.2.1 Normal

In this mode, all device functions are available. This mode is entered by a SPI watchdog refresh command from Normal Request mode, or from INIT mode. During Normal mode, the device watchdog function is operating, and a periodic watchdog refresh must occur. In case of an incorrect or missing watchdog refresh command, the device enters into Reset mode.

From Normal mode, the device can be set by a SPI command into Low-power modes (Low-power V_{DD} ON or Low-power V_{DD} OFF). Dedicated secured SPI commands can be used to enter from Normal mode in Reset mode, INIT mode, or Flash mode.

4.3.1.2.2 Debug

Debug is a special operation condition of the device which allows the system easy software and hardware debugging. The debug operation is detected after power up if the WDI pin is set above 10 V.

When debug is detected, all the software watchdog operations are disabled: 256 ms of INIT mode, watchdog refresh of Normal mode and Flash mode of 256 ms, or a user defined timeout of Normal request mode, are not operating and does not lead to a transition into INIT reset or Reset mode.

4.3.1.3 Flash

In this mode, the software watchdog period is extended up to typically 32 seconds. This allows the MCU flash memory to be reloaded, while the software overhead refreshes the watchdog is limited. The Flash mode is left by the SPI command and the device enters into Reset mode. In case of an incorrect or missing watchdog refresh, the command device enters into Reset mode.

4.3.1.3.1 Low-power modes

The device has two main Low-power modes: Low-power mode with V_{DD} OFF, and Low-power mode with V_{DD} ON.

4.3.1.3.2 Low-power - V_{DD} off

In this mode, V_{DD} is turned OFF and the MCU connected to VDD is unsupplied. This mode is entered by the SPI. In order to prevent accidental VDD turn off, a VDDoff en control bit is used. This bit must be set to "1" for Low-power - VDD OFF mode to be activated.It can also be entered by automatic transition due to fail-safe management. The 5 V-CAN and VAUX regulators are also turned off.

When the device is in Low-power V_{DD} OFF mode, it monitors external events to wake-up and leave the LP mode. The wake-up events can occur from:

- CAN bus
- LIN bus
- Expiration of an internal timer
- SG input

When a wake-up event is detected, the device enters into Reset mode and then into Normal Request mode. The wake-up source is reported into the device SPI registers. In summary, a wake-up event from LP V_{DD} OFF, leads to a V_{DD} regulator turn ON, and an MCU operation restart.

4.3.1.3.3 Low-power - V_{DD} on

In this mode, the voltage at the VDD pin remains at 5.0 V (or 3.3 V, depending upon device part number). The objective is to maintain the MCU in a reduced power consumption mode. In this mode, the DC output current is expected to be limited to a few 100 μA or some mA, as the ECU is in reduced power operation mode. The 5 V-CAN and VAUX regulators are turned OFF.

However, in Low-power V_{DD} ON mode, the device is able to deliver several micro amps of current on VDD (up to typ. 2.0 mA). The current delivery can be time limited, by a selectable internal timer. Timer duration is up to 32 ms, and is triggered when the output current exceeds the output current threshold, typically 2.0 mA. This allows, for instance, a periodic activation of the MCU while the device remains in LP V_{DD} ON mode. If the duration exceeds the selected time (ex 32 ms), the device detects a wake-up.

The same wake-up event as in LP V_{DD} OFF mode (CAN, SGx, timer, cyclic sense) are available in LP V_{DD} ON mode. In addition, two additional wake-up conditions are available.

- By a dedicated SPI command (hex 0x49000010).
- Output current from V_{DD} exceeding typically a 2.0 mA threshold, the device wakes up, provided additional conditions are met (timing detection...).
- If V_{DD} maximum load is exceeded (>80 ma), V_{DD} starts to fall. When V_{DD} falls below approximately 1.0 V, the device then wakes up and issue a reset.

Wake-up events are reported to the MCU via a low level pulse at the INT pin. The MCU detects the INT pulse and resume operation.

4.3.1.3.4 Watchdog function in LP V_{DD} on mode

It is possible to enable the watchdog function in low-power V_{DD} ON mode, for timeout functionality.

Refresh of the watchdog is done either by:

- a dedicated SPI command (different from any other SPI command, or simple CS activation, which would wake-up)
- or by a temporary (less than 32 ms max) V_{DD} overcurrent wake-up (I_{DD} > 2.0 mA typ).

As long as the watchdog refresh occurs, the device remains in LP V_{DD} ON mode.

4.3.1.3.5 Cyclic sense operation

This function can be used in both Low-power modes (LP V_{DD} OFF and LP V_{DD} ON). Cyclic sense is a specific detection of an event on an SGx, during the cyclic activation of the SGx input. Cyclic sense principle (synchronous cyclic sense):

A dedicated timer allows to select a cyclic sense period from 3.0 to 512 ms (selection in timer B). At the end of the period, the SGx is activated for a duration of t_{SCAN}. During the TSCAN duration, the SGx is monitored. If it is it the expected level, the device detects a wake-up. Cyclic sense can operate for both Low-power modes: Low-power V_{DD} ON and Low-power V_{DD} OFF.

Cyclic sense period is selected by the SPI configuration prior to entering Low-power mode. The expected level on SGx is selected at the time the device is set into Low-power mode. This means prior to entering Low-power mode, SGx must be activated, so the level of SGx can be sampled. During device Low-power mode, if the opposite level on SGx is reached during the SGx activation mode, the device wakes up.

During Cyclic Sense active time (t_{SCAN}), the level of SGx is the same as the one before entering Low-power mode. So full flexibility is offered, as the SGx high-side or low-side switch can be activated by the SPI in Normal mode. The level of SGx is sensed during the SGx active time, and is deglitched for a duration of typically 30 μs. This means SGx should be in the expected state for a duration longer than the deglitcher time.

4.3.1.3.6 CAN functional block

The 33909 has an enhanced High Speed CAN physical interface. A single CAN5V pin is used for a capacitor for the internal 5.0 V regulator to power the CAN interface. There is also a single dedicated Ground for the CAN bus (CANGND).

The CAN5V regulator supplies a maximum of 200 mA, while the CAN physical layer is designed to current limit to less than 100 mA in case of a short on the bus. If the user does not use the physical layer, the user may use the CAN5V supply as another supply rail. The CAN5V regulator turns OFF in LP modes.

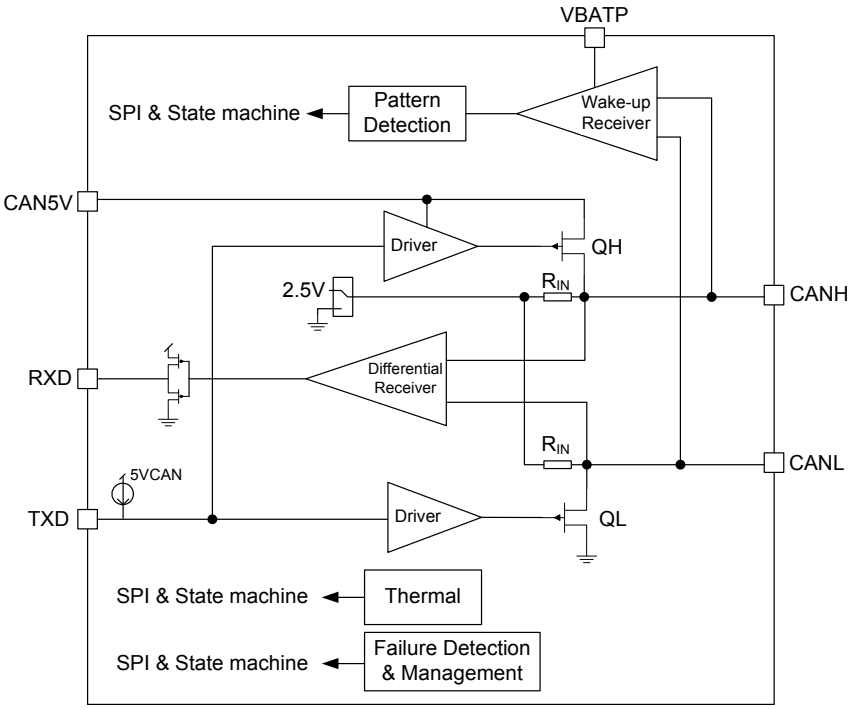


Figure 20. CAN interface block diagram

4.3.1.3.7 TX/RX mode

In TX/RX mode, both the CAN driver and the receiver are ON. In this mode, the CAN lines are controlled by the TXD pin level, and the CAN bus state is reported on the RXD pin.

The CAN5V regulator must be ON. It supplies the CAN driver and receiver.

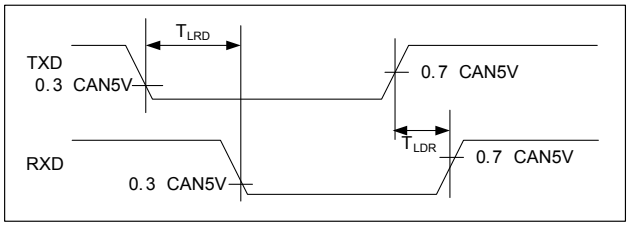


Figure 21. CAN propagation delays TXD to CAN and CAN to RXD

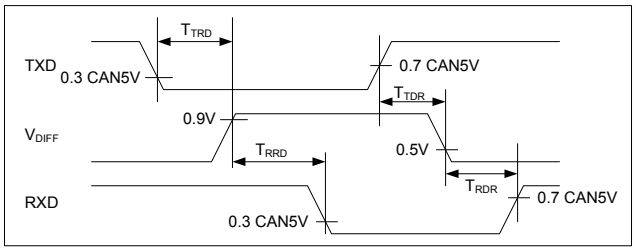


Figure 22. CAN propagation delays TXD to CAN and CAN to RXD

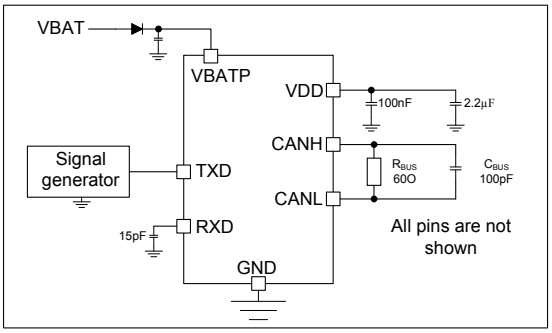


Figure 23. CAN test setup

4.3.1.3.8 Sleep mode

Sleep mode is a reduced current consumption mode. CANH and CANL lines are terminated to GND via the R_{IN} resistor (typ 25 kΩ). In order to monitor bus activities, the CAN wake-up receiver is ON.

Wake-up events occurring on the CAN bus pin are reporting by dedicated flags in SPI, and results in a device mode transition out of Low-power mode.

4.3.1.3.9 Listen only mode

This mode is used to disable the CAN driver, but leave the CAN receiver active. In this mode, the device is only able to report the CAN state on the RXD pin. The TXD pin has no effect on CAN bus lines. The CAN5V regulator must be ON.

4.3.1.3.10 CAN interface supply

The supply voltage for the CAN driver is the CAN5V pin. The CAN interface also has a supply path from the battery line, through the VBATP pin. This path is used in CAN sleep mode to allow wake-up detection. During CAN communication (transmission and reception), the CAN interface current is sourced from the CAN5V pin. During CAN Low-power mode, the current is sourced from the VBATP pin.

4.3.1.3.11 CAN driver operation in TX/RX mode

The CAN drive can be enabled via SPI as soon as the device is in normal mode. When the CAN interface is in Normal mode, the driver has two states: recessive or dominant. The driver state is controlled by the TXD pin. The bus state is reported through the RXD pin.

When TXD is high, the driver is set in the recessive state, and CANH and CANL lines are biased to the voltage set with CAN5V divided by 2, or approximately 2.5 V. When TXD is low, the bus is set into the dominant state, and CANL and CANH drivers are active. CANL is pulled low and CANH is pulled high.

The RXD pin reports the bus state: CANH minus the CANL voltage is compared versus an internal threshold (a few hundred mV).

If “CANH minus CANL” is below the threshold, the bus is recessive and RXD is set high.

If “CANH minus CANL” is above the threshold, the bus is dominant and RXD is set low.

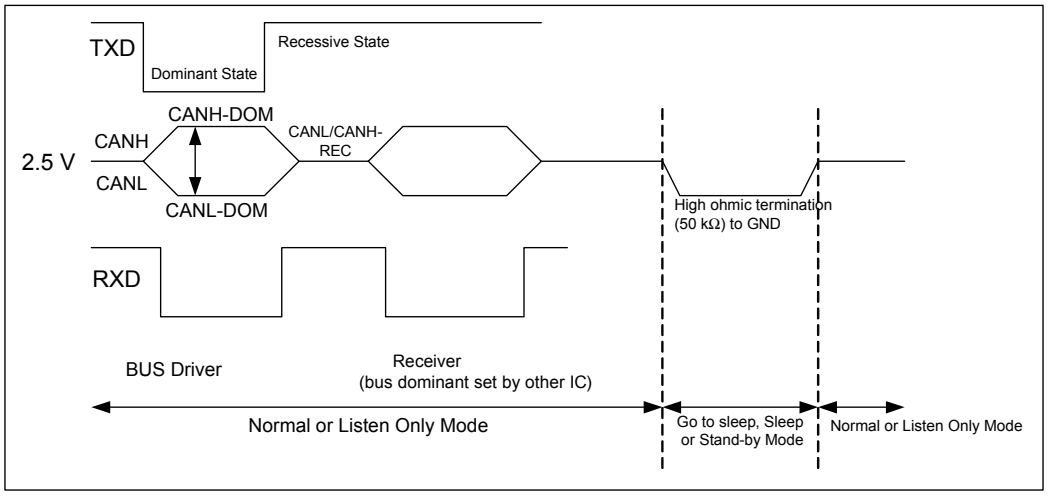


Figure 24. BUS signal in Tx/Rx and low-power mode_48LD

4.3.1.3.12 Minimum baud rate

The minimum baud is determined by the shortest TXD permanent dominant timing detection. The maximum number of consecutive dominant bits in a frame is twelve (six bits of active error flag and its echo error flag). The shortest TXD dominant detection time of 300 μs lead to a single bit time of: 300 μs/12 = 25 μs, so the minimum Baud rate is 1/25 μs = 40 kBaud.

4.3.1.3.13 Termination

The device supports differential termination resistors between CANH and CANL lines. Refer to device typical application.

4.3.1.3.14 Low-power mode

In Low-power mode, the CAN is internally supplied from the VBATP pin. In Low-power mode, the CANH and CANL drivers are disabled, and the receiver is also disabled. CANH and CANL have a typical 25 kΩ impedance to GND. The wake-up receiver can be activated if wake-up is enabled by the SPI command. When the device is set back into Normal mode, CANH and CANL are set back into the recessive level. This is illustrated in Figure 24.

4.3.1.3.15 Wake-up

When the CAN interface is in Sleep mode with wake-up enabled, the CAN bus traffic is detected. The CAN bus wake-up is a pattern wake-up. The wake-up by the CAN is enabled or disabled via the SPI. There are two methods for wake-up, Three dominant pulses or a single dominant pulse described in the figures below. The default condition is for the three dominant pulses to cause a wake-up.

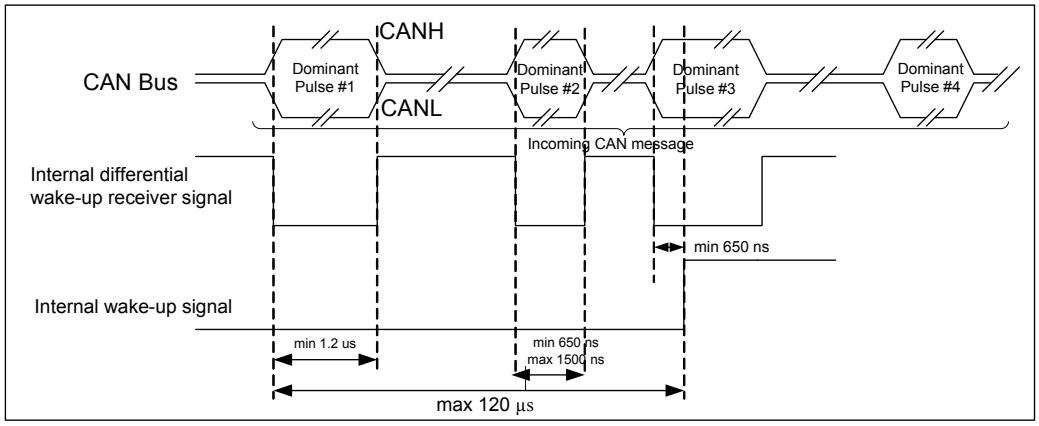


Figure 25. Three dominant pulses pattern wake-up

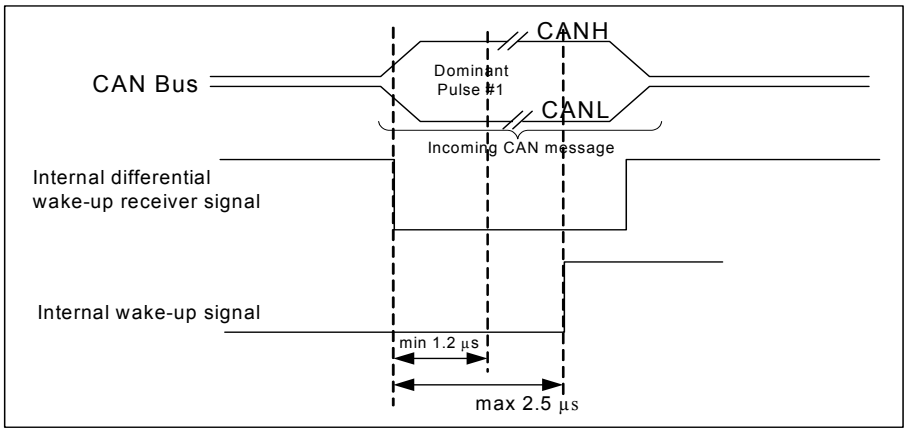


Figure 26. Single pulse pattern wake-up

4.3.1.3.16 CAN wake-up report

The CAN wake reporting is done via the device state machine.

4.3.1.3.17 Pattern wake-up

In order to wake-up the CAN interface, the wake-up receiver must receive a series of three consecutive valid dominant pulses, by default when the CANWU bit is low. CANWU bit can be set high by SPI and the wake-up occurs after a single pulse duration of 1.0 µs (typ).

A valid dominant pulse is longer than 500 ns. The three pulses occur in a time frame of 120 µs, to be considered valid. When three pulses meet these conditions, the wake signal is detected. This is illustrated by Figure 25.

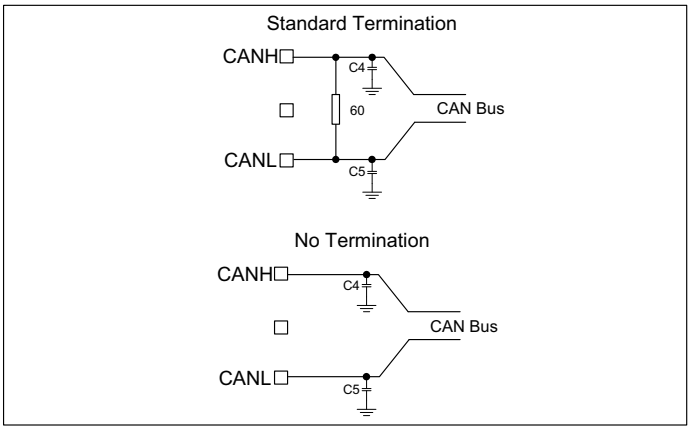


Figure 27. Typical application and bus termination options

4.3.1.3.18 State transition

CAN5V regulator OFF only in low-power, or disable by a SPI command. CAN5V can be enabled by SPI after power up and in the INIT state. This gains the reset, time to charge the external capacitor and have the CAN5V active in Debug and Flash modes. Refer to the Figure 19.

4.3.1.3.19 CAN bus diagnostic

The aim is to implement a diagnostic of bus short-circuit to GND, VBATP, and internal ECU 5.0 V. Several comparators are implemented on CANH and CANL lines. These comparators monitor the bus level in the recessive and dominant states. The information is then managed by a logic circuitry to properly determine the failure and report it. Table 8 indicates the state of the comparators in case of a bus failure, and depending upon the driver state.

Table 8. CAN failure detection truth table

Failure description	Driver recessive state		Driver dominant state	
	Lg (threshold 1.75 V)	Hg (threshold 1.75 V)	Lg (threshold 1.75 V)	Hg (threshold 1.75 V)
No failure	1	1	0	1
CANL to GND	0	0	0	1
CANH to GND	0	0	0	0
	Lb (threshold V_{BATP}-2.0 V)	Hb (threshold V_{BATP}-2.0 V)	Lb (threshold V_{BATP}-2.0 V)	Hb (threshold V_{BATP}-2.0 V)
No failure	0	0	0	0
CANL to VBATP	1	1	1	1
CANH to VBATP	1	1	0	1

4.3.1.3.20 Detection principle

In the recessive state, if one of the two bus lines are shorted to GND or VBATP, the voltage at the other line follows the shorted line, due to the bus termination resistance. For example: if CANL is shorted to GND, the CANL voltage is zero, the CANH voltage measured by the Hg comparator is also close to zero.

In the recessive state, the failure detection to GND or VBATP is possible. However, it is not possible with the above implementation to distinguish which of the CANL or CANH lines are shorted to GND or VBATP. A complete diagnostic is possible once the driver is turned on, and in the dominant state.

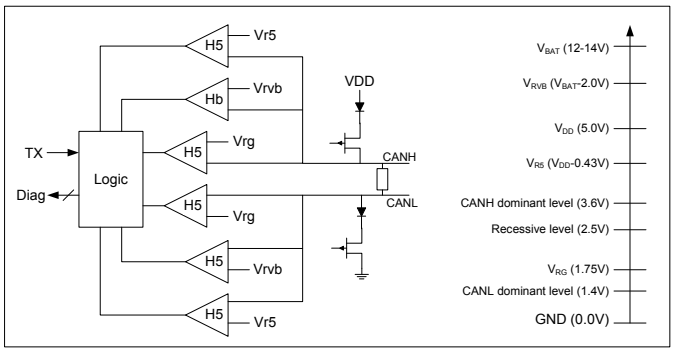


Figure 28. CAN bus simplified structure truth table for failure detection

4.3.1.3.21 Number of samples for proper failure detection

The failure detector requires at least one cycle of the recessive and dominant states to properly recognize the bus failure. The error is fully detected after five cycles of the recessive-dominant states. As long as the failure detection circuitry has not detected the same error for five recessive-dominant cycles, the error is not reported.

4.3.1.3.22 Bus clamping detection

If the bus is detected to be in dominant for a time longer than (TDOM), the bus failure flag is set and the error is reported in the SPI.

Such condition could occur in case the CANH line is shorted to a high voltage. In this case, current flows from the high voltage short-circuit through the bus termination resistors (60 Ω), and the device CANH and CANL input resistors, which are terminated to internal 2.5 V biasing or to GND (sleep mode).

Depending upon the high voltage short-circuit, the number of nodes, RIN actual resistor, and node state (sleep or active), the voltage across the bus termination can be sufficient to create a positive dominant voltage between CANH and CANL, and RXD pin is low. This would prevent start of any CAN communication, and thus a proper failure identification (requires five pulses on TXD). The bus dominant clamp circuit helps to determine such failure situation.

4.3.1.3.23 RX permanent recessive failure

The aim of this detection is to diagnose an external hardware failure at the RX output pin and ensure a permanent failure at RX does not disturb the network communication. If RX is shorted to a logic high signal, the CAN protocol module within the MCU does not recognize any incoming message. In addition, it is not be able to easily distinguish the bus idle state and can start communication at any time. In order to prevent this, an RX failure detection is necessary.

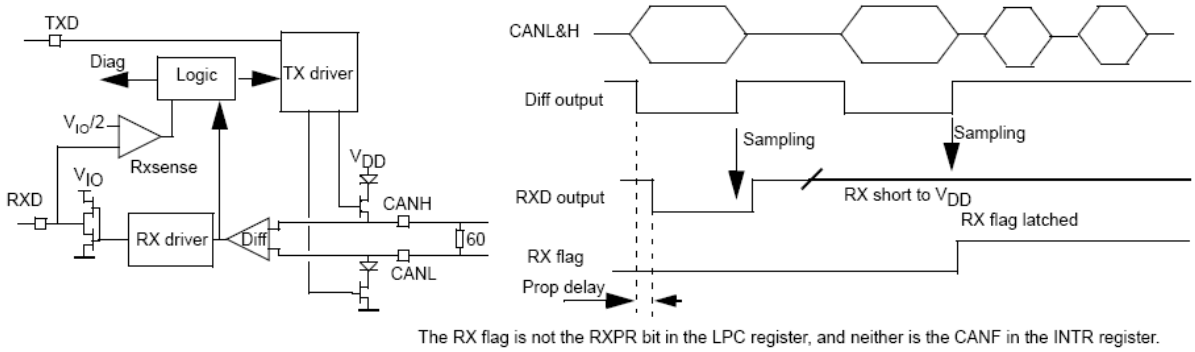


Figure 29. RX path simplified schematic, RX short to V_{DD} detection

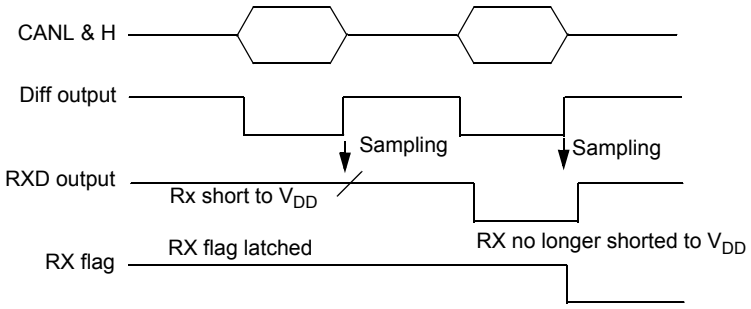
4.3.1.4 Implementation for detection

The proposed implementation is to sense the RXD output voltage at each low to high transition of the differential receiver. Excluding the internal propagation delay, the RXD output is low when the differential receiver is low. In case of an external short to V_{DD} at the RXD output, RXD is tied to a high level and can be detected at the next low to high transition of the differential receiver.

As soon as the RXD permanent recessive is detected, the RXD driver is deactivated. Once the error is detected, the flag is latched and the driver is disabled.

4.3.1.4.1 Recovery condition

The internal recovery is done by sampling a correct low level at TXD, as shown in Figure 30.



The RX flag is not the RXPR bit in the LPC register, and neither is the CANF in the INTR register.

Figure 30. RX path simplified schematic, RX short to V_{DD} detection

4.3.1.4.2 Important information for bus driver reactivation

The driver stays disabled until the failure is cleared (RX is no longer permanent recessive). One transition on the CAN bus (internal differential receiver transition) and the bus driver is activated by entering into Normal mode.

4.3.1.4.3 TXD permanent dominant

Principle

If the TXD is set to a permanent low level, the CAN bus is set into dominant level and no communication is possible. The device has a TXD permanent timeout detector. After the timeout, the bus driver is disabled and the bus is released into a recessive state. The TXD permanent flag is set.

Recovery

The TXD permanent dominant is also used and activated, in case of a TXD short to RXD. The recovery condition for a TXD permanent dominant (recovery means the re-activation of the CAN drivers) is done by entering into a Normal mode controlled by the MCU, or when TXD is recessive while RXD changes from recessive to dominant.

4.3.1.5 TXD to RXD short-circuit

4.3.1.5.1 Principle

In case TXD is shorted to RXD, during incoming dominant information, RXD is set low. Consequently, the TXD pin is low and drives CANH and CANL into a dominant state. Thus the bus is stuck in dominant. No further communication is possible.

4.3.1.5.2 Detection and recovery

The TXD permanent dominant timeout activates and releases the CANL and CANH drivers. However, at the next incoming dominant bit, the bus is stuck in dominant again. The recovery condition is same as the TXD dominant failure.

4.3.1.5.3 CAN functional pin: TXD

CAN bus transmit data input. Internal pull-up to V_{DD}

4.3.1.5.4 CAN functional pin: RXD

CAN bus receive data output.

4.3.1.5.5 CAN functional pin: CANH

CAN high output.

4.3.1.5.6 CAN functional pin: CANL

CAN low output.

4.3.1.6 LIN interface functional block

The 33909 has 4 LIN interfaces which fulfill LIN protocol specification 2.1 and SAEJ2602-2. The LIN pin represents the single-wire bus transmitter and receiver, and is suited for automotive bus systems. The LIN interface is only active during Normal mode. The CAN5V regulator serves as the internal supply for the LIN and must be enabled for LIN functionality.

The LIN driver is a low-side MOSFET with internal overcurrent thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a slave node. An additional pull-up resistor of 1.0 kΩ must be added when the device is used in the master node. The LIN pin exhibits no reverse current from the LIN bus line to VBATP, even in the event of GND shift or VBATP disconnection. The transmitter has a 20 kbps baud rate (normal mode) or 10 kbps baud rate (slow mode) which is configurable via the SPI.

The receiver thresholds are ratiometric with the device supply pin. If the LIN voltage goes below the LIN undervoltage threshold (V_{UVL}, V_{UVH}), the bus enters in recessive state, even if communication is sent on TXD. In case of LIN Thermal Shutdown, the transceiver and receiver are disabled. When the temperature is below the T_{LINSD}, the T_{SD} flag must be cleared and the LIN is able to continue communication. The LIN driver remains OFF until the T_{SD} flag is cleared.

4.3.1.6.1 Data input pin (TXD)

The TXD input pin is the MCU interface to control the state of the LIN output. When TXD is LOW (dominant), LIN output is LOW; when TXD is HIGH (recessive), the LIN output transistor is turned OFF. The threshold is 3.3 V and 5.0 V compatible. This pin has an internal pull-up current source to force the recessive state, in case the input pin is left floating.

4.3.1.6.2 Data output pin (RXD)

The RXD output pin is the MCU interface, which reports the state of the LIN bus voltage. In Normal or Slow mode, LIN HIGH (recessive) is reported by a high voltage on RXD; LIN LOW (dominant) is reported by a low voltage on RXD. In Fast mode, the RXD output signal is inverted compare to the LIN: a high level on the LIN reports a low level on RXD, and a low level on the LIN reports a high level on RXD. The RXD output structure is a buffer tristate output.

It is the receiver output of the LIN interface. The low level is fixed. The high level is dependant on the V_{DD} voltage. If V_{DD} is set at 3.3 V, RXD V_{OH} is 3.3 V. If V_{DD} is set at 5.0 V, RXD V_{OH} is 5.0 V. In the sleep mode, RXD is high-impedance. Due to internal biasing, the RXD pin cannot be pulled up to another supply besides V_{DD}. When a wake-up event is recognized from the LIN bus pin, RXD is pulled LOW to report the wake-up event. For this, an external pull-up resistor connected on RXD pin is needed.

4.3.1.6.3 Normal mode

In the Normal mode, the LIN bus can transmit and receive information. The default condition is the 20 kbps mode and has slew rate and timing compatible with Normal Baud Rate and LIN protocol specification 2.1. The 10 kbps selection is SPI configurable and has slew rate and timing compatible with Low Baud Rate. From Normal mode the device can enter in Fast Baud Rate (Toggle function).

4.3.1.6.4 Fast mode

In the Fast mode, the slew rate is around 10 times faster than the Normal mode. This allows very fast data transmission (>100 kbps), for instance, for electronic control unit (ECU) tests and microcontroller program downloads. The bus pull-up resistor might be reduced to ensure a correct RC time constant in line with the high baud rate used. Fast mode is entered via the SPI.

4.3.1.6.5 Sleep mode

In the Sleep mode, the transmission path is disabled and the device is in low-power mode. Supply current from VBATP is very low. Wake-up can occur from LIN bus activity. After a wake-up event, the device enters in Awake Mode. In the Sleep mode, the internal 725 kΩ pull-up resistor is connected and the 30 kΩ disconnected.

4.3.1.6.6 Remote wake from LIN bus (awake transitional mode)

The LIN bus wake-up is recognized by a recessive-to-dominant transition, followed by a dominant level with a duration greater than 70 μs, followed by a dominant-to-recessive transition. This is illustrated in Figure 7 and Figure 8. Once the wake-up is detected, the device enters to the Awake transitional mode with RXD pulled LOW.

4.3.2 Fail-safe features

Table 9 describes the protections.

Table 9. Fail-safe protections

Block	Fault	Function mode	Condition	Fallout	Recovery
LIN	undervoltage	Normal	LIN voltage < 5.8 V (Typical)	LIN transmitter in recessive state	Condition gone
	TXD pin permanent Dominant		TXD pin low for more then 1.0 s (Typ)	LIN transmitter in recessive state	Condition gone
	LIN thermal shutdown	Normal and Awake modes	Temperature > 160 °C (Typ)	LIN transmitter in recessive state High-side turned off.	Condition gone

4.3.2.0.1 LIN functional pin: LINx

LIN bus.

4.3.2.0.2 LIN functional pin: TXD-Lx

LIN bus transmit data input. Includes an internal pull-up resistor to V_{DD}.

4.3.2.0.3 LIN functional pin: RXD-Lx

LIN bus receive data output

4.3.2.1 VPRE regulator functional block

The 33909 has a VPRE pre-regulator designed to run as a non-inverting Buck - Boost supply for the VDD and VAUX power supplies. This regulator provides efficient DC-DC conversion as well as boost operation at low input voltage (low battery). The output voltage level is 6.5 V.

The converter has both a high and low-side FET and requires a single inductor for operation. The high-side FET is integrated into the 33909. The low-side Boost FET is external. The converter uses external diodes instead of synchronous switches to reduce the number of pins.

The 33909 has a Low-power mode to reduce quiescent current when full power is not needed by the micro. In Low-power mode, the buck boost converter is placed in a zero quiescent current mode and a small internal regulator is employed to power the VPRE node.

The V_{PRE} supply contains a thermal limit circuit, which is used to supply a thermal warning as well as provide a thermal limit which turns OFF the IC. A flag exists for both of these functions. When thermal limit is reached the V_{PRE} supply turns off. The thermal shutdown limit was designed to be above the other IC thermal thresholds. The user should take care when the IC thermal limits are reached in order to maintain Voltage regulator operation of V_{PRE} and V_{DD}.

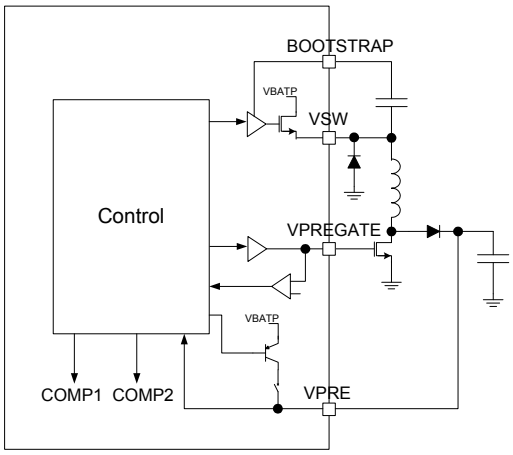


Figure 31. VPRE block diagram

4.3.2.1.1 VPRE pin functions:

There are four pins associated with the VPRE regulator

- VPREGATE - Gate drive for low-side (Boost) FET.
- VSW - Switching node of high-side (Buck) FET.
- BOOT - Supply for high-side (internal) pre-driver.
- VPRE - Pre-regulator output (6.5 V).

4.3.2.1.2 VPRE pin functions: BOOT

An external bootstrap 0.1 μF capacitor connected between VSW and the BOOT pin is used to generate a high voltage supply for the high-side driver circuit of the buck controller. The capacitor is pre-charged to approximately 10 V, while the internal FET is off. On switching, the VSW pin is pulled up to VBATP, causing the BOOT pin to rise to approximately VBATP + 10 V.

4.3.2.1.3 VPRE pin functions: VPREGATE

This is an output for driving an external FET for boost mode operation. Due to the fact the gate drive supply voltage is VPRE, the external power MOSFET should be a logic level device. It also has to have a low $R_{DS(ON)}$ for acceptable efficiency. During Buck mode, this gate output is held low.

To use the 33909 in Buck Only mode, the VPREGATE pin is held at Ground and an internal comparator alerts the IC it is in Buck Only mode.

4.3.2.1.4 VPRE pin functions: VPRE

The output of the switching regulator is brought into the chip at the VPRE pin. This voltage is required for both the switching regulator control and as the supply voltage for all the linear regulators. The VPRE pin functions as a supply rail for some IC functions, including the rail for the SG input current sources. The VPRE supply also supplies the CAN5V internal rail.

4.3.2.1.5 VPRE pin functions: VSW

The internal switching transistor is an N-channel power MOSFET. The $R_{DS(ON)}$ of this internal power FET is approximately 0.25 Ω at +125 ºC. The nominal instantaneous current limits well below the saturation current of the MOSFET and external surface mounted inductor, to supply the current for the linear regulators connected to the VPRE pin. The input to the drain of the internal n-channel MOSFET must be protected by an external series blocking diode, for reverse battery protection.

4.3.2.1.6 VPRE external components

The V_{PRE} power supply requires external components for the Buck and Boost mode architecture. The V_{PRE} supply uses an external inductor, MOSFET and two diodes. Buck-Boost usage case

Usage of the Buck-Boost feature is the most widely used case. In this case, all of the external components are populated and V_{PRE} produces approximately 6.5 V through the full battery operation range. This use case allows the 33909 to remain fully functional during the battery crank profile down to 2.5 V.

The Boost circuitry remains OFF when the VBATP pin is above the $VBATP_{THD}$ threshold and the Buck circuitry operates as required in Boost mode when the VBATP pin is below $VBATP_{THU}$ as seen in Figure 32. In the range between $VBATP_{THD}$ and $VBATP_{THU}$, the IC operates as needed to supply V_{PRE} at 6.5 V.

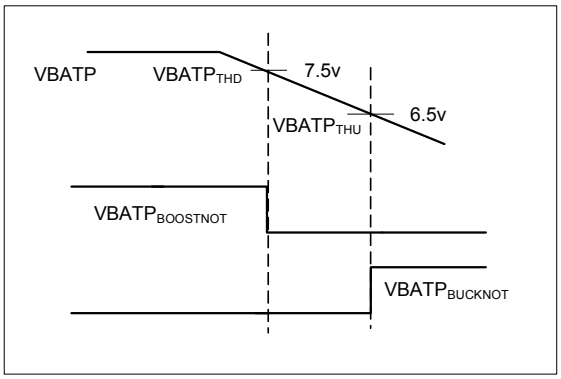


Figure 32. VPRE buck-boost voltage levels

4.3.2.2 Buck usage case

A second option for the user is to use only the Buck circuitry and not the Boost circuitry (saving the added cost if Boost is not required). When using the Buck only mode, the user does not populate the low-side FET (VPREGATE) and the associated diode. In this case, the user grounds the VPREGATE and the 33909 detects this during startup. The VBATP pin voltage range in this mode is ~7.0 V to 35 V.

As the battery voltage decreases, the high-side switch turns ON to 100% duty cycle and operate in a “pass thru” mode. The following figures illustrate some of the device mode transitions.

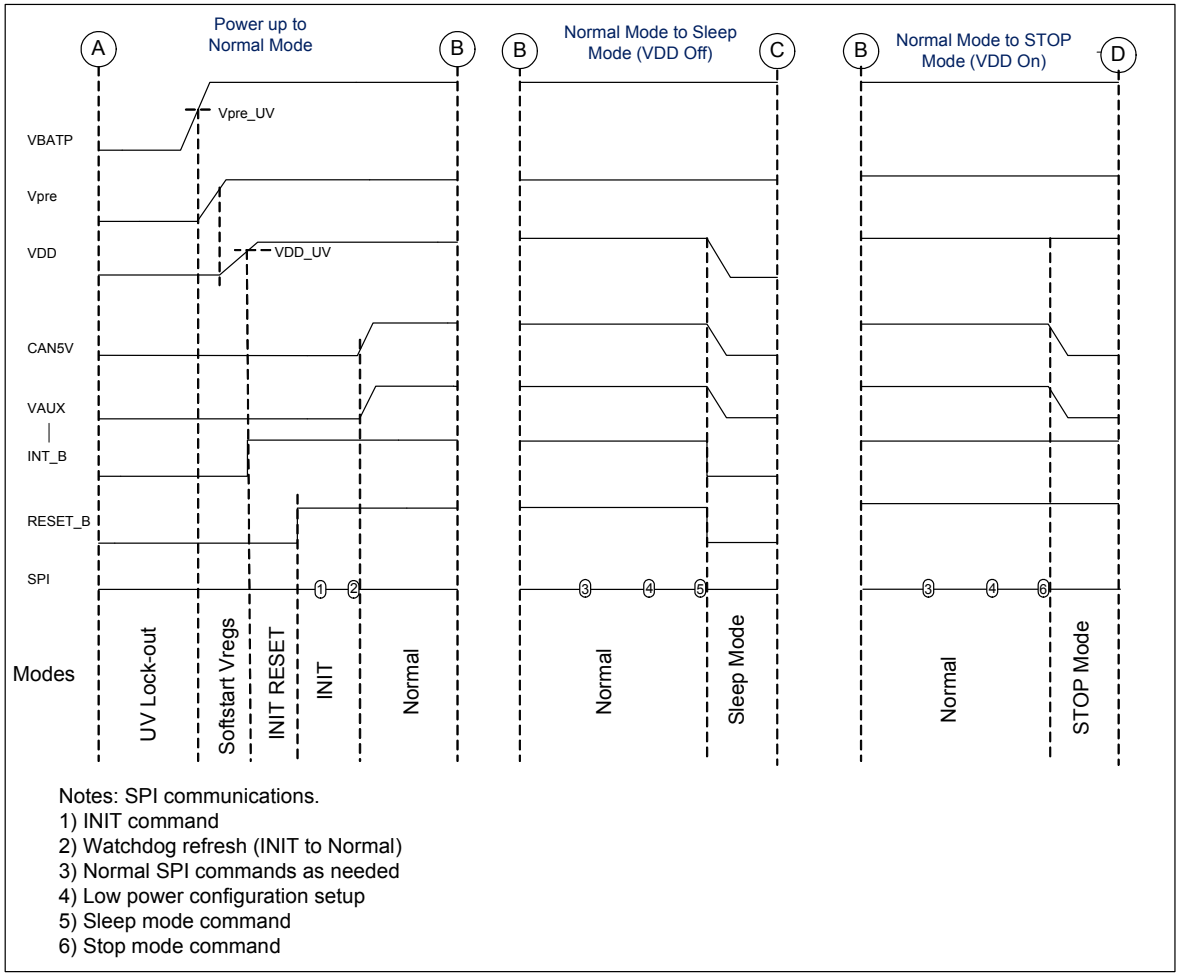
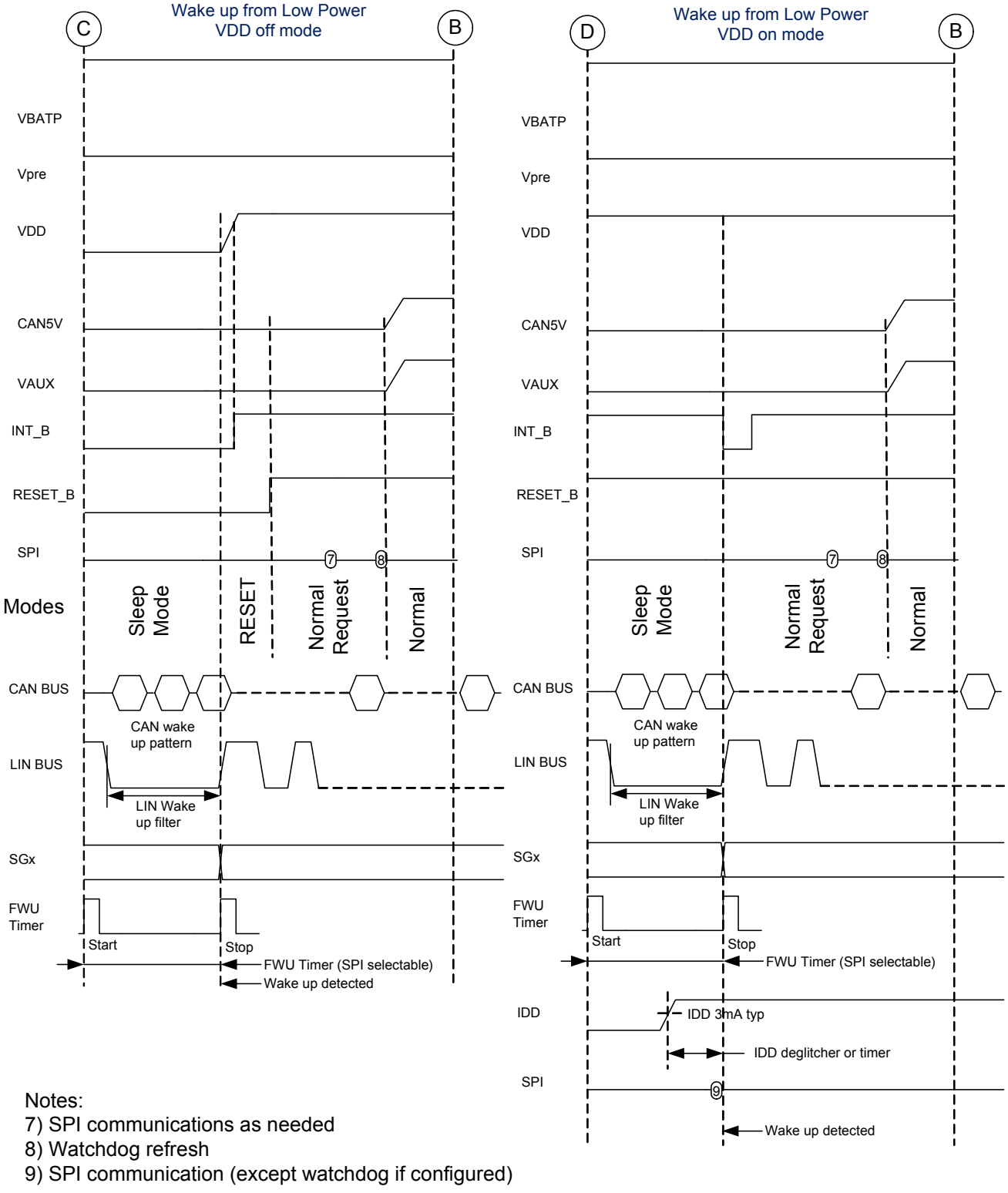


Figure 33. Power up to normal and to low-power modes



Notes:
7) SPI communications as needed
8) Watchdog refresh
9) SPI communication (except watchdog if configured)

Figure 34. Wake-up from low-power modes

4.3.2.3 V_{DD} supply

The VDD output is an external LDO regulator supplying +5.0 V (3.0 V selectable via a different part number) with ±2.0% accuracy. The V_{DD} supply is capable of sourcing a maximum of 500 mA steady state current from VPRE (6.5 V typical) for VBATP pin voltages from 2.5 V to 35 V (45 V transient) [Buck only to V_{BATP} = 7.0 V]. This regulator incorporates external current limit short-circuit protection and internal thermal protection. The regulator remains on in current limitation. The voltage output is stable under all load/line conditions. The V_{DD} rail does not turn on until the specified voltage can be obtained from the VPRE node.

4.3.2.3.1 VDD pins

There are three pins associated with the VDD regulator

- VDDE - Emitter connection for external LDO device.
- VDDB - Base connection for external LDO device.
- VDD - Feedback voltage and main supply voltage node

4.3.2.3.2 VDD pin functions: VDDE

Input pin used to sense the voltage (V_{DDSNS}) across the external sense resistor from VPRE to VDDE. Current limit is derived from this sense voltage measurement. Kelvin lines is used by the user to ensure proper voltage sensing, therefore careful layout planning is required.

4.3.2.3.3 VDD pin functions: VDDB

Output pin used to for the base drive of the external LDO device.

4.3.2.3.4 VDD pin functions: VDD

Input pin used for feedback control loop of the V_{DD} supply. A Kelvin trace is provided to the VDD pin for proper feedback control.

4.3.2.3.5 VDD external components

The V_{DD} power supply requires an external PNP be connected to the VPRE pin. The V_{DD} supply uses an external resistor to monitor and limit the V_{DDSNS} voltage and provide load current limit; this is placed between the VPRE and VDDE pins.

4.3.2.4 V_{AUX} regulator functional block

The V_{AUX} regulator uses an external PNP pass device referenced to the pre regulator voltage, VPRE, via an internal short to battery protection switch. V_{AUX} is capable of driving up to 200mA of load current and can be configured for an output voltage of 5.0 V or 3.3 V with 3.0% accuracy. Additionally, V_{AUX} can be configured as a tracking regulator. In tracking mode, V_{AUX} tracks the V_{DD} regulator voltage to within 15 mV, but note that tracking mode is only possible when the V_{DD} regulator is configured as a 5.0 V supply, as shown in the Table 10.

The V_{AUX} regulator is short to battery protected and current limited (200 mA min.). No external components are required for these two features. In low-power mode, V_{AUX} is disabled and draws zero quiescent current. Upon power up, V_{AUX} is disabled. V_{AUX} is enabled by writing to bits 7 and 6 of the REG register as shown by the following:

Table 10. REG register

Bits	Description
b7 b6	V_{AUX}[1], V_{AUX}[0]- Vauxilary regulator control
00	Regulator OFF
01	Regulator ON. Undervoltage (UV) and overcurrent (OC) and overvoltage (OV) monitoring flags not reported. V_{AUX}disable in case OC or UV detected after 1.0 ms blanking time (monitoring of flags not reported).
10	Regulator ON. Undervoltage (UV) and overcurrent (OC) and overvoltage (OV) monitoring flags active. V_{AUX} disable in case OC or UV detected after 1.0 ms blanking time. (monitoring of flags not reported).
11	Regulator ON. Undervoltage (UV) and overcurrent (OC) and overvoltage (OV) monitoring flags active. V_{AUX} disable in case OC or UV detected after 25 µs blanking time.

At power up, when the device is in its INIT state, the REG INIT register can be written to set V_{AUX} to 3.3 V or 5.0 V or 5.0 V tracking, as shown by the following:

Table 11. Setting VAUX to 3.3 V or 5.0 V

Bits	Description
b2	[V_{AUX}5/3]- Select Vauxilary output voltage
0	V_{AUX} = 3.3 V
1	V_{AUX} = 5.0 V
b1	Tracking Enable
0	VAUX is independent of VDD
1	VAUX tracks VDD (VAUX does not turn ON if set in 3.3 V part)

Writing to this initialization register is locked out when the device leaves the INIT state. Also, note that the logic does not allow tracking mode if V_{DD} is set to 3.3 V, as Table 12 illustrates.

Table 12. V_{AUX} tracking vs. supply

V_{DD} value	V_{AUX} value	V_{AUX} tracking	V_{AUX} supply
5.0 V	5.0 V	SPI Configurable	SPI configurable
5.0 V	3.3 V	Not capable	Default
3.3 V	5.0 V	Not capable	SPI configurable
3.3 V	3.3 V	Not capable	Default

The V_{AUX} regulator also contains a digitally controlled soft start to minimize overshoots upon power up. Also included in V_{AUX}, is a fold-back current limit.

4.3.2.4.1 VAUX pins

There are three pins exclusively associated with the V_{AUX} regulator

- VAUXB - This pin is connected to the base of the external PNP and provides the necessary base current.
- VAUXE - This pin is connected to the emitter of the external PNP transistor. 33909 includes short to battery blocking FET between VPRE and VAUXE.
- VAUX - This pin is the feedback pin as well as the main supply node for supply the voltage (3.3/5.0 V).

Additionally:

- VPRE - supply to VAUX and also note all V_{AUX} load current flows into 33909 via the VPRE pin before reaching the external PNP.

4.3.2.4.2 VAUX external components

VAUX requires an external PNP with sufficient beta to provide up to 200 mA load current within the constraints of the max base drive available from the VAUXB pin. Also, a capacitor is required for loop stability and transient load response.

4.3.2.4.3 VAUX fault mode behavior

Current Limit: V_{AUX} limits the load current to 200 mA minimum, 360 mA maximum. A current limit event can be reported via the SPI and INT pin if configured as such in the REG register.

Undervoltage: After V_{AUX} has come up, an undervoltage event can be reported via the SPI and INT pin if configured as such in the REG register. The undervoltage event disables the V_{AUX} regulator if configured as such in the REG register. If configured to disable, the V_{AUX} can only be turned back ON by re-writing to the REG register.

Overvoltage: Overvoltage, or short to V_{BAT} causes an internal switch between the VPRE and VAUX_E to be turned off. This is done to protect the VAUX PNP device and other things on the Vpre line. This event is not latched. When the overvoltage event has ended, the internal switch is re-activated and VAUX returns to normal operation.

4.3.2.5 VBATSNS

The 33909 contains a VBATSNS function to allow the user to see the battery voltage via the AMUX pin. This pin connects directly to the battery (before the series diode connected to VBATP). The VBATSNS is used for additional functions internal to the die and should have pcb traces capable of running up to some current. The ratio of the resister divider is 1/5.94 (5.0 V part) or 1/8.9 (3.3 V part).

4.3.2.5.1 VBATSNS pin functions: VBATSNS

Direct battery voltage input sense. A series resistor is required to limit the input current during high voltage transients.

4.3.2.5.2 MUX output (AMUX)

Various signals may be brought out via the analog multiplexer (AMUX) pin. The AMUX pin is referenced to V_{DD} and can be selected via the SPI. The signals which can be viewed on the AMUX are located in Table 13. The AMUX output pin is clamped to a maximum of V_{DD} volts regardless of the higher voltages present on the input pin.

For SG inputs, when an input has been selected to output on the AMUX, the corresponding bit in the MISO data stream is logic [0]. When selecting a channel to be read out the AMUX, the user may also set the desired current (16 mA, 2.0 mA, or high-impedance) in the SPI word. The MCU may change or update the analog select register via software at any time in Normal Mode when set for SPI selection.

Table 13. AMUX SPI selection

Bits	Description
b8 b7 b6 b5 b4 b3	MUX_4, MUX_3, MUX_2, MUX_1, MUX_0 - Selection of the device external input signal or internal signal to be measured at AMUX pin
0 00000	All functions disable. AMUX pin high-impedance
0 00001	Voltage at SG0
0 00101	Voltage at SG1
0 00110	Voltage at SG2
0 00111	Voltage at SG3
0 01000	Voltage at SG4
0 01011	Voltage at SG5
0 10001	Ground
0 10010	Voltage at VBATSNS pin. Refer to electrical table for attenuation ratio (approximately 6 for VDD = 5.0 V, approximately 9 for VDD = 3.3 V) [Default]
0 10011	Device internal temperature sensor voltage

A diode/circuit is brought out the AMUX pin to allow for knowledge of the temperature on the IC. The diode is characterized and a voltage/temperature curve generated to allow for temperature monitoring of the IC.

4.3.2.5.3 MUX pin functions: AMUX

The MUX output delivers an internal analog voltage to the MCU A/D input. Value is selected via the SPI. Output is clamped at VDD.

4.3.2.5.4 Undervoltage reset and reset function (RST_B)

The RST_B pin is an open drain structure with an internal pull-up current source. The low-side driver has limited current capability when asserted low, in order to tolerate a short to high level (i.e short to 5.0 V).The RST_B pin voltage is monitored in order to detect a failure (e.g. RST_B pin shorted to 5.0 V or GND).

During sleep mode the under voltage detect circuit polls during normal scan timer periods to determine if V_{BATP} is in an undervoltage condition. If the IC is in under voltage the IC wakes up and issues a reset to the system.

The RESET pin reports the MCU undervoltage condition at the VDD pin, as well as a failure in the watchdog refresh operation. VDD undervoltage reset operates also in Low-power V_{DD} ON Mode.

The undervoltage threshold at VDD can lead to a Reset or an Interrupt. This is selected by the SPI. When “RST-TH1-5”is selected in Normal mode, an INT is asserted when VDD falls below “RST-TH1-5”. This allows the MCU to operate in a degraded mode (e.g. with V_{DD} = 4.0 V).

4.3.2.5.5 RESET pin functions: RST_B

The RESET pin is an open drain structure with an internal pull-up current source.

4.3.2.5.6 Serial peripheral interface (SPI)

The 33909 contains a serial peripheral interface consisting of Serial Clock (SCLK), Serial Data Out (MISO), Serial Data In (MOSI), and Chip Select Bar (CS_B). The SPI interface is used (as applicable) to provide configuration, control, and status functions. This device is configured as an SPI slave. The 33909 contains a data valid method via SCLK input to keep non-modulo 32-bit transmissions from being written into the IC.

4.3.2.5.7 Chip select low (CS_B)

The CS_B input selects this device for serial transfers. On the falling edge of CS_B, the MISO pin is released from tri-state mode, and all status information are latched in the SPI shift register. While CS_B is asserted, register data is shifted in the MOSI pin and shifted out the MISO pin on each subsequent SCLK. On the rising edge of CS_B, the MISO pin is tri-stated and the fault register reloaded (latched) with the current filtered status data. To allow sufficient time to reload the fault registers, the CS_B pin must remain low for a minimum of t_{CSN} prior to going high again. The CS_B is immune to spurious pulses of shorter duration than t_{CSGRT} (MISO may come out of tri-state, but neither status bits nor control bits are altered).

The CS_B input contains a passive pull-up to VDD to command the de-asserted state should an open circuit condition occur. This pin has threshold compatible voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply.

4.3.2.5.8 Serial clock (SCLK)

The SCLK input is the clock signal input for synchronization of serial data transfer. This pin has threshold compatible voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply.

When CS_B is asserted, both the Master Microprocessor and this device latch input data on the rising edge of SCLK. The SPI master typically shifts data out on the falling edge of SCLK, while this device shifts data out on the rising edge of SCLK, to allow more time to drive the MISO pin to the proper level.

This input is used as the input for the modulo-32 bit counter validation. Any SPI transmissions which are NOT exact multiples of 32-bits (i.e. clock edges) is treated as an illegal transmission. The entire frame aborts and no information is changed in the configuration or control registers. The entire frame aborts and no information is changed in the configuration or control registers.

4.3.2.5.9 Serial data output (MISO)

The MISO output pin is in a tri-state condition when CS_B is negated. When CS_B is asserted, MISO is driven to the state of the MSB of the internal register and is the first bit transmitted on MISO. This pin supplies a “rail to rail” output, depending on the voltage at the VDD pin.

4.3.2.5.10 Serial data input (MOSI)

The MOSI input takes data from the master microprocessor while CS_B is asserted. The MSB is the first bit of each word received on MOSI and the LSB is the last bit of each word received on MOSI. This pin has a threshold level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 V (V_{DD}) supply.

4.3.2.5.11 Secured SPI description

A request is done by sending a specific SPI command the 33909 device provides an unpredictable “random code” on MISO. Software must perform a logical change on the code and return it to the device with the new SPI command to perform the desired action. The “random code” is different at every exercise of the secured procedure and can be read back at any time. The SPI secure uses the Special MODE register for the following transitions:

- from Normal mode to Init mode

- from INIT mode to activate SAFE_B mode

- from Normal mode to Flash mode

- from Normal mode to Reset mode (reset request).

- from Normal mode to Reset SG registers (reset request).

“Random code” is also used when the “advance watchdog” is selected.

Changing of device critical parameter

Some critical parameters are configured one time at device power ON only, while the batfail flag is set in the INIT mode. If a change is required while device is no longer in INIT mode, device must be set back in INIT mode using the secured SPI procedure.

4.3.2.5.12 SPI control register definition for SBC operations

The device uses a 32 -bit SPI word and does not have the ability to daisy chain to another IC. The IC decodes the first byte of the MOSI word and supply the requested data on the following 3 bytes. In read register mode, the IC decodes the first byte and provides the full contents of the registers called out in the address in the next three bytes. This causes the device status (12-bits) to be cut off at 8-bits.

In write register mode, the IC decodes the first byte then writes the contents of the MOSI word to the correct address. The MISO word sends the full device status and the contents of all the SG registers. In the read flags mode, the IC decodes the first byte and provides the full contents of the device flag depending on the address. In some cases the first bit of the second byte (bit 23 is used to determine which registers are provided). The MISO output is the full device status along with the contents of the selected device flags address.

The SPI word structure is as follows:

MOSI, Master Out Slave In bits:

- bits 31 and 30 (called C1 and C0) are control bits to select the SPI operation mode (write control bit to device register, read back of the control bits, read of device flag).
- bit 29 to 24 (A5 to A0) to select the register address (read and write).
- bits 23 to 0 (D23 to D0): control bits

MISO, Master IN Slave Out bits:

- bits 31 to 20 is the Device status registers (Do31 to Do20)
- bits 19 to 17 (Do19 to Do17) are unused in normal (write) MISO words.
- bits 16 to 0 (Do16 to Do0) the SGn Status register bits.

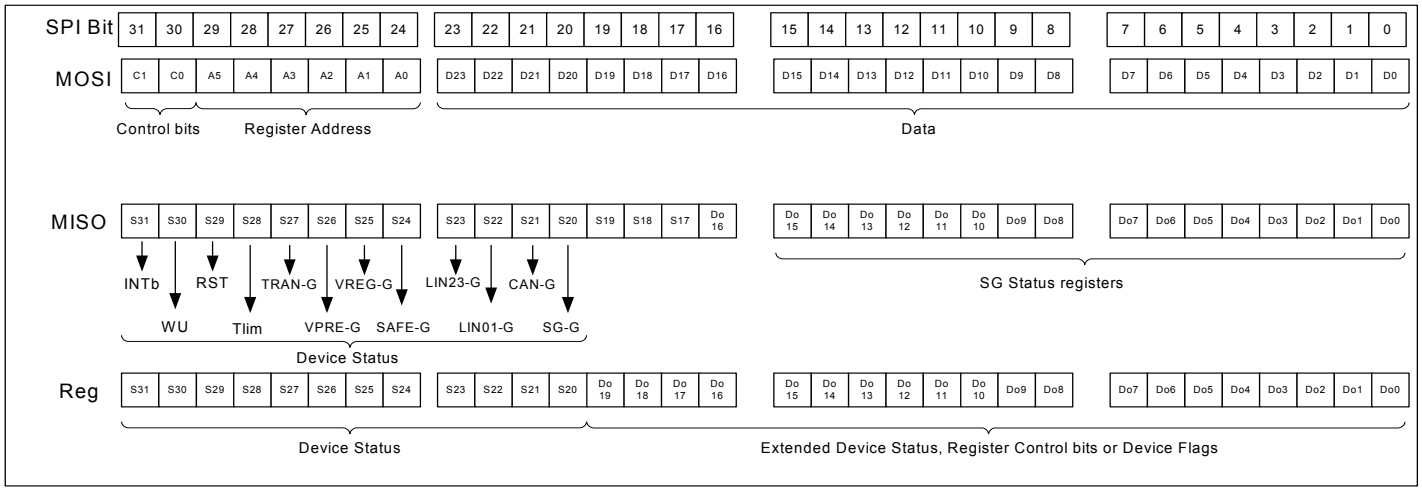


Figure 35. SPI word

Table 14. SPI control bits

Control bits MOSI [31-30] C1-C0	Type of command	Note
00	Read back of register content	Allows user to read back any register.
01	Write to register address, to control device operation and read back of device status register and SG status register set.	Write to any register for operational control. This SPI word results in the “normal” MISO SPI pattern.
10	Read of device flags form a register address	Read back device flags. There are multiple flag registers containing various device information of interest.
11	Reserved	Not used

The device contains several registers. Their address is coded on 6-bits (bits 29 to 24). Each register controls or reports part of the device function. Data can be written to the register to control the device operation or set the default value or behavior. Every register can also be read back to ensure its content (default setting or value previously written) is correct.

In addition, some of the registers are used to report device flags. The device returns one of three messages, a read of an existing register, normal MISO, or a register set of Flags depending on the previous command. After a POR the default word is for the normal MISO registers to be read out with the next word determined by the previous SPI command control bits.

MISO: When a write operation is performed to store data or control bit into the device, MISO pin report a 32-bits fixed device status composed of 4 bytes: In a read operation, MISO reports the fixed device status (bits 31 to 24) and the next 24-bits are the content of the selected register is the list of device registers and their associated address, coded with bits 29 to 24.

Table 15. SPI command overview

Address MOSI [31-30]A29...A24	Description	Quick reference name	Functionality
00_0000	Unused		
00_0001	Memory Word A	RAM_A	1) Write “data word” to register address. 2) Read back “data word” from register address
00_0010	Memory Word B	RAM_B	
00_0011	Initialization Regulators	Init REG	1) Write “device initialization control bits” to register address. 2) Read back “initialization control bits” from register address
	Initialization Watchdog	Init W/D	
	Initialization Miscellaneous functions	Init MISC	
00_0100	Specific Modes	SPE_MODE	1) Write to register to select device Specific Mode, using “Inverted Random Code”. 2) Read “Random Code”.

Table 15. SPI command overview (continued)

Address MOSI [31-30]A29...A24	Description	Quick reference name	Functionality
00_0101	Timer_A: W/D & Low-power MCU consumption	TIM_A	1) Write “timing values” to register address. 2) Read back register “timing values”
	Timer_B: Periodic scan & Cyclic Interrupt	TIM_B	
	Timer_C: W/D Low-power & Forced Wake-up	TIM_C	
00_0110	Analog Multiplexer	MUX	1) Write “device control bits” to register address. 2) Read back register “control bits”
00_0111	Watchdog Refresh	W/D	Watchdog Refresh Commands
00_1000	Interrupt Control	Interrupt	1) Write “device control bits” to register address, to select device operation. 2) Read back register “control bits”
00_1001	Mode register	MODE	1) Write to register to select Low-power mode, with optional “Inverted Random code” and select wake-up functionality. 2) Read operations: Read back device “Current Mode” Read “Random Code”, Leave “Debug Mode”
00_1010	Regulator Control	REG	1) Write “device control bits” to register address, to select device operation. 2) Read back register “control bits”. 3) Read device flags from each of the register addresses.
00_1011	CAN interface control	CAN	
00_1100	LIN 0-1	LIN01	
00_1101	LIN 2-3	LIN23	
00_1110	SG wake-up enable	SGWU	Enable for wake-up from sleep after a change of state for SG inputs: Wake-up enable = 1, Non-wake-up = 0 (Default = 1)
00_1111	Fast scan for SG5-0	SGFS	Enable polling at 1.0 ms for fast wake-up independent of nominal sleep polling timer: Override polling settings for SG5-0 to 1.0 ms = 1, use polling setting as defined in sleep state command = 0 (Default = 0)
01_0000	SG wake-up delay enable	SGWUD	Enable for wake-up from sleep after a change of state for SG inputs after three consecutive polling results confirming change of state: Wake-up enable = 1, Non-wake-up = 0 (Default = 0)
01_0001	Wetting Command Register 0	SGM0	Configure Wetting current sources to desired current level for SG4-0 (Default = 101 = 16 mA)
01_0010	Wetting Command Register 1	SGM1	Configure Wetting current sources to desired current level for SG5 (Default = 101 = 16 mA)
01_0011	Wetting current timer	SGMT	Enable Wetting current source timer: Enable Wetting current source timer = 1, disable – Wetting current ON full time = 0 (Default = 1)
01_0100	Tri-state command	SGT	Enable tristate at input: Enable tristate = 1, Input active = 0 (Default = 1)

Additionally, there are three specific SPI words to carry out certain functions on the IC.

Table 16. SPI specific instructions

SPI MOSI Word	Function	Resulting Behavior
0x5E000000	Command Part of Watchdog Inhibit mode	Even with WDI pin > 10 V, IC leaves WD Inhibit mode (requires WD refreshed)
0x5F000000	Acknowledge Safe condition	Clears SAFE registers and unasserts SAFE_B pin (after SAFE condition is gone)
0x49000010	Wake-up via the SPI	Wakes the IC from low-power mode (VDD ON) with specific SPI word

Table 17. Overview individual bits

Type of command	MOSI/ MISO	Control bits [31-30]	Address [29-24]	Bits [23-0]
Read back of “device control bits”	MOSI	00	address	All 0’s (except when noted)
	MISO	Device Fixed Status (8 bits)		Register control bits content
Write device control bit to address selected by bits (29-24). MISO return 32-bits status	MOSI	01	address	Control Bits
	MISO	Device Fixed Status (12 bits)		Normal MISO status registers
Read device flags and wake-up flags, from register address (bit29-24). MISO return fixed device status (bit 31-20) + flags from the selected address (requires a double write)	MOSI	10	address	Read of device flags from a register address, and sub address LOW (bit 23)
	MISO	Device Fixed Status (12 bits)		Flag Registers

Table 18. MISO device status bits description

Flag	Description
INT	Indicates an INT has occurred and INT flags are pending to be read.
WU	Indicates a Wake-up has occurred and Wake-up flags are pending to be read.
RST	Indicates an Reset has occurred and the flags reporting the Reset source are pending to be read.
TLIM	Indicates a TLIM has occurred and TLIM flags are pending to be read.
TRAN-G	The INT, or WU or RST source is a transceiver interface (CAN or LIN).
VPRE-G	The INT, or WU or RST source is the VPRE switch mode power supply.
VREG-G	The INT, or WU or RST source is a regulator supply (V_{DD} or V_{AUX}).
SAFE_B-G	The INT, or WU or RST source is from a SAFE condition.
LIN23-G	The INT, or WU or RST source is a LIN bus (LIN2 or LIN3).
LIN01-G	The INT, or WU or RST source is a LIN bus (LIN0 or LIN1).
CAN-G	The INT, or WU or RST source is CAN interface. CAN local or CAN bus source.
SG-G	The INT, or WU or RST source is SG interface, flag from SG inputs.

Table 19. Internal memory registers A and B, RAM_A and RAM_B

MOSI First Byte [31-24] [b_31 b_30] 00_0xxx	MOSI, bits 23-0																							
	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a13	a12	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
Default state	0																							
Condition for default	POR																							
RAM_A 00_0001	Rb23	Rb22	Rb21	Rb20	Rb19	Rb18	Rb17	Rb16	Rb15	Rb14	Rb13	Rb12	Rb11	Rb10	Rb9	Rb8	Rb7	Rb6	Rb5	Rb4	Rb3	Rb2	Rb1	Rb0
Default state	0																							
Condition for default	POR																							
RAM_B 00_0010	Rb23	Rb22	Rb21	Rb20	Rb19	Rb18	Rb17	Rb16	Rb15	Rb14	Rb13	Rb12	Rb11	Rb10	Rb9	Rb8	Rb7	Rb6	Rb5	Rb4	Rb3	Rb2	Rb1	Rb0
Default state	0																							
Condition for default	POR																							

Table 20. Initialization registers - regulator, INIT REG

MOSI bits [31-24] [b_31 b_30] 00_0011	MOSI bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00_0011	VPRE_Disable	VDDLrst[1]	VDDLrst[0]	VDDrstD[1]	VDDrstD[0]	VAUX5/3	VAUXtracker	Unused
Default state	0	0	0	1	0	0	0	0
Condition for default	POR/Reset							

Table 21. Individual bits (watchdog)

Bit	Description
b7	VPRE_Disable
0	V_{PRE} is enabled and used by the IC
1	Disable VPRE internal circuitry (use external source to power VPRE node)
b6, b5	V_{DDLRST}[1] $V_{DDL\ RST}$[0] - Select the V_{DD} undervoltage threshold, to activate Reset pin and/or INT
00	Reset at approximately 0.9 V_{DD}.
01	INT at approximately 0.9 V_{DD}, Reset at approximately 0.7 V_{DD}
10	Reset at approximately 0.7 V_{DD}
11	Reset at approximately 0.9 V_{DD}
b4, b3	V_{DDRST}D[1] V_{DDRST}D[0] - Select the Reset pin low lev duration, after V_{DD} rises above the V_{DD} undervoltage threshold
00	1.0 ms
01	5.0 ms
10	10 ms [Default]
11	20 ms
b2	[VAUX5/3]- Select Vauxilary output voltage
0	V_{AUX} = 3.3 V
1	V_{AUX} = 5.0 V
b1	Tracking Enable
0	V_{AUX} is independent of V_{DD}
1	V_{AUX} tracks V_{DD} (ignored if V_{DD} and V_{AUX} not set to 5.0 V)
b0	Unused

Table 22. Initialization registers - watchdog

MOSI bits [31-24] [b_31 b_30] 00_0011	MOSI bits 15-8							
	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
00_0011	WD2INT	MCU_OC	OC-TIM	WD SAFE_B[1]	WD SAFE_B[0]	WD_spi[1]	WD_spi[0]	WD N/Win
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Table 23. Individual bits (watchdog)

Bit	Description
b15	WD2INT - Select the maximum time delay between INT occurrence and INT source read SPI command
0	Function disabled. No constraint between INT occurrence and INT source read.
1	INT source read must occur before the remaining of the current W/D period plus 2 complete W/D periods.
b14, b13	MCU_OC, OC-TIM - In Low-power VDDON, select watchdog refresh and VDD current monitoring functionality.VDD_OC_LP threshold is defined in device electrical parameters (approximately 2.0 mA)
In low-power mode, W/D is not selected	
no W/D + 00	In Low-power V_{DD} ON mode, V_{DD} overcurrent has no effect.
no W/D + 01	In Low-power V_{DD} ON mode, V_{DD} overcurrent has no effect.
no W/D + 10	In Low-power V_{DD} ON mode, V_{DD} current > $V_{DD\_OC\_LP}$ threshold for a time > I_mcu_OC is a wake-up event. I_mcu_OC time is selected in Timer register (selection range from 0.1 to 32 ms – 8 total options).
no W/D + 11	Unused
In low-power mode W/D is selected	
W/D + 00	In Low-power V_{DD} ON mode, V_{DD} current > $V_{DD\_OC\_LP}$ threshold has no effect. W/D refresh must occur by SPI command.
W/D + 01	In Low-power V_{DD} ON mode, V_{DD} current > $V_{DD\_OC\_LP}$ threshold has no effect. W/D refresh must occur by SPI command.
W/D + 10	In Low-power V_{DD} ON mode, V_{DD} current > $V_{DD\_OC\_LP}$ threshold for a time < I_mcu_OC is a W/D refresh condition. V_{DD} current > $V_{DD\_OC\_LP}$ threshold for a time > I_mcu_OC is wake-up event. I_mcu_OC time is selected in Timer register (selection range from 0.1 to 32 ms – 8 total options)
W/D + 11	Unused
b12, b11	WD SAFE_B - Select the activation of the SAFE_B pin low, at first or second consecutive RESET pulse.
00	SAFE_B pin is set low at the time of the RESET pin low activation
01	SAFE_B pin is set low at the second consecutive time RESET pulse
10	SAFE_B pin is set low at the third consecutive time RESET pulse
11	SAFE_B pin is set low at the fifth consecutive time RESET pulse
b10, b9	WD_spi[1] WD_spi[0] - Select the Watchdog (W/D) Operation
00	Simple Watchdog selection: W/D refresh done by a 8 bits or 32 bits SPI
01	Enhanced 1: Refresh is done using the Random Code, and by a single 32 bits.
10	Enhanced 2: Refresh is done using the Random Code, and by two 32 bit commands.
11	Enhanced 4: Refresh is done using the Random Code, and by four 32 bit commands.
b8	WD N/Win - Select the Watchdog (W/D) Window or Timeout operation
0	Watchdog operation is TIMEOUT, W/D refresh can occur anytime in the period
1	Watchdog operation is WINDOW, W/D refresh must occur in the open window (second half of period)

Table 24. Initialization registers - miscellaneous, INIT MISC

MOSI bits [31-24] [b_31 b_30] 00_0011	MOSI, bits 23-16							
	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
00_0011	LPM w RND	AMUX config	INT_B pulse	INT_B width	INT_B flash	SAFE_B[2]	SAFE_B[1]	SAFE_B[0]
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Table 25. Individual bits (INIT MISC)

Bit	Description
b23	LPM w RND - Select the functionality to change mode (enter in Low-power) using the device Random Code
0	Function disable: the Low-power mode can be entered without usage of Random Code
1	Function enabled: the Low-power mode is entered using the Random Code
b22	AMUX SPI configured
0	AMUX is determined by the SPI
1	N/A
b21	INT_B pulse - Select INT pin operation: low level pulse or low level
0	INT_B pin asserts a low level pulse, duration selected by bit [b4]
1	INT_B pin assert a permanent low level (no pulse)
b20	INT_B width - Select the INT pulse duration
0	INT_B pulse duration is typ. 100 µs. Refer to dynamic parameter table for exact value.
1	INT_B pulse duration is typ. 25 µs. Refer to dynamic parameter table for exact value.
b19	INT_B flash - Select INT pulse generation at 50% of the Watchdog Period in Flash mode
0	Function disable
1	Function enable: an INT pulse occurs at 50% of the Watchdog Period when device in Flash mode.
b18, b17, b16	SAFE_B[2], SAFE_B[1], SAFE_B[0] - Set state of Safe operation
0xx	Function disable (W/D inhibit mode)
100	RB3
101	RB2
110	RB1
111	RA

Table 26. Specific mode register SPE-MODE

MOSI bits [31-24] [b_31 b_30] 00_0100	MOSI bits 23-11	MOSI, bits 7-0							
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00_0100	Unused	Rnd_C7b	Rnd_C6b	Rnd_C5b	Rnd_C4b	Rnd_C3b	Rnd_C2b	Rnd_C1b	Rnd_C0b
Default state	0	0	0	0		0	0	0	0
Condition for default	POR								

Table 27. Specific mode register SPE-MODE

MOSI bits [31-24] [b_31 b_30] 00_0100	MOSI bits 23-11	MOSI, bits 10-8		
		bit 10	bit 9	bit 8
00_0100	Unused	Sel_Mod[2]	Sel_Mod[1]	Sel_Mod[0]
Default state	0	0	0	0
Condition for default	POR			

Table 28. Individual bit description (SPE-MODE)

Bit	Description
b10, b9, b8	Sel_Mod[2] Sel_Mod[1], Sel_Mod[0]- Mode selection: these 3 bits are used to select which mode the device enters upon a SPI command.
000	RESET mode
001	INIT mode
010	FLASH mode
011	RESET SG inputs
100 - 111	N/A
b7....b0	[Rnd_C7b... Rnd_C0b]- Random Code inverted, these 8 bits are the inverted bits obtained from the SPE-MODE Register read command.

The SPE MODE register is used for the following operation:

- Set the device in Reset mode, to exercise or test the Reset functions.

- Go to Init mode, using the Secure SPI command.

- Go to Flash mode (in this mode the watchdog timer can be extended up to 32 sec).

- Reset the registers for SG (switch to ground) inputs only.

- Activate the SAFE_B pin by S/W.

These mode (called Special Mode) are accessible via secured SPI command, which consist in two commands:

1. Reading a random code and
2. Write the inverted random code plus mode selection or SAFE_B pin activation:

Return to INIT mode is done as follow (this is done from Normal mode only):

1. Read random code:

MOSI: 0000 0100 0000 0000 0000 0000 0000 0000 [Hex:0x 04 00 00 00]

MISO report 32 bits, random code are bits (7-0)

MISO = xxxx xxxx xxxx xxxx xxxx xxxx R7 R6 R5 R4 R3 R2 R1 R0 (Rx = 8 bits random code)

2. Write INIT mode + random code inverted

MOSI: 0100 0100 0000 0000 0000 0001 Ri7 Ri6 Ri5 Ri4 Ri3 Ri2 Ri1 Ri0 [Hex:0x 44 00 01 HH] (Rix = random code inverted)

MISO: xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx (don't care)

SAFE_B pin activation: SAFE_B pin can be set low, in INIT and Normal mode, with following commands:

1. Read random code:

MOSI: 0000 0100 0000 0000 0000 0000 0000 0000 [Hex:0x 04 00 00 00]

MISO report 32 bits, random code are bits (7-0)

MISO = xxxx xxxx xxxx xxxx xxxx xxxx R7 R6 R5 R4 R3 R2 R1 R0 (Rx = 8 bits random code)

2. Write INIT mode + random code bits 7:6 not inverted and random code bits 5:0 inverted

MOSI: 0100 0100 0000 0000 0000 0001 R7 R6 Ri5 Ri4 Ri3 Ri2 Ri1 Ri0 [Hex 0x 44 00 01 HH] (Ri7-6 = random code, Ri5-0 = random code inverted)

MISO: xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx (don't care)

Go to Reset mode is done as follow (this is done from Normal mode only):

1. Read random code:

MOSI: 0000 0100 0000 0000 0000 0000 0000 0000 [Hex:0x 04 00 00 00]

MISO report 32 bits, random code are bits (7-0)

MISO = xxxx xxxx xxxx xxxx xxxx xxxx R7 R6 R5 R4 R3 R2 R1 R0 (Rx = 8 bits random code)

2. Write Reset mode + random code bits inverted

MOSI: 0100 0100 0000 0000 0000 0000 Ri7 Ri6 Ri5 Ri4 Ri3 Ri2 Ri1 Ri0 [Hex 0x 44 00 00 HH] (RiX = random code inverted)

MISO: xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx (don't care)

Go to Flash mode is done as follow (this is done from Normal mode only):

1. Read random code:

MOSI: 0000 0100 0000 0000 0000 0000 0000 0000 [Hex:0x 04 00 00 00]

MISO report 32 bits, random code are bits (7-0)

MISO = xxxx xxxx xxxx xxxx xxxx xxxx R7 R6 R5 R4 R3 R2 R1 R0 (Rx = 8 bits random code)

2. Write INIT mode + random code bits 7:6 not inverted and random code bits 5:0 inverted

MOSI: 0100 0100 0000 0000 0000 0010 Ri7 Ri6 Ri5 Ri4 Ri3 Ri2 Ri1 Ri0 [Hex 0x 44 00 02 HH] (RiX = random code inverted)

MISO: xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx (don't care)

Reset SG registers is done as follow (this is done from Normal mode only):

1. Read random code:

MOSI: 0000 0100 0000 0000 0000 0000 0000 0000 [Hex:0x 04 00 03 00]

MISO report 32 bits, random code are bits (7-0)

MISO = xxxx xxxx xxxx xxxx xxxx xxxx R7 R6 R5 R4 R3 R2 R1 R0 (Rx = 8 bits random code)

2. Write SG reset mode + random code bits inverted

MOSI: 0100 0100 0000 0000 0000 0011 Ri7 Ri6 Ri5 Ri4 Ri3 Ri2 Ri1 Ri0 [Hex 0x 44 00 03 HH] (RiX = random code inverted)

MISO: xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx (don't care).

Table 29. Watchdog and low-power MCU consumption, TIM_A

MOSI bits [31-24] [b_31 b_30] 00_0101	MOSI, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00_0101	I_mcu[2]	I_mcu[1]	I_mcu[0]	W/D Nor[4]	W/D_N[3]	W/D_Nor[2]	W/D_N[1]	W/D_Nor[0]
Default state	0	0	0	1	1	1	1	0
Condition for default	POR							

Table 30. Individual bit description for I_mcu timer

Typical Timing Value (in ms)				
b7	b6, b5			
	00	01	10	11
0	3 (def)	6	12	24
1	4	8	16	32

Table 31. Individual bit description for watchdog period in device normal mode

Typical Timing Value (in ms)								
b4, b3	b2, b1, b0							
	000	001	010	011	100	101	110	111
00	2.5	5	10	20	40	80	160	320
01	3	6	12	24	48	96	192	384
10	3.5	7	14	28	56	112	224	448
11	4	8	16	32	64	128	256 (def)	512

Table 32. Timer register B, periodic scan and cyclic INT, in device low-power mode, TIM_B

	MOSI, bits 15-8							
	bit 15	**bit 14**	**bit 13**	**bit 12**	**bit 11**	**bit 10**	**bit 9**	**bit 8**
	Cyc-sen[3]	Cyc-sen[2]	Cyc-sen[1]	Cyc-sen[0]	Cyc-int[3]	Cyc-int[2]	Cyc-int[1]	Cyc-int[0]
Default state	1	1	0	0	0	0	0	0
Condition for default	POR							

Table 33. Individual bit description for periodic scan

Typical timing value (in ms)								
b15	**b14, b13, b12**							
	000	001	010	011	100	101	110	111
0	3	6	12	24	48	96	192	384
1	4	8	16	32	64 (def)	128	256	512

Table 34. Individual bit description for periodic interrupt

Typical timing value (in ms)								
b11	**b10, b9, b8**							
	000	001	010	011	100	101	110	111
0	6 (def)	12	24	48	96	192	384	768
1	8	16	32	64	128	258	512	1024

Table 35. Timer register C, watchdog LP mode and forced wake-up timer, TIM_C

	MOSI bits 23-16							
	bit 23	**bit 22**	**bit 21**	**bit 20**	**bit 19**	**bit 18**	**bit 17**	**bit 16**
	WD-LP-F[3]	WD-LP-F[2]	WD-LP-F[1]	WD-LP-F[0]	FWU[3]	FWU[2]	FWU[1]	FWU[0]
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Table 36. Individual bit description for watchdog in low-power VDD on mode

Typical timing value (in ms)								
b23	b22, b21, b20							
	000	001	010	011	100	101	110	111
0	12 (def)	24	48	96	192	384	768	1536
1	16	32	64	128	256	512	1024	2048

Table 37. Individual bit description for watchdog in flash mode

Typical timing value (in ms)								
b23	b22, b21, b20							
	000	001	010	011	100	101	110	111
0	48 (def)	96	192	384	768	1536	3072	6144
1	256	512	1024	2048	4096	8192	16384	32768

Table 38. Individual bit description for forced wake-up

Typical timing value (in ms)								
b19	b18, b17, b16							
	000	001	010	011	100	101	110	111
0	48 (def)	96	192	384	768	1536	3072	6144
1	64	128	258	512	1024	2048	4096	8192

Table 39. AMUX

MOSI First Byte [31-24] [b_31 b_30] 00_0110	**MOSI, bits 23-8**	**MOSI, bits 7-0**							
		bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
00_0110	Unused	MUX_4	MUX_3	MUX_2	MUX_1	MUX_0	Unused	Unused	Unused
Default state	0	0	0	0	0	0	0	0	0
Condition for default	POR								

Table 40. Individual bits AMUX

Bits	Description
b8 b7 b6 b5 b4 b3	MUX_4, MUX_3, MUX_2, MUX_1, MUX_0 - Selection of the device external input signal or internal signal to be measured at AMUX pin
0 00000	All functions disable. AMUX pin high-impedance.
0 00001	Voltage at SG0
0 00101	Voltage at SG1
0 00110	Voltage at SG2
0 00111	Voltage at SG3
0 01000	Voltage at SG4
0 01011	Voltage at SG5
0 10010	Voltage at VBATSNS pin. Refer to electrical table for attenuation ratio (approximately 6 for V_{DD} = 5.0 V, approximately 9 for V_{DD} = 3.3 V) [Default].
0 10011	Device internal temperature sensor voltage

Table 41. Watchdog refresh register, W/D

MOSI bits [31-24] [b_31 b_30] 00_0111	MOSI bits 23-8	MOSI bits 7-0							
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00_0111	0	0	0	0	0	0	0	0	0
Default state	0	1	1	1	1	1	1	1	1
Condition for default	POR								

Table 42. INT_B register[(25)]

MOSI bits [31-24] [b_31 b_30] 00_1000	MOSI bits 23-9	MOSI bits 7-0								
		bit8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00_1000	Unused	MCU req	LIN3 fail	LIN2fail	LIN1 fail	LIN0 fail	SAFE_B		CAN failure	Vmon
Default state		0	0	0	0	0	0	0	0	0
Condition for default	POR									

Notes

25. The first time the device is set in Normal mode, the CAN is in Sleep wake-up enable (10). The next time device is set in Normal mode, the CAN state is controlled by the bit7 and bit6 states.

Table 43. Individual bit description (INT_B register)

Bits	Description
b8	MCU req- Control bit to request an INT. INT occurs once when the bit is enabled.
0	INT disable
1	INT enable
b7	LIN3 Fail
0	INT disable
1	INT enable
b6	LIN2 Fail
0	INT disable
1	INT enable
b5	LIN1 Fail
0	INT disable
1	INT enable
b4	LIN0 Fail
0	NT disable
1	INT enable
b3	SAFE_B- description to be done
0	INT disable
1	INT enable
b2	
0	INT disable
1	INT enable

Table 43. Individual bit description (INT_B register) (continued)

Bits	Description
b1	CAN failure- control bit for CAN failure INT (CANH/L to GND, VDD or VBATP, CAN overcurrent, Driver Over Temp, TX-PD, RX-PR, RX2HIGH, and CANBUS Dominate clamp)
0	INT disable
1	INT enable
b0	Vmon- enable interruption by voltage monitoring of one of the voltage regulator: VAUX, CAN5V, VDD(IDD overcurrent, overvoltage, undervoltage), VSUV, VSOV, VBATP$_{BATFAIL}$, CAN5V low or thermal shutdown, VAUXlow or VAUXovercurrent
0	INT disable
1	INT enable

Table 44. MODE register, moDE

MOSI bits [31-24] [b_31 b_30] 00_1001	MOSI bits 23-8	MOSI bits 7-0							
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00_1001	Unused	Mode[4]	Mode[3]	Mode[2]	Mode[1]	Mode[0]	Rnd_b[2]	Rnd_b[1]	Rnd_b[0]
Default state	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 45. Individual bit description for low-power V_{DD} off selection and operation mode

Low-power V_{DD} OFF Selection and Function		
b7, b6, b5, b4, b3	FWU	Periodic Sense
0 1100	OFF	OFF
0 1101	OFF	ON
0 1110	ON	OFF
0 1111	ON	ON

Table 46. Individual bit description for low-power V_{DD} on selection and operation mode

Low-power V_{DD} on selection and function				
b7, b6, b5, b4, b3	FWU	Periodic Sense	Periodic INT	Watchdog
1 0000	OFF	OFF	OFF	OFF
1 0001	OFF	OFF	OFF	ON
1 0010	OFF	OFF	ON	OFF
1 0011	OFF	OFF	ON	ON
1 0100	OFF	ON	OFF	OFF
1 0101	OFF	ON	OFF	ON
1 0110	OFF	ON	ON	OFF
1 0111	OFF	ON	ON	ON
1 1000	ON	OFF	OFF	OFF
1 1001	ON	OFF	OFF	ON
1 1010	ON	OFF	ON	OFF
1 1011	ON	OFF	ON	ON
1 1100	ON	ON	OFF	OFF

Table 46. Individual bit description for low-power V_{DD} on selection and operation mode (continued)

Low-power V_{DD} on selection and function				
b7, b6, b5, b4, b3	**FWU**	**Periodic Sense**	**Periodic INT**	**Watchdog**
1 1101	ON	ON	OFF	ON
1 1110	ON	ON	ON	OFF
1 1111	ON	ON	ON	ON

Table 47. REGULATOR register, REG

MOSI bits [31-24] [b_31 b_30] 00_1010	MOSI bits 23-8	MOSI bits 7-0							
		bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
00_1010	Unused	VAUX[1]	VAUX[0]	Unused	CAN5V[1]	CAN5V[0]	Unused	Unused	VDDoff en
Default state	0	0	0	N/A	0	0	N/A	N/A	N/A
Condition for default	POR				POR				

Table 48. Individual bit description (REG)

Bits	Description
b7 b6	VAUX[1], VAUX[0]- Vauxilary regulator control
00	Regulator OFF
01	Regulator ON. Undervoltage (UV) and overcurrent (OC) and overvoltage (OV) monitoring flags not reported. VAUX disable in case OC or UV detected after 1.0 ms blanking time (monitoring of flags not reported).
10	Regulator ON. Undervoltage (UV) and overcurrent (OC) and overvoltage (OV) monitoring flags active. VAUX disable in case OC or UV detected after 1.0 ms blanking time. (monitoring of flags not reported).
11	Regulator ON. Undervoltage (UV) and overcurrent (OC) and overvoltage (OV) monitoring flags active. VAUX disable in case OC or UV detected after 25 µs blanking time.
b4 b3	CAN5V[1], CAN5V[0]- CAN5V regulator control
00	Regulator OFF
01	Regulator ON. Thermal protection active. Undervoltage (UV) and overcurrent (OC) monitoring flags not reported.
10	Regulator ON. Thermal protection active. Undervoltage (UV) and overcurrent (OC) monitoring flags active.
11	Regulator ON. Thermal protection active. Undervoltage (UV) and overcurrent (OC) monitoring flags active. CAN5V disable in case OC or UV detected after 25 µs blanking time.
b0	VDDoff en - Control bit to allow transition into Low-power VDDOFF mode (to prevent VDD turn OFF)
0	Disable Usage of Low-power V_{DD} OFF mode
1	Enable Usage of Low-power V_{DD} OFF mode

Table 49. CAN registers, CAN[(26)]

MOSI bits [31-24] [b_31 b_30] 00_1011	MOSI bits 7-0							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
00_1011	Unused	Unused	Unused	CMFB Enable	Wake-up 1/3	CAN mod[1]	CAN mod[0]	CAN int
Default state	0	0	0	0	0	1	0	0
Condition for default	POR					note		POR

Note:
26. The first time the device is set in Normal mode, the CAN is in Sleep wake-up enable (10). The next time the device is set in Normal mode, the CAN state is controlled by the bit 2 and bit 1 states.

Table 50. Individual bit description (CAN)

Bits	Description
b4	CMFB enable for CAN
0	Common Mode Feed Back circuit is turned off
1	Common Mode Feed Back circuit is turned on
b3	Wake-up 1/3- Selection of CAN wake-up mechanism
0	Three dominant pulses wake-up mechanism
1	Single dominant pulse wake-up mechanism
b2 b1	CAN mod[1], CAN mod[0]- CAN interface mode control, wake-up enable/disable
00	CAN interface in sleep mode, CAN wake-up disable.
01	CAN interface in receive only mode, CAN driver disable.
10	CAN interface is in sleep mode, CAN wake-up enabled. In device low-power mode, CAN wake-up is reported by device wake-up. In device normal mode, CAN wake-up reported by INT and Flags generated.
11	CAN interface in transmit and receive mode
b0	CAN INT - Select the CAN failure detection reporting
0	Select INT generation when a bus failure is fully identified and decoded (i.e. after five dominant pulses on TxCAN)
1	Select INT generation as soon as a bus failure is detected, event if not fully identified.

Table 51. LIN 0-1 register

MOSI bits [31-24] [b_31 b_30] 00_1100	MOSI bits 23-10	MOSI bits 9-0									
		bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00_1100	Unused	LIN1 mode[1]	LIN1mode [0]	LIN1 Slew rate[1]	LIN1 Slew rate[0]	LIN1 J2602	LIN0 mode[1]	LIN0 mode[0]	LIN0 Slew rate[1]	LIN0 Slew rate[0]	LIN0 J2602
Default state	0	1	0	0	0	0	1	0	0	0	0
Condition for default	POR										

Table 52. Individual bit description (LIN0-1)

Bits	Description
b9 b8	LIN1 mode [1], LIN1 mode [0]- LIN 1 interface mode control, wake-up enable/disable
00	LIN1 disable, wake-up capability disable
01	not used
10	LIN1 disable, wake-up capability enable
11	LIN1 Transmit Receive mode
b7 b6	Slew rate[1], Slew rate[0] LIN 1 slew rate selection
00	Slew rate for 20 kbit/s baud rate
01	Slew rate for 10 kbit/s baud rate
10	Slew rate for fast baud rate
11	Slew rate for fast baud rate
b5	LIN1 J2602
0	LIN1 remain recessive
1	LIN1 operates below 6 V

Table 52. Individual bit description (LIN0-1) (continued)

Bits	Description
b4 b3	LIN0 mode [1], LIN0 mode [0]- LIN 0 interface mode control, wake-up enable/disable
00	LIN0 disable, wake-up capability disable
01	not used
10	LIN0 disable, wake-up capability enable
11	LIN0 Transmit Receive mode
b2 b1	Slew rate[1], Slew rate[0] LIN0 slew rate selection
00	Slew rate for 20 kbit/s baud rate
01	Slew rate for 10 kbit/s baud rate
10	Slew rate for fast baud rate
11	Slew rate for fast baud rate
b0	LIN0 J2602
0	LIN0 remain recessive
1	LIN0 operate below 6.0 V

Table 53. LIN 2-3 register

MOSI bits [31-24] [b_31 b_30] 00_1101	MOSI bits 23-10	MOSI bits 9-0									
		bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00_1101	Unused	LIN3 mode[1]	LIN3 mode[0]	LIN3 Slew rate[1]	LIN3 Slew rate[0]	LIN3 J2602	LIN2 mode[1]	LIN2 mode[0]	LIN2 Slew rate[1]	LIN2 Slew rate[0]	LIN2 J2602
Default state	0	1	0	0	0	0	1	0	0	0	0
Condition for default	POR										

Table 54. Individual bit description (LIN2-3)

Bits	Description
b9 b8	LIN3 mode [1], LIN3 mode [0]- LIN 3 interface mode control, wake-up enable/disable
00	LIN3 disable, wake-up capability disable
01	Not used
10	LIN3 disable, wake-up capability enable
11	LIN3 Transmit Receive mode
b7 b6	Slew rate[1], Slew rate[0] LIN 3 slew rate selection
00	Slew rate for 20 kbit/s baud rate
01	Slew rate for 10 kbit/s baud rate
10	Slew rate for fast baud rate
11	Slew rate for fast baud rate
b5	LIN3 J2602
0	LIN3 remain recessive
1	LIN3 operate below 6.0 V
b4 b3	LIN2 mode [1], LIN2 mode [0]- LIN2 interface mode control, wake-up enable/disable
00	LIN2 disable, wake-up capability disable

Table 54. Individual bit description (LIN2-3) (continued)

Bits	Description
01	Not used
10	LIN2 disable, wake-up capability enable
11	LIN2 Transmit Receive mode
b2 b1	Slew rate[1], Slew rate[0] LIN 2 slew rate selection
00	Slew rate for 20 kbit/s baud rate
01	Slew rate for 10 kbit/s baud rate
10	Slew rate for fast baud rate
11	Slew rate for fast baud rate
b5	LIN2 J2602
0	LIN2 remain recessive
1	LIN2 operate below 6.0 V

Table 55. SG wake-up enable

MOSI bits [31-24] [b_31 b_30] 00_1110	MOSI bits 23-0												
	bit 23-17	bit 15-11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00_ 1110	Unused	Unused	SG5	Unused	Unused	SG4	SG3	SG2	SG1	Unused	Unused	Unused	SG0
Default state	0	1	1										
Condition for default	POR/Reset command												

Table 56. SG5-0 fast scan enable

MOSI bits [31-24] [b_31 b_30] 00_1111	MOSI bits 23-0												
	bit 23-17	bit 15-0	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00_ 1111	Unused	Unused	SG5	Unused	Unused	SG4	SG3	SG2	SG1	Unused	Unused	Unused	SG0
Default state	0	0	0										
Condition for default	POR/Reset command												

Table 57. Individual bit description (SG5-0 fast scan enable)

Bits	Description
b10,b7-4,b0	SG5-0 (Default = 0)
0	Use normal wake-up timing as defined in sleep state command.
1	Enables fast wake-up at 1.0 ms polling independent of normal wake-up selected in sleep state command.

Table 58. SG wake-up delay enable

MOSI bits [31-24] [b_31 b_30] 01_0000	MOSI bits 23-0												
	bit 23-17	bit 15-11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01_ 0000	Unused	Unused	SG5	Unused	Unused	SG4	SG3	SG2	SG1	Unused	Unused	Unused	SG0
Default state	0	0	0										
Condition for default	POR/Reset command												

Table 59. Individual bit description (wake-up delay enable)

Bits	Description
b10,b7-4,b0	Controls SG5 – SG0 to Enable/Disable Wake-up delay during sleep mode. (Default = 0)
0	Disables wake-up delay for SGn from sleep mode (Device does not wake up with change of state on SGn).
1	Enable wake-up delay for SGn from sleep mode (Device wakes up with change of state on SGn)

Table 60. Wetting current register 0

MOSI bits [31-24] [b_31 b_30] 01_0001	MOSI bits 23-0							
	bits 23-21	bit 20-18	bits 17-15	bits 14-12	bits 11-9	bits 8-6	bit 5-3	bit 2-0
01_ 0001	SG4	SG3	SG2	SG1	Unused	Unused	Unused	SG0
Default state	110	110	110	110	Unused	Unused	Unused	110
Condition for default	POR/Reset command							

Table 61. Individual bit description (wetting current register 0)

Bits	Description
b[cba]	Bit pattern for Wetting current level for input pins (Default = 110)
000	Sets the Wetting current Off
001	Sets the Wetting current level to 6.0 mA
010	Sets the Wetting current level to 8.0 mA
011	Sets the Wetting current level to 10 mA
100	Sets the Wetting current level to 12 mA
101	Sets the Wetting current level to 14 mA
110	Sets the Wetting current level to 16 mA
111	Sets the Wetting current level to 20 mA
b23-21	Controls SG4 Wetting current setting. (Default = 110)
b20-18	Controls SG3 Wetting current setting. (Default = 110)
b17-15	Controls SG2 Wetting current setting. (Default = 110)
b14-12	Controls SG1 Wetting current setting. (Default = 110)
b2-0	Controls SG0 Wetting current setting. (Default = 110)

Table 62. Wetting current register 1

MOSI bits [31-24] [b_31 b_30] 01_0010	MOSI bits 23-0							
	bits 23-21	bit 20-18	bits 17-15	bits 14-12	bits 11-9	bits 8-6	bit 5-3	bit 2-0
01_ 0010	Unused	Unused	Unused	Unused	Unused	SG5	Unused	Unused
Default state	Unused	Unused	Unused	Unused	Unused	110	Unused	Unused
Condition for default	POR/Reset command							

Table 63. Individual bit description (wetting current register 1)

Bits	Description
b[cba]	Bit pattern for Wetting current level for input pins (Default = 110)
000	Sets the Wetting current to Off
001	Sets the Wetting current level to 6.0 mA
010	Sets the Wetting current level to 8.0 mA
011	Sets the Wetting current level to 10 mA
100	Sets the Wetting current level to 12 mA
101	Sets the Wetting current level to 14 mA
110	Sets the Wetting current level to 16 mA
111	Sets the Wetting current level to 20 mA
b8-6	Controls SG5 Wetting current setting. (Default = 110)

Table 64. SG wetting current timer enable

MOSI bits [31-24] [b_31 b_30] 01_0011	MOSI bits 23-0												
	bit 23-17	bit 15-11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01_ 0011	Unused	Unused	SG5	Unused	Unused	SG4	SG3	SG2	SG1	Unused	Unused	Unused	SG0
Default state	0	0	1										
Condition for default	POR/Reset command												

Table 65. Individual bit description (wetting current timer enable)

Bits	Description
b10,b7-b4,b0	Controls SG5-0 Wetting current timer enable. (Default = 1). This enables a 20 ms (nominal) timer turns off the Wetting current
0	Disables timer and results in the Wetting current to run continuously
1	Enables timer to turn off Wetting current after 20 ms (nominal)

Table 66. SG tristate

MOSI bits [31-24] [b_31 b_30] 01_0100	MOSI bits 23-0												
	bit 23-17	bit 15-11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01_ 0100	Unused	Unused	SG5	Unused	Unused	SG4	SG3	SG2	SG1	Unused	Unused	Unused	SG0
Default state	0	0	1										
Condition for default	POR/Reset command												

Table 67. Individual bit description (Tristate)

Bits	Description
b10,b7-b4,b0	Set SG5-0 to tri-state (Default = 1)
0	Sets input to active mode.
1	Sets input to tristate (Hi Z) mode.

4.3.3 Device flags registers

Table 68. Device flags - MISC

MOSI bits [31-24] 10 00_1001	MOSI bits 23-10	MISO bits 8-0									
		bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10 00_1001	Unused	WD INT at 50% Flash mode	SAFE_B Activated	FSM State (bit4)	FSM State (bit3)	FSM State (bit2)	FSM State (bit1)	FSM State (bit0)	WDI mode	WDI pin status (bit 1)	WDI pin status (bit 0)
Default state	0	0	0	0	0	0	1	0	0	0	0
Condition for default	POR										

Table 69. Individual bit description - MISC

Bits		Description
b23-10		Unused
b9	WD INT at 50% Flash mode	
	Description	Watchdog interrupt pulse generation at 50% of the watchdog period in Flash mode
	Set/Reset condition	Set: Time elapsed to 50% of watchdog timer in Flash mode. Reset: Flag read (SPI) Note: Flag resets only after exiting Flash mode and then SPI flag read.
b8	SAFE_B activated	
	Description	SAFE_B pin activated for any reason
	Set/Reset condition	Set: Safe mode activated. Reset: POR or SPI read
b7, b6, b5, b4, b3	FSM State (Bit 4,3,2,1,0)	
	Description	Determine what state the device is in (see **Table 70** for description)
	Set/Reset condition	Set: Determined by state of IC. Reset: POR
b2	WDI Mode	
	Description	In watchdog inhibit mode
	Set/Reset condition	Set: Voltage at WDI greater then threshold. Reset: Voltage lowered below threshold or POR
b1, b0	WDI pin status (BIT1,0)	
	Description	WDI pin in Safe mode A [00], B1 [01], B2 [10], B3 [11]
	Set/Reset condition	Set: WDI set during INIT Reset. Reset: POR.

Table 70. FSM state

Bits	Description
b7, b6, b5, b4, b3	State
00000	INIT
00010	Normal Request
00011	Normal
00001	Flash
10000	Low-power V_{DD} ON – xxx = SPI Mode command bits 6:3 (forced wake-up, periodic interrupt, watchdog)

Table 71. Device flags - regulators

MOSI bits [31-24] 10 00_1010	MOSI bits 23-20	MISO bits 7-0							
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10 00_1010	Unused	VAUX Undervoltage	VAUX overcurrent	CAN5V Thermal shutdown	CAN5V UV	CAN5Voverc urrent	VBATP batfail	VBATP Undervoltage	VBATP Overvoltage
Default state	0	0	0	0	0	0	0	0	0
Condition for default	POR								

Table 72. Device flags - regulators

MOSI bits [31-24] 10 00_1010	MOSI bits 23-20	MISO bits 15-8							
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
10 00_1010	Unused	VPRE Thermal Shutdown	VPRE Boosted	I_{DD} Overcurrent Low-power V_{DD} On mode	I_{DD} Overcurrent NORMAL mode	V_{DD} Overvoltage	V_{DD} Undervolta ge	V_{DD} Undervoltage > 100 ms	V_{AUX} Overvoltage
Default state	0	0	0	0	0	0	0	0	0
Condition for default	POR								

Table 73. Device flags - regulators

MOSI bits [31-24] 10 00_1010	MOSI bits 23-20	MISO bits 19-16			
		bit 19	bit 18	bit 17	bit 16
10 00_1010	Unused	VPRE IPFF	VPRE Overcurrent	VPRE Overvoltage	VPRE Undervoltage
Default state	0	0	0	0	0
Condition for default	POR				

Table 74. Individual bit description - regulators

Bits		Description
b23-8		Unused
b19	VPRE IPFF	
	Description	Report V_{PRE} IPFF
	Set/Reset condition	Set: V_{PRE} IPFF. Reset: V_{PRE} out of IPFF and flag read (SPI)
b18	VPRE Overcurrent	
	Description	Reports current out of V_{PRE} is higher than the I_{PRE-OC} threshold.
	Set/Reset condition	Set: current above threshold for t > 100 µs typ. Reset; current below threshold and flag read (SPI)
b17	VPRE Overvoltage	
	Description	Reports when V_{PRE} was above overvoltage threshold
	Set/Reset condition	Set: V_{PRE} was above OV threshold. Reset: V_{PRE} below OV and flag read (SPI)
b16	VPRE Undervoltage	
	Description	Reports when V_{PRE} is below undervoltage threshold
	Set/Reset condition	Set: V_{PRE} below threshold for t > 100 µs typ. Reset: V_{PRE} above threshold and flag read (SPI)

Table 74. Individual bit description - regulators (continued)

Bits		Description
b15	VPRE Thermal Shutdown	
	Description	Reports the V_{PRE} has reached overtemperature threshold, and was turned off.
	Set/Reset condition	Set: V_{PRE} OFF due to thermal condition. Reset: VPRE recover and flag read (SPI)
b14	VPRE_Boosted	
	Description	Reports V_{PRE} boost circuit activated
	Set/Reset condition	Set: V_{PRE} boost activated. Reset: V_{PRE} out of boost mode and flag read (SPI)
b13	I_{DD} Overcurrent Low-power V_{DD} On mode	
	Description	Reports current out of V_{DD} pin is higher than the I_{DD-OC} threshold LP, while device is in Low-power V_{DD} ON mode.
	Set/Reset condition	Set: current above threshold for t > 100 µs typ. Reset; current below threshold and flag read (SPI)
b12	I_{DD} Overcurrent NORMAL mode	
	Description	Reports current out of V_{DD} pin is higher than I_{DD-OC} threshold, while device is in Normal mode.
	Set/Reset condition	Set: current above threshold for t > 100 µs typ. Reset; current below threshold and flag read (SPI)
b11	V_{DD} Overvoltage	
	Description	Reports VDD pin is higher than the typ V_{DD} + 0.6 V threshold (27)
	Set/Reset condition	Set: V_{DD} above threshold for t >100 µs typ. Reset: V_{DD} below threshold and flag read (SPI)
b10	V_{DD} low interrupt	
	Description	Reports V_{DD} output voltage is lower than the V_{DD_UV} threshold and causing an Interrupt, based on the VDDLRST[1:0] bits set in the INIT register. This flag only sets if the setup in INIT is set to cause an Interrupt on an undervoltage.
	Set/Reset condition	Set: V_{DD} below threshold for t > 100 µs typ. Reset: V_{DD} above threshold and flag read (SPI)
b9	V_{DD} low >100 ms	
	Description	Reports VDD pin is lower than the V_{DDUV} threshold for a time longer than 100 ms (27)
	Set/Reset condition	Set: V_{DD} below threshold for t > 100 ms typ. Reset: V_{DD} above threshold and flag read (SPI)
b8	V_{AUX} Overvoltage	
	Description	Reports VAUX pin is higher than the typ V_{AUX} + 0.6 V threshold.
	Set/Reset condition	Set: VAUX above threshold for t > 100 µs typ. Reset: V_{AUX} below threshold and flag read (SPI)
b7	V_{AUX} Under voltage	
	Description	Reports V_{AUX} regulator output voltage is lower than the V_{AUX_UV} threshold. The VAUX undervoltage flag typically occurs in conjunction with the VAUX overcurrent flag, due to the functional cause.
	Set/Reset condition	Set: V_{AUX} below threshold for t > 100 µs typ. Reset: V_{AUX} above threshold and flag read (SPI)
b6	$V_{AUX\_OVERCURRENT}$	
	Description	Report current out of V_{AUX} regulator is above V_{AUX_OC} threshold.
	Set/Reset condition	Set: Current above threshold for t > 100 µs. Reset: Current below threshold and flag read by SPI.
b5	CAN5V Thermal shutdown	
	Description	Report the CAN5V regulator has reached overtemperature threshold.
	Set/Reset condition	Set: CAN5V thermal sensor above threshold. Reset: thermal sensor below threshold and flag read (SPI)
b4	CAN5V UV	
	Description	Reports CAN5V regulator output voltage is lower than the CAN5V UV threshold.
	Set/Reset condition	Set: CAN5V below CAN5V UV for t > 100 µs typ. Reset: CAN5V > threshold and flag read (SPI)

Table 74. Individual bit description - regulators (continued)

Bits		Description
b3	CAN5V overcurrent	
	Description	Report the CAN driver output current is above threshold.
	Set/Reset condition	Set: CAN5V current above threshold for t > 100 μs. Reset: CAN5V current below threshold and flag read (SPI)
b2	VBATP batfail	
	Description	Report the device voltage at VBATP pin was below BATFAIL threshold.
	Set/Reset condition	Set: V_{BATP} below BATFAIL. Reset: V_{BATP} above threshold, and flag read (SPI)
b1	$V_{BATP\_underVOLTAGE}$	
	Description	Reports VBATP pin is lower than the VBATP low resoled.
	Set/Reset condition	Set: V_{BATP} below threshold for t > 100 μs typ. Reset: V_{BATP} above threshold and flag read (SPI)
b0	V_{BATP} Overvoltage	
	Description	Report V_{BATP} was above overvoltage threshold
	Set/Reset condition	Set: V_{BATP} was above OV threshold. Reset: VBATP below OV and flag read (SPI)

Notes

27. When a V_{DD} overvoltage condition occurs, the flag register for V_{DD} undervoltage > 100 ms is also set. This was done to logically enable a SAFE condition when the over voltage occurs.

Table 75. Device flags – CAN

MOSI bits [31-24] 10 00_1011	MOSI bit 23 Select bit	MOSI bits 22-17	MISO bits 7-0							
			bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10 00_1011	0	Unused	CAN wake-up	-	CAN Overtemp	RxD low	RxD high	TxD dom	Bus Dom clamp	CAN Overcurrent
Default state		0	0	0	0	0	0	0	0	0
Condition for default		POR								

Table 76. Device flags – CAN

MOSI bits [31-24] 10 00_1011	MOSI bit 23 Select bit	MOSI bits 22-16	MISO bits 7-0							
			bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
10 00_1011	0	Unused	CAN_UF	CAN_F	CANL to VBAT	Unused	CANL to GND	CANH to VBAT	Unused	CANH to GND
Default state		0	0	0	0	0	0	0	0	0
Condition for default		POR								

Table 77. Individual bit description – CAN

Bits		Description
b15	CAN_UF	
	Description	Report the CAN failure detection has not yet identified the bus failure
	Set/Reset condition	Set: bus failure pre detection. Reset: CAN bus failure recovered and flag read
b14	CAN_F	
	Description	Report the CAN failure detection has identified the bus failure
	Set/Reset condition	Set: bus failure complete detetction.Reset: CAN bus failure recovered and flag read

Table 77. Individual bit description – CAN (continued)

Bits		Description
b13	CANL to VBAT	
	Description	Report CAN L short to VBAT failure
	Set/Reset condition	Set: failure detected. Reset failure recovered and flag read (SPI)
b11	CANL to GND	
	Description	Report CAN L short to GND failure
	Set/Reset condition	Set: failure detected. Reset failure recovered and flag read (SPI)
b10	CANH to VBAT	
	Description	Report CAN H short to VBAT failure
	Set/Reset condition	Set: failure detected. Reset failure recovered and flag read (SPI)
b8	CANH to GND	
	Description	Reports CAN H short to VBATP failure
	Set/Reset condition	Set: failure detected. Reset failure recovered and flag read (SPI)
b7	CAN wake-up	
	Description	Reports the wake-up source is CAN
	Set/Reset condition	Set: after CAN wake detected. Reset: Flag read (SPI)
b5	CAN Overtemp	
	Description	Reports the CAN interface has reach overtemperature threshold.
	Set/Reset condition	Set: CAN thermal sensor above threshold. Reset: thermal sensor below threshold and flag read (SPI)
b4	RxD low	
	Description	Reports the Rx pin is shorted to GND.
	Set/Reset condition	Set: Rx low failure detected. Reset: failure recovered and flag read (SPI)
b3	RxD high	
	Description	Reports the Rx pin is shorted to recessive voltage.
	Set/Reset condition	Set: Rx high failure detected. Reset: failure recovered and flag read (SPI)
b2	TxD dom	
	Description	Reports the Tx pin is shorted to GND
	Set/Reset condition	Set: Tx low failure detected. Reset: failure recovered and flag read (SPI)
b1	Bus Dom clamp	
	Description	Reports the CAN bus is dominant for a time longer than t_{DOM}
	Set/Reset condition	Set: Bus dominant clamp failure detected. Reset: failure recovered and flag read (SPI)
b0	CAN Overcurrent	
	Description	Reports the CAN current is above CAN overcurrent threshold.
	Set/Reset condition	Set: CAN current above threshold. Reset: current below threshold and flag read (SPI)

Table 78. Device flags – interrupt

MOSI bits [31-24] 10 00_1000	MOSI bits 23-16	MISO bits 7-0							
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10 00_1000	Unused	INT request	RST high	Reset request	Unused	Unused	RESET Low < 100 ms	SAFE SPI resistor mismatch	VPRE thermal warning
Default state	0	0	0	0	0	0	0	0	0
Condition for default	POR								

Table 79. Device flags – interrupt

MOSI bits [31-24] 10 00_1000	MOSI bits 23-16	MISO bits 15-8							
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
10 00_1000	Unused	INT service Timeout	FWU	SPI Wake-up	Unused	VDD low RST	RST low > 100 ms	multiple Resets	W/D refresh failure
Default state	0	0	0	0	0	0	0	0	0
Condition for default	POR								

Table 80. Individual bit description – interrupt

Bits		Description
b15	INT service Timeout	
	Description	Reports the INT timeout error detected. An interrupt occurrence stays asserted for more than three watchdog periods without ever being cleared.
	Set/Reset condition	Set: INT service timeout expired and WD2INT set. Reset: flag read and original INT cleared.
b14	FWU	
	Description	Reports the wake-up source is Forced Wake-up
	Set/Reset condition	Set: after Forced Wake-up detected. Reset: Flag read (SPI)
b13	SPI Wake-up	
	Description	Reports the wake-up source is SPI command, in Low-power V_{DD} on.
	Set/Reset condition	Set: after SPI Wake-up detected. Reset: Flag read (SPI)
b11	VDD low RST	
	Description	Reports V_{DD} is below the V_{DD} undervoltage threshold and causes a RESET, based on the VDDLRST [1:0] bits set in the INIT register.
	Set/Reset condition	Set: V_{DD} below threshold. Reset: flag read (SPI)
b10	RST low > 100ms	
	Description	Reports the Reset pin has detected a low level, longer than 100 ms (Reset permanent low)
	Set/Reset condition	Set: after detection of reset low pulse. Reset: Reset pulse terminated and flag read (SPI)
b9	Multiple Resets	
	Description	Reports the more than 8 consecutive reset pulses occurred, due to missing or wrong W/D refresh.
	Set/Reset condition	Set: after detection of multiple reset pulses. Reset: flag read (SPI)
b8	W/D refresh failure	
	Description	Reports a wrong or missing W/D failure occurred
	Set/Reset condition	Set: Failure detected. Reset: flag read (SPI)

Table 80. Individual bit description – interrupt (continued)

Bits		Description
b7	INT request	
	Description	Reports the INT source is an INT request from a SPI command.
	Set/Reset condition	Set: INT occurred. Reset: flag read (SPI)
b6	RST high	
	Description	Reports the RST_B pin is shorted to high voltage.
	Set/Reset condition	Set: RST failure detection. Reset: flag read.
b5	Reset Request	
	Description	Reports the RST source is an request from a SPI command (go to RST mode).
	Set/Reset condition	Set: After reset occurred due to SPI request. Reset: flag read (SPI)
b2	RESET Low < 100 ms	
	Description	Reports the Reset pin has detected a low level, shorter than 100 ms
	Set/Reset condition	Set: after detection of reset low pulse. Reset: Reset pulse terminated and flag read (SPI)
b1	SAFE SPI resistor mismatch	
	Description	Reports the SPI word setting the state of SAFE (A, B1, B2, B3) does not match the resistor value set at startup
	Set/Reset condition	Set: after SPI command to set SAFE mode and if it does not match. Reset: POR or matching SPI word sent.
b0	VPRE thermal warning	
	Description	Reports the VPRE thermal warning temperature has been reached
	Set/Reset condition	Set: after V_{PRE} thermal warning: Reset Temperature falls below thermal warning limit and SPI read.

Table 81. Device flags – LIN01

MOSI bits [31-24] 10 00_1100	MOSI bits 23-16	MISO bits 7-0							
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10 00_1100	Unused	Unused	LIN0 wake-up	Unused	LIN 0 Overtemp	RxD0 low	RxD0 high	TxD0 dom	LIN0 bus dom clamp
Default state	0	0	0	0	0	0	0	0	0
Condition for default	POR								

Table 82. Device flags – LIN01

MOSI bits [31-24] 10 00_1100	MOSI bits 23-16	MISO bits 7-0							
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
10 00_1100	Unused	Unused	LIN1wake-up	Unused	LIN 1Overtemp	RxD1 low	RxD1 high	TxD1 dom	LIN1 bus dom clamp
Default state	0	0	0	0	0	0	0	0	0
Condition for default	POR								

Table 83. Individual bit description – LIN01

Bits		Description
b14	LIN1 wake-up	
	Description	Reports the wake-up source is LIN1
	Set/Reset condition	Set: after CAN wake detected. Reset: Flag read (SPI)
b12	LIN 1 Overtemp	
	Description	Reports the LIN1 interface has reach overtemperature threshold.
	Set/Reset condition	Set: CAN thermal sensor above threshold. Reset: thermal sensor below threshold and flag read (SPI)
b11	RxD1 low	
	Description	Reports the RxDL pin is shorted to GND.
	Set/Reset condition	Set: Rx low failure detected. Reset: failure recovered and flag read (SPI)
b10	RxD1 high	
	Description	Reports the RxDL pin is shorted to recessive voltage.
	Set/Reset condition	Set: Rx high failure detected. Reset: failure recovered and flag read (SPI)
b9	TxD1 dom	
	Description	Reports the TxDL pin is shorted to GND.
	Set/Reset condition	Set: Tx low failure detected. Reset: failure recovered and flag read (SPI)
b8	LIN1 busdom clamp	
	Description	Reports the LIN1 bus is dominant for a time longer than t_{DOM}
	Set/Reset condition	Set: Bus dominant clamp failure detected. Reset: failure recovered and flag read (SPI)
b6	LIN0 wake-up	
	Description	Reports the wake-up source is LIN0
	Set/Reset condition	Set: after CAN wake detected. Reset: Flag read (SPI)
b4	LIN 0 Overtemp	
	Description	Reports the LIN0 interface has reach overtemperature threshold.
	Set/Reset condition	Set: CAN thermal sensor above threshold. Reset: thermal sensor below threshold and flag read (SPI)
b3	RxD0 low	
	Description	Reports the RxDL pin is shorted to GND.
	Set/Reset condition	Set: Rx low failure detected. Reset: failure recovered and flag read (SPI)
b2	RxD0 high	
	Description	Reports the RxDL pin is shorted to recessive voltage.
	Set/Reset condition	Set: Rx high failure detected. Reset: failure recovered and flag read (SPI)
b1	TxD0 dom	
	Description	Reports the TxDL pin is shorted to GND.
	Set/Reset condition	Set: Tx low failure detected. Reset: failure recovered and flag read (SPI)
b0	LIN0 busdom clamp	
	Description	Reports the LIN0 bus is dominant for a time longer than t_{DOM}
	Set/Reset condition	Set: Bus dominant clamp failure detected. Reset: failure recovered and flag read (SPI)

Table 84. Device flags – LIN23

MOSI bits [31-24] 10 00_1101	MOSI bits 23-16	MISO bits 7-0							
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10 00_1101	Unused	Unused	LIN2 wake-up	Unused	LIN 2 Overtemp	RxD2 low	RxD2 high	TxD2 dom	LIN2 busdom clamp
Default state	0	0	0	0	0	0	0	0	0
Condition for default	POR								

Table 85. Device flags – LIN23

MOSI bits [31-24] 10 00_1101	MOSI bits 23-16	MISO bits 7-0							
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
10 00_1101	Unused	Unused	LIN3 wake-up	Unused	LIN 3 Overtemp	RxD3 low	RxD3 high	TxD3 dom	LIN3 busdom clamp
Default state	0	0	0	0	0	0	0	0	0
Condition for default	POR								

Table 86. Individual bit description – LIN23

Bits		Description
b14	LIN3 wake-up	
	Description	Reports the wake-up source is LIN3
	Set/Reset condition	Set: after CAN wake detected. Reset: Flag read (SPI)
b12	LIN 3 Overtemp	
	Description	Reports the LIN3 interface has reach overtemperature threshold.
	Set/Reset condition	Set: CAN thermal sensor above threshold. Reset: thermal sensor below threshold and flag read (SPI)
b11	RxD3 low	
	Description	Reports the RxDL pin is shorted to GND.
	Set/Reset condition	Set: Rx low failure detected. Reset: failure recovered and flag read (SPI)
b10	RxD3 high	
	Description	Reports the RxDL pin is shorted to recessive voltage.
	Set/Reset condition	Set: Rx high failure detected. Reset: failure recovered and flag read (SPI)
b9	TxD3 dom	
	Description	Reports the TxDL pin is shorted to GND.
	Set/Reset condition	Set: Tx low failure detected. Reset: failure recovered and flag read (SPI)
b8	LIN3 busdom clamp	
	Description	Reports the LINx bus is dominant for a time longer than t_{DOM}
	Set/Reset condition	Set: Bus dominant clamp failure detected. Reset: failure recovered and flag read (SPI)
b6	LIN2 wake-up	
	Description	Reports the wake-up source is LIN2
	Set/Reset condition	Set: after CAN wake detected. Reset: Flag read (SPI)
b4	LIN 2 Overtemp	
	Description	Reports the LIN2 interface has reach overtemperature threshold.
	Set/Reset condition	Set: CAN thermal sensor above threshold. Reset: thermal sensor below threshold and flag read (SPI)

Table 86. Individual bit description – LIN23 (continued)

Bits		Description
b3	RxD2 low	
	Description	Reports the RxDL pin is shorted to GND.
	Set/Reset condition	Set: Rx low failure detected. Reset: failure recovered and flag read (SPI)
b2	RxD2 high	
	Description	Reports the RxDL pin is shorted to recessive voltage.
	Set/Reset condition	Set: Rx high failure detected. Reset: failure recovered and flag read (SPI)
b1	TxD2 dom	
	Description	Reports the TxDL pin is shorted to GND.
	Set/Reset condition	Set: Tx low failure detected. Reset: failure recovered and flag read (SPI)
b0	LIN2 busdom clamp	
	Description	Reports the LINx bus is dominant for a time longer than t_{DOM}
	Set/Reset condition	Set: Bus dominant clamp failure detected. Reset: failure recovered and flag read (SPI)

4.3.3.1 Abnormal operation (as applicable to each specific ASIC)

The 33909 is subject to various conditions considered abnormal as defined within this section.

4.3.3.1.1 Jump start

Complete functionality is guaranteed for a battery voltage of 26.5 V (or other application specific value) up to $T_A \leq 50$ °C for at least two minutes. A complete characterization is completed at this voltage and temperature. Performance at two minutes is guaranteed by bench characterization. No internal faults is set or abnormal operation noted as a result of operating in this range.

4.3.3.1.2 Load dump

The device must be capable of withstanding a typical load dump transient voltage of 40 V (or other application specific value) over the entire specified operating temperature range. Full parametric conformance is not required, Functionality up to overvoltage shutdown is guaranteed as well as up to the thermal capability of the package and external components with the exception of internal diagnostics, which are not required. No internal faults are set as a result of operating in this range.

4.3.3.1.3 Low-voltage operation

The low-voltage operating range is the application specific voltage range where full parametric conformance is not required of the device. However, all functions remain in stable operation and return to their proper behavior upon return to the normal operation voltage range.

4.3.3.1.4 Undervoltage lockout

This undervoltage lockout voltage range is dependent upon the silicon technology and the design, but is defined as the voltage range where all applicable output drivers are maintained in their OFF state. This range is intended to define the voltages at which the device is not capable of meeting internal threshold requirements to guarantee functionality. While in undervoltage lockout, the driver outputs are not be allowed to 'float' and inadvertently turn an output ON.

4.3.3.1.5 Reverse battery

This device with applicable external components is not damaged by exposure to reverse battery conditions of -14 V (or other application specific values). This test is performed for a period of one minute at 25 °C. In addition, this negative voltage condition does not force any of the logic level I/O pins to a negative voltage less than -0.6 V at 10 mA, or to a positive voltage greater the 5.0 V DC. This insures protection of the digital device interfacing with this device.

4.3.3.1.6 Ground offset

The applicable driver outputs and/or current sense inputs are capable of operation with a ground offset of ±2.0 V DC. The device is not damaged by exposure to this condition and maintains specified functionality.

4.3.3.1.7 Shorts to ground

All I/O's of the device are available at the module connector and are protected against shorts to ground with maximum ground offset considered (i.e. -2.0 V referenced to device ground or other application specific value). The device is not be damaged by this condition.

4.3.3.1.8 Shorts to battery

All I/O's of the device are available at the module connector and are protected against a short to battery (voltage value is application dependent, there may be cases where short to jump start or load dump voltage values are required). The device is not damaged by this condition.

4.3.3.1.9 Unpowered shorts to battery

All I/O's of the device are available at the module connector and are protected against unpowered (battery to the module is open) shorts to battery per application specifics. The device is not damaged by this condition, does not enable any outputs, and does not back feed onto the power rails (i.e, VBATP, VDD) or the digital I/O pins.

4.3.3.1.10 Loss of module ground

The definition of a loss of ground condition at the device level is, all pins of the IC see very low-impedance to battery. The nomenclature is suited to a test environment. In the application, a loss of ground condition results in all I/O pins floating to battery voltage, while all externally referenced I/O pins are at worst case pulled to ground. All applicable driver outputs and current sense inputs are protected against excessive leakage current due to loads are referenced to an external ground (i.e, high-side drivers).

4.3.3.1.11 Loss of module battery

The loss of battery condition at the parts level is, the power input pins of the IC see infinite impedance to the battery supply voltage (depending upon the application), but there is some undefined impedance looking from these pins to ground. All applicable driver outputs and current sense inputs are protected against excessive leakage current due to loads are referenced to an external battery connection (i.e., low-side drivers).

4.3.3.1.12 Stress tests (as applicable to each specific ASIC)

Each of the outputs must have a series of stress tests performed on 100% of the parts shipped. Experience has shown failure to incorporate these tests results in field and plant failures. The following is a list of the tests required and a brief description of each test. In general, for all of the following tests a significant number of parts must be tested to failure for the parameter in question so a statistically valid destruction level can be found. After this level is determined for each of the following parameters, a level for a production test is determined. This level must not be so high as to damage a normal part, but it must fail parts which do not fit in the normal process window.

Note: In all cases, the stress test must be performed to the level found during the previous part characterization and is not be tested to the specification level. Even if the part meets this specification, but the parameter in question does not fall within the proper statistical window, the part must be rejected. The only way a part can be considered good if it does not fall within the normal statistical window is if an exact root cause analysis is performed and a detailed explanation is given, along with an assessment of risk. Any stress test limits arrived at must at least meet the minimum requirements listed in this specification or the test has no validity.

4.3.3.1.13 Gate stress tests (as applicable to large power MOSFET drivers)

The gate stress test helps to test out random manufacturing defects within the gate oxide of the MOSFET. An initial gate-to-source leakage test is performed with as high a voltage as possible without causing significant leakage of the Gate-to-source zener clamp. The leakage is measured and recorded. Now a higher voltage (18 Volts, process and design related.) is applied to the gate of the MOSFET for a short period of time. The leakage is again tested at the lower voltage and recorded. If the leakage is above an absolute value, or if possible above a delta increase, the part is bad and must be rejected.

4.3.3.1.14 BV_{DSS} test (as applicable to power output drivers)

The purpose of this test is to ensure there is adequate headroom between the breakdown of the MOSFET output and the maximum clamp voltage. Provisions need to be made to be able to defeat the drain-to-gate clamp diode so that the BV_{DSS} value can be measured. It is also acceptable if the exact value is not found, but that a minimum guard band is tested to. A guard band of 5.0 to 10 V would be typical.

4.3.3.1.15 Elevated supply voltage stress

The purpose of this test is to find weak devices might fail if an unusual transient was seen. An elevated voltage of 40 Volts (Process dependent) is applied to the VBATP pin.

4.3.3.1.16 IDDQ stress test

The purpose of this test is to identify defects (shorted or leaky devices) which cannot be detected by conventional functional testing. IDDQ testing is required to be done separately for digital and analog circuit blocks. Test definition is per AEC Q100-007.

4.3.3.1.17 SCAN testing

The purpose of this test is to identify defects (shorted or leaky devices) which cannot be detected by conventional functional testing. IDDQ testing is required to be done separately for digital and analog circuit blocks. Test definition is per AEC Q100-007.

5 Typical applications

The 33909 System basis chip is a highly integrated system basis chip with switch to ground input detection inputs. The 33909 was designed to supply microprocessors and module power along with many of the most commonly needed functions in body modules.

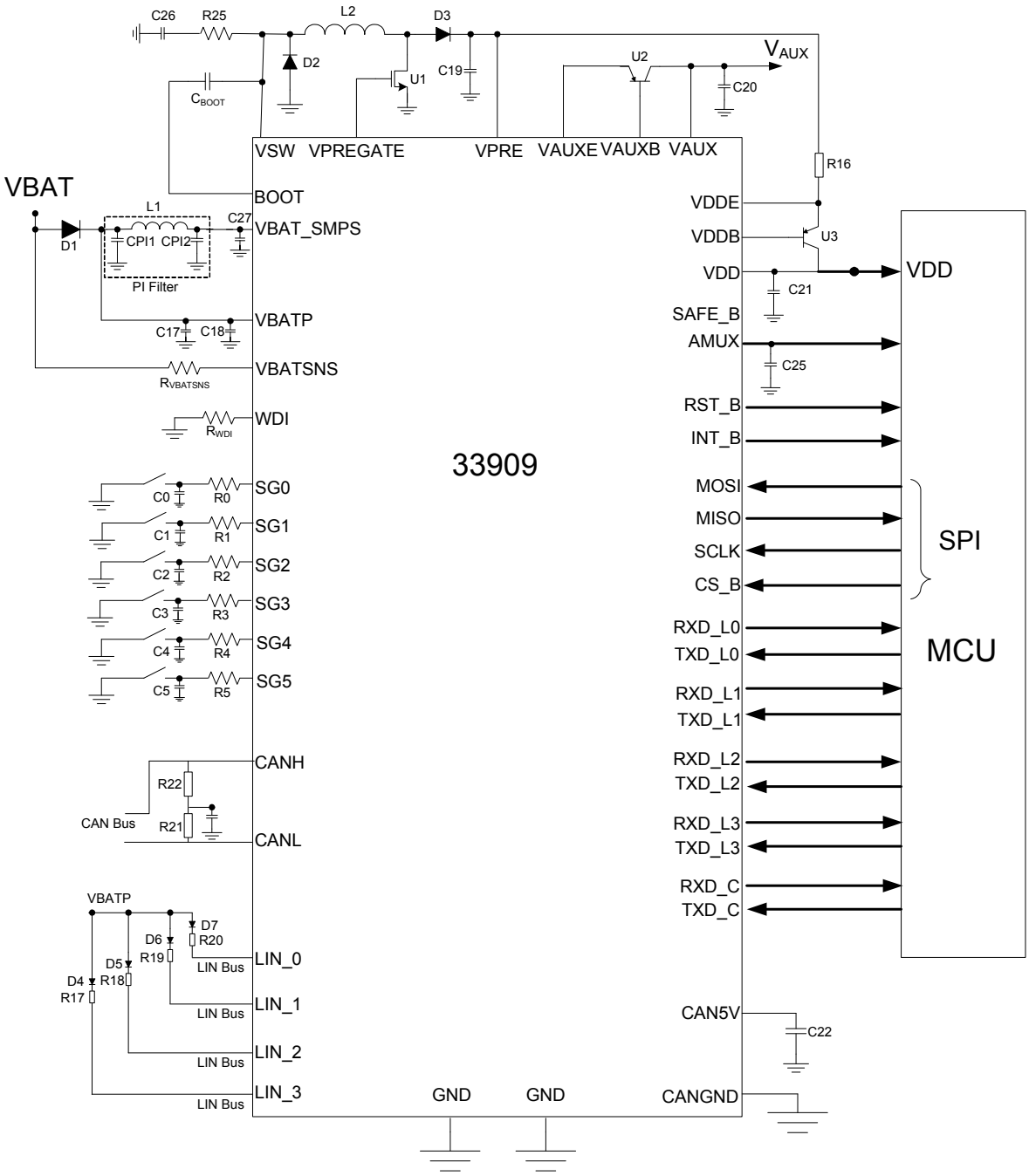


Figure 36. 33909AD typical application diagram

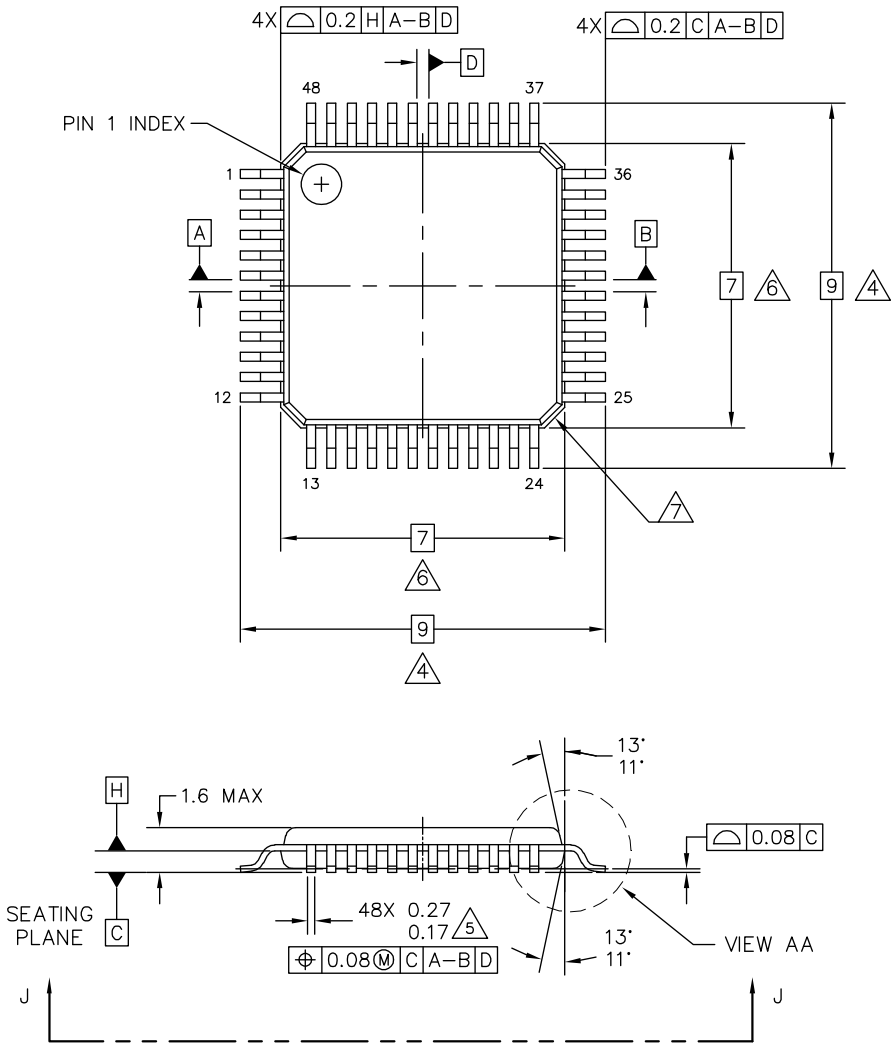
6 Packaging

6.1 Package dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.freescale.com and perform a keyword search for the drawing's document number.

Table 87.

Package	Suffix	Package outline drawing number
48-Pin LQFP	AD	98ASA00737D



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TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.15X4.15 EXPOSED PAD	DOCUMENT NO: 98ASA00737D	REV: A
	STANDARD: JEDEC MS-026 BBC	
	SOT1571-3	12 JAN 2016

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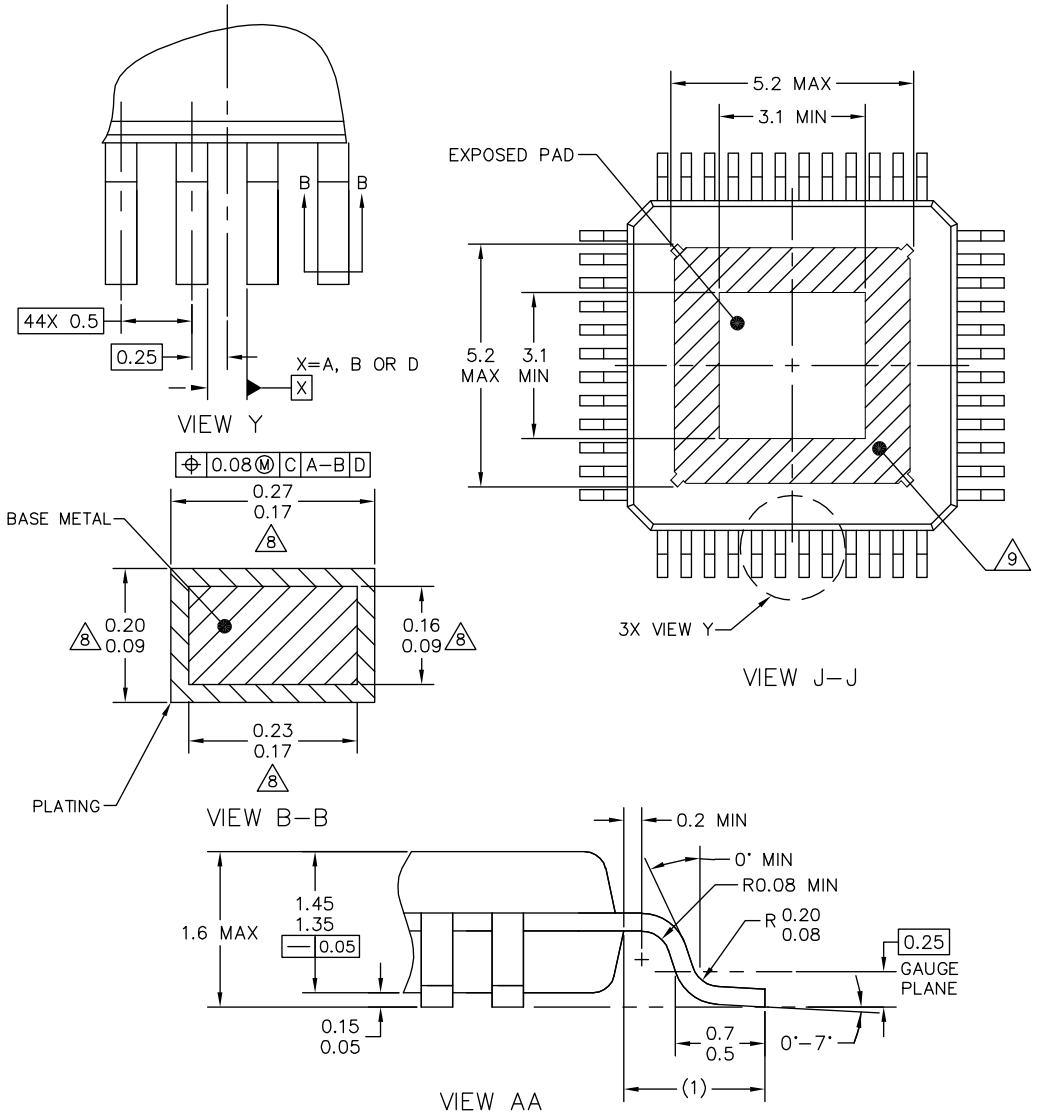

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TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.15X4.15 EXPOSED PAD	DOCUMENT NO: 98ASA00737D	REV: A
	STANDARD: JEDEC MS-026 BBC	
	SOT1571-3	12 JAN 2016

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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1MM AND 0.25MM FROM THE LEAD TIP.
9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

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TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.15X4.15 EXPOSED PAD	DOCUMENT NO: 98ASA00737D	REV: A
	STANDARD: JEDEC MS-026 BBC	
	SOT1571-3	12 JAN 2016

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7 Revision history

Revision	Date	Description of changes
1.0	10/2013	• Initial Release
2.0	1/2015	• Removed 64-pin version • Major update
3.0	3/2015	• Added DC/DC to device description. • Updated Electrical Characteristics tables for I_{LOAD_BUCK}, V_{DD} Undervoltage, SPI V_{IH}/V_{IL} specs. • Updated text to match current device. • Updated SPI tables to remove unused bits.
	4/2015	• Changed device status in Orderable parts from PC to MC.
4.0	7/2015	• Added SG Low-power Mode Timing Diagram • Corrected TXD pin timing in Table 9
	8/2016	• Added missing Interrupt table to Dynamic electrical characteristics • Updated to NXP document form and style

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Document Number: MC33909
Rev. 4.0
8/2016