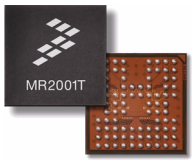
Document Number: MC33MR2001T
Rev. 6.0, 8/2016

76-77 GHz RF transmitter front-end for W-band radar applications

MR2001T

ADVANCED DRIVER ASSISTANCE SYSTEM



VK SUFFIX (PB-FREE)
98ASA00541D
6.0 X 6.0 X 0.95 RCPBGA

The MR2001 is an expandable three package solution for automotive radar modules. The chipset consists of a VCO (voltage controlled oscillator), a two-channel Tx transmitter, and a three-channel Rx receiver.

The MR2001T is a high performance, highly integrated, two-channel, transmitter (TX) ideally suited for automotive radar applications. In conjunction with the MR2001V, a four-channel voltage controlled oscillator, and the MR2001R, a three-channel receiver, it provides an expandable three package solution for automotive radar modules.

The chips are connected together via the LO signal around 38 GHz. The individual control of each chip is realized by SPI. The main controller and modulation master is a single microprocessor (MCU) with integrated high-speed analog to digital converters (ADC) and appropriate signal processing capability such as fast fourier transforms.

The front-end solution is specifically architected to be controlled by NXP's Qorivva MPC5775 MCU. Especially the baseband functionality (high-pass filters, variable gain amplifiers, anti-aliasing filters) on the receiver chips has been designed to work with the MPC5775 MCU.

Features

- Scalable to 4 TX channels and 12 RX channels
- Advanced packaging technology
- High performance supports fast modulation with simultaneous active channels
- Excellent spatial resolution and detection accuracy
- Local oscillator at 38 GHz to lower the distribution loss and reduce impact on antenna pattern
- Best phase noise < -75 dBc/Hz at 100 kHz offset
- Low power consumption of 2.5 W for the total transceiver
- Integrated system level calibration when combined with Qorivva MPC577xK MCU
- Compatible with all leading MCUs
- Optimized for the NXP Qorivva MPC577xK MCU
- Scalable approach to support SRR, MRR and LRR applications
- Reduced number of external components due to higher integration level
- Baseband integration on receiver suitable to work with the MPC577xK Qorivva MCU
- Bi-phase modulator on the transmitter chip

Applications

- Automotive proximity radar
- LRR, MRR and SRR
- ADAS
- Industrial surveillance and security systems

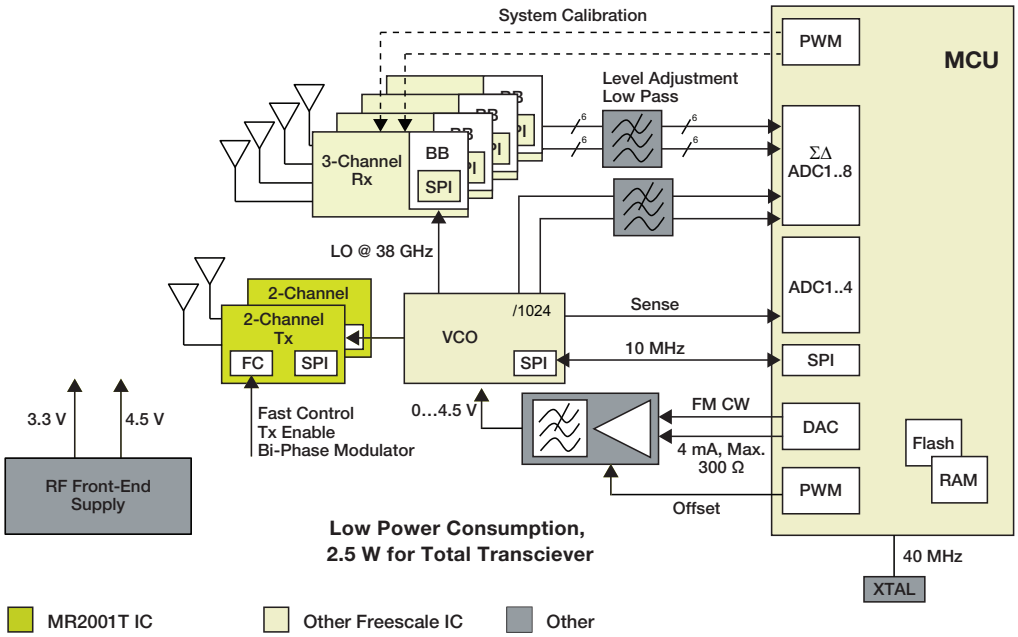


Figure 1. MR2001T simplified application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table of contents

1 Orderable parts

Table 1. Orderable part variations

Part number	Temperature (temp)	Package	Notes
MC33MR2001TVK	-40 °C to 125 °C	6.0 x 6.0 mm RCP (10 x 11 array) 0.5 mm pitch	(1) (2)

Notes

1. To order parts in Tape & Reel, add R2 to the suffix of the part number.
2. The device is packaged inside a 6.0 mm x 6.0 mm RCP with 10 x 11 solder balls. The pitch of the solder balls is 0.5 mm.

2 Internal block diagram

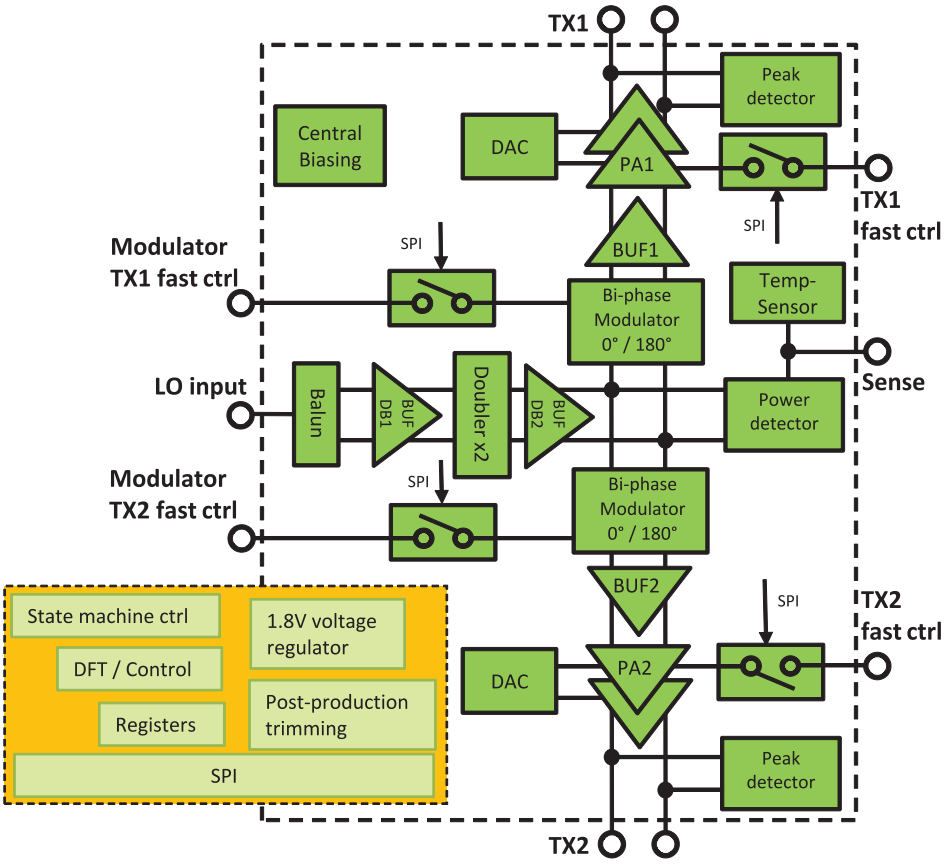


Figure 2. MR2001T two-channel transmitter block diagram

3 Pin connections

3.1 Pinout diagram

The layout and arrangement of the signal pads are shown in Figure 3.

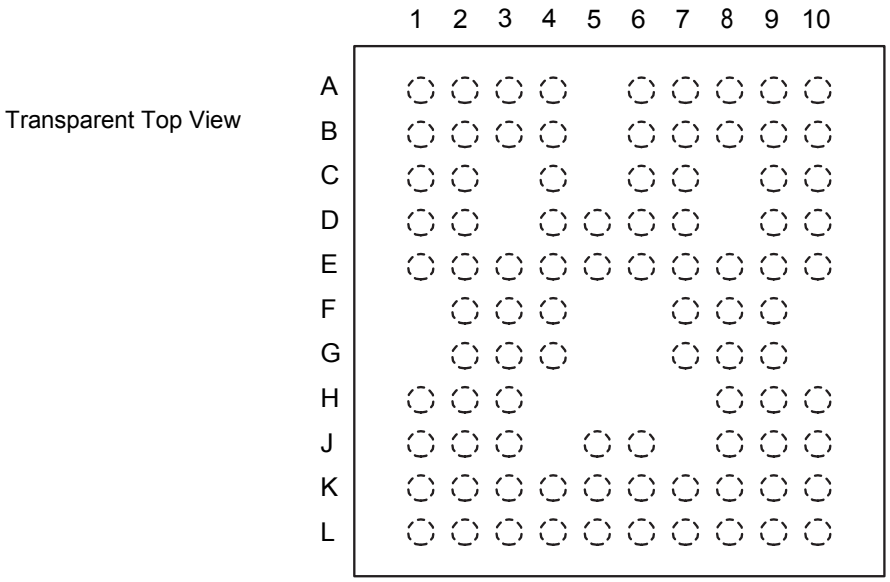


Figure 3. MR2001T pinout (ball) diagram

3.2 Pin definitions (ball)

A functional description of each pin for the MR2001T can be found in Table 2. Equivalent I/O schematics is found in Table 3

Table 2. MR2001T pin definitions

Ball location	Pin name	Pin function	Pin type	Level	Description
A1, A2, B2, C2	VCC2 (3)	3.3 V Power Supply	Power	3.3 V	
A3, B3, B7, B8, C7, D1, D2, D7, D9, D10, E7, F4, F7, G4, G7, J2, J3, J8, J9, K2, K3, K4, K7, K8, K9, L1, L10	GND (4)	DC Ground	Power	0.0 V	
A4, A6, B4, B6, C4, C6, D4, D6, E1, E2, E3, E4, E5, E6, E8, E9, E10, F3, F8, G3, G8, H1, H2, H3, H8, H9, H10	GND1 (4)	RF Ground	Power	0.0 V	
A7	TEST	Output to monitor internal bias nodes via ASCAN	Analog Output	0 to 3.3 V	
A8	ADR0	Chip key bit [0]	Digital Input	0 to 3.3 V	
A9, A10, B9, C9	VCC3 (3)	3.3 V Power Supply	Power	3.3 V	
B1	SENS	Sensor output (temperature and power peak detector)	Analog output	0 to 3.3 V	
B10	RN	Bandgap reference resistor (negative temperature slope)	Analog Input	0 to 3.3 V	See Table 6

Table 2. MR2001T pin definitions (continued)

Ball location	Pin name	Pin function	Pin type	Level	Description
C1	TREG	1.8 V Regulator Output	Analog Output	0 to 3.3 V	
C10	RP	Bandgap reference resistor (positive temperature slope)	Analog Input	0 to 3.3 V	See Table 6
D5	LO	38 GHz LO input	RF Input	0.0 V	
F2	TX1N	77 GHz differential output channel 1	RF Output	0 V	
F9	TX2N	77 GHz differential output channel 2	RF Output	0 V	
G2	TX1P	77 GHz differential output channel 1	RF Output	0 V	
G9	TX2P	77 GHz differential output channel 2	RF Output	0 V	
J1	PH1F	Bi-Phase modulator TX channel 1	Digital Input	0 to 3.3 V	
J10	PH2F	Bi-Phase modulator TX channel 2	Digital Input	0 to 3.3 V	
K1	TX1F	Fast on/off activation of TX channel 1	Digital Input	0 to 3.3 V	
K10	TX2F	Fast on/off activation of TX channel 2	Digital Input	0 to 3.3 V	
L2	SCLK	SPI serial clock	Digital Input	0 to 3.3 V	
L3	MISO	SPI MISO (master in, slave out)	Digital Output	0 to 3.3 V	
L4	MOSI	SPI MOSI (master out, slave in)	Digital Input	0 to 3.3 V	
L5, L6, K5, K6, J5, J6	VCC1 [3]	3.3 V Power Supply	Power	3.3 V	
L7	SCANB	Digital scan test	Digital Input	0 to 3.3 V	
L8	RSETB	Digital hard reset signal	Digital Input	0 to 3.3 V	
L9	SEB	SPI enable (chip enable)	Digital Input	0 to 3.3 V	

Notes

3. VCC1, VCC2, VCC3 are only connected via the on-chip metal layers. It is mandatory for each supply domain to be connected to the common power supply.
4. GND and GND1 are connected together in the package via the interconnection layer. GND1 is mandatory to be connected, to realize a suitable RF PCB to package transition.

3.3 Equivalent schematics

Table 3. Equivalent I/O schematics for pin descriptions

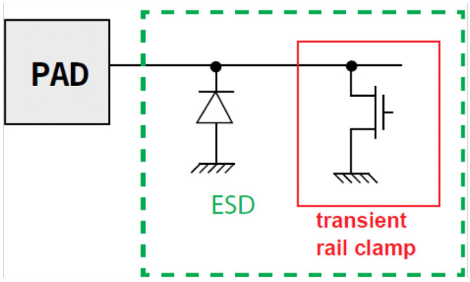
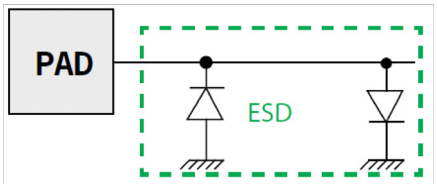
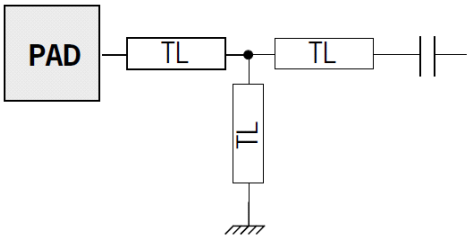
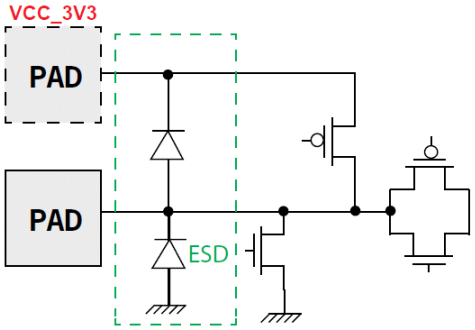
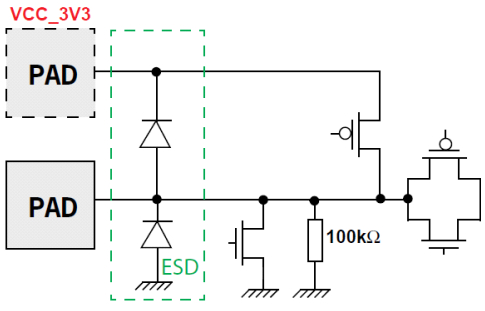
Ball location	Pin function	Equivalent I/O schematic
L5, L6, K5, K6, J5, J6 A1, A2, B2, C2 A9, A10, B9, C9	3.3V Power Supply	
A4, A6, B4, B6, C4, C6, D4, D6, E1, E2, E3, E4, E5, E6, E8, E9, E10, F3, F8, G3, G8, H1, H2, H3, H8, H9, H10	RF Ground	
A3, B3, B7, B8, C7, D1, D2, D7, D9, D10, E7, F4, F7, G4, G7, J2, J3, J8, J9, K2, K3, K4, K5, K7, K8, K9, L1, L10	DC Ground	
D5	38 GHz LO input	
G2, F2	77 GHz RF Output channel 1	
F9, G9	77 GHz RF Output channel 2	
L3	SPI MISO (master in, slave out)	
L4	SPI MOSI (master out, slave in)	
L2	SPI serial clock	

Table 3. Equivalent I/O schematics for pin descriptions

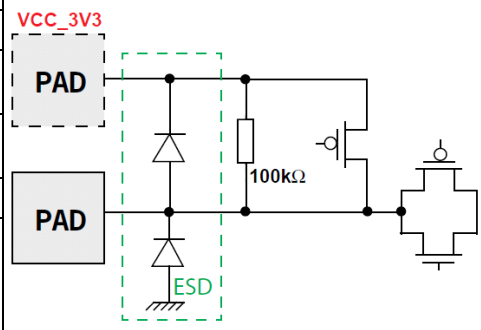
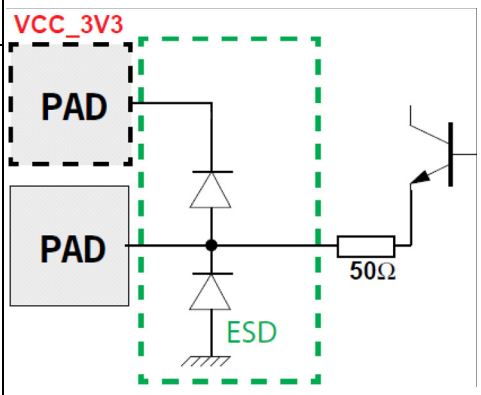
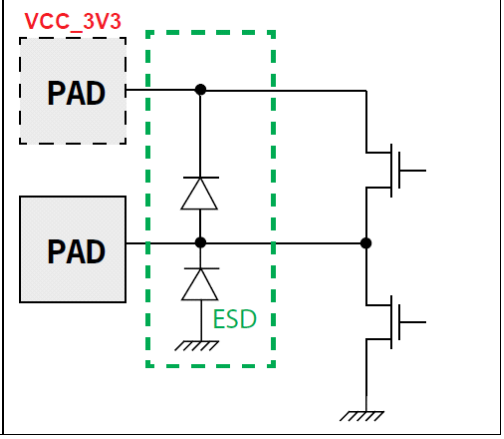
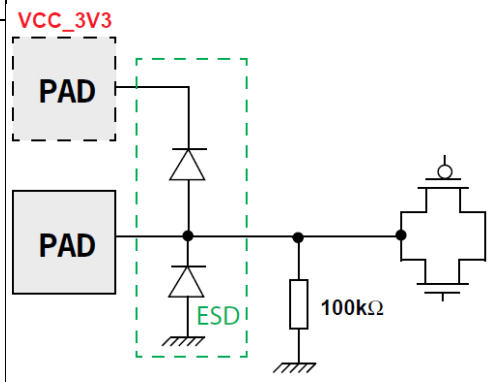
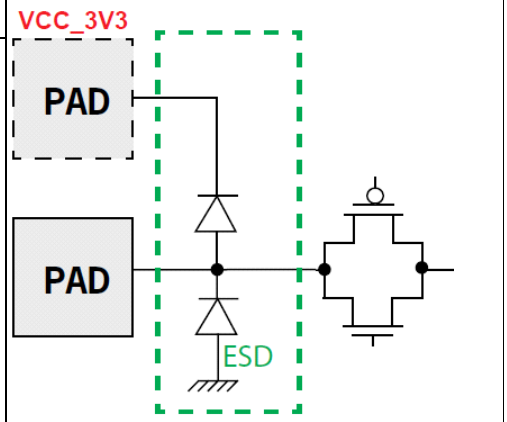
Ball location	Pin function	Equivalent I/O schematic
L8	Digital hard reset signal	
L9	SPI enable (chip enable)	
K1	Fast on/off activation of TX channel 1	
K10	Fast on/off activation of TX channel 2	
A8	Chip key bit [0]	
L7	Digital scan test	
B10	Bandgap reference resistor (negative temperature slope)	
C10	Bandgap reference resistor (positive temperature slope)	
C1	1.8 V Regulator Output	

Table 3. Equivalent I/O schematics for pin descriptions

Ball location	Pin function	Equivalent I/O schematic
J1	Bi-Phase Modulator TX channel 2	
J10	Bi-Phase Modulator TX channel 2	
B1	Sensor output (temperature and power peak detector)	
A7	Output to monitor internal bias nodes via ASCAN	

4 General product characteristics

4.1 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Min.	Max.	Unit	Notes
V_{STATIC_MAX}	Supply Voltage (static)	-0.30	3.63	V	
V_{DYN_MAX}	Supply Voltage (dynamic) • allowed < 10% of product total llifetime.	-0.30	4.00	V	
V_{DIG_MAX}	Digital Supply Voltage (static, dynamic)	-0.30	3.63	V	
V_{IN_MAX}	Voltage Applied to All Used I/O Pins	-0.30	3.63	V	
ESD					
ESD_HBM	ESD for Human Body Model (HBM) Digital I/O, Analog, RF	-2000	2000	V	
ESD_MM	ESD for Machine Model (MM)	-200	200	V	
R1	HBM Circuit Description I	–	±1500	W	
C	HBM Circuit Description II	–	±100	pF	
	ESD for human body model (HBM) digital I/O	-1000	1000	V	
	ESD HBM, RF I/O	-100	100	V	

4.2 General operating conditions

Table 5. General operation conditions

Temp = -40 °C to +125 °C, f_{OUT} = 76 to 77 GHz, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
dpack	Package Thickness (mounted condition)	–	950	1200	µm	
Temp	Ambient Package Temperature	-40	27	125	°C	
LU	Latch Up (LU) for DC and Bias Pads • Pulsed current injection method	-100	–	+100	mA	
Pitch	BGA Pitch	–	500	–	µm	
dchip	Chip Thickness	113	—	143	µm	
St_temp	Storage Temperature	-55	—	150	°C	
I_{PAD_MAX}	Pad withstanding	—	—	150	mA	
Number of pulses per pad						
	Number of positive pulses (HBM)	—	—	1		
	Number of negative Pulses (HBM)	—	—	1		
	Interval of Pulses	—	—	1	s	

5 General IC function description and application information

NXP provides a total system solution with next-generation embedded radar-based products that include the Qorivva MPC577xK MCU and 77 GHz packaged radar front-end chipset for both low- and high-end radar modules. This pairing delivers a complete embedded radar system for automotive designs. Our total solution advances automotive safety by enabling vehicles to sense potential crash situations. This radar solution provides long- and mid-range functionality, allowing automotive systems to monitor the environment around the vehicle to help prevent crashes.

A typical radar module consists of a transmit solution (Tx), VCO and three-channel receiver IC (Rx), along with an MCU. The chips are connected via the local oscillator signal, around 38 GHz. The individual control of each chip is implemented by a serial peripheral interface (SPI) bus. The main controller and modulation master is a single MCU with integrated high-speed analog-to-digital converters (ADCs) and appropriate signal processing capability, such as fast Fourier transforms (FFTs).

5.1 Features

- 76 GHz to 77 GHz TX output and 38 GHz to 38.5 GHz LO input
- Supply voltage 3.3 V ±5.0%
- Supply current typ. 260 mA
- Power dissipation typ. 0.86 W
- Power Control (6-bit)
- Tx Power typ. 2 x 10 dBm
- Bi-Phase Modulation
- SPI (slow, 10 MHz) and dedicated control (fast, 100 MHz)

5.2 Electrical characteristics

5.2.1 Transmitter Tx

Table 6. Interface levels

Temp = -40 °C to +125 °C, f_{OUT} = 76 to 77 GHz, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{CC}	Supply Voltage • Nominal supply ±5% variation	3.135	3.3	3.465	V	
I_{CC}	Supply Current • Measured at PACODE 35	–	260	350	mA	(5)
P_{DIS_1CH}	Power consumption (one Tx channel on)	–	0.86	1.21	W	
P_{DIS_2CH}	Power Consumption (two Tx channels on)	–	1.16	1.84	W	
Frequency and # of channels						
n_ch_LO	Number of LO Input Channels (at 38 GHz) • Single-ended input	–	–	1		
n_ch_TX	Number of TX Output Channels (at 76 GHz) • Differential configuration	–	–	2		
f_{LO}	LO Input Frequency Range	38	–	38.5	GHz	
f_{TX}	TX Output Frequency Range at 76 to 77 GHz	76	–	77	GHz	

Notes

5. All PACODE values are decimal unless otherwise noted.

Table 6. Interface levels

Temp = -40 °C to +125 °C, f_{OUT} = 76 to 77 GHz, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Thermal parameters						
R_{TH}	Thermal Resistance	–	15	22	K/W	
Return loss						
G_LO	LO-Input Return Loss (50 Ω at 38 to 38.5 GHz)	12	–	–	dB	
G_TX	TX-Output Return Loss (50 Ω) • Differential configuration, single-ended measurement not measured in production	8.0	–	–	dB	
Power						
PINM	TX Input Power	-6.0	–	–	dBm	
POUTM	TX Output Power • Differential configuration, PACODE 35, one channel active	2 x 7	2 x 10	–	dBm	
PDRIFT	Output Power Variation Over Full Temperature Range at Fixed Frequency • single-ended, PACODE 35, for each chip, const. V_{CC}, const. frequency	0.0	–	3.0	dB	
GC	Power Control Range • |Pout@PAcode=35 - Pout@PAcode=08|	10	–	–	dB	
dP_1dB	Power Control, Attenuation 1.0 dB • |P at PAcode = 35 at chip(i) - P at PAcode = 30 at chip(i)| at T = T(j) at V_{CC} = V_{CCN} at f = 76.5GHz	0	1.0	2.0	dB	
dP_2.5dB	Power Control, Attenuation 2.5 dB • |P at PAcode = 35 at chip(i) - P at PAcode = 25 at chip(i)| at T = T(j) at V_{CC} = V_{CCN} at f = 76.5GHz	0.7	2.5	4.0	dB	
dP_4dB	Power Control, Attenuation 4.0 dB • |P at PAcode = 35 at chip(i) - P at PAcode = 21 at chip(i)| at T = T(j) at V_{CC} = V_{CCN} at f = 76.5GHz	2.0	4.0	6.0	dB	
dP_6dB	Power Control, Attenuation 6.0 dB • |P at PAcode = 35 at chip(i) - P at PAcode = 17 at chip(i)| at T = T(j) at V_{CC} = V_{CCN} at f = 76.5GHz	4.0	6.0	8.5	dB	
dP_10dB	Power Control, Attenuation 10 dB • |P at PAcode = 35 at chip(i) - P at PAcode = 12 at chip(i)| at T = T(j) at V_{CC} = V_{CCN} at f = 76.5GHz	7.0	10	12.2	dB	
POUTM_V	Pout variation due to VCC • For VCC ±5% PACODE 35	-1.0	–	1.0	dB	
POUT_SLOPE	Output Power Frequency Slope • PACODE 35	–	–	0.2	dB/ 100MHz	
POUT_RIPPLE	Output Power Ripple • PACODE 35	-0.5	–	0.5	dB	
SW_FAST	PA Switch Attenuation (fast switch) • PACODE 35	22	–	–	dB	
PA_SW	PA Switch Attenuation (enable switch) • Controlled via SPI; one channel on, the other deactivated, for PACODE 35	30	–	–	dB	
PA_SUPP	PA Channel to Channel Suppression • Correlated, incl. bi-phase modulator	30	–	–	dB	
PA_S0	PA Attenuation at S0 • For 38 and 77 GHz signals	40	–	–	dB	
t_{RISE}	Rise Time • Rise time definition of the external signal to switch between PA and dummy PA	30	–	100	ns	

Table 6. Interface levels

Temp = -40 °C to +125 °C, f_{OUT} = 76 to 77 GHz, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Spurious						
SPUR_f_{LO}	Harmonic Spurious at f_{LO}, Leakage	–	–	-47	dBm	
SPUR_f_{TX}	Harmonic Spurious at f_{TX}, Leakage • All channels disabled, input stage on	–	–	-25	dBm	
NON_HARM	Nonharmonic Spurious • Referred to POUTM	–	–	-85	dBc	
Bi-phase modulator						
DPHASE	Phase Difference • Phase difference between two states. Measurement accuracy limited to ±10deg in production	170	180	190	degree	
DPOUTM	Power Variation Due to Phase Switching	-0.5	0	0.5	dB	
$t_{\_PHASE}$	Phase Shift Switching Time	0.0	–	30	ns	
Peak detector Tx output						
$V_{PPD\_AT\_PA\_CO\ DE=35}$	Peak Detector Output Voltage V_{PPD} at PAcode = 35	70	–	–	mV	
$V_{PPD\_AT\_PA\_CO\ DE=10}$	Peak Detector Output Voltage V_{PPD} at PAcode = 10	–	–	40	mV	
$t_{\_DET\_TX}$	Peak Detector Set-up Time	–	10	–	µs	
Peak detector Tx input						
$V_{\_DET\_TX\_RANGE}$	Peak Detector Output Voltage Range • Two sequential readings required	0.0	–	V_{CC}	V	
V_{DET_TX}	Peak Detector Threshold Voltage - two sequential readings required. V_Det_Tx > min. value guarantees functionality of Tx • at -40 ° • at 27 °C • at 125 °C	 400 350 250	 – – –	 – – –	mV	
Control functionality						
SPI	SPI Functionality • 10 MHz clock required	Yes				
DISABLE_CTRL_SLOW	Control Functionality, (TX slow enable, disable)	Via SPI				
DISABLE_CTRL_FAST	Control Functionality, Disable (Phase switch, TX fast enable) - each channel individually controlled	-0.3	–	20% *V_{CC3P3}	V	
ENABLE_CTRL_FAST	Control Functionality, Enable (Phase switch, TX fast enable) - each channel individually controlled	80% *V_{CC3P3}	–	V_{CC3P3} +0.3	V	
Amplitude noise						
AN_10kHz	Amplitude Noise at 10 kHz Offset at 77 GHz	–	–	-130	dBc/Hz	
AN_100kHz	Amplitude Noise at 100 kHz Offset at 77 GHz	–	–	-140	dBc/Hz	
AN_1MHz	Amplitude Noise at 1.0 MHz Offset at 77 GHz	–	–	-145	dBc/Hz	
Sensor output						
S_IMP_DIS	Sensor High Output Impedance (temp. sensor) • If corresponding sensor is disabled the output should show high-impedance	Yes				
R_{S_LOAD}	Sensor Load Resistance • To ground (temp, peak detector)	90	100	110	kΩ	
C_{S_LOAD}	Sensor Load Capacity • To ground (temp, peak detector)	–	–	30	pF	

Table 6. Interface levels

Temp = -40 °C to +125 °C, f_{OUT} = 76 to 77 GHz, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Temperature sensor						
T_SLOPE	Temperature Sensor Sensitivity • Two sequential readings required	–	0.55	–	mV/K	
T_SLOPE_VAR	Temperature Sensor Tolerance • Deviation from mean slope (T_slope) over temperature, max. precision at high temp. requested	-5.0	0.0	5.0	K	
T_RANGE	Temperature Sensor Output Voltage Range • Max. value achieved at 150 °C	0.4	–	3.0	V	
RP	External Resistor 1 • E96, ±1.0%, TK = ±100 ppm/K SMD, 0402 or smaller, 50 µA current	–	2.15	–	kΩ	
RN	External Resistor 1 • E96, ±1.0%, TK = ±100 ppm/K SMD, 0402 or smaller, 50 µA current	–	14.7	–	kΩ	

6 Functional block requirements and behaviors

NXP millimeter wave and radar products enable advanced, high-performance, multi-channel systems for use in automotive radar, automotive advanced driver assistance systems (ADAS), automotive safety systems and other high-performance communication infrastructure and industrial systems.

The MR2001 is a high-performance 77 GHz radar transceiver chipset scalable for multi-channel operation enabling a single radar platform with electronic beam steering and wide field of view to support long-range radar (LRR), mid-range radar (MRR) and short-range radar (SRR) applications. This new radar chipset consists of a VCO (MR2001VC), a two-channel Tx transmitter (MR2001TX) and a three-channel Rx receiver (MR2001RX). This 77 GHz radar transceiver chipset is compatible with all leading MCUs, including the Qorivva MPC577xK MCU.

The MR2001 radar chipset is designed to support fast modulation with simultaneous active channels, enabling excellent spatial resolution and detection accuracy across a wide field of view. It supports a large variety of chirps in open loop VCO radar system architectures and consumes minimal power. An integrated BB filter and VGA saves on the total bill of materials. The MR2001 radar chipset uses advanced packaging technology to ensure the highest performance and minimum signal interference on the printed circuit board (PCB).

6.1 SPI communication

6.1.1 SPI interface

SPI read and write are illustrated in Figure 4 and Figure 5. Figure 6 shows the SPI read/write operation to ASCAN.

a[5:0] is the SPI address to be written, as shown in the memory map.

d[7:2] is the data that is written to, or read from this address.Bit [1:0] are reserved.

rwb is the read write bit. Read is done when rwb is ‘1’, write is done when rwb is ‘0’.

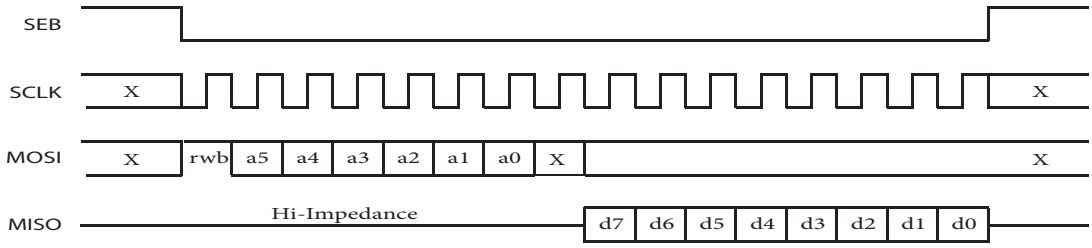


Figure 4. SPI read from internal registers

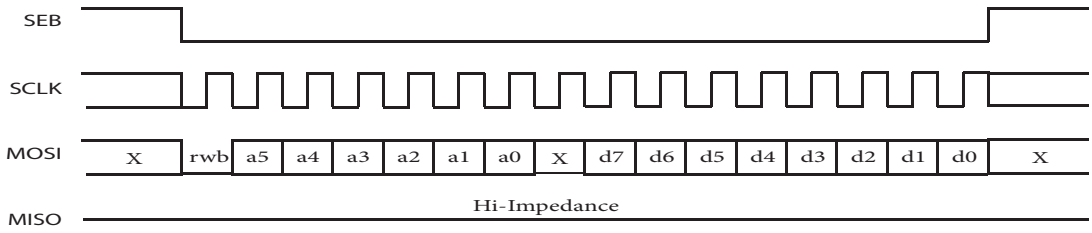


Figure 5. SPI write to internal registers

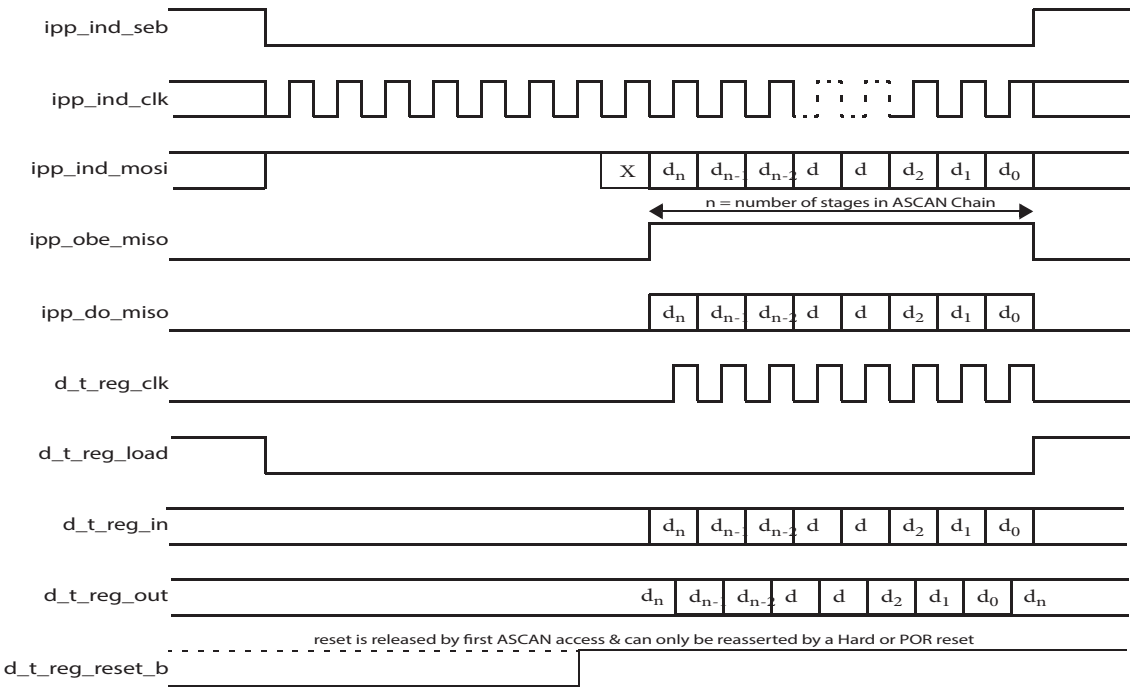


Figure 6. SPI write/read to ASCAN

6.1.2 Timing

SPI timings are described in Table 7 and illustrated in Figure 7. The SPI timing diagram, with the temperature and supply voltage conditions described in this document, and a maximum load capacitance, CL = 20 pF.

Table 7. SPI timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes [6]
t_{SCLK}	SCLK Cycle Time - SCLK pin	100	–	–	ns	(1)
t_{CSC}	SEB to SCLK Delay - SEB, SCLK pin	90	–	–	ns	(2)
t_{ASC}	After SCLK Delay - SCLK, SEB pin	2.5	–	–	ns	(3)
t_{SDC}	SCLK Duty Cycle - SCLK pin	0.9* (t_{SCLK}/2)	–	1.1* (t_{SCLK}/2)	ns	(4) [7]
t_{SUI}	Data Setup Time for Inputs - MOSI, SCLK pin	40	–	–	ns	(5)
t_{HI}	Data Hold Time for Inputs - MOSI, SCLK pin	40	–	–	ns	(6)
t_{SUO}	Data Valid (after SCLK edge) - MISO, SCLK pin	–	–	50	ns	(7)
t_{HO}	Data Hold Time for Outputs - MISO, SCLK pin	50	–	–	ns	(8)
H_{ZSEB}	High-impedance to SEB - MOSI, SEB pin	0.0	–	–	ns	(9)

Notes

6. The numbers under the Notes heading refer to the corresponding numbers in Figure 7.
7. For the maximum clock speed of 10 MHz

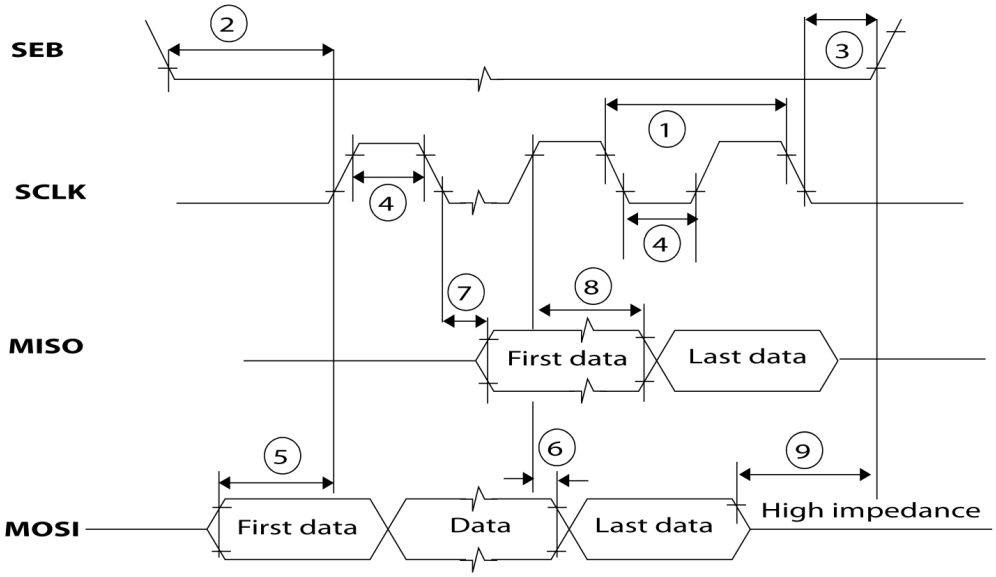


Figure 7. Typical SPI timing chart

6.2 External address solder balls ADR0 and ADR1

To minimize the effort on hardware wiring of signals, the MR2001T uses a combination of hardware and software coded addressing of each individual chip. Due to this procedure the hardware SEB (chip select) signal usage can be minimized.

If the software addressing is not longer sufficient (e.g. more than 4 RX chips) than a combination of SEB and software addressing is recommended.

Depending on the chip up to two external solder balls (address bit) are available (ADR0, ADR1). A connection to VCC represents a logical "1" and a connection to GND represents a logical "0", respectively. By default the logical "1" is already activated by a connection on the Die. If the corresponding pin is not connected to GND (used ball, not soldered ball), then this represents a logical "1".

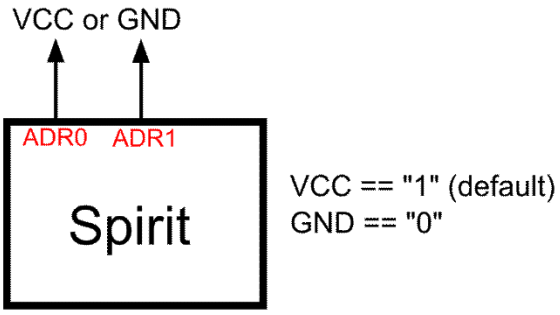


Figure 8. External connection of address pins ADR0 and ADR1 to define the identification key of the chip

6.3 System partitioning

Using the "software" addressing scheme of Spirit chips, any system up to max. one VCO, two transmitter (TX) and 4 receiver (RX) chips are supported.

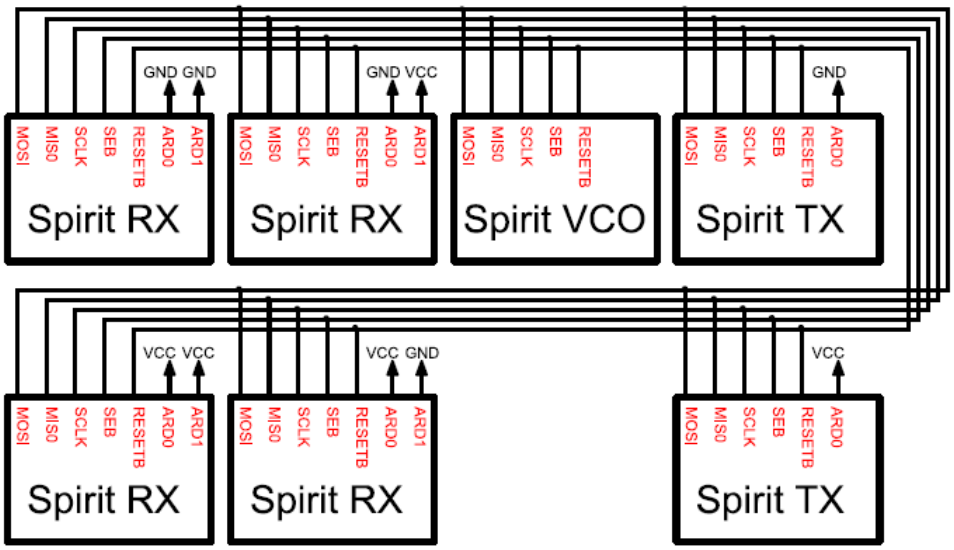


Figure 9. Chip partitioning using only software addressing of individual chips

If a system requires more than 4 Rx chips and/or 2 Tx chips and/or 1 VCO chip. Table 10 shows a proposed way to address the chips with a combination of the SEB (chip select) signal and "software" addressing.

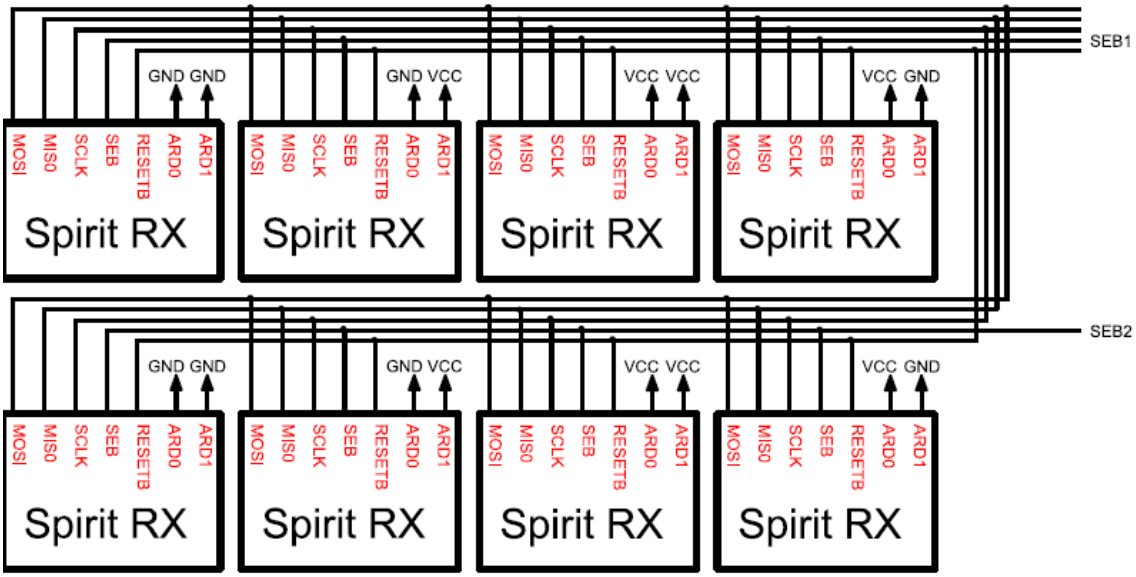


Figure 10. Typical Rx chip partitioning for more than four receivers. individual SEB signals for more than four Rx chips are required

6.4 Identification key

The Identification key is used to address the correct chip via SPI and it is composed of four up to six internal (on the chip hard wired) bits and up to two external bits defined by the voltage level applied to the ADR0 and ADR1 solder balls.

Table 8. Identification key

Chip	Internal bits	ADR0	ADR1	Chip key
RX1	1010	0	0	101000
RX2	1010	1	0	101001
RX3	1010	0	1	101010
RX4	1010	1	1	101011
TX1	01110	0	-	011100
TX2	01110	1	-	011101
VCO	101100	-	-	101100

If more individual chips must be addressed then the chip select (SEB) signal must be used.

6.5 Access protocol

6.5.1 Write access

Write access to the device is done as follows:

Table 9. Write access

SPI_WRITE(add0, RX1 key)	access to RX1 is activated
SPI_WRITE(add1, data1)	write data1 to the RX1 register at address 1
SPI_WRITE(add0, VCO key)	access to VCO is activated
SPI_WRITE(add3, data3)	write data3 to the VCO register at address 3

6.5.2 Read access

Read access to the device is done as follows:

Table 10. Read access

SPI_WRITE(add0, RX1 key)	access to RX1 is activated
SPI_READ(add1, data1)	read data1 to the RX1 register at address 1
SPI_WRITE(add0, VCO key)	access to VCO is activated
SPI_READ(add3, data3)	read data3 to the VCO register at address 3

7 Memory map

7.1 Generic memory map

All three MR2001T chips share the same general memory map which simplifies the programming and minimizes the error due to changes in varying register addresses.

Table 11. Generic memory map

Addr	Register	Type	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	KEY	R/W	0x00	KEY_5	KEY_4	KEY_3	KEY_2	KEY_1	KEY_0	RESERVED	RESERVED
0x01	FSM0	R/W	0x04	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S0_F	RESERVED	RESERVED
0x02	FSM1	R/W	0x00	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S1_F	RESERVED	RESERVED
0x03	EN	R/W	0x00	EN_5	EN_4	EN_3	EN_2	EN_1	EN_0	RESERVED	RESERVED
0x04	CTRL0	R/W	0x00	CTRL0_5	CTRL0_4	CTRL0_3	CTRL0_2	CTRL0_1	CTRL0_0	RESERVED	RESERVED
0x05	CTRL1	R/W	0x00	CTRL1_5	CTRL1_4	CTRL1_3	CTRL1_2	CTRL1_1	CTRL1_0	RESERVED	RESERVED
0x06	CTRL2	R/W	0x00	CTRL2_5	CTRL2_4	CTRL2_3	CTRL2_2	CTRL2_1	CTRL2_0	RESERVED	RESERVED
0x07	CTRL3	R/W	0x00	CTRL3_5	CTRL3_4	CTRL3_3	CTRL3_2	CTRL3_1	CTRL3_0	RESERVED	RESERVED
0x08	SNSOUT	R/W	0x00	SNSOUT_5	SNSOUT_4	SNSOUT_3	SNSOUT_2	SNSOUT_1	SNSOUT_0	RESERVED	RESERVED
0x09	TST	R/W	0x00	TST_5	TST_4	TST_3	TST_2	TST_1	TST_0	RESERVED	RESERVED

As an example, the register 0x03 describes the control enable/disable functionality. The level of control/enable can be different for each individual chip. Details can be found in the register map of each chip.

7.2 TX memory map

Table 12. TX memory map

Addr	Register	Type	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	KEY	R/W	0x00	KEY_5	KEY_4	KEY_3	KEY_2	KEY_1	KEY_0	RESERVED	RESERVED
0x01	FSM0	R/W	0x04	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S0_F	RESERVED	RESERVED
0x02	FSM1	R/W	0x00	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S1_F	RESERVED	RESERVED
0x03	EN	R/W	0x00	TX2	TX1	LOPD_EN	LOPD_SEL	TX_IN	NOT_USED	RESERVED	RESERVED
0x04	CTRL0	R/W	0x00	PAPWR6_ ch1	PAPWR5_ ch1	PAPWR4_ ch1	PAPWR3_ ch1	PAPWR2_ ch1	PAPWR1_ ch1	RESERVED	RESERVED
0x05	CTRL1	R/W	0x00	PAPWR6_ ch2	PAPWR5_ ch2	PAPWR4_ ch2	PAPWR3_ ch2	PAPWR2_ ch2	PAPWR1_ ch2	RESERVED	RESERVED
0x06	CTRL2	R/W	0x00	PA1_LW_N	PA2_LW_N	PA2_FS	PA2_FS_ SEL	PA1_FS	PA1_FS_SEL	RESERVED	RESERVED
0x07	CTRL3	R/W	0x00	NOT_USED	NOT_USED	BP2_PH	BP2_SEL	BP1_PH	BP1_SEL	RESERVED	RESERVED
0x08	SNSOUT	R/W	0x00	TMP_EN	TMP_SEL	PD1_EN	PD_SEL	PD2_EN	SNS_RSET	RESERVED	RESERVED
0x09	TST	R/W	0x00	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	TMP_TYP	RESERVED	RESERVED

7.2.1 0x00 TX key register

Address	0x00					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	KEY_5	KEY_4	KEY_3	KEY_2	KEY_1	KEY_0	RESERVED	RESERVED
Reset	0	0	0	0	0	0	N/A	N/A

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[7:2]	KEY	Device Identification Key

7.2.2 0x01 TX S0 state machine register (disabled)

Address	0x01					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S0_F	RESERVED	RESERVED
Reset	0	0	0	0	0	1	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	S0_F	State machine register. When S0_F is set to 1 the state machine is changing from S1 (enable) to S0 (disable)
[7:3]	NOT_USED	Unused bits

7.2.3 0x02 TX S1 state machine register (enabled)

Address	0x02					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S1_F	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	S1_F	State machine register. When S1_F is set to 1 the state machine is changing from S0 (disable) to S1 (enable)
[7:3]	NOT_USED	Unused bits

7.2.4 0x03 TX enable and LO input peak detector bits

Address	0x03					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	TX2	TX1	LOPD_TX_EN	LOPD_TX_SEL	TX_IN	NOT_USED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	NOT_USED	Unused bit
[3]	TX_IN	Enable Input buffer (LO Input)
[4]	LOPD_TX_SEL	LO Power detector output selection 0: diode row 1 1: diode row 2
[5]	LOPD_TX_EN	Activate LO power detector (After on-chip LO doubler)
[6]	TX1	Enable TX channel 1
[7]	TX2	Enable TX channel 2

The LO, Tx peak (power) detectors and temperature sensor cannot be enabled simultaneously. Only the activation of one sensor is supported.

Table 13. LO power detector sensor activation

SPI_WRITE(0x00, TX key)	access to TX is activated
SPI_WRITE(0x08, 04h)	Activate sensor reset SNS_RSET (discharge on-chip capacitance)
SPI_WRITE(0x08, 00h)	De-activate sensor reset SNS_RSET (discharge on-chip capacitance)
SPI_WRITE(0x03, 20h)	Enable LO peak detector (diode row 0)
<measure V1>	Measure voltage V1 at sense output
SPI_WRITE(0x08, 04h)	Activate sensor reset SNS_RSET (discharge on-chip capacitance)
SPI_WRITE(0x08, 00h)	De-activate sensor reset SNS_RSET (discharge on-chip capacitance)
SPI_WRITE(0x03, 30h)	Enable LO peak detector (diode row 1)
<measure V2>	Measure voltage V2 at sense output

|V1-V2| gives a voltage which is proportional to the LO power at the output of the on-chip doubler. SNS_RSET (sensor reset) activation discharges an on-chip capacitance to pull-down the output to GND. The activation maybe required between each change of the sensor branch to speed up communication. It is not allowed to have the sensor active while there is a reset operation.

7.2.5 0x04 TX power control - channel 1

Address	0x04					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	PAPWR6_ch1	PAPWR5_ch1	PAPWR4_ch1	PAPWR3_ch1	PAPWR2_ch1	PAPWR1_ch1	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[7:2]	PAPWRx_ch1	6 bit power control for TX channel 1 101101 == 0 dB attenuation (max. output power) 100111 == 1.0 dB attenuation 100001 == 2.5 dB attenuation 011000 == 4.0 dB attenuation 010101 == 6.0 dB attenuation 001111 == 10 dB attenuation 000000 == max. attenuation Other power control combinations are available resulting in different attenuation levels. See Figure 15 for plot of PACODE vs. output power.

7.2.6 0x05 TX power control - channel 2

Address	0x05					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	PAPWR6_ch2	PAPWR5_ch2	PAPWR4_ch2	PAPWR3_ch2	PAPWR2_ch2	PAPWR1_ch2	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[7:2]	PAPWRx_ch2	6 bit power control for TX channel 2 101101 == 0 dB attenuation (max. output power) 100111 == 1.0 dB attenuation 100001 == 2.5 dB attenuation 011000 == 4.0 dB attenuation 010101 == 6.0 dB attenuation 001111 == 10 dB attenuation 000000 == max. attenuation

7.2.7 0x06 TX modulator/channel control

Address	0x06					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	PA1_LW_N	PA2_LW_N	PA2_FS	PA2_FS_SEL	PA1_FS	PA1_FS_SEL	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	PA1_FS_SEL	Channel 1 fast switch select 0 : External signal control enabled 1 : Control via SPI enabled
[3]	PA1_FS	Channel 1 fast switch control 0 : Channel 1 de-activated 1 : Channel 1 activated
[4]	PA2_FS_SEL	Channel 2 fast switch select 0 : External signal control enabled 1 : Control via SPI enabled
[5]	PA2_FS	Channel 2 fast switch control 0 : Channel 1 de-activated 1 : Channel 1 activated
[6]	PA2_LW_N	Enable low noise setting of the reference current for channel 2
[7]	PA1_LW_N	Enable low noise setting of the reference current for channel 1

7.2.8 0x07 TX bi-phase modulator

Address	0x07					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	NOT_USED	NOT_USED	BP2_PH	BP2_SEL	BP1_PH	BP1_SEL	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	BP1_SEL	Channel 1 bi-phase modulator control 0 : External signal control enabled 1 : Control via SPI enabled
[3]	BP1_PH	Channel 1 modulator settings 0 : 0 ° 1 : 180 °
[4]	BP2_SEL	Channel 2 bi-phase modulator control 0 : External signal control enabled 1 : Control via SPI enabled
[5]	BP2_PH	Channel 2modulator settings 0 : 0 ° 1 : 180 °
[7:6]	NOT_USED	Unused bits

7.2.9 0x08 TX sensor register

Address	0x08					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	TMP_EN	TMP_SEL	PD1_EN	PD_SEL	PD2_EN	SNS_RSET	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	SNS_RSET	Sensor reset
[3]	PD2_EN	Enable peak detector channel 2
[4]	PD_SEL	Peak detector reference branch selection 0 : main signal branch activated 1 : reference branch activated
[5]	PD1_EN	Enable peak detector channel 1
[6]	TMP_SEL	Temperature sensor output selection 0: diode row 1 1: diode row 2
[7]	TMP_EN	Enable temperature sensor

Only the temperature sensor or the peak detector can be enabled at a time. The activation of both sensors must be avoided. The temperature sensor uses a reference (diode row = 0) and a signal branch (diode row = 1). Only the absolute difference between these two voltages gives a voltage with is proportional to temperature, and peak voltage level.

Table 14. Temperature sensor activation

SPI_WRITE(0x00, TX key)	access to TX is activated
SPI_WRITE(0x08, 04h)	Activate sensor reset SNS_RSET (discharge on-chip capacitance)
SPI_WRITE(0x08, 8Ch)	Enable temperature sensor at diode row 0
<measure V1>	Measure voltage V1 at sense output
SPI_WRITE(0x08, 04h)	Activate sensor reset SNS_RSET (discharge on-chip capacitance)
SPI_WRITE(0x08, C8h)	Enable temperature sensor at diode row 1
<measure V2>	Measure voltage V2 at sense output

|V1-V2| gives a voltage which is proportional to the on-chip temperature. SNS_RSET (sensor reset) activation discharges an on-chip capacitance to pull down the output to GND. The activation maybe required between each change of the sensor branch to speed up communication. Similar scheme must be used to read out values of the peak detector.

7.2.10 0x09 TX test register

Address	0x09					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	TMP_TYP	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	TMP_TYP	Activate temperature sensor 1: Temperature sensor activated
[7:3]	NOT_USED	Unused bits

7.3 State machine

The MR2001 chipset contains a digital controller which provides a simplied enable/disable control of the key analog blocks. The state maschine has only two states S0 and S1. S0 corresponds to the OFF (disabled) mode and S1 corresponds to the ON (enabled) mode, respectively.

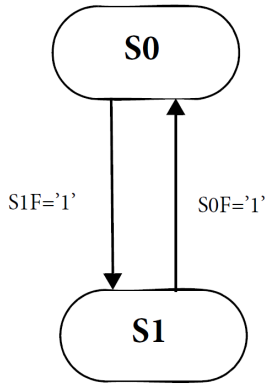


Figure 11. MR2001T state machine with the two states S0 and S1

The signals, block controlled by the state machine are listed in the following table.

Internal signal names	Chip	State machine S1 (register 0x02 set to 0x04)	State machine S0 (register 0x01 set to 0x04)
d_out10	Tx	PA1 buffer enabled	PA1 buffer disabled
d_out10	Tx	TX1 enabled	TX1 disabled
d_out12	Tx	PA2 buffer enabled	PA2 buffer disabled
d_out12	Tx	TX2 enabled	TX2 disabled
d_out20	Tx	Doubler and buffer after doubler enabled	Doubler and buffer after doubler disabled
d_out20	Tx	Phase selection 1 enabled	Phase selection 1 disabled
d_out20	Tx	Phase selection 2 enabled	Phase selection 2 disabled
d_out8	Tx	LO peak detector Tx input enabled	LO peak detector Tx input disabled
d_out6	Tx	LO peak detector Tx input/output selection	LO peak detector Tx output disabled

8 Typical applications

8.1 Introduction

The MR2001 is an expandable three package solution for automotive radar modules. The chipset consists of a VCO (voltage controlled oscillator), a two-channel Tx transmitter, and a three-channel Rx receiver.

The MR2001T is a high performance, highly integrated, two-channel, transmitter (TX) ideally suited for automotive radar applications. In conjunction with the MR2001V, a four-channel voltage controlled oscillator, and the MR2001R, a Three-channel transmitter, it provides an expandable three package solution for automotive radar modules.

The chips are connected together via the LO signal around 38 GHz. The individual control of each chip is realized by SPI. The main controller and modulation master is a single microprocessor (MCU) with integrated high-speed analog to digital converters (ADC) and appropriate signal processing capability such as fast fourier transforms.

The front-end solution is specifically architected to be controlled by NXP's Qorivva MPC5775 MCU. Especially the baseband functionality (high-pass filters, variable gain amplifiers, anti-aliasing filters) on the receiver chips has been designed to work with the MPC5775 MCU.

8.2 Typical application

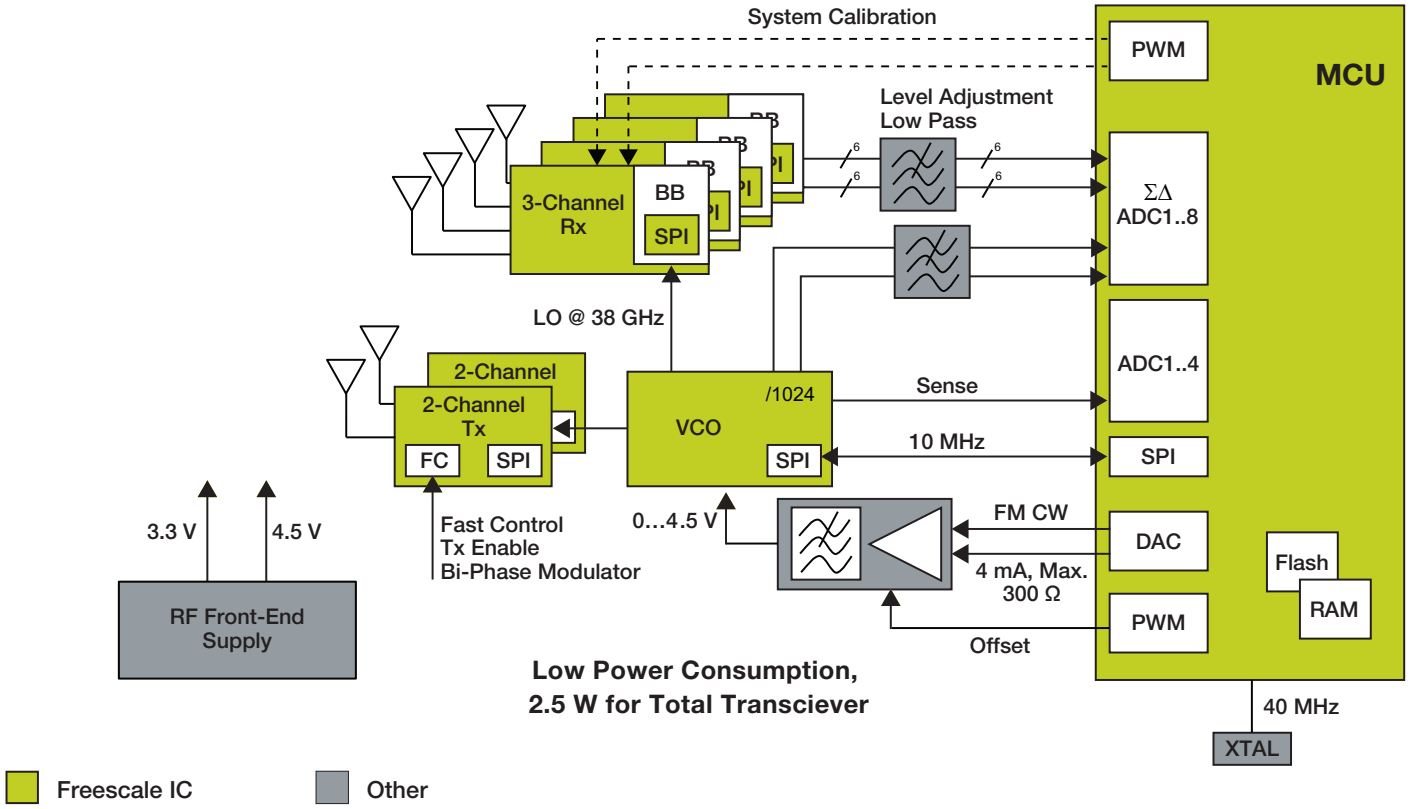


Figure 12. Typical application diagram

8.3 Measurement results

In the following chapters can find some typical measurement results which should help to guide a Radar system design.

8.3.1 Common results

8.3.1.1 Temperature sensor

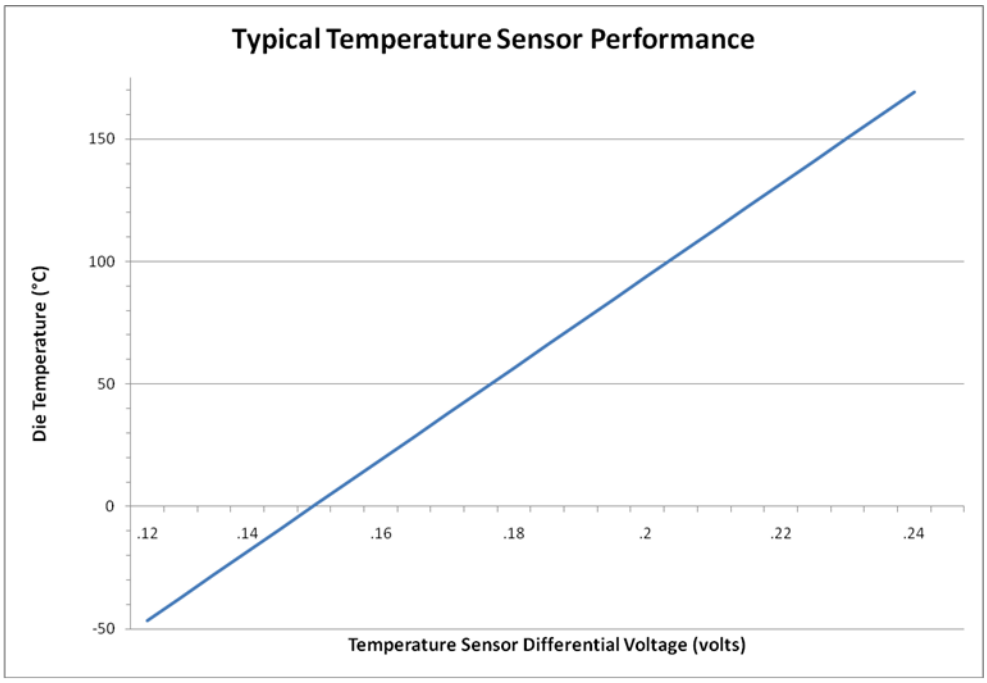


Figure 13. Typical slope of the temperature sensor of all 3 chips.
The derived equation can be used to calculate the on-chip temperature at the position of the sensor

The derived equation: Die Temp[°C]= ΔV_{TEMP} * 1875.0 - 280.94, with ΔV_{TEMP} the difference between the two sequential reading on the sense output, can be used to calculate the on-chip temperature. See 0x08 TX sensor register.

8.3.1.2 Thermal resistance

Figure 14 shows electrical measurements done on the 2-channel transmitter chip mounted on a multi-layer FR4/RO3003 PCB mounted on a mechanical carrier, which is attached to an on-wafer chuck. Due to the test set-up the extracted thermal resistance is combination of the PCB to heatsink thermal resitance and the resistance of the RCP itself. Taking this into account, the thermal resistance of the RCP package itself is in the range of approx. 15 K/W.

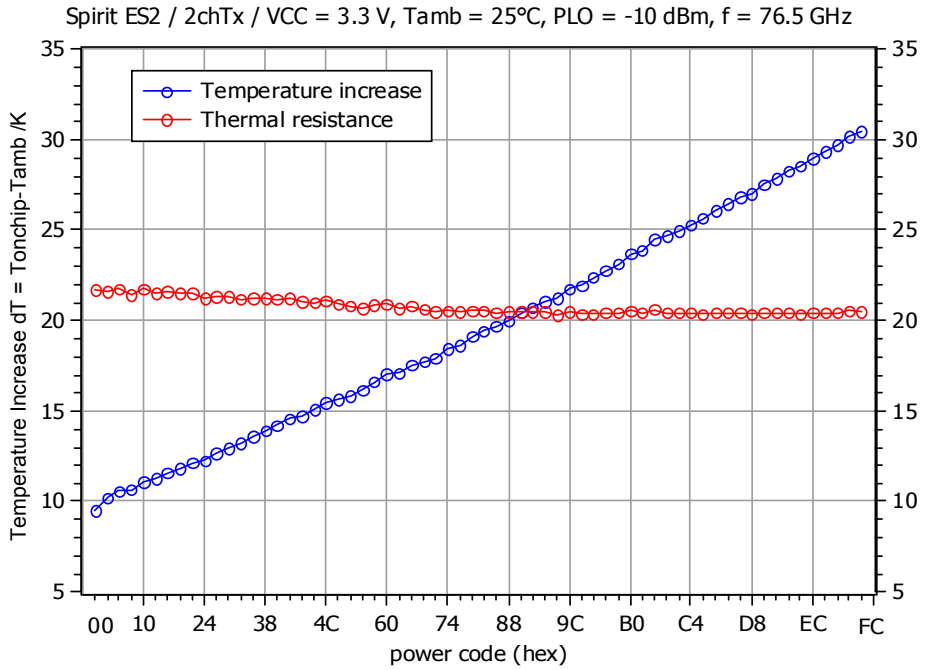


Figure 14. Electrical measurements of the thermal resistance of the RCP including PCB (FR4/RO3003), mechanical carrier and attachment to the on-wafer chuck.

8.3.2 2-channel transmitter Tx

8.3.2.1 Output power and current consumption vs. power code

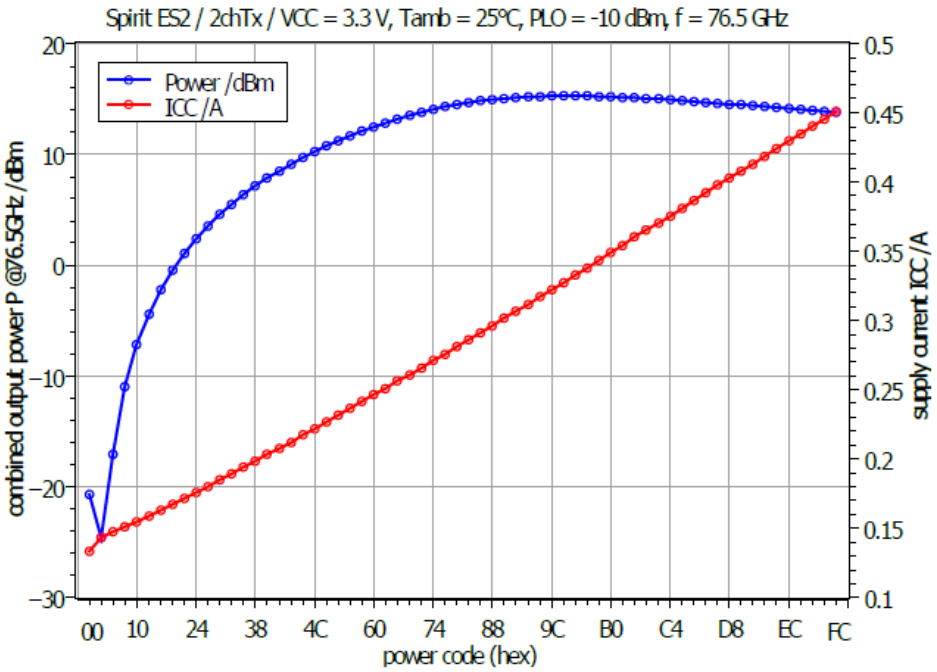


Figure 15. Typical transmitter output power and current consumption in dependence on the power code

8.3.2.2 Amplitude noise

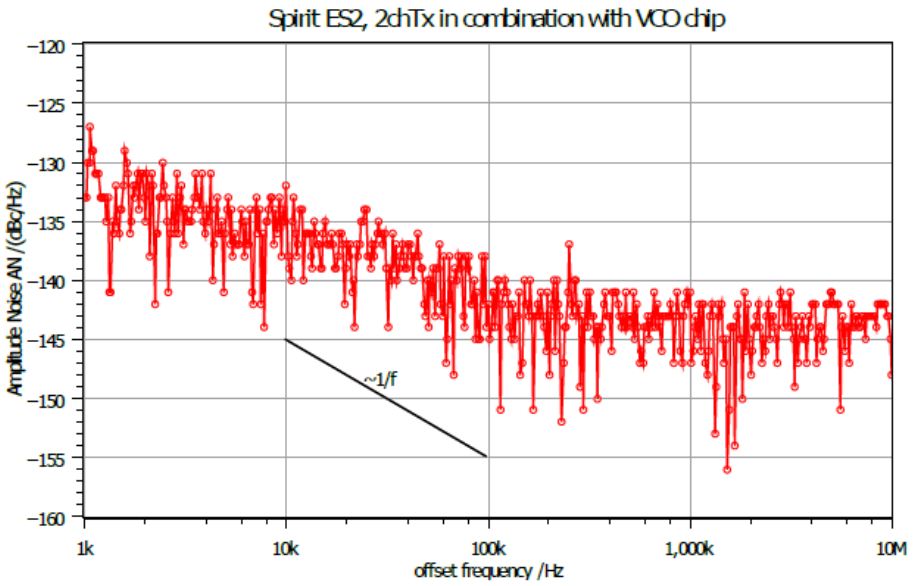


Figure 16. Amplitude noise in dependence on the offset frequency.

The input signal of the transmitter chip is provided by the MR2001 VCO to obtain a realistic measurement representative for a real system

8.3.2.3 Tx enable/disable switching time

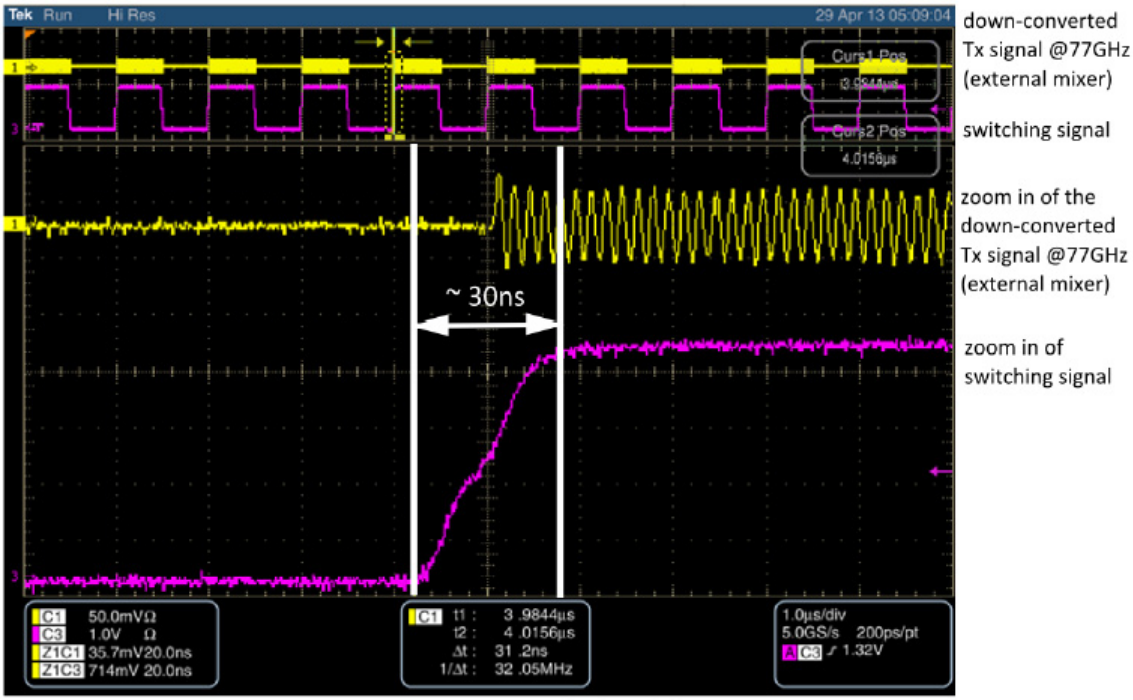


Figure 17. Switching of the Tx output signal at 77 GHz using the dedicated fast control signals

8.3.2.4 Tx bi-phase modulator switching time

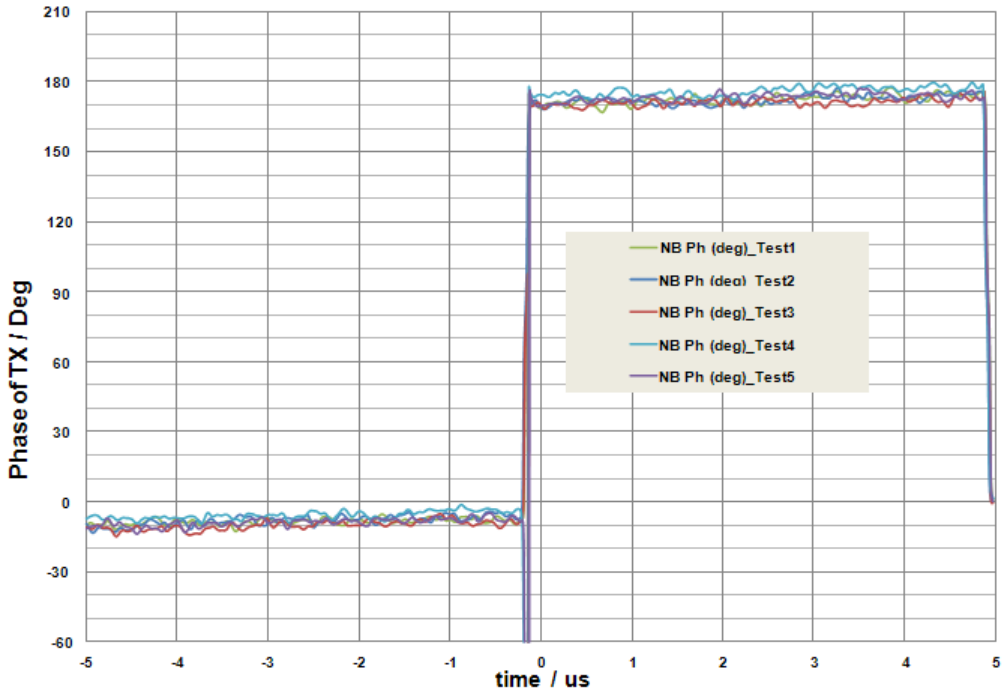


Figure 18. Bi-phase modulator switching time

Table 15. Bi-phase modulator accuracy

Phase modulator tests: max. phase devariation			
Board number	**Temp. = -40 °C**		
	dPH_VCCN	dPH_VCCN	dPH_VCCN
79	3.48979352	3.00369858	3.51679007
51	4.29737721	3.60926265	3.58143264
93	4.18885615	4.44115113	4.4606723
97	2.86346822	3.26335298	3.5343957
Board number	**Temp. = 25 °C**		
	dPH_VCCN	dPH_VCCN	dPH_VCCN
79	0.43866804	0.62846025	0.30926482
51	1.34644524	1.13013042	2.25861293
93	0.73030537	0.33466792	0.84329248
97	0.60180711	1.06668807	0.25107081
Board number	**Temp. = 125 °C**		
	dPH_VCCN	dPH_VCCN	dPH_VCCN
79	2.74077045	1.83352347	5.12341654
51	5.35388709	3.75971579	5.78778351
93	3.93749411	3.00785361	4.52890949
97	2.56610758	2.2756504	2.29983061

8.3.2.5 Tx channel-to-channel isolation

RCP part#83							
Temp	VCC	TX1 enabled, TX2 disabled			TX2 enabled, TX1 disabled		
		PTX1 (dBm)	PTX2 (dBm)	Suppression of Tx1 to Tx2	PTX2 (dBm)	PTX1 (dBm)	Suppression of Tx2 to Tx1
25°C	VCCL	13.3780307	-31.1264364	44.5044671	13.19151078	-29.7696062	42.96111698
	VCCN	13.62436295	-29.1294747	42.75383765	13.36192185	-32.0277503	45.38967215
	VCCH	14.0060923	-31.7361246	45.7422169	13.6991058	-33.2508626	46.9499684
-40°C	VCCL	14.4708857	-27.5821481	42.0530338	14.8101941	-28.8657611	43.6759552
	VCCN	14.7848906	-28.4344435	43.2193341	15.056465	-28.2465677	43.3030327
	VCCH	14.8796449	-28.1951796	43.0748245	15.2787074	-26.8268638	42.1055712
125°C	VCCL	8.76883911	-39.7677032	48.53654231	7.53366858	-34.78867	42.32233858
	VCCN	9.20925148	-34.2685666	43.47781808	8.29215917	-34.2835165	42.57567567
	VCCH	9.81352394	-32.9420409	42.75556484	9.33657767	-33.6667823	43.00335997
RCP part#51							
25°C	VCCL	13.07302771	-31.0045348	44.07756251	13.08234414	-33.2682381	46.35058224
	VCCN	13.29718998	-30.2506283	43.54781828	13.49046736	-32.6963831	46.18685046
	VCCH	13.72432399	-30.2506283	43.97495229	13.49046736	-31.8611661	45.35163346
-40°C	VCCL	15.2261243	-28.8169732	44.0430975	15.3214754	-28.9628814	44.2843568
	VCCN	15.3885285	-29.4959551	44.8844836	15.5578723	-29.412148	44.9700203
	VCCH	15.6991826	-26.613318	42.3125006	15.7764402	-29.5893435	45.3657837
125°C	VCCL	8.19685217	-34.0769752	42.27382737	8.17217095	-30.6462421	38.81841305
	VCCN	9.08600147	-31.5774057	40.66340717	8.81054076	-31.7414643	40.55200506
	VCCH	9.80552616	-32.5313485	42.33687466	9.44048906	-31.1813001	40.62178916
RCP part#43							
25°C	VCCL	13.39617028	-31.7524247	45.14859498	13.37088892	-28.7878954	42.15878432
	VCCN	13.64543027	-30.2277605	43.87319077	13.42866905	-28.6826972	42.11136625
	VCCH	14.0915816	-29.811769	43.9033506	13.86252472	-28.152426	42.01495072
-40°C	VCCL	14.3357337	-26.9784695	41.3142032	14.5279138	-26.6057624	41.1336762
	VCCN	14.1015644	-27.9931902	42.0947546	14.7878311	-26.109081	40.8969121
	VCCH	14.2521621	-26.1792575	40.4314196	14.9028976	-28.6983833	43.6012809
125°C	VCCL	7.1184971	-42.2858229	49.40432	6.84635617	-32.4024482	39.24880437
	VCCN	8.35771842	-36.7117331	45.06945152	7.86623494	-34.1218315	41.98806644
	VCCH	9.29117076	-35.4860466	44.77721736	8.86259113	-33.4061688	42.26875993
			min. suppression	40.4314196		min. suppression	38.81841305

Figure 19. Channel-to-channel isolation for all conditions > 39 dB

Table 16. TX leakage at Lo frequency

VCC	Temp		
	25 °C	-40 °C	125 °C
V_{CCL}	-57.5	-57.5	-58
V_{CCN}	-57.5	-57.4	-58
V_{CCH}	-57.7	-57.2	-57.7

f_{IN} = 38.25 GHz, V_{CCL} = 3.3 V -5%, V_{CCN} = 3.3 V, V_{CCH} = 3.3 V +5%. Values in the table are in dBm and measured after combination of the differential signals using the balun described in Figure 26.

8.4 External components

8.4.1 Biasing

8.4.1.1 External blocking capacitors

To achieve defined specifications, the supply to the chip must be regarding spurious and noise level as good as possible. For this reason, typically external filters are added between the sensor supply domain and the on-chip supply domains. Figure 20 shows such a typical supply scheme. The blocking caps should be placed as close as possible to the package. This is dependent on application board material and manufacturer.

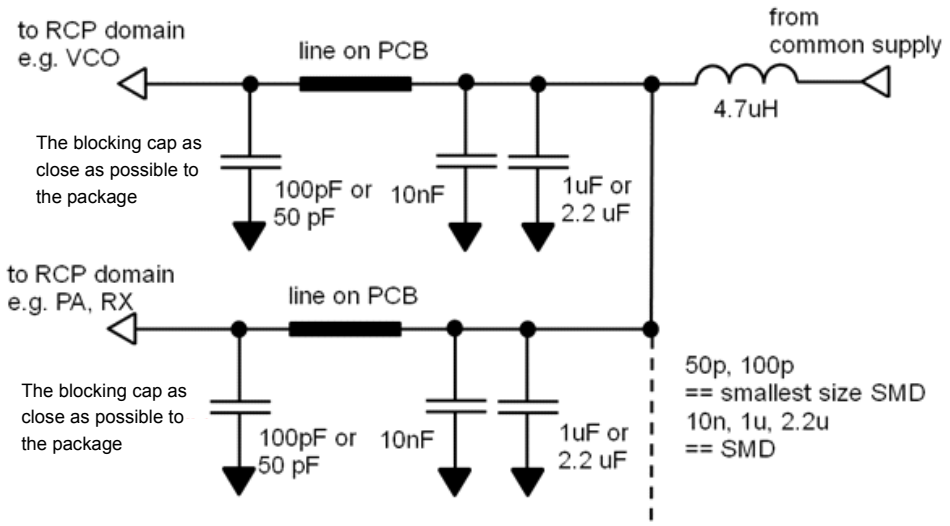


Figure 20. Typical arrangement and values of blocking capacitors to supply the chips

8.4.1.2 External biasing resistors

To operate the MR2001 chip-set, it is mandatory to connect each chip to two external resistors RN, RP, respectively. Without these two resistors the chips cannot be functional.

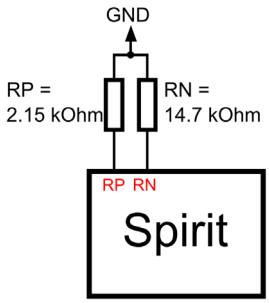


Figure 21. Required external resistors RN and RP for each individual MR2001Chip

External resistors	Value	Recommendation
RP	2.15 kΩ	E96, ±1.0%, TK = ±100 ppm/K, SMD, 0402 or smaller, 50 µA current
RN	14.7 kΩ	E96, ±1.0%, TK = ±100 ppm/K, SMD, 0402 or smaller, 50 µA current

The two external resistors are part of the on-chip bandgap references. Due to the lower tolerances of the external resistors (±1.0% compared to on-chip ±10%) the supply current variation from package to package is drastically reduced.

8.4.2 Sense outputs

8.4.2.1 Tri-state sense outputs

The MR2001 chip-set provides tri-state sensing output signal which allows simplified wiring and signaling. All sense signals can be connected together to share the same hardwired signal line.

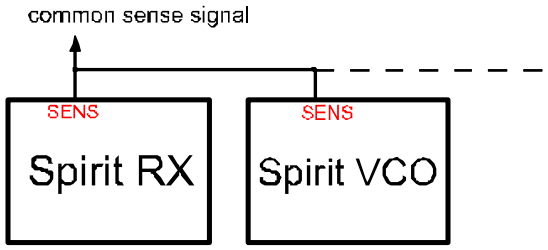


Figure 22. Block diagram and the relevant pin signals

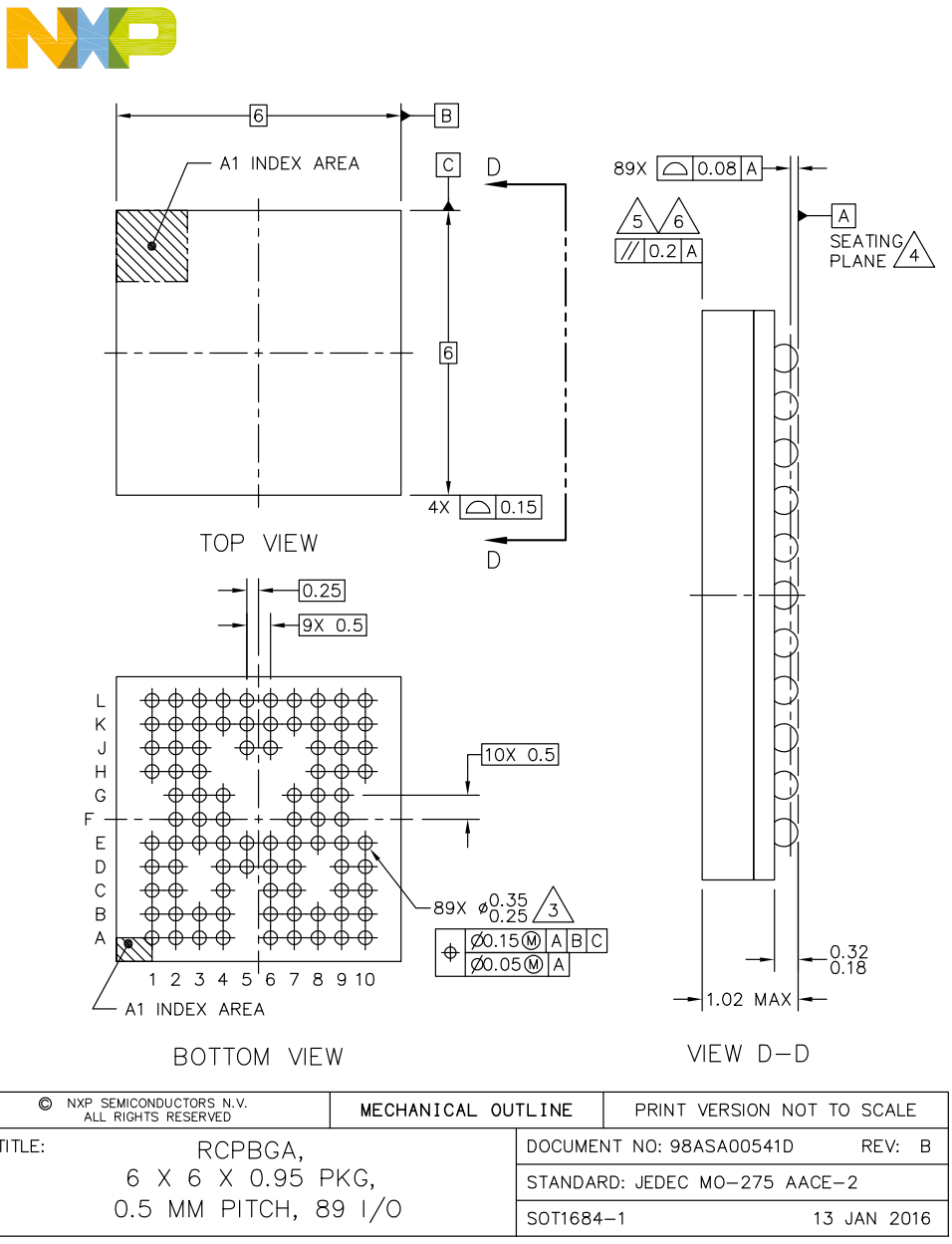
9 Packaging

9.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 17. Packaging information

Package	Suffix	Package outline drawing number
6.0 x 6.0 mm RCP, (10 x 11 array) 0.5 mm pitch	VK	98ASA00541D



MR2001T

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. SCORING OR GROOVES ON TOP SURFACE OF PACKAGE IS NOT PERMITTED.
7. NO VOIDS IN ENCAPSULATION PERMITTED.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: RCPBGA, 6 X 6 X 0.95 PKG, 0.5 MM PITCH, 89 I/O	DOCUMENT NO: 98ASA00541D REV: B
	STANDARD: JEDEC MO–275 AACE–2
	SOT1684–1 13 JAN 2016

9.2 PCB and RCP environment

9.2.1 NXP test board

9.2.1.1 RO3003 on FR4

For the NXP test boards a multi-layer PCB composed of 127 µm thick Rogers 3003 on top of standard FR4 core is used. The manufacturer for these boards is Elekonta/Marek (http://www.elekonta.de/).

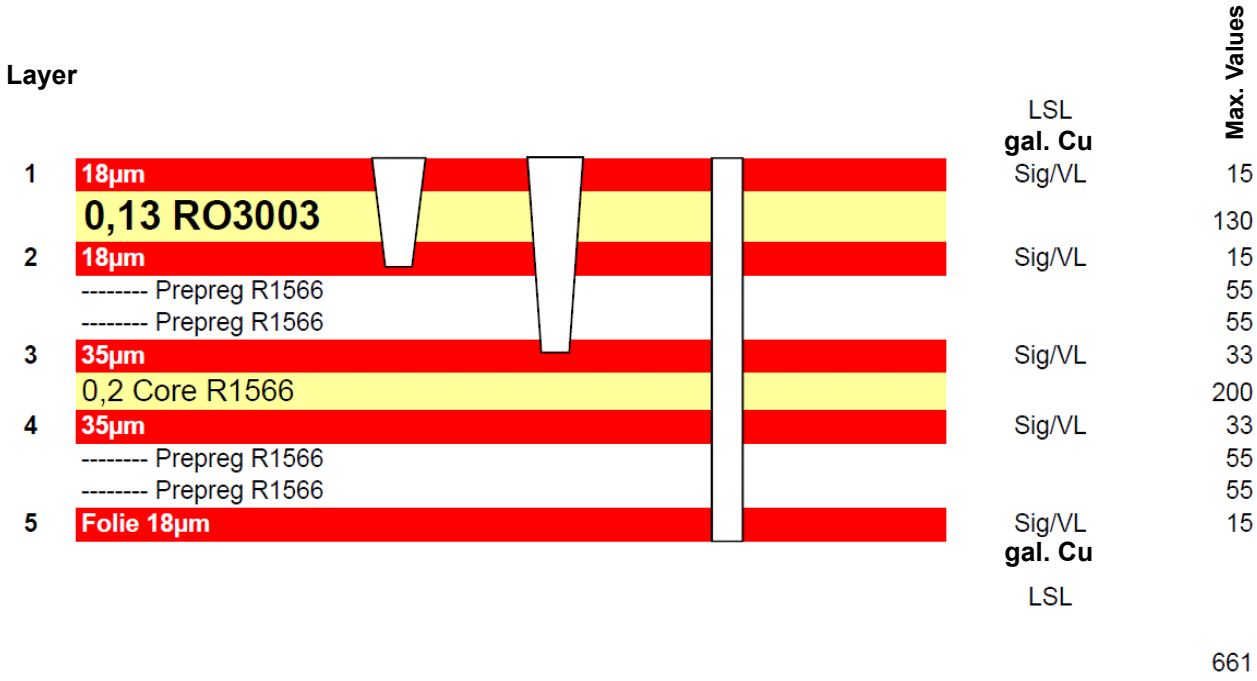
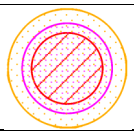
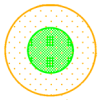


Figure 23. RO3003 on top of a FR4 core

9.2.1.2 Layout rules

The Figure 24 shows the solder ball arrangement including thermal and rf vias of typical PCB. Solder ball locations are shown in magenta with a label in blue, thermal via's have a wider diameter and are also shown in magenta without any blue label, important gnd via's to achieve rf perfromance are shown in green. Thermal vias are located in the area where no solder ball is available, so that they can occupay the full area of a solder ball.

Type	Shape	Geometry
solder ball		~∅ 300 um
thermal via		> ∅ 200 um, thru PCB (non filled, or filled)
gnd via for rf performance		∅ 200 um (non filled, or filled)

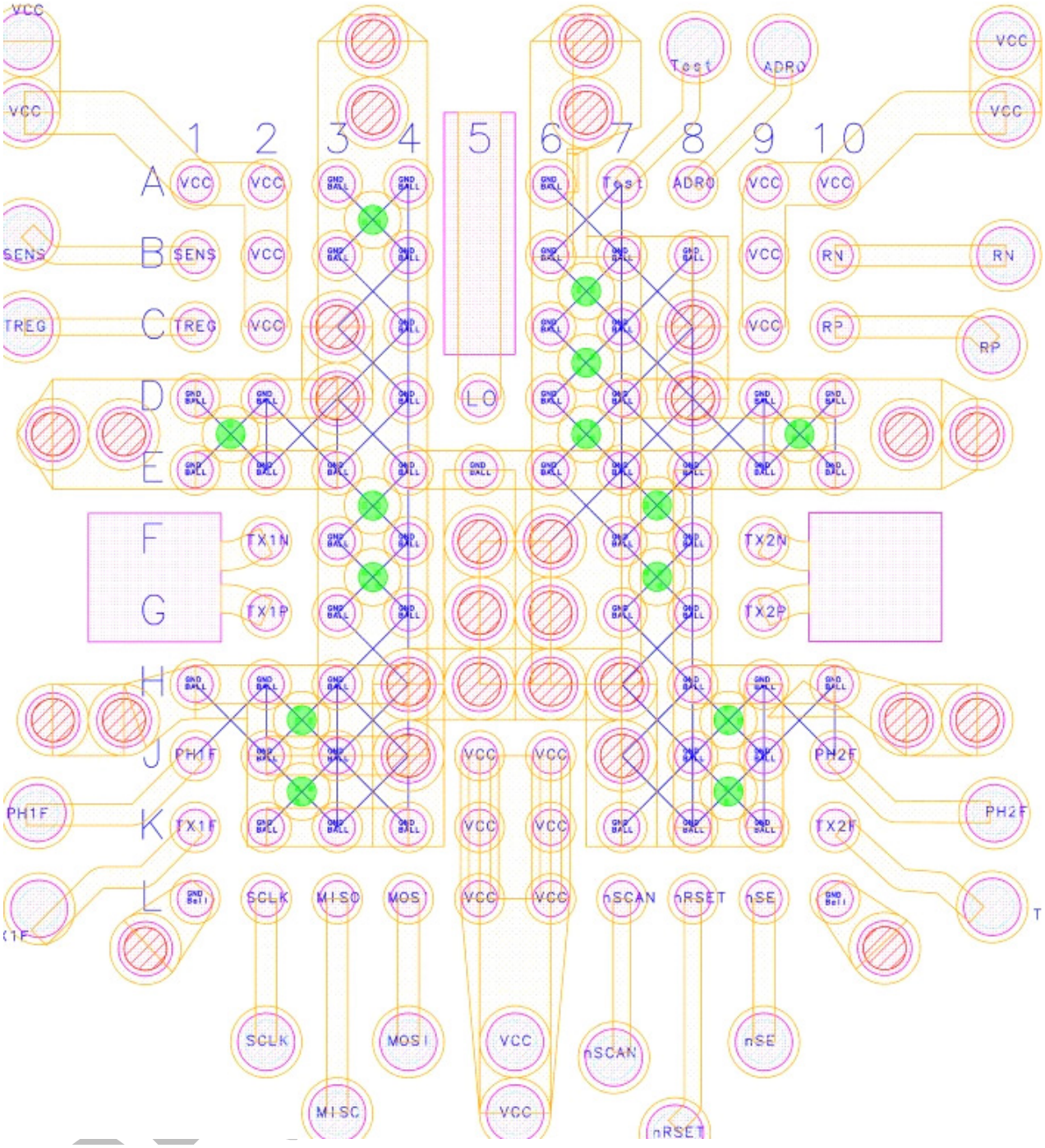


Figure 24. Top view of the Tx solder ball arrangement (magenta with blue label) including gnd vias (green, 200 um) to obtain rf-performance and thermal vias (> 200 um) to guarantee temperature range

The layout of the RCPs and the solder ball arrangement have been already done to allow space for thermal vias in the area where no solder balls are placed. It is recommended that this area is fully filled with thermal vias to lower the thermal resisstance.

9.2.1.3 Single-ended RF connection at 38 GHz (PCB microstip lines)

For 38 GHz input and output signals no special matching structure on the PCB is required. A standard 50 Ω microstrip transmission line directly connected to the solder ball is fully sufficient.

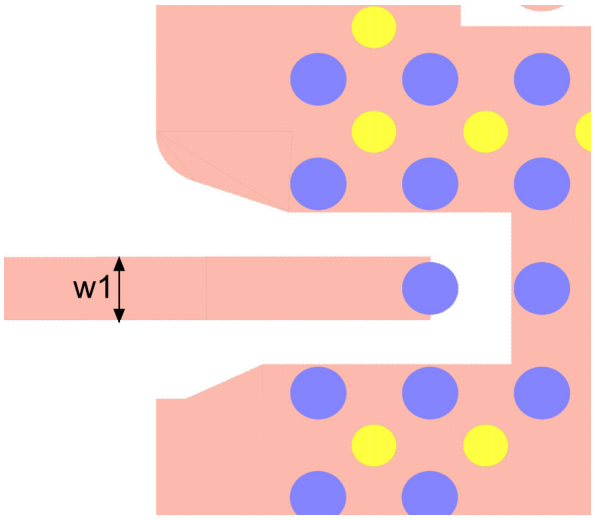


Figure 25. Example for the RF connection of a 38 GHz input and output signal. Shown in the picture is the LO input of the receiver chip

9.2.1.4 Differential RF connection at 77 GHz (PCB microstip lines)

To combine the differential Tx signals on the PCB, a simplified balun can be used. The layout of such structure and the geometrical details is shown in Figure 26. The port definitions for the EM simulations are also displayed.

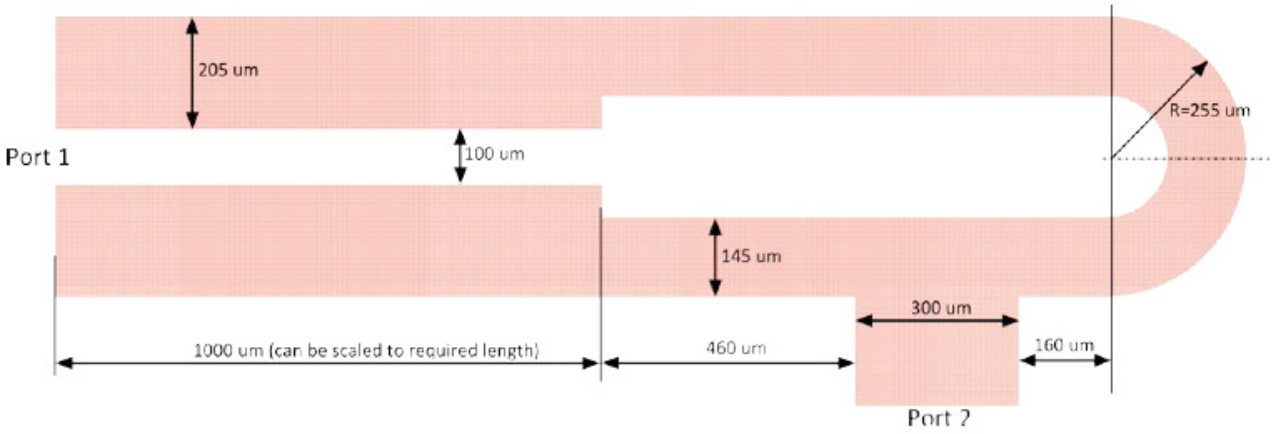


Figure 26. Layout and dimensions of a microstrip balun for the frequency range from 76 to 81 GHz

Figure 16 shows simulation results (Momentum ADS 2009U1) based on typical substrate parameters for RO3003 at 77 GHz (r = 3.13, tand = 0.01, substrate thickness t = 127 µm). The attenuation in the desired frequency range is approx. 0.6 dB and the input and output matching is always better as 15 dB.

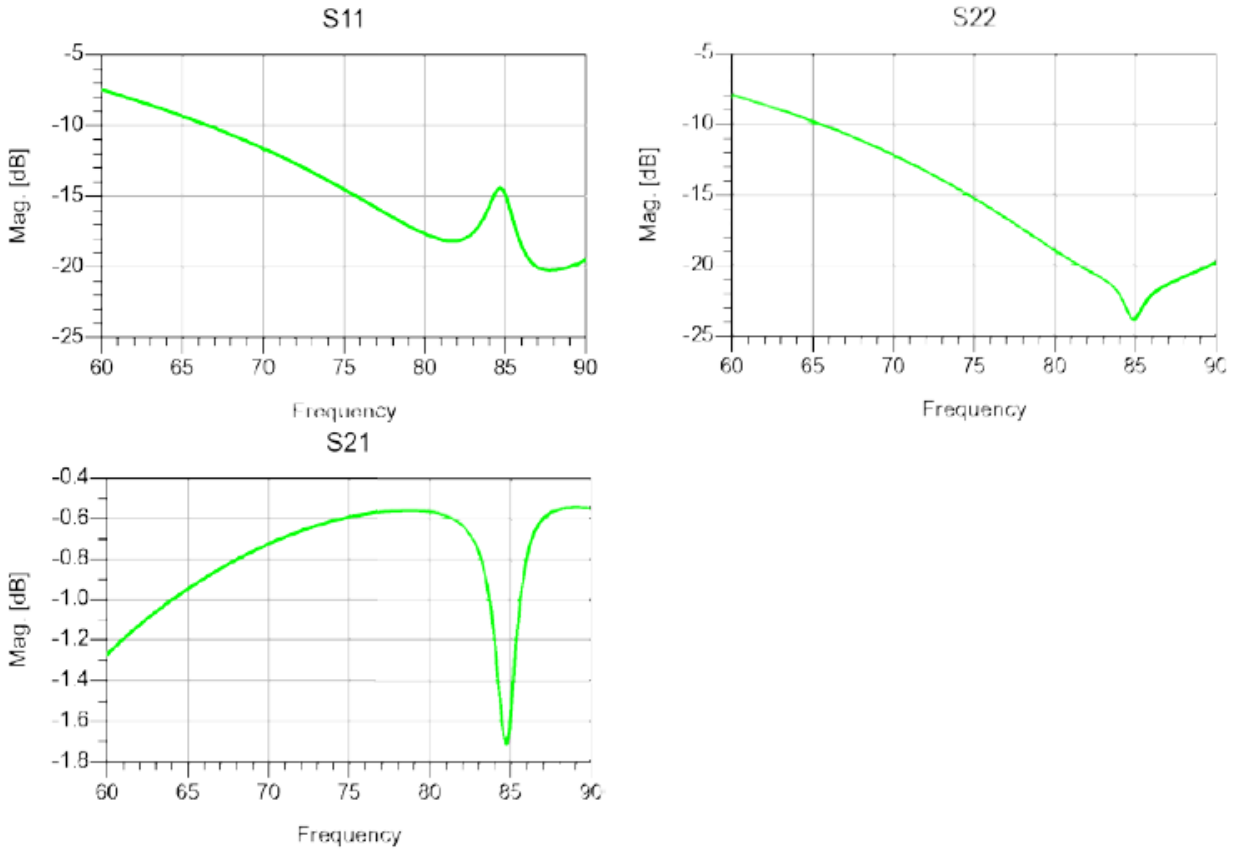


Figure 27. 2.5D EM simulation results of the balun structure shown in Figure 26

9.3 Assembly conditions

The following are basic recommendations for the NXP RCP aseembly:

- Avoid non solder mask defined (NSMD) defined pads
- Pad size 280 µm minimum
- Solder mask defined board pad
- Solder mask opening 200 µm minimum
- Stencil thickness 100 µm
- Solder paste opening 200 µm
- Lead-free solder paste (SAC405)
- ±35 µm placement of component
- Reflow following paste supplier suggested temperatures, or…
- Reflow peak is 260 °C, time above liquidus (217 °C) for 60 to 120 seconds

Figure 28. Solder mask (SMD) and non-solder mask defined (NSMD) pads

The typical reflow profile for the chip-set is shown in Figure 29.

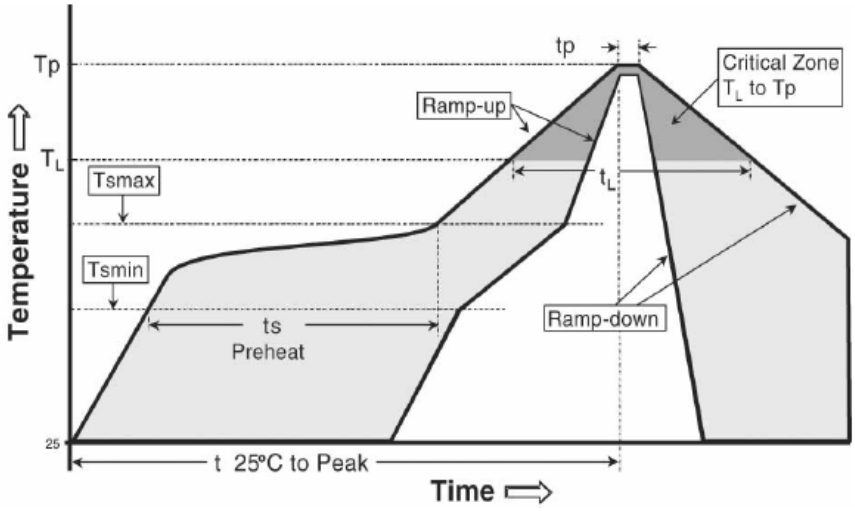


Figure 29. Typical MR2001 reflow profile

Profile parameter	
Average ramp-up rate(TSmax to Tp)	3.0 °C/second max.
Pre-heat • Temperature Min. (TSmin) • Temperature Max. (TSmax) • Time (TSmin to TSmax) (ts)	150 °C 200 °C 60 – 120 seconds
Time maintained above: • Temperature (TL) • Time (tL)	217 °C 60-150 seconds
Peak Temperature (Tp)	260 °C
Time within 5.0 °C of actual Peak Temperature (tp)	10 – 30 seconds
Ramp-down Rate	6.0 °C/second max.
Time 25 °C to Peak Temperature	8 minutes max.

Notes

8. Reflow profile as per IPC/JEDEC J-STD-020D.1

10 Revision history

Revision	Date	Description of Changes
1.0	11/2014	• Initial release
2.0	12/2014	• Made typographic corrections to bring the document into compliance.
3.0	12/2014	• Updated limits for Peak Detector Output Voltage and Power Control
4.0	2/2015	• Clarification on slow and fast modulation times • Clarification on SPI interface • Clarification on LO power detector sensor activation • Update on peak detector threshold voltages • Update on control functionality voltages
5.0	11/2015	• Clarification of POUTM and PDRIFT at PACODE35 • Added formula to ENABLE_FAST and DISABLE_FAST • Updated reflow profile table as per IPC/JEDEC J-STD-020D.1
6.0	8/2016	• Updated to NXP document form and style • Removed RF test concept • Corrected SPI access to temperature sensor and temperature sensor graph, and parameters on reflow profile

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Document Number: MC33MR2001T
Rev. 6.0
8/2016