38-38.5 GHz RF 4-channel voltage controlled oscillator front-end for W-band radar applications

MR2001V

ADVANCED DRIVER ASSISTANCE SYSTEM

The MR2001 is an expandable three package solution for automotive radar modules. The chipset consists of a VCO (voltage controlled oscillator), a two-channel Tx transmitter, and a three-channel Rx receiver.

The MR2001V is a high performance, highly integrated, four-channel VCO, ideally suited for automotive radar applications. In conjunction with the MR2001T, the two-channel transmitter, and the MR2001R, a three-channel receiver, it provides an expandable three package solution for automotive radar modules.

The chips are connected together via the LO signal around 38 GHz. The individual control of each chip is realized by SPI. The main controller and modulation master is a single microprocessor (MCU) with integrated high-speed analog to digital converters (ADC) and appropriate signal processing capability such as fast fourier transforms.

The front-end solution is specifically architected to be controlled by NXP's Qorivva MPC5775 MCU. Especially the baseband functionality (high-pass filters, variable gain amplifiers, anti-aliasing filters) on the receiver chips has been designed to work with the MPC5775 MCU.

VK SUFFIX (PB-FREE)
98ASA00542D
6.0 X 6.0 X 0.95 RCPBGA

Features
- Scalable to 4 TX channels and 12 RX channels
- Advanced packaging technology
- High performance supports fast modulation with simultaneous active channels
- Excellent spatial resolution and detection accuracy
- Local oscillator at 38 GHz to lower the distribution loss and reduce impact on antenna pattern
- Best phase noise < -75 dBc/Hz at 100 kHz offset
- Low power consumption of 2.5 W for the total transceiver
- Integrated system level calibration when combined with Qorivva MPC577xK MCU
- Compatible with all leading MCUs
- Optimized for the NXP Qorivva MPC577xK MCU
- Scalable approach to support SRR, MRR and LRR applications
- Reduced number of external components due to higher integration level
- Baseband integration on receiver suitable to work with the MPC577xK Qorivva MCU
- Bi-phase modulator on the transmitter chip
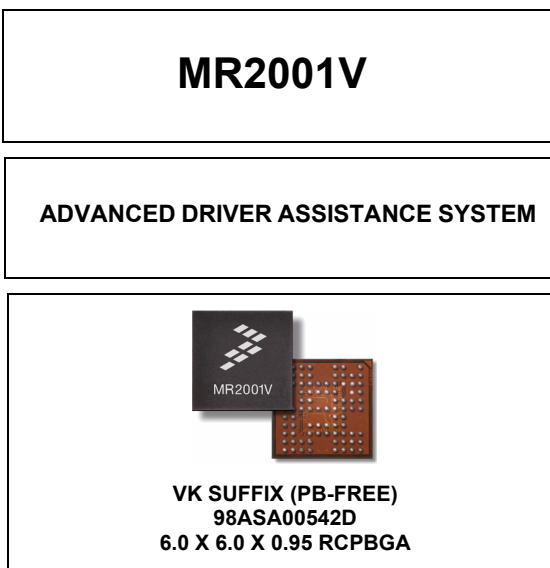
Applications
- Automotive proximity radar
- LRR, MRR and SRR
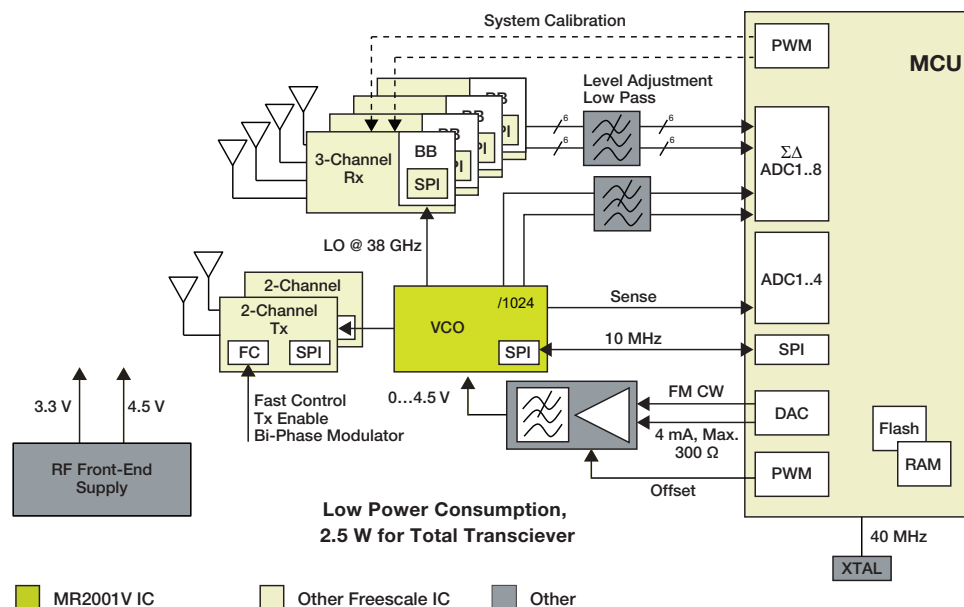- ADAS
- Industrial surveillance and security systems

Figure 1. MR2001V simplified application diagram

Table of contents

1   Orderable parts

Table 1. Orderable part variations

Part number	Temperature (temp)	Package	Notes
MC33MR2001VVK	-40 °C to 125 °C	6.0 x 6.0 mm RCP (10 x 11 array) 0.5 mm pitch	(1) (2)

Notes
1. To order parts in Tape & Reel, add R2 to the suffix of the part number.
2. The device is packaged inside a 6.0 mm x 6.0 mm RCP with 10 x 11 solder balls. The pitch of the solder balls is 0.5 mm.
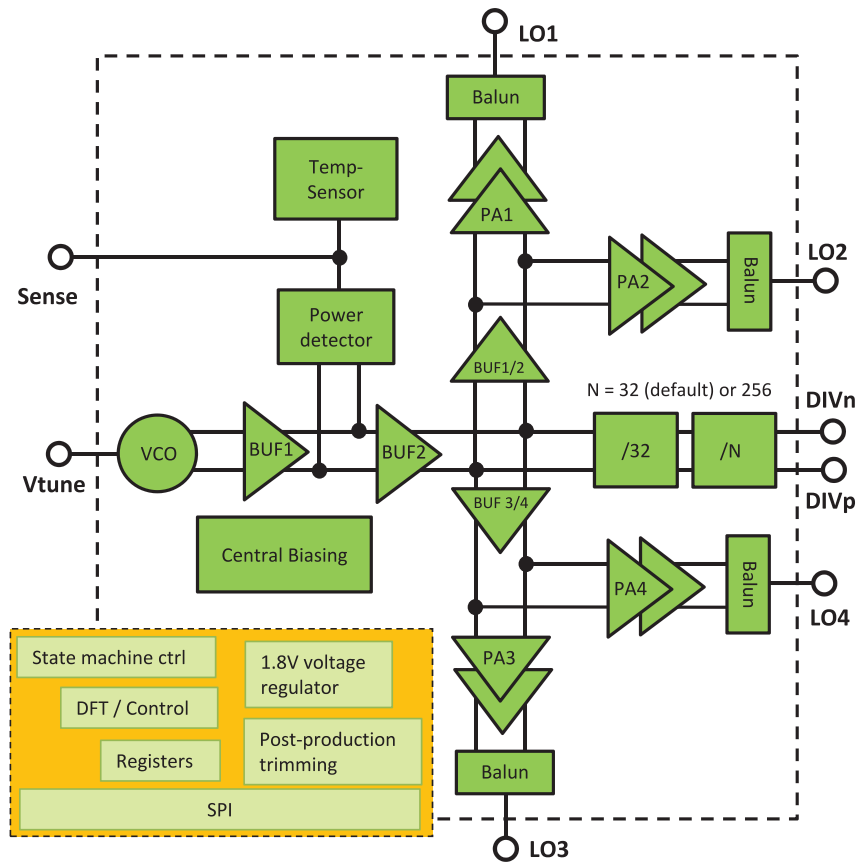
2   Internal block diagram

Figure 2. MR2001V four-channel VCO block diagram

3 Pin connections

3.1 Pinout diagram

The layout and arrangement of the signal pads are shown in Figure 3.
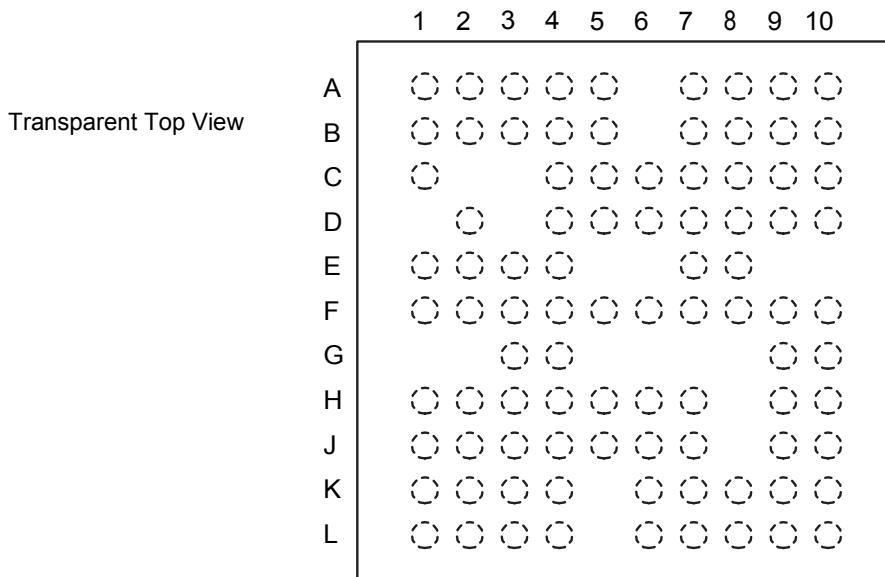

Figure 3. MR2001V pinout (ball) diagram

3.2 Pin definitions (ball)

A functional description of each pin for the MR2001V can be found in Table 2. Equivalent I/O schematics is found in Table 3

Table 2. MR2001V pin definitions

Ball location	Pin name	Pin function	Pin type	Level	Description
A1, B2, B3, B4, B10, C4, C8, C9, D4, E3, E4, F5, F6, G9, H7, H9, J2, J3, J9, K9, L3, L10	GND [4]	DC Ground	Power	0.0 V	
A2	RSETB	Digital hard reset signal	Digital Input	0 to 3.3 V	
A3	DIVp	Differential Frequency Divider Output	Analog Output	0 to 3.3 V	
A4	DIVn	Differential Frequency Divider Output	Analog Output	0 to 3.3 V	
A5, A7, B5, B7, C5, C7, D5, D6, D7, D8, D9, D10, E7, F1, F2, F3, F4, F7, F8, F9, F10, G4, H1, H2, H3, H4, H5, H6, J4, J6, K4, K6, L4, L6	GND1 [4]	RF Ground	Power	0.0 V	
A8, A9, A10, B8, B9, K1, K2, K3, L1, L2	VCC1 [3]	3.3 V Power Supply	Power	3.3 V	
B1	TREG	1.8 V Regulator Output	Analog Output	0 to 3.3 V	
C1	SEB	SPI enable (chip enable)	Digital Input	0 to 3.3 V	
C10	SCANB	Digital scan test	Digital Input	0 to 3.3 V	

MR2001V

Table 2. MR2001V pin definitions (continued)

Ball location	Pin name	Pin function	Pin type	Level	Description
C6	LO4	38 GHz LO output channel 4	RF Output	0 V	
D2	SCLK	SPI serial clock	Digital Input	0 to 3.3 V	
E1	MISO	SPI MISO (master in, slave out)	Digital Output	0 to 3.3 V	
E2	MOSI	SPI MOSI (master out, slave in)	Digital Input	0 to 3.3 V	
E8	LO3	38 GHz LO output channel 3	RF Output	0 V	
G10	RP	Bandgap reference resistor (positive temperature slope)	Analog Input	0 to 3.3 V	See Table 6
G3	LO1	38 GHz LO output channel 1	RF Output	0 V	
H10	RN	Bandgap reference resistor (negative temperature slope)	Analog Input	0 to 3.3 V	See Table 6
J1	TEST	Output to monitor internal bias nodes via ASCAN	Analog Output	0 to 3.3 V	
J10	VVCO	4.5 V Power Supply (only for the VCO core)	Power	4.5 V	
J5	LO2	38 GHz LO output channel 2	RF Output	0 V	
J7, K7, K8, L8, L9	VCC2 [3]	3.3 V Power Supply	Power	3.3 V	
K10	VTUNE	Tuning Voltage	Analog Input	0 to 4.5 V	
L7	SENS	Sensor output (temperature and power peak detector)	Analog output	0 to 3.3 V	

Notes

3. VCC1, VCC2, VCC3 are only connected via the on-chip metal layers. It is mandatory for each supply domain to be connected to the common power supply.
4. GND and GND1 are connected together in the package via the interconnection layer. GND1 is mandatory to be connected, to realize a suitable RF PCB to package transition.

3.3 Equivalent schematics
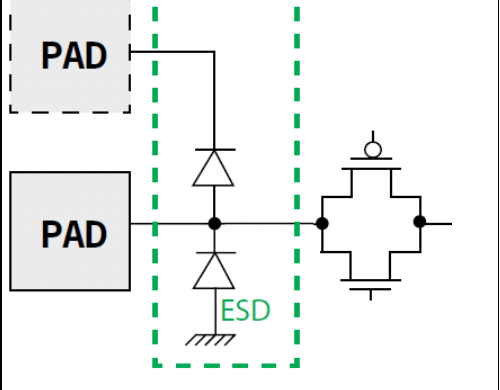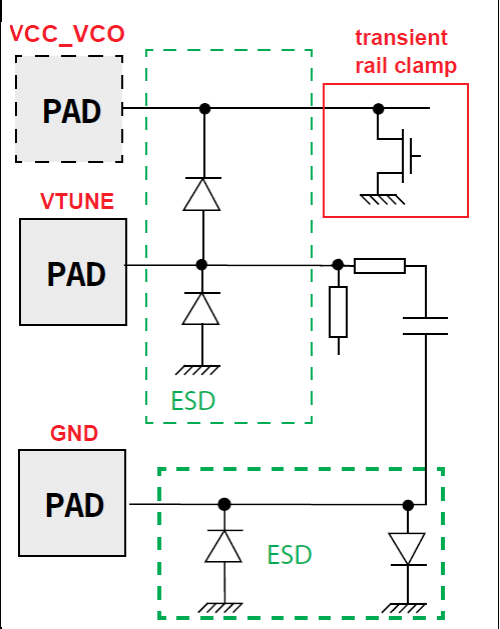
Table 3. Equivalent I/O schematics for pin descriptions

Ball location	Pin function	Equivalent I/O schematic
A8, A9, A10, B8, B9, K1, K2, K3, L1, L2 J7, K7, K8, L8, L9	3.3 V Power Supply	
J10	4.5 V Power Supply (only for the VCO core)	
A5, A7, B5, B7, C5, C7, D5, D6, D7, D8, D9, D10, E7, F1, F2, F3, F4, F7, F8, F9, F10, G4, H1, H2, H3, H4, H5, H6, J4, J6, K4, K6, L4, L6	RF Ground	
A1, B2, B3, B4, B10, C4, C8, C9, D4, E3, E4, F5, F6, G9, H7, H9, J2, J3, J9, K9, L3, L10	DC Ground	
G3	38 GHz LO output channel 1	
J5	38 GHz LO output channel 2	
E8	38 GHz LO output channel 3	
C6	38 GHz LO output channel 4	
E1	SPI MISO (master in, slave out)	
E2	SPI MOSI (master out, slave in)	
D2	SPI serial clock	

Table 3. Equivalent I/O schematics for pin descriptions

Ball location	Pin function	Equivalent I/O schematic
A2	Digital hard reset signal	
C1	SPI enable (chip enable)	
C10	Digital scan test	
H10	Bandgap reference resistor (negative temperature slope)	
G10	Bandgap reference resistor (positive temperature slope)	
B1	1.8 V Regulator Output	
A3		
A4	Differential Frequency Divider Output	

MR2001V

Table 3. Equivalent I/O schematics for pin descriptions

Ball location	Pin function	Equivalent I/O schematic
L7	Sensor output (temperature and power peak detector)	
J1	Output to monitor internal bias nodes via ASCAN	
K10	Tuning Voltage	

4 General product characteristics

4.1 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Min.	Max.	Unit	Notes
V_{STATIC_MAX}	Supply Voltage (static)	-0.30	3.63	V	
V_{DYN_MAX}	Supply Voltage (dynamic) • allowed < 10% of product total llifetime.	-0.30	4.00	V	
V_{VCO_MAX}	VCO Core Supply	-0.30	4.95	V	
V_{DIG_MAX}	Digital Supply Voltage (static, dynamic)	-0.30	3.63	V	
V_{TUNE_MAX}	Tuning Voltage • V_{CC_VCO} +0.3 V	-0.30	4.80	V	
V_{IN_MAX}	Voltage Applied to All Used I/O Pins	-0.30	3.63	V	
ESD					
ESD_HBM	ESD for Human Body Model (HBM) Digital I/O, Analog, RF	-2000	2000	V	
ESD_MM	ESD for Machine Model (MM)	-200	200	V	
R1	HBM Circuit Description I	–	±1500	W	
C	HBM Circuit Description II	–	±100	pF	
	ESD for human body model (HBM) digital I/O	-1000	1000	V	
	ESD HBM, RF I/O	-100	100	V	

4.2 General operating conditions

Table 5. General operation conditions

Temp = -40 °C to +125 °C, f_{OUT} = 38 to 38.5 GHz, V_{CC4P0} = 4.5 V ±5.0%, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
dpack	Package Thickness (mounted condition)	–	950	1200	μm	
Temp	Ambient Package Temperature	-40	27	125	°C	
LU	Latch Up (LU) for DC and Bias Pads • Pulsed current injection method	-100	–	+100	mA	
Pitch	BGA Pitch	–	500	–	μm	
dchip	Chip Thickness	113	—	143	μm	
St_temp	Storage Temperature	-55	—	150	°C	
I_{PAD_MAX}	Pad withstanding	—	—	150	mA	
Number of pulses per pad						
	Number of positive pulses (HBM)	—	—	1		
	Number of negative Pulses (HBM)	—	—	1		
	Interval of Pulses	—	—	1	s	

MR2001V

5 General IC function description and application information

5.1 Introduction

NXP provides a total system solution with next-generation embedded radar-based products that include the Qorivva MPC577xK MCU and 77 GHz packaged radar front-end chipset for both low- and high-end radar modules. This pairing delivers a complete embedded radar system for automotive designs. Our total solution advances automotive safety by enabling vehicles to sense potential crash situations. This radar solution provides long- and mid-range functionality, allowing automotive systems to monitor the environment around the vehicle to help prevent crashes.

A typical radar module consists of a transmit solution (Tx), VCO and three-channel receiver IC (Rx), along with an MCU. The chips are connected via the local oscillator signal, around 38 GHz. The individual control of each chip is implemented by a serial peripheral interface (SPI) bus. The main controller and modulation master is a single MCU with integrated high-speed analog-to-digital converters (ADCs) and appropriate signal processing capability, such as fast Fourier transforms (FFTs).

5.1.1 Features

* 38 GHz to 38.5 GHz TX output
* Supply voltage 3.3 V, 4.5 V ±5.0%
* Supply current typ. 180 mA, 50 mA
* Power dissipation typ. 0.8 W
* KVCO 2.5 GHz/V
* Pushing typ. 250 MHz/V
* Static Pulling < 10 MHz
* Phase Noise typ. -95 dBc/Hz at 1.0 MHz
* LO Power min. 3.0 dBm

Power Control (4 steps)

5.2 Electrical characteristics

5.2.1 Voltage controlled oscillator VCO

Table 6. Interface levels

Temp = -40 °C to +125 °C, f_{OUT} = 38 to 38.5 GHz, V_{CC4P0} = 4.5 V ±5.0%, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{CC}	Supply Voltage (VCO not included) • Nominal supply ±5% variation	3.135	3.3	3.465	V	
I_{CC1}	Supply Current (all channels on, VCO not included) • All channels ON	–	170	210	mA	
V_{CC_VCO}	VCO Supply Voltage	4.275	4.5	4.725	V	
I_{CC_VCO}	VCO Supply Current	40	50	55	mA	
P_{DIS}	Power Consumption (all channels ON) • all channels ON, max. power	–	0.79	0.987	W	
Thermal parameters						
R_{TH}	Thermal Resistance • Measured on RO3003/FR4 stack	–	15	22	K/W	
Control						
SPI	SPI functionality • 10 MHz clock required	Yes				

MR2001V

Table 6. Interface levels

Temp = -40 °C to +125 °C, f_{OUT} = 38 to 38.5 GHz, V_{CC4P0} = 4.5 V ±5.0%, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Frequency and # of channels						
n_ch	Number of LO Output Channels (at 38 GHz) - 4 x single-ended	–	–	4.0		
f_{VCO_MIN}	Min. VCO Frequency	–	–	38	GHz	
f_{VCO_MAX}	Max. VCO Frequency	38.5	–	–	GHz	
V_{TUNE_MIN}	Min. VCO Tuning Voltage to Achieve 38 GHz	0.2	–	–	V	
V_{TUNE_MAX}	Max. VCO Tuning Voltage	–	–	4.2	V	
V_{TUNE}	VCO Tuning Voltage • VCO, divider and all control functions (SPI) must be guaranteed	0.0	–	4.2	V	
KVCO	VCO tuning sensitivity (Δf/ΔV) at 76-77 GHz	0.6	2.5	4.0	GHz/V	
R_KVCO	Ratio of KVCO at 38 G/KVCO at 38.5 G • For fixed V_{CC} and temperature	–	–	2.0		
t_{DRIFT}	Thermal Frequency Drift	-25	-17	2.0	MHz/K	
R_{TUNE}	Input Impedance of Tuning Port Up to 100 MHz	100	–	–	kΩ	
C_{TUNE}	Tuning Port Input Capacity • Up to 10 MHz nearly only capacitive behavior	–	–	2.5	pF	
TUNING_SPEED	VCO Tuning Speed	1000	–	–	MHz/µs	
Set-up & response time						
t_{TURNON}	Max. Frequency Setting Time After Power ON	0.0	–	1.0	ms	
$t_{IMPULSE1}$	Impulse Response Time I • For a frequency step from 76 G to 77 G and 77 G stable within ±2.0 MHz not measured in production	0.0	–	1.0	µs	
$t_{IMPULSE2}$	Impulse Response Time II • For a frequency step from 76 G to 77 G and 77 G stable within ±250 kHz not measured in production	0.0	–	0.5	ms	
Pushing/pulling						
PUSHING	VCO Frequency Change Versus VCC at 76 to 77 GHz	0.0	250	450	MHz/V	
STATIC PULLING	VCO Frequency Versus Load (static) at 76 to 77 GHz • All phases, 10 dB mismatch not measured in production	0.0	–	10	MHz	
DYNAMIC PULLING	VCO Frequency Versus Load (dynamic) at 76 to 77 GHz • All phases, 10 dB mismatch not measured in production	0.0	–	0.5	MHz	
Phase noise						
PN_10kHz	Phase noise at 10 kHz offset at 77 GHz • PN at 38 GHz is 6.0 dB lower	–	–	-40	dBc/Hz	
PN_100kHz	Phase noise at 100 kHz offset at 77 GHz • PN at 38 GHz is 6.0 dB lower	–	-73	-67	dBc/Hz	
PN_1.0MHz	Phase noise at 1.0 MHz offset at 77 GHz • PN at 38 GHz is 6.0 dB lower	–	–	-92	dBc/Hz	
PN_10MHz	Phase noise at 10 MHz offset at 77 GHz • PN at 38 GHz is 6.0 dB lower	–	–	-112	dBc/Hz	
Spurious						
HARMSPUR	Harmonic Spurious (n x F_VCO), n > 1 • Referred to P_LO_OUT (3.0 dBm output power)	–	–	-25	dBc	
NHARMSPUR	Nonharmonic Spurious • Referred to P_LO_OUT, divider enabled	–	–	-65	dBc	

MR2001V

Table 6. Interface levels

Temp = -40 °C to +125 °C, f_{OUT} = 38 to 38.5 GHz, V_{CC4P0} = 4.5 V ±5.0%, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Return loss						
G_LO	LO-port Return Loss (50 Ω) • Single-ended configuration	10	–	–	dB	
Power						
P_LO_OUT	LO Output Power • Single-ended configuration, power code 2	-2.0	–	–	dBm	
P_LO_RIPPLE	LO Output Power Ripple	-1.0	–	1.0	dB	
P_LO_CTRL	LO Output Power Control • Four steps via SPI	–	3.0	–	dB	
P_CTRL_R	LO Power Control • Each with ~3.5 dB, via SPI, each channel independent, 4 steps only: 0, -3.5, -7.0, -10.5	7.0	–	–	dB	
DISABLE_CTRL	Enable,Disable Functionality (FD_en, LO_en)	Via SPI				
Frequency divider						
NDIV	Division Ratio • Based on VCO at 38 GHz	1024	–	1024		
FDIV	Frequency Divider Output Frequency (fundamental)	37.1	–	37.6	MHz	
VDIV	Divider Output Voltage • Balanced output at defined load impedance	0.87	–	1.64	V_{PP}	
RDIV	Divider Output Load Resistance • 100 Ω single-ended	200 (balanced)	–	–	W	
CDIV	Divider Output Load Capacity • single-ended C (each side)	–	–	30	pF	
DC	Duty Cycle	48	50	52	%	
	# of Last Stages to Disable - via SPI	–	5.0	–		
Sensor output						
S_IMP_DIS	Sensor High Output Impedance (temp. sensor) • If corresponding sensor is disabled the output should show high impedance	Yes				
S_LOAD_R	Sensor Load Resistance • To ground (temp, peak detector)	90	100	110	kΩ	
S_LOAD_C	Sensor Load Capacity • To ground (temp, peak detector)	–	–	30	pF	
Temperature sensor						
T_SLOPE	Temperature Sensor Sensitivity • Two sequential readings required	–	0.55	–	mV/K	
T_SLOPE_VAR	Temperature Sensor Tolerance • Deviation from mean slope (T_slope) over temperature	-5.0	0.0	5.0	K	
T_RANGE	Temperature Sensor Output Voltage Range • Max. value achieved at 150 °C	0.4	–	3.0	V	
External resistors for biasing						
RP	External Resistor 1 • E96, ±1.0%, TK = ±100 ppm/K SMD, 0402 or smaller, 50 μA current	–	2.15	–	kΩ	
RN	External Resistor 2 • E96, ±1.0%, TK = ±100 ppm/K SMD, 0402 or smaller, 50 μA current	–	14.7	–	kΩ	

MR2001V

NXP Semiconductors

6 Functional block requirements and behaviors

NXP millimeter wave and radar products enable advanced, high-performance, multi-channel systems for use in automotive radar, automotive advanced driver assistance systems (ADAS), automotive safety systems and other high-performance communication infrastructure and industrial systems.

The MR2001 is a high-performance 77 GHz radar transceiver chipset scalable for multi-channel operation enabling a single radar platform with electronic beam steering and wide field of view to support long-range radar (LRR), mid-range radar (MRR) and short-range radar (SRR) applications. This new radar chipset consists of a VCO (MR2001VC), a two-channel Tx transmitter (MR2001TX) and a three-channel Rx receiver (MR2001RX). This 77 GHz radar transceiver chipset is compatible with all leading MCUs, including the Qorivva MPC577xK MCU.

The MR2001 radar chipset is designed to support fast modulation with simultaneous active channels, enabling excellent spatial resolution and detection accuracy across a wide field of view. It supports a large variety of chirps in open loop VCO radar system architectures and consumes minimal power. An integrated BB filter and VGA saves on the total bill of materials. The MR2001 radar chipset uses advanced packaging technology to ensure the highest performance and minimum signal interference on the printed circuit board (PCB).

6.1 SPI communication

6.1.1 SPI interface

SPI read and write are illustrated in Figure 4 and Figure 5. Figure 6 shows the SPI read/write operation to ASCAN.

a[5:0] is the SPI address to be written, as shown in the memory map.

d[7:2] is the data that is written to, or read from this address.Bit [1:0] are reserved.

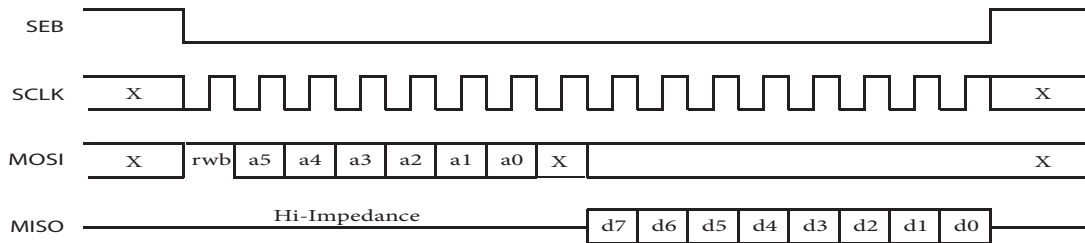rwb is the read write bit. Read is done when rwb is '1', write is done when rwb is '0'.

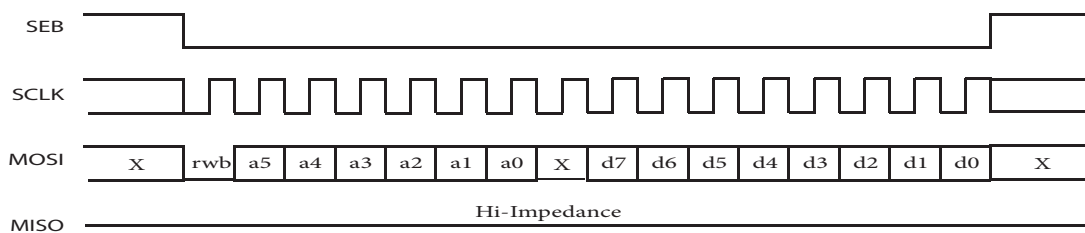
Figure 4. SPI read from internal registers

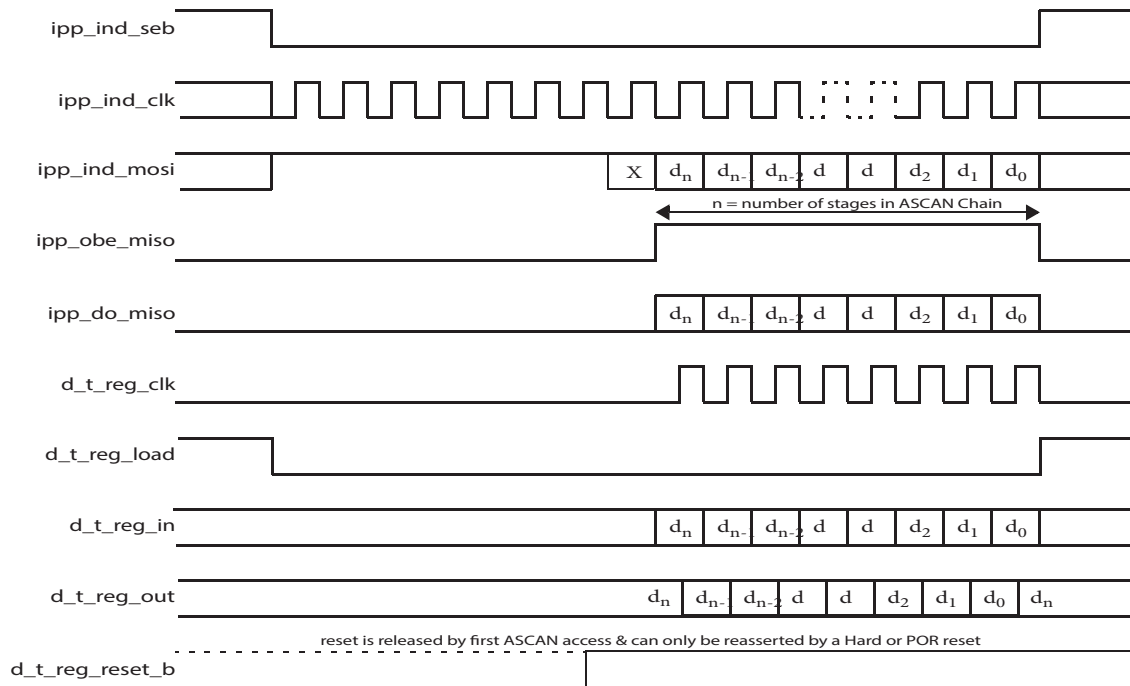**Figure 5. SPI write to internal registers**

MR2001V

Figure 6. SPI write/read to ASCAN

6.1.2 Timing

SPI timings are described in Table 7 and illustrated in Figure 7. The SPI timing diagram, with the temperature and supply voltage conditions described in this document, and a maximum load capacitance, CL = 20 pF.

Table 7. SPI timing

Symbol	Parameter	Min	Typ	Max	Unit	Notes [5]
t_{SCLK}	SCLK Cycle Time - SCLK pin	100	–	–	ns	(1)
t_{CSC}	SEB to SCLK Delay - SEB, SCLK pin	90	–	–	ns	(2)
t_{ASC}	After SCLK Delay - SCLK, SEB pin	2.5	–	–	ns	(3)
t_{SDC}	SCLK Duty Cycle - SCLK pin	0.9* $(t_{SCLK}/2)$	–	1.1* $(t_{SCLK}/2)$	ns	(4) [6]
t_{SUI}	Data Setup Time for Inputs - MOSI, SCLK pin	40	–	–	ns	(5)
t_{HI}	Data Hold Time for Inputs - MOSI, SCLK pin	40	–	–	ns	(6)
t_{SUO}	Data Valid (after SCLK edge) - MISO, SCLK pin	–	–	50	ns	(7)
t_{HO}	Data Hold Time for Outputs - MISO, SCLK pin	50	–	–	ns	(8)
H_{ZSEB}	High-impedance to SEB - MOSI, SEB pin	0.0	–	–	ns	(9)

Notes
5. The numbers under the Notes heading refer to the corresponding numbers in Figure 7.
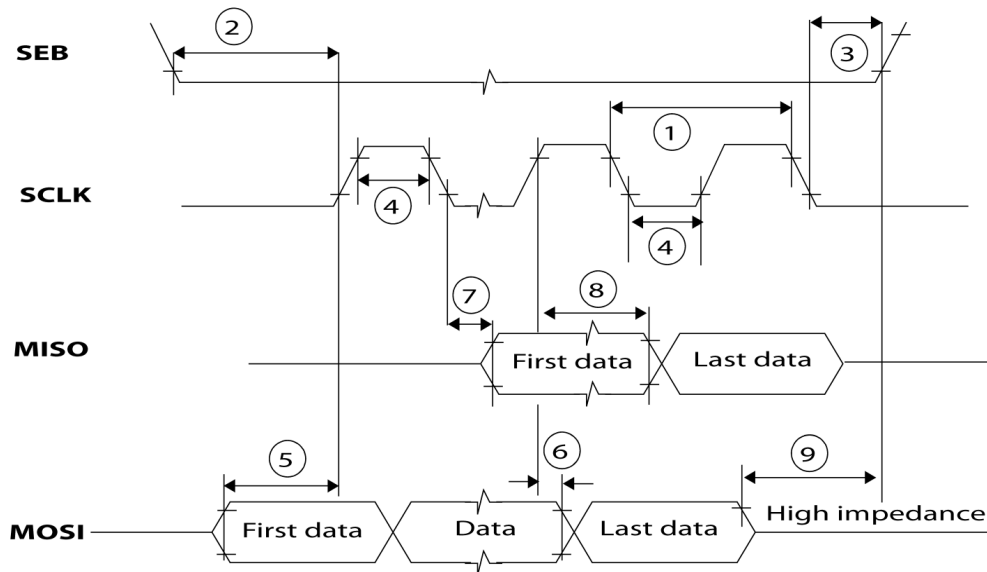6. For the maximum clock speed of 10 MHz

Figure 7. Typical SPI timing chart

6.2   External address solder balls ADR0 and ADR1

To minimize the effort on hardware wiring of signals, the MR2001V uses a combination of hardware and software coded addressing of each individual chip. Due to this procedure the hardware SEB (chip select) signal usage can be minimized.

If the software addressing is not longer sufficient (e.g. more than 4 RX chips) than a combination of SEB and software addressing is recommended.

Depending on the chip up to two external solder balls (address bit) are available (ADR0, ADR1). A connection to VCC represents a logical "1" and a connection to GND represents a logical "0", respectively. By default the logical "1" is already activated by a connection on the Die. If the corresponding pin is not connected to GND (used ball, not soldered ball), then this represents a logical "1".
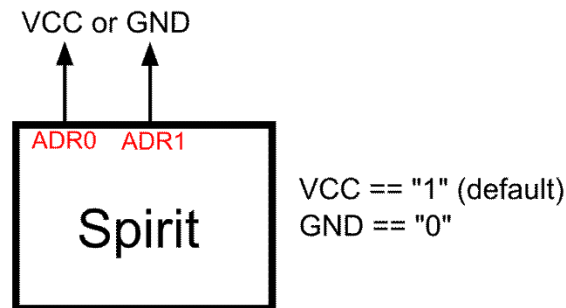

Figure 8. External connection of address pins ADR0 and ADR1 to define the identification key of the chip

6.3   System partitioning

Using the "software" addressing scheme of Spirit chips, any system up to max. one VCO, two transmitter (TX) and 4 receiver (RX) chips are supported.
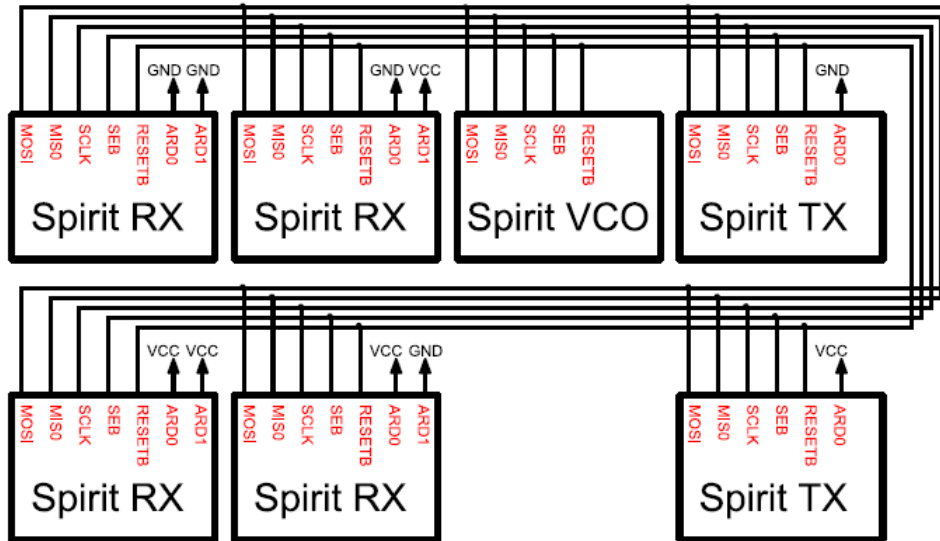

Figure 9. Chip partitioning using only software addressing of individual chips

If a system requires more than 4 Rx chips and/or 2 Tx chips and/or 1 VCO chip. Table 10 shows a proposed way to address the chips with a combination of the SEB (chip select) signal and "software" addressing.
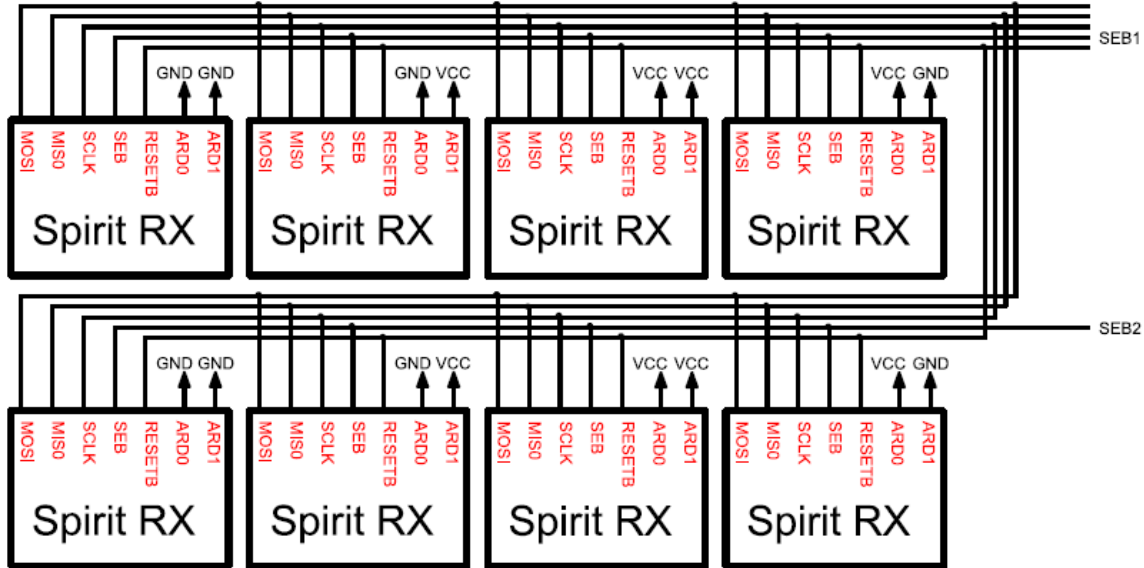

Figure 10. Typical Rx chip partitioning for more than four receivers.
Individual SEB signals for more than four Rx chips are required

6.4 Identification key

The Identification key is used to address the correct chip via SPI and it is composed of four up to six internal (on the chip hard wired) bits and up to two external bits defined by the voltage level applied to the ADR0 and ADR1 solder balls.

Table 8. Identification key

Chip	Internal bits	ADR0	ADR1	Chip key
RX1	1010	0	0	101000
RX2	1010	1	0	101001
RX3	1010	0	1	101010
RX4	1010	1	1	101011
TX1	01110	0	-	011100
TX2	01110	1	-	011101
VCO	101100	-	-	101100

If more individual chips must be addressed then the chip select (SEB) signal must be used.

6.5 Access protocol

6.5.1 Write access

Write access to the device is done as follows:

Table 9. Write access

SPI_WRITE(add0, RX1 key)	access to RX1 is activated
SPI_WRITE(add1, data1)	write data1 to the RX1 register at address 1
SPI_WRITE(add0, VCO key)	access to VCO is activated
SPI_WRITE(add3, data3)	write data3 to the VCO register at address 3

6.5.2 Read access

Read access to the device is done as follows:

Table 10. Read access

SPI_WRITE(add0, RX1 key)	access to RX1 is activated
SPI_READ(add1, data1)	read data1 to the RX1 register at address 1
SPI_WRITE(add0, VCO key)	access to VCO is activated
SPI_READ(add3, data3)	read data3 to the VCO register at address 3

7 Memory map

7.1 Generic memory map

All three MR2001 chips share the same general memory map which simplifies the programming and minimizes the error due to changes in varying register addresses.

Table 11. Generic memory map

Addr	Register	Type	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	KEY	R/W	0x00	KEY_5	KEY_4	KEY_3	KEY_2	KEY_1	KEY_0	RESERVED	RESERVED
0x01	FSM0	R/W	0x04	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S0_F	RESERVED	RESERVED
0x02	FSM1	R/W	0x00	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S1_F	RESERVED	RESERVED
0x03	EN	R/W	0x00	EN_5	EN_4	EN_3	EN_2	EN_1	EN_0	RESERVED	RESERVED
0x04	CTRL0	R/W	0x00	CTRL0_5	CTRL0_4	CTRL0_3	CTRL0_2	CTRL0_1	CTRL0_0	RESERVED	RESERVED
0x05	CTRL1	R/W	0x00	CTRL1_5	CTRL1_4	CTRL1_3	CTRL1_2	CTRL1_1	CTRL1_0	RESERVED	RESERVED
0x06	CTRL2	R/W	0x00	CTRL2_5	CTRL2_4	CTRL2_3	CTRL2_2	CTRL2_1	CTRL2_0	RESERVED	RESERVED
0x07	CTRL3	R/W	0x00	CTRL3_5	CTRL3_4	CTRL3_3	CTRL3_2	CTRL3_1	CTRL3_0	RESERVED	RESERVED
0x08	SNSOUT	R/W	0x00	SNSOUT_5	SNSOUT_4	SNSOUT_3	SNSOUT_2	SNSOUT_1	SNSOUT_0	RESERVED	RESERVED
0x09	TST	R/W	0x00	TST_5	TST_4	TST_3	TST_2	TST_1	TST_0	RESERVED	RESERVED

As an example, the register 0x03 describes the control enable/disable functionality. The level of control/enable can be different for each individual chip. Details can be found in the register map of each chip.

7.2 VCO memory map

Table 12. VCO Memory Map

Addr	Register	Type	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	KEY	R/W	0x00	KEY_5	KEY_4	KEY_3	KEY_2	KEY_1	KEY_0	RESERVED	RESERVED
0x01	FSM0	R/W	0x04	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S0_F	RESERVED	RESERVED
0x02	FSM1	R/W	0x00	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S1_F	RESERVED	RESERVED
0x03	EN	R/W	0x00	LO4	LO3	LO2	LO1	DIV_OUT	VCO_BUFEN	RESERVED	RESERVED
0x04	CTRL0	R/W	0x00	NOT_USED	NOT_USED	LOPWR4_ch1	LOPWR3_ch1	LOPWR2_ch1	LOPWR1_ch1	RESERVED	RESERVED
0x05	CTRL1	R/W	0x00	NOT_USED	NOT_USED	LOPWR4_ch2	LOPWR3_ch2	LOPWR2_ch2	LOPWR1_ch2	RESERVED	RESERVED
0x06	CTRL2	R/W	0x00	NOT_USED	NOT_USED	LOPWR4_ch3	LOPWR3_ch3	LOPWR2_ch3	LOPWR1_ch3	RESERVED	RESERVED
0x07	CTRL3	R/W	0x00	NOT_USED	DIV8_EN	LOPWR4_ch4	LOPWR3_ch4	LOPWR2_ch4	LOPWR1_ch4	RESERVED	RESERVED
0x08	SNSOUT	R/W	0x00	TMP_EN	TMP_SEL	PD_EN	PD_SEL0	TMP_TYP	SNS_RSET	RESERVED	RESERVED

MR2001V

7.2.1   0x00 VCO key register

Address	0x00					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	KEY_5	KEY_4	KEY_3	KEY_2	KEY_1	KEY_0	RESERVED	RESERVED
Reset	0	0	0	0	0	0	N/A	N/A

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[7:2]	KEY	Device Identification Key

7.2.2   0x01 VCO S0 state machine register (disabled)

Address	0x01					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S0_F	RESERVED	RESERVED
Reset	0	0	0	0	0	1	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	S0_F	State machine register. When S0_F is set to 1 the state machine is changing from S1 (enable) to S0 (disable)
[7:3]	NOT_USED	Unused bits

7.2.3   0x02 VCO S1 state machine register (enabled)

Address	0x02					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S1_F	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	S1_F	State machine register. When S1_F is set to 1 the state machine is changing from S0 (disable) to S1 (enable)
[7:3]	NOT_USED	Unused bits

7.2.4 0x03 VCO enable and LO input peak detector bits

Address	0x03					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	LO4	LO3	LO2	LO1	DIV_OUT	VC0_BUFEN	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	VC0_BUFEN	Enable VCO buffer
[3]	DIV_OUT	Enable last 5 divder stages
[4]	LO1	Enable LO output 1. LOPWR_ch1 need to be set different from 0 prior to LO1 activation
[5]	LO2	Enable LO output 2. LOPWR_ch2 need to be set different from 0 prior to LO2 activation
[6]	LO3	Enable LO output 3. LOPWR_ch3 need to be set different from 0 prior to LO3 activation
[7]	LO4	Enable LO output 4. LOPWR_ch4 need to be set different from 0 prior to LO4 activation

7.2.5 0x04 VCO LO1 control register

Address	0x04					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	NOT_USED	NOT_USED	LOPWR4_ch1	LOPWR3_ch1	LOPWR2_ch1	LOPWR1_ch1	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[7:6]	NOT_USED	Unused bits

Field [5]	Field [4]	Field [3]	Field [2]	LO1 output power level:
0	0	0	0	No current to output stage; highest possible attenuation
0	0	0	1	Approx. 10.5 dB attenuation, P_{OUT} ~ -7.0 dBm
0	0	1	0	-4.0 dBm > P_{OUT} > -7.0 dBm
0	0	1	1	Approx. 7.0 dB attenuation, P_{OUT} ~ -4.0 dBm
0	1	0	0	0 dBm > P_{OUT} > -4.0 dBm
0	1	0	1	0 dBm > P_{OUT} > -4.0 dBm
0	1	1	0	0 dBm > P_{OUT} > -4.0 dBm
0	1	1	1	Approx. 3.5 dB attenuation, P_{OUT} ~ 0 dBm
1	0	0	0	3.0 dBm > P_{OUT} > 0 dBm
1	0	0	1	3.0 dBm > P_{OUT} > 0 dBm

Field [5]	Field [4]	Field [3]	Field [2]	LO1 output power level:
1	0	1	0	3.0 dBm > P_{OUT} > 0 dBm
1	0	1	1	3.0 dBm > P_{OUT} > 0 dBm
1	1	0	0	3.0 dBm > P_{OUT} > 0 dBm
1	1	0	1	3.0 dBm > P_{OUT} > 0 dBm
1	1	1	0	3.0 dBm > P_{OUT} > 0 dBm
1	1	1	1	Max. output power, > approx. 3.0 dBm

7.2.6　0x05 VCO LO2 control register

Address	0x05					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	NOT_USED	NOT_USED	LOPWR4_ch2	LOPWR3_ch2	LOPWR2_ch2	LOPWR1_ch2	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[7:6]	NOT_USED	Unused bits

Field [5]	Field [4]	Field [3]	Field [2]	LO2 output power level:
0	0	0	0	No current to output stage; highest possible attenuation
0	0	0	1	Approx. 10.5 dB attenuation, P_{OUT} ~ -7.0 dBm
0	0	1	0	-4.0 dBm > P_{OUT} > -7.0 dBm
0	0	1	1	Approx. 7.0 dB attenuation, P_{OUT} ~ -4.0 dBm
0	1	0	0	0 dBm > P_{OUT} > -4.0 dBm
0	1	0	1	0 dBm > P_{OUT} > -4.0 dBm
0	1	1	0	0 dBm > P_{OUT} > -4.0 dBm
0	1	1	1	Approx. 3.5 dB attenuation, P_{OUT} ~ 0 dBm
1	0	0	0	3.0 dBm > P_{OUT} > 0 dBm
1	0	0	1	3.0 dBm > P_{OUT} > 0 dBm
1	0	1	0	3.0 dBm > P_{OUT} > 0 dBm
1	0	1	1	3.0 dBm > P_{OUT} > 0 dBm
1	1	0	0	3.0 dBm > P_{OUT} > 0 dBm
1	1	0	1	3.0 dBm > P_{OUT} > 0 dBm
1	1	1	0	3.0 dBm > P_{OUT} > 0 dBm
1	1	1	1	Max. output power, > approx. 3.0 dBm

7.2.7 0x06 VCO LO3 control register

Address	0x05						Access: user read write	
Bit	7	6	5	4	3	2	1	0
R/W	NOT_USED	NOT_USED	LOPWR4_ch3	LOPWR3_ch3	LOPWR2_ch3	LOPWR1_ch3	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[7:6]	NOT_USED	Unused bits

Field [5]	Field [4]	Field [3]	Field [2]	LO3 output power level:
0	0	0	0	No current to output stage; highest possible attenuation
0	0	0	1	Approx. 10.5 dB attenuation, P_{OUT} ~ -7.0 dBm
0	0	1	0	-4.0 dBm > P_{OUT} > -7.0 dBm
0	0	1	1	Approx. 7.0 dB attenuation, P_{OUT} ~ -4.0 dBm
0	1	0	0	0 dBm > P_{OUT} > -4.0 dBm
0	1	0	1	0 dBm > P_{OUT} > -4.0 dBm
0	1	1	0	0 dBm > P_{OUT} > -4.0 dBm
0	1	1	1	Approx. 3.5 dB attenuation, P_{OUT} ~ 0 dBm
1	0	0	0	3.0 dBm > P_{OUT} > 0 dBm
1	0	0	1	3.0 dBm > P_{OUT} > 0 dBm
1	0	1	0	3.0 dBm > P_{OUT} > 0 dBm
1	0	1	1	3.0 dBm > P_{OUT} > 0 dBm
1	1	0	0	3.0 dBm > P_{OUT} > 0 dBm
1	1	0	1	3.0 dBm > P_{OUT} > 0 dBm
1	1	1	0	3.0 dBm > P_{OUT} > 0 dBm
1	1	1	1	Max. output power, > approx. 3.0 dBm

7.2.8 0x07 VCO LO4 control register

Address	0x05						Access: user read write	
Bit	7	6	5	4	3	2	1	0
R/W	NOT_USED	DIV8_EN	LOPWR4_ch4	LOPWR3_ch4	LOPWR2_ch4	LOPWR1_ch4	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[6]	DIV8_EN	Enables divider ratio of 8192 (default is 1024)
[7]	NOT_USED	Unused bits

MR2001V

Field [5]	Field [4]	Field [3]	Field [2]	LO4 output power level:
0	0	0	0	No current to output stage; highest possible attenuation
0	0	0	1	Approx. 10.5 dB attenuation, P_{OUT} ~ -7.0 dBm
0	0	1	0	-4.0 dBm > P_{OUT} > -7.0 dBm
0	0	1	1	Approx. 7.0 dB attenuation, P_{OUT} ~ -4.0 dBm
0	1	0	0	0 dBm > P_{OUT} > -4.0 dBm
0	1	0	1	0 dBm > P_{OUT} > -4.0 dBm
0	1	1	0	0 dBm > P_{OUT} > -4.0 dBm
0	1	1	1	Approx. 3.5 dB attenuation, P_{OUT} ~ 0 dBm
1	0	0	0	3.0 dBm > P_{OUT} > 0 dBm
1	0	0	1	3.0 dBm > P_{OUT} > 0 dBm
1	0	1	0	3.0 dBm > P_{OUT} > 0 dBm
1	0	1	1	3.0 dBm > P_{OUT} > 0 dBm
1	1	0	0	3.0 dBm > P_{OUT} > 0 dBm
1	1	0	1	3.0 dBm > P_{OUT} > 0 dBm
1	1	1	0	3.0 dBm > P_{OUT} > 0 dBm
1	1	1	1	Max. output power, > approx. 3.0 dBm

7.2.9   0x08 VCO sensor register

Address	0x08					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	TMP_EN	TMP_SEL	PD_EN	PD_SEL0	TMP_TYP	SNS_RSET	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	SNS_RSET	Sensor reset (discharge of internal capacitance)
[3]	TMP_TYP	Activate temperature sensor 1: Temperature sensor activated
[4]	PD_SEL0	Peak power detector reference branch selection 0: diode row 1 1: diode row 2
[5]	PD_EN	Enable peak power detector
[6]	TMP_SEL	Temperature sensor output selection 0: diode row 1 1: diode row 2
[7]	TMP_EN	Enable temperature sensor

Only the temperature sensor or the peak detector can be enabled at a time. The temperature sensor is using a reference (diode row = 0) and a signal branch (diode row = 1) only the absolute difference between these two voltages gives a voltage with is proportional to temperature, and peak voltage level. Example for the temperature sensor activation is as follows.

MR2001V

Table 13. Temperature sensor activation

SPI_WRITE(0x00, VCO key)	access to VCO is activated
SPI_WRITE(0x08, 04h)	Activate sensor reset SNS_RSET (discharge on-chip capacitance)
SPI_WRITE(0x08, 88h)	Enable temperature sensor at diode row 0
<measure V1>	Measure voltage V1 at sense output
SPI_WRITE(0x08, 04h)	Activate sensor reset SNS_RSET (discharge on-chip capacitance)
SPI_WRITE(0x08, C8h)	Enable temperature sensor at diode row 1
<measure V2>	Measure voltage V2 at sense output

|V1-V2| gives a voltage which is proportional to the on-chip temperature. SNS_RSET (sensor reset) activation discharges an on-chip capacitance (pull down the output to GND). The activation maybe required between each change of the sensor branch to speed up communication. Similar scheme must be used to read out values of the peak detector.

7.3   State machine

The MR2001 chipset contains a digital controller which provides a simplied enable/disable control of the key analog blocks. The state maschine has only two states S0 and S1. S0 corresponds to the OFF (disabled) mode and S1 corresponds to the ON (enabled) mode, respectively.
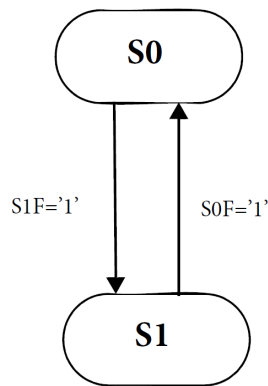
Figure 11. MR2001V state machine with the two states S0 and S1

The signals, block controlled by the state machine are listed in the following table.

Internal signal names	Chip	State machine S1 (register 0x02 set to 0x04)	State machine S0 (register 0x01 set to 0x04)
d_out2	VCO	VCO core enabled	VCO core disabled
d_out3	VCO	Divider chain except last five stages enabled	Divider chain except last five stages disabled
d_out3	VCO	VCO buffer and PA buffer enabled	VCO buffer and PA buffer disabled
d_out6	VCO	LO1 output buffer enabled	LO1 output buffer disabled
d_out8	VCO	LO2 output buffer enabled	LO2 output buffer disabled
d_out10	VCO	LO3 output buffer enabled	LO3 output buffer disabled
d_out12	VCO	LO4 output buffer enabled	LO4 output buffer disabled
d_out14	VCO	enabled last five divider chain stages	last five divider chain stages disabled

MR2001V

NXP Semiconductors

8 Typical applications

8.1 Introduction

The MR2001 is an expandable three package solution for automotive radar modules. The chipset consists of a VCO (voltage controlled oscillator), a two-channel Tx transmitter, and a three-channel Rx receiver.

The MR2001V is a high performance, highly integrated, four-channel VCO, ideally suited for automotive radar applications. In conjunction with the MR2001T, the two-channel transmitter, and the MR2001R, a three-channel receiver, it provides an expandable three package solution for automotive radar modules.

The chips are connected together via the LO signal around 38 GHz. The individual control of each chip is realized by SPI. The main controller and modulation master is a single microprocessor (MCU) with integrated high-speed analog to digital converters (ADC) and appropriate signal processing capability such as fast fourier transforms.

The front-end solution is specifically architected to be controlled by NXP's Qorivva MPC5775 MCU. Especially the baseband functionality (high-pass filters, variable gain amplifiers, anti-aliasing filters) on the receiver chips has been designed to work with the MPC5775 MCU.

8.2 Typical application
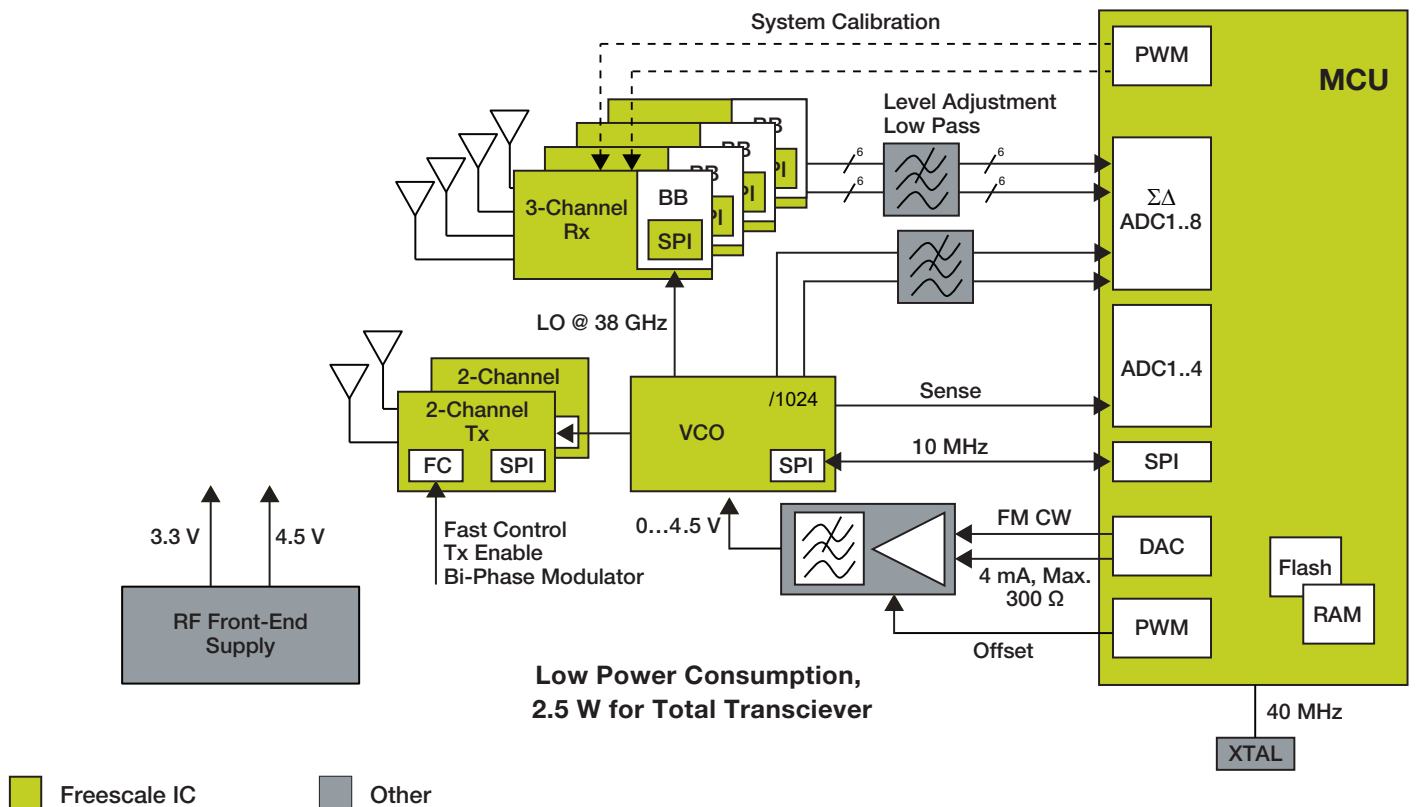
Figure 12. Typical application diagram

8.3 Measurement results

In the following chapters can find some typical measurement results which should help to guide a Radar system design.

8.3.1 Common results

8.3.1.1 Temperature sensor
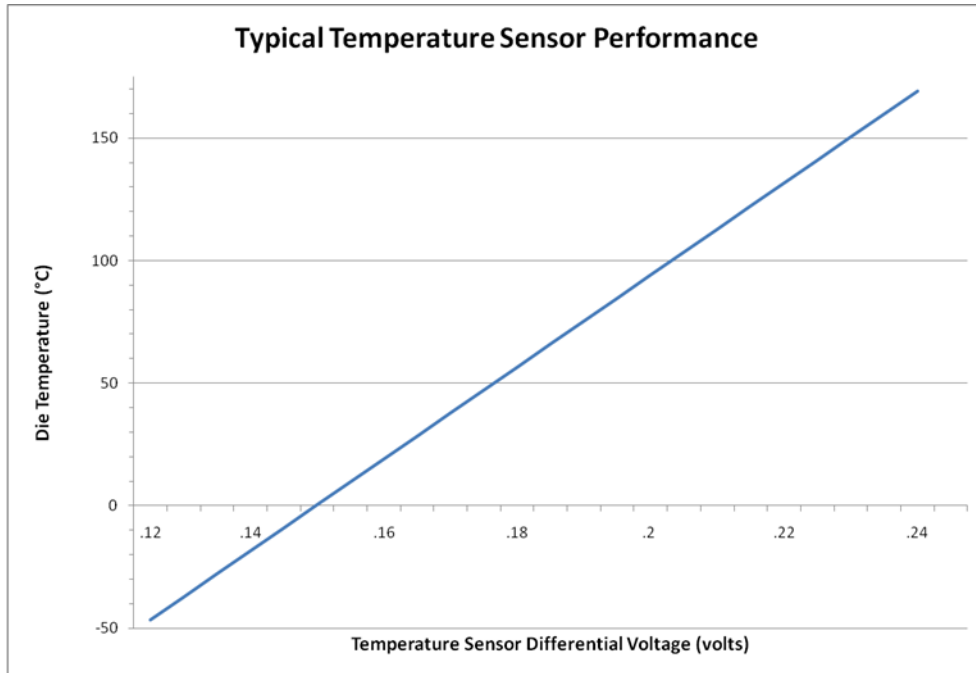
Figure 13. Typical slope of the temperature sensor of all 3 chips.
The derived equation can be used to calculate the on-chip temperature at the position of the sensor

The derived equation: Die Temp[°C]= ΔV_{TEMP} * 1875.0 - 280.94, with ΔV_{TEMP} the difference between the two sequential reading on the sense output, can be used to calculate the on-chip temperature. See 0x08 VCO sensor register.

8.3.1.2 Thermal resistance

Figure 14 shows electrical measurements done on the 2-channel transmitter chip mounted on a multi-layer FR4/RO3003 PCB mounted on a mechanical carrier, which is attached to an on-wafer chuck. Due to the test set-up the extracted thermal resistance is combination of the PCB to heatsink thermal resitance and the resistance of the RCP itself. Taking this into account, the thermal resistance of the RCP package itself is in the range of approx. 15 K/W.
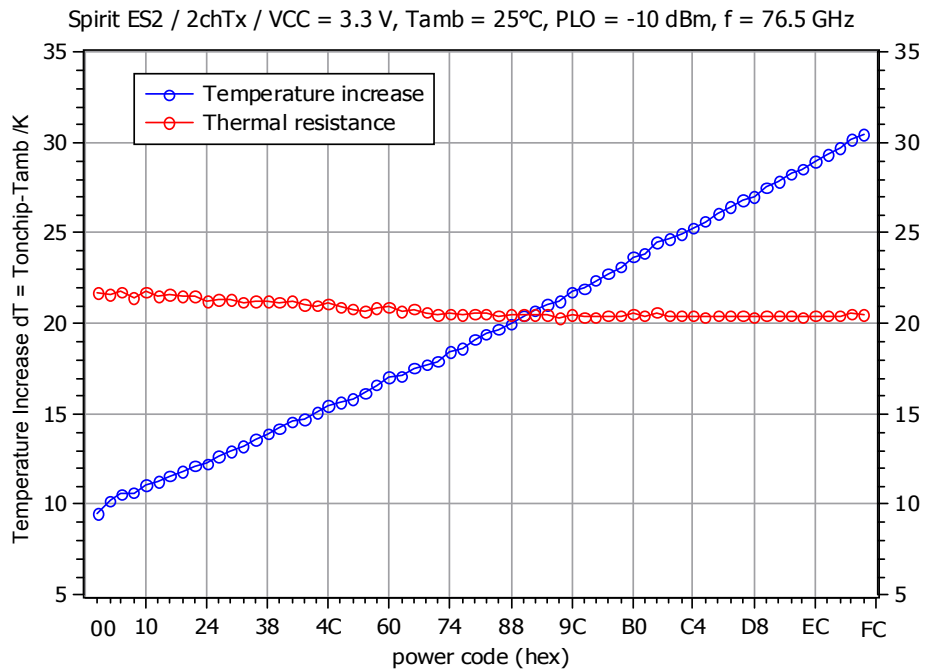
Figure 14. **Electrical measurements of the thermal resistance of the RCP including PCB (FR4/RO3003), mechanical carrier and attachment to the on-wafer chuck.**

8.3.2 Four-channel voltage controlled oscillator VCO

8.3.2.1 Tuning characteristics
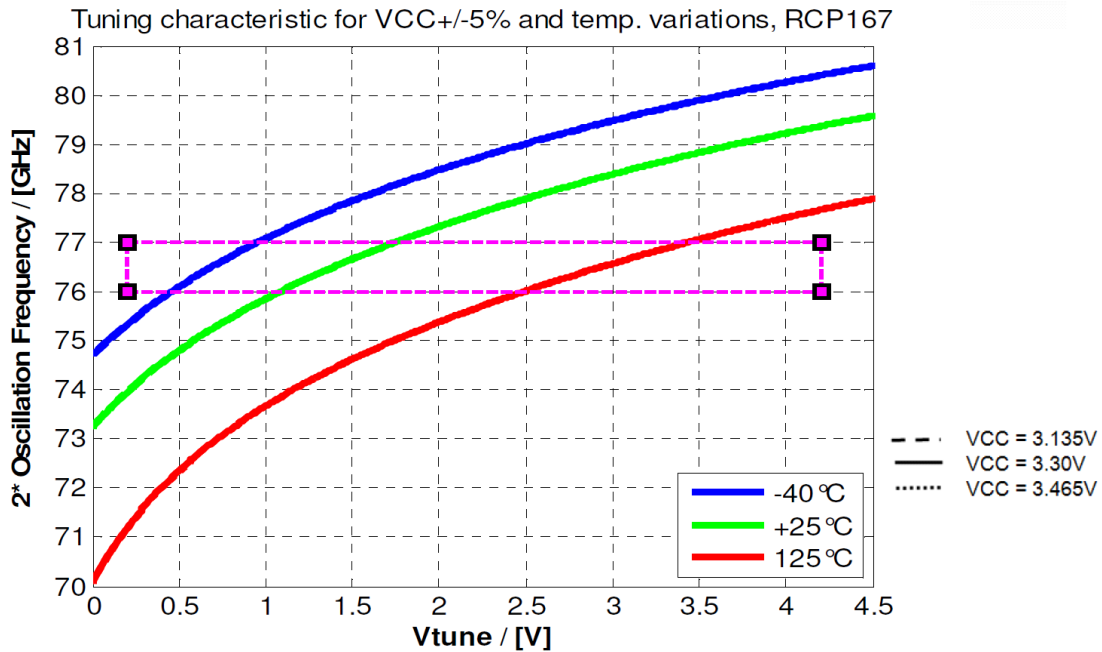
Figure 15. **Two time the oscillation frequency in dependence on the tuning voltage for different supply voltages and temperatures**

MR2001V

8.3.2.2   Tuning sensitivity
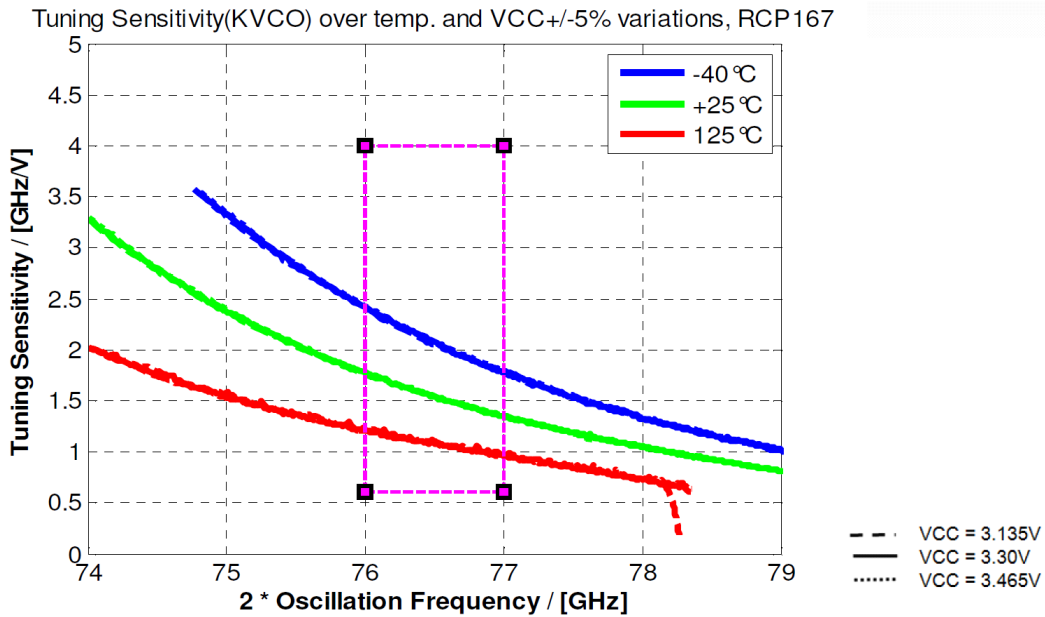
Figure 16. Tuning sensitivity in dependence on the oscillation frequency for different supply volatges and temperatures

8.3.2.3   Pushing
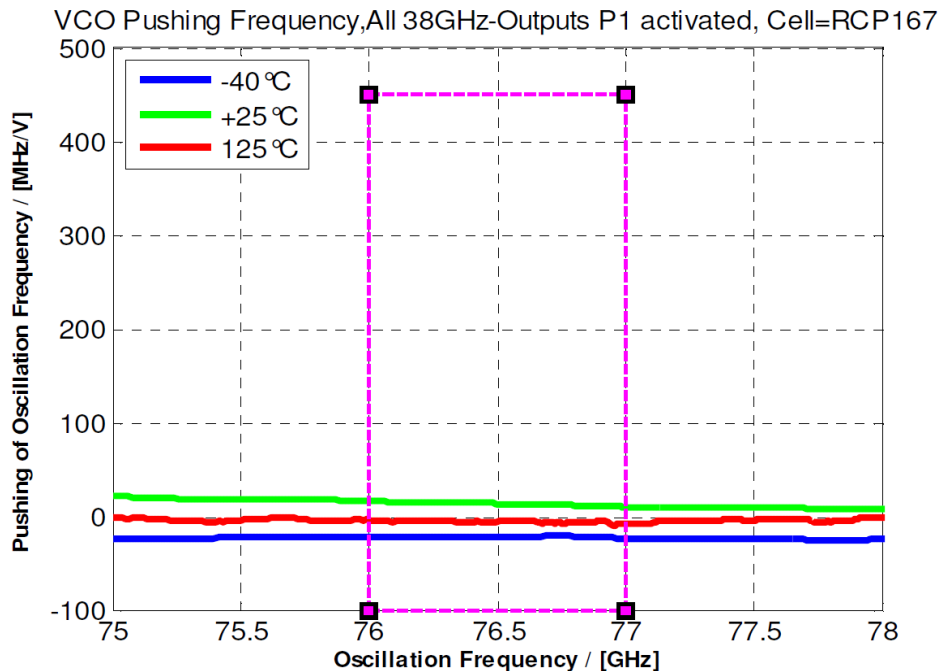
Figure 17. VCO pushing frequency in dependence on the oscillation frequency for different supply volatges and temperatures

8.3.2.4   Phase noise
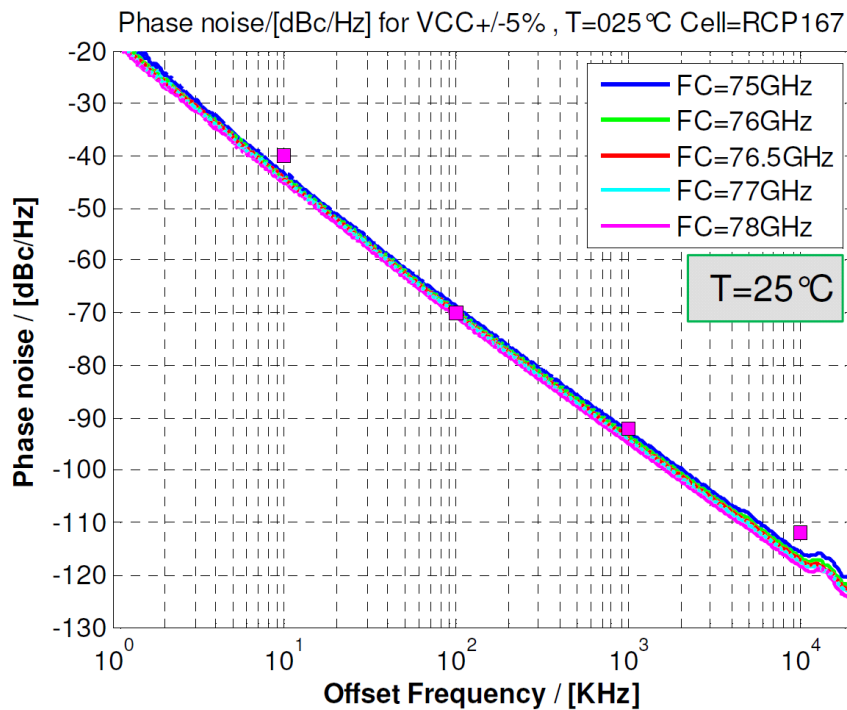
Figure 18. Phase noise in dependence on the offset frequency for different supply voltages and carrier frequencies

8.3.2.5   Output power
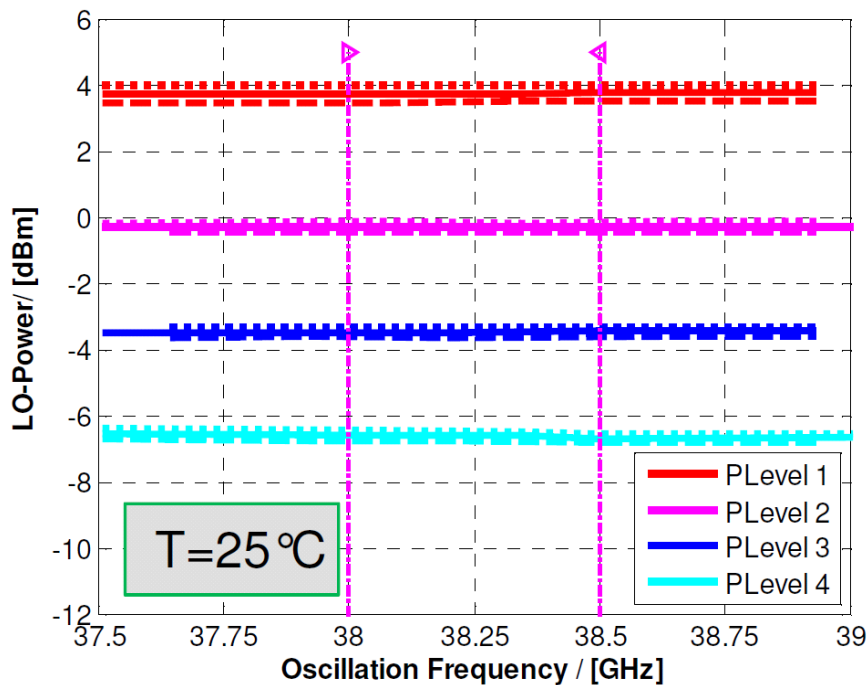
Figure 19. Output power in dependence on the osciallation frequency for four major power control settings

8.4 External components

8.4.1 Biasing

8.4.1.1 External blocking capacitors

To achieve defined specifications, the supply to the chip must be regarding spurious and noise level as good as possible. For this reason, typically external filters are added between the sensor supply domain and the on-chip supply domains. Figure 20 shows such a typical supply scheme. The blocking caps should be placed as close as possible to the package. This is dependent on application board material and manufacturer.
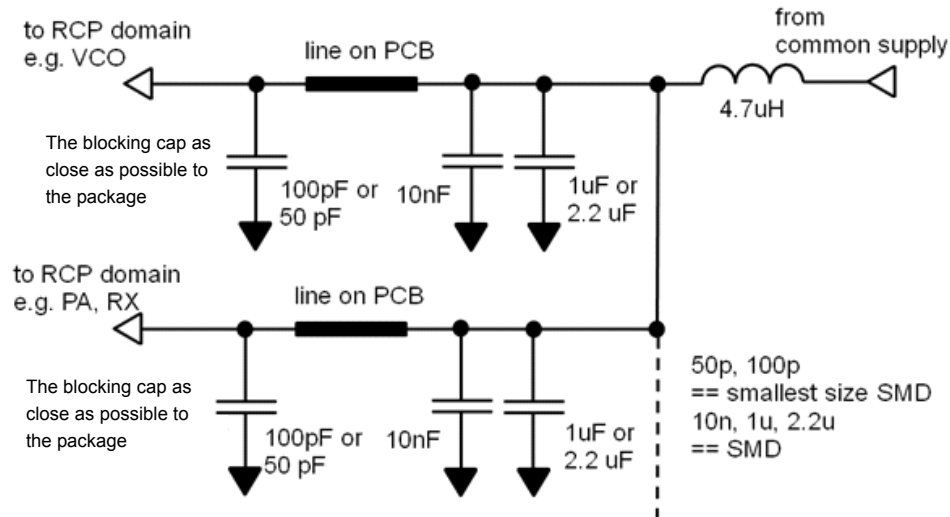
Figure 20. Typical arrangement and values of blocking capacitors to supply the chips

8.4.1.2 External biasing resistors

To operate the MR2001 chip-set, it is mandatory to connect each chip to two external resistors RN, RP, respectively. Without these two resistors the chips cannot be functional.
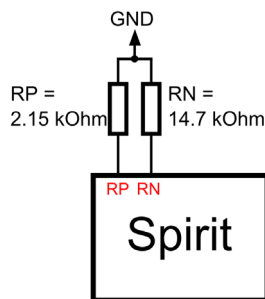
Figure 21. Required external resistors RN and RP for each individual MR2001chip

External resistors	Value	Recommendation
RP	2.15 kΩ	E96, ±1.0%, TK = ±100 ppm/K, SMD, 0402 or smaller, 50 μA current
RN	14.7 kΩ	E96, ±1.0%, TK = ±100 ppm/K, SMD, 0402 or smaller, 50 μA current

The two external resistors are part of the on-chip bandgap references. Due to the lower tolerances of the external resistors (±1.0% compared to on-chip ±10%) the supply current variation from package to package is drastically reduced.

MR2001V

8.4.2   Sense outputs

8.4.2.1   Tri-state sense outputs

The MR2001 chip-set provides tri-state sensing output signal which allows simplified wiring and signaling. All sense signals can be connected together to share the same hardwired signal line.
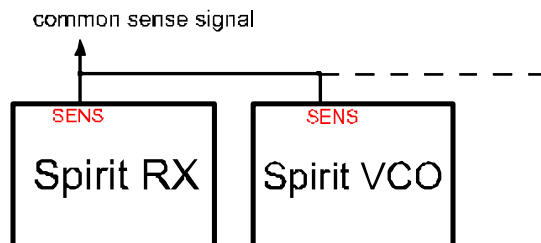
Figure 22. Block diagram and the relevant pin signals

9 Packaging

9.1 Package Mechanical Dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 14. Packaging information

Package	Suffix	Package outline drawing number
6.0 x 6.0 mm RCP, (10 x 11 array) 0.5 mm pitch	VK	98ASA00542D
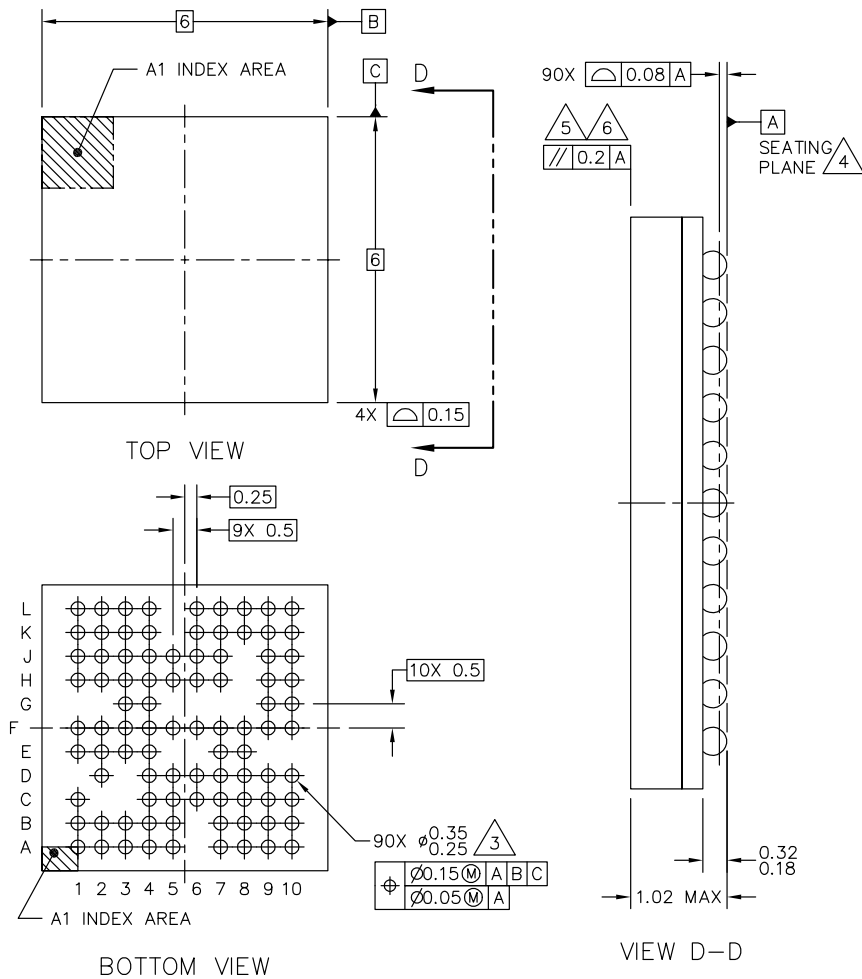
© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: RCPBGA, 6 X 6 X 0.95 PKG, 0.5 MM PITCH, 90 I/O	DOCUMENT NO: 98ASA00542D REV: B	
	STANDARD: JEDEC MO—275 AACE—2	
	SOT1685—1 13 JAN 2016	

MR2001V

9.2 PCB and RCP environment

9.2.1 NXP test board

9.2.1.1 RO3003 on FR4

For the NXP test boards a multi-layer PCB composed of 127 μm thick Rogers 3003 on top of standard FR4 core is used. The manufacturer for these boards is Elekonta/Marek (http://www.elekonta.de/).
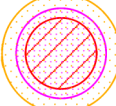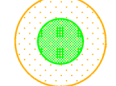
Layer		LSL gal. Cu	Max. Values
1	18μm	Sig/VL	15
	0,13 RO3003		130
2	18μm	Sig/VL	15
	-------- Prepreg R1566		55
	-------- Prepreg R1566		55
3	35μm	Sig/VL	33
	0,2 Core R1566		200
4	35μm	Sig/VL	33
	-------- Prepreg R1566		55
	-------- Prepreg R1566		55
5	Folie 18μm	Sig/VL gal. Cu	15
		LSL	
			661

Figure 23. RO3003 on Top of a FR4 core

9.2.1.2 Layout rules

The Figure 24 shows the solder ball arrangement including thermal and rf vias of typical PCB. Solder ball locations are shown in magenta with a label in blue, thermal via's have a wider diameter and are also shown in magenta without any blue label, important gnd via's to achieve rf perfromance are shown in green. Thermal vias are located in the area where no solder ball is available, so that they can occupay the full area of a solder ball.

Type	Shape	Geometry
solder ball	ADR0	~∅ 300 um
thermal via		> ∅ 200 um, thru PCB (non filled, or filled)
gnd via for rf performance		∅ 200 um (non filled, or filled)
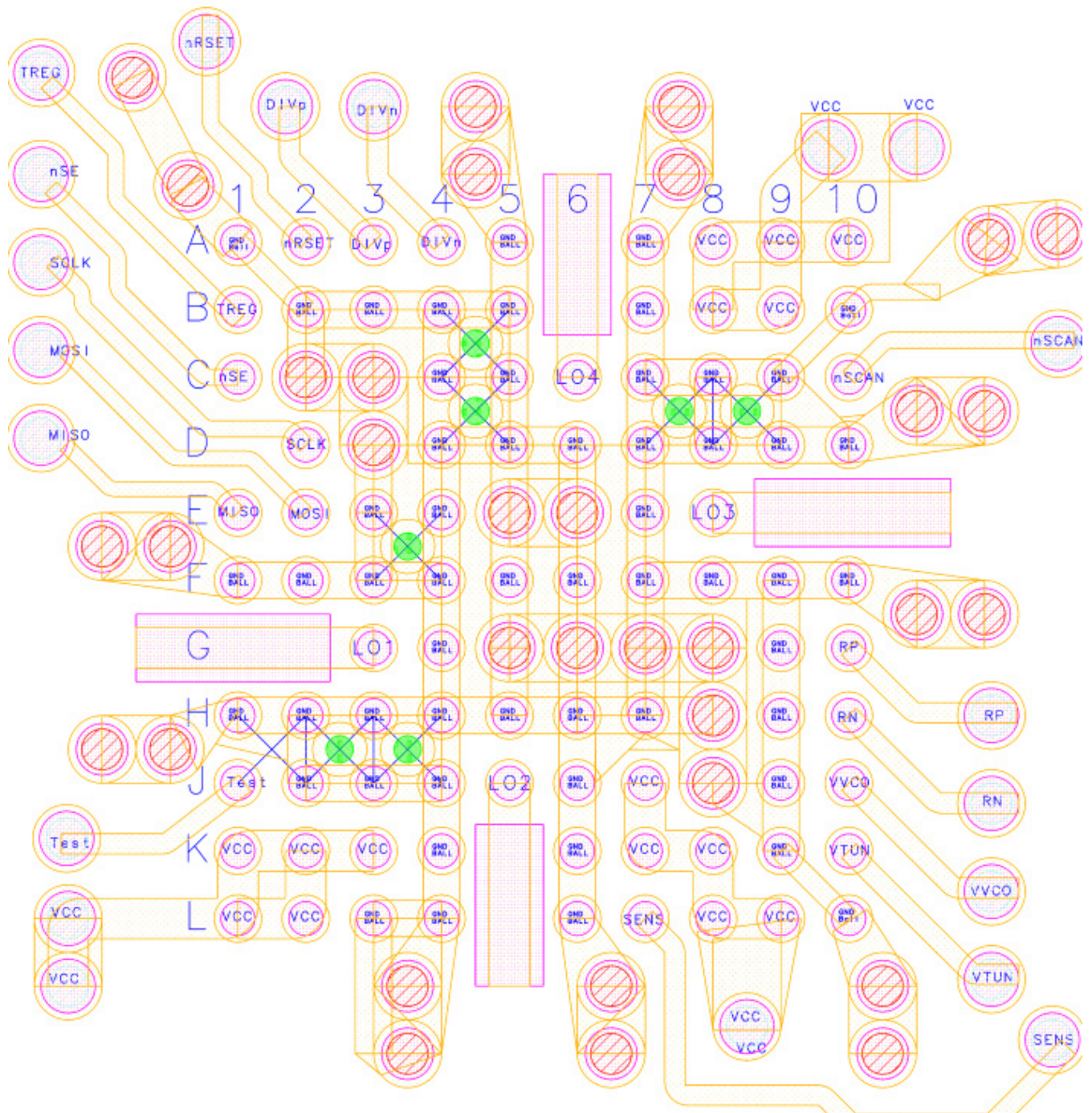
Figure 24. Top view of the VCO solder ball arrangement (magenta with blue label) including gnd vias (green, 200 um) to obtain rf-performance and thermal vias (> 200 um) to guarantee temperature range

The layout of the RCPs and the solder ball arrangement have been already done to allow space for thermal vias in the area where no solder balls are placed. It is recommended that this area is fully filled with thermal vias to lower the thermal resisstance.

9.2.1.3 Single-ended RF connection at 38 GHz (PCB microstip lines)

For 38 GHz input and output signals no special matching structure on the PCB is required. A standard 50 Ω microstrip transmission line directly connected to the solder ball is fully sufficient.
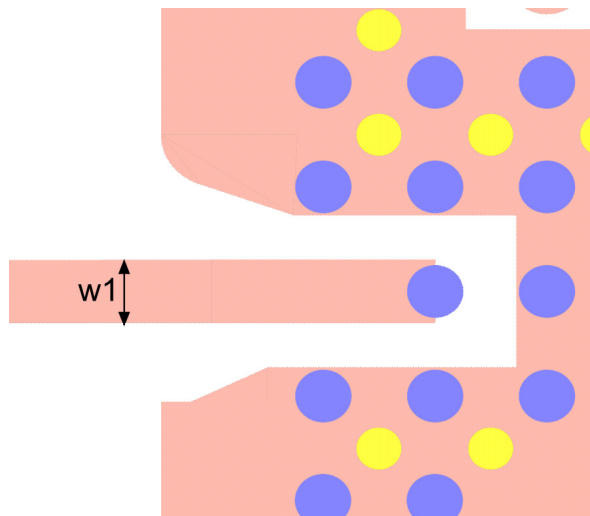
Figure 25. Example for the RF Connection of a 38 GHz Input and Output Signal. Shown in the picture is the LO input of the receiver chip

9.3 Assembly conditions

The following are basic recommendations for the NXP RCP aseembly:
- Avoid non solder mask defined (NSMD) defined pads
- Pad size 280 µm minimum
- Solder mask defined board pad
- Solder mask opening 200 µm minimum
- Stencil thickness 100 µm
- Solder paste opening 200 µm
- Lead-free solder paste (SAC405)
- ±35 µm placement of component
- Reflow following paste supplier suggested temperatures, or…
- Reflow peak is 260 °C, time above liquidus (217 °C) for 60 to 120 seconds

Figure 26. Solder mask (SMD) and non-solder mask defined (NSMD) pads

The typical reflow profile for the chip-set is shown in .
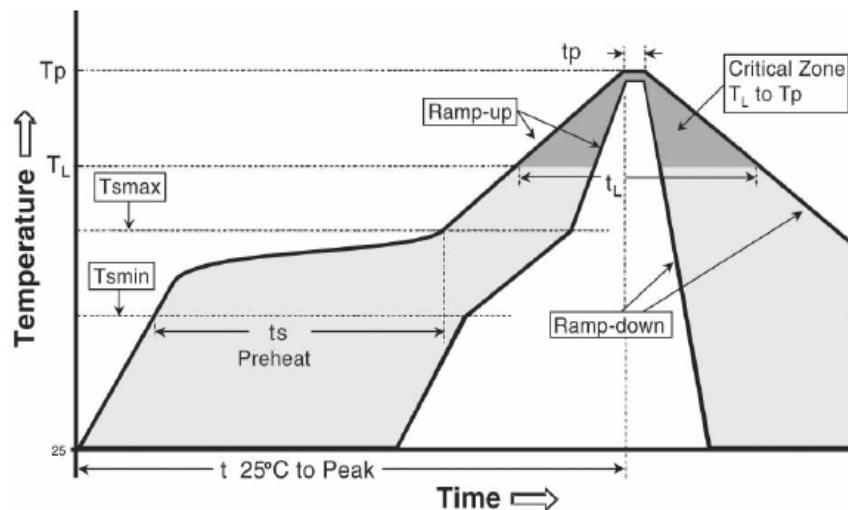
Figure 27. Typical MR2001 reflow profile

Profile parameter	
Average ramp-up rate(TSmax to Tp)	3.0 °C/second max.

Pre-heat
  • Temperature Min. (TSmin)
  • Temperature Max. (TSmax)
  • Time (TSmin to TSmax) (ts)
	150 °C
	200 °C
	60 – 120 seconds

Time maintained above:
  • Temperature (TL)
  • Time (tL)
	217 °C
	60-150 seconds

Peak Temperature (Tp)	260 °C
Time within 5.0 °C of actual Peak Temperature (tp)	10 – 30 seconds
Ramp-down Rate	6.0 °C/second max.
Time 25 °C to Peak Temperature	8 minutes max.

Notes
  7. Reflow profile as per IPC/JEDEC J-STD-020D.1

10   Revision history

Revision	Date	Description of changes
1.0	11/2014	• Initial release
2.0	12/2014	• Made typographic corrections to bring the document into compliance.
3.0	2/2015	• Impulse response stabilization, from 2.0 MHz to 250 kHz • Clarification on SPI interface
4.0	11/2015	• Updated reflow profile table as per IPC/JEDEC J-STD-020D.1
5.0	8/2016	• Updated to NXP document form and style • Removed RF test concept • Corrected SPI access to temperature sensor and temperature sensor graph, and parameters on reflow profile

Document Number: MC33MR2001V
Rev. 5.0
8/2016