Implementing an 8 bit Eprom for an MC68EC040/MC68360 System

By Gordon Lawton & Ray Cornyn
Motorola, East Kilbride, Scotland

The MC68360 has a mode whereby the internal CPU32+ core may by disabled allowing another external processor to use the QUICC's peripherals. The QUICC has dedicated features for providing a glueless interface to an external MC68EC040 (or other M68040 family member), called MC68040 companion mode. The following Design Concept outlines a method whereby a MC68EC040/360 system may be booted from a single 8-bit Eprom. It is assumed that the reader is familiar with both the MC68EC040 and the MC68360 nomenclature.

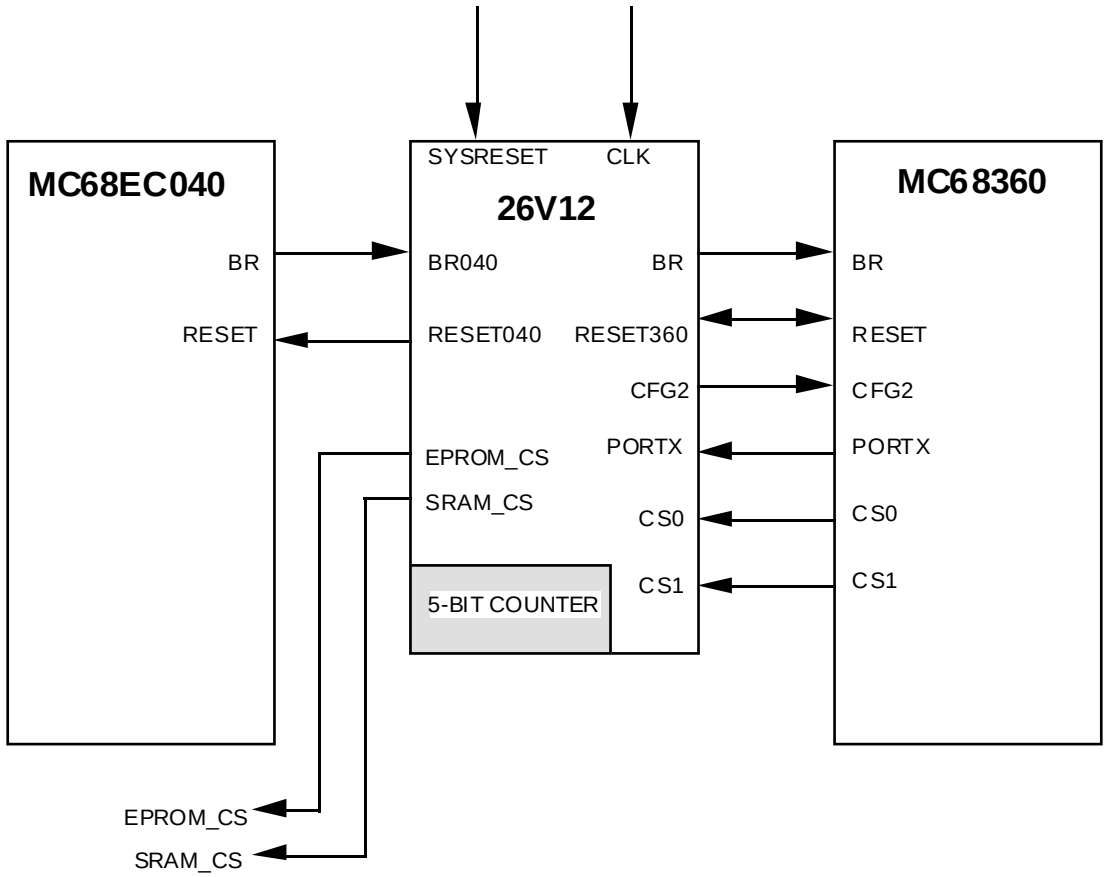

Figure 1. Block Diagram for 360/040 8-Bit Boot Eprom

System Overview

In many embedded designs it is desirable to have an 8-bit boot Eprom to hold the application code. This saves on both cost and board space. Unfortunately the MC68EC040 does not directly support dynamic bus sizing, and without external hardware requires code to be held in 32-bit wide memory. There are several solutions to this problem, including using an external dynamic bus sizer, such as the MC68150, or implementing this functionality in discrete logic. The main drawbacks with such schemes are cost for the former and

component count for the later. The following scheme uses the MC68360's CPU Configuration logic and IDMA capablity to enable a MC68EC040/360 system to boot from 8-bit memory using only one PAL. A suitable device for this is the 26V12.

The proposed solution is illustrated in Figure 1. On reset the system is initially configured with the MC68360 in CPU enabled mode and the MC68EC040 held in reset. This is controlled by a simple state machine in the PAL. The MC68360 boots from an 8-bit EPROM, which also holds the MC68040 application code. This is then copied using the IDMA from the 8-bit EPROM to 32-bit wide SRAM. Once the IDMA transfer is complete the system is reset again, this time with the MC68360 in companion mode allowing the MC68EC040 to boot from the 32-bit SRAM.

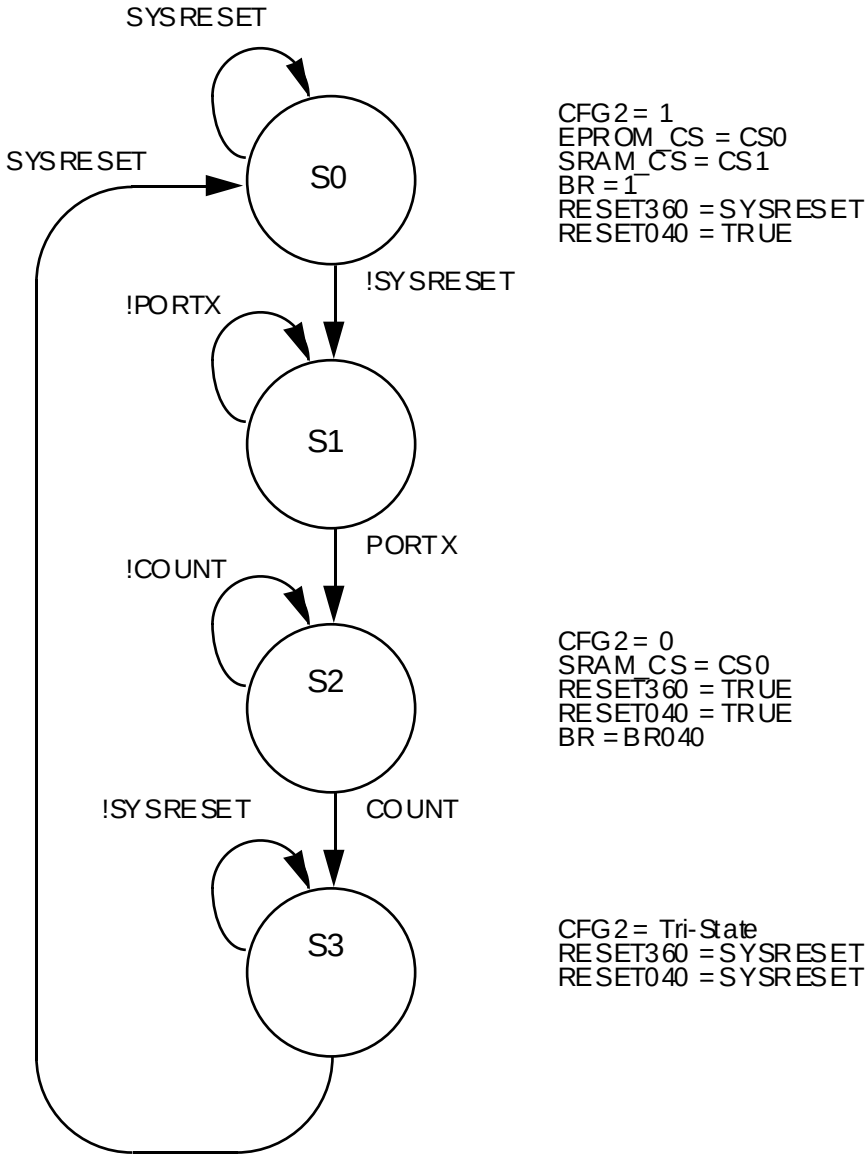

Figure 2. Reset State Machine for 360/040 8-Bit Boot Eprom

The PAL used to contol the reset operation and is used to implement the state machine in Figure 2. When using a 26V12 two bits are required to implement the state machine, 5-bits for the reset counter and the remaining 5 outputs used for; EPROM_CS, SRAM_CS, RESET040, RESET360 and CFG2. Note that care should be taken to facilate alternative reset sources if required, for example if the system is required to reset after a Double Bus Fault.

Reset State Machine Operation

At system reset, the PAL state machine in Figure 2 is held in state S0. The System Reset line SYSRESET is used to reset both the 040 and the QUICC. The QUICC is configured in CPU enabled mode with CS0 routed to the EPROM and CS1 routed to the SRAM. When Bus Request (BR) is asserted by the 040 it is not fed directly to the 040, instead it is fed through the PAL to the 360. This means the Bus Grant (BG) signal it is not asserted to the 040, therefore it shall remain in tri-state.

When SYSRESET negates then the state machine switches to state S1. At this point the MC68360 copies the 040 boot code from the 8-bit EPROM to the 32-bit SRAM. The most efficient method for this is to configure the MC68360's IDMA to transfer a 8-bit wide block in the EPROM to a 32-bit wide block in the SRAM. Consult the MC68360 User's Manual from more information on configuring the IDMA.

When the transfer is complete the MC68360 asserts a port line, causing the state machine to switch to state S2. In S2 RESETH is asserted to the MC68360, but this time it is configured in companion mode with CS1 routed to the EPROM and CS0 routed to the SRAM. A count is required so that the MC68360 RESETH is asserted for the minimum 32 clock cycles and the MC68EC040 RESET is asserted for 10 clocks. This is implemented as a 5-bit counter within the PAL.

Once the count is complete state S3 is entered. During this state both the MC68360 and the MC68EC040 will assert their respective reset lines. When the QUICC is completely reset it shall assert BG to the 040, thus enabling it to boot from the 32-bit wide SRAM. The state machine remains in this state until another system reset occurs.