SEMICONDUCTOR
TECHNICAL DATA

MC68HC05C9

Addendum to
MC68HC05C9
HCMOS Microcontroller Unit
Technical Data

This addendum provides the following information:

- **CORRECTIONS/ADDITIONS** to the *MC68HC05C9 Technical Data* (Motorola document number MC68HC05C9/D);
- **SECTION 15 ORDERING INFORMATION** (replacement);
- **APPENDIX A**, containing data for the erasable, programmable, read-only memory (EPROM) version of the MC68HC05C9, the MC68HC705C9.

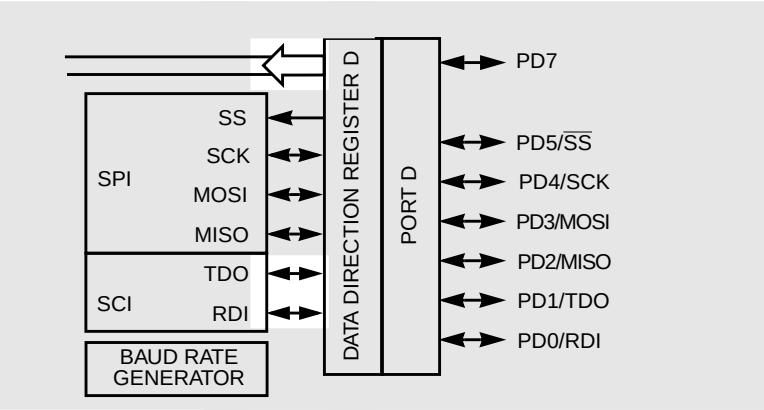
Intentionally left blank

Corrections/Additions
MC68HC05C9/D

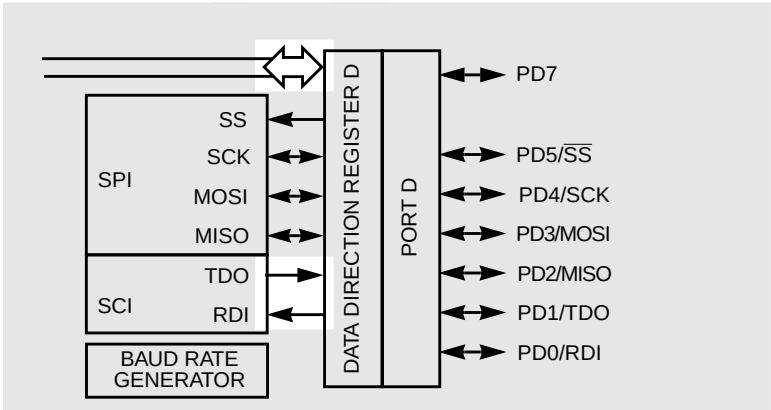
Corrections and/or additions to *MC68HC05C9 Technical Data* are as follows:

Page 1-3, **Figure 1-2. MC68HC05C9 Block Diagram**, correct Port D as follows:

From:



To:



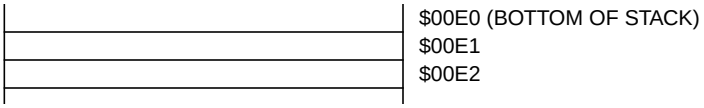
Page 3-3, **3.1.3 Stack Pointer**, from the second paragraph, correct as follows:

From: If subroutines and interrupts use more than 64 stack locations, the stack pointer wraps around to address $00C0 and begins writing over the previously stored data.

To: If subroutines and interrupts use more than 64 stack locations, the stack pointer wraps around to address $00FF and begins writing over the previously stored data.

Page 4-5, **Figure 4-2. Interrupt Stacking Order**, correct as follows:

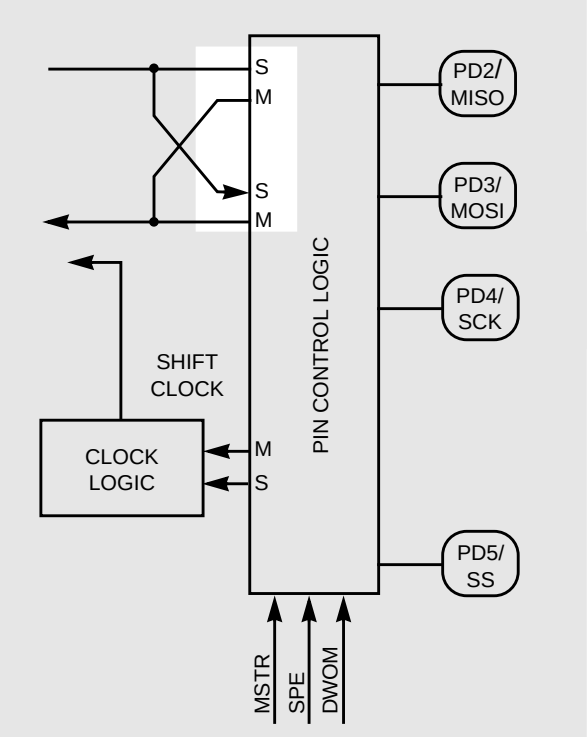
From:



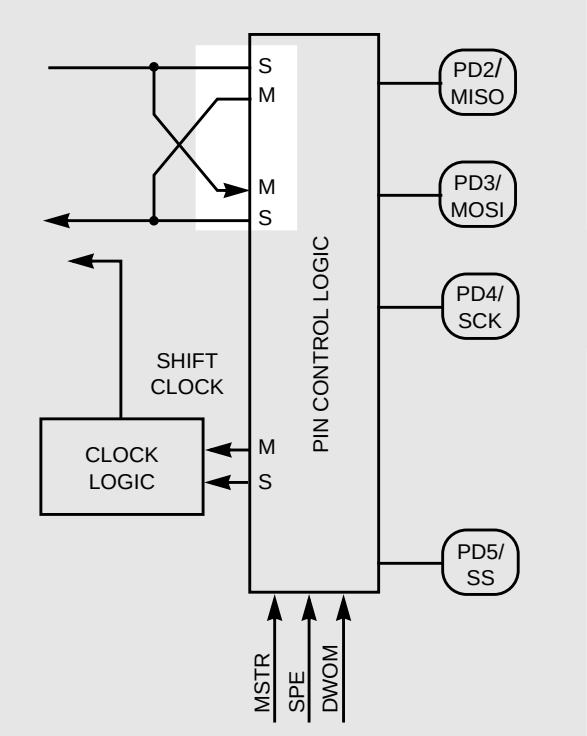
To:

Page 10-2, **Figure 10-1. SPI Block Diagram**, correct as follows:

From:

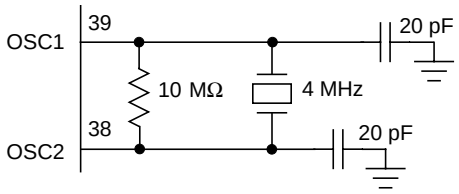


To:

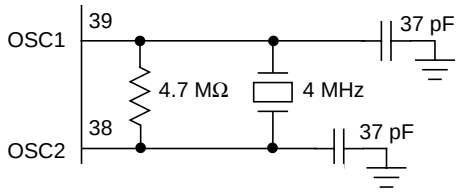


Page 11-2, **Figure 11-1. Self-Check Circuit Schematic**, correct as follows:

From:



To:



Page 12-9, **Table 12-7. Register/Memory Instructions**, add the following instruction:

EXCLUSIVE OR Accumulator with Memory Byte	EOR

Page 12-10, **12.2.2. Read-Modify-Write Instructions**, add the following paragraph below the bulleted items:

For BSET and BCLR instructions, only direct addressing is valid. Also, because BSET and BCLR are read-modify-write instructions, they cannot be used with write-only registers. A read-modify-write operation will read undefined data, modify it as appropriate, and then write it back to the register. But because the original data is undefined, the data written back will be undefined.

Page 12-10, **Table 12-8. Read-Modify-Write Instructions**, add the following instructions:

Clear Bit in Memory	BCLR
Set Bit in Memory	BSET

Page 12-12, **Table 12-11. Control Instructions**, correct as follows:

From:

Return from Subroutine	RTI

To:

Return from Interrupt	RTI
Return from Subroutine	RTS

Page 12-18, **Table 12-13. Opcode Map**, correct as follows (unshaded areas show corrections):

Bit Manipulation **Read-Modify-Write**

	From: DIR	To: DIR	From: DIR	To: DIR	From: IX1	To: IX1	From: IX	To: IX
HI	1	1	3	3	6	6	7	7
LO	0001	0001	0011	0011	0110	0110	0111	0111
0 0000	BSET0 5 2 DIR	BSET0 5 2 DIR	NEG 5 2 DIR	NEG 5 2 DIR	NEG 6 2 IX1	NEG 6 2 IX1	NEG 5 1 IX	NEG 5 1 IX
1 0001	BCLR0 5 2 DIR	BCLR0 5 2 DIR						
2 0010	BSET1 5 2 DIR	BSET1 5 2 DIR						
3 0011	BSCLR1 5 2 DIR	BCLR1 5 2 DIR	COM 5 2 DIR	COM 5 2 DIR	COM 6 2 IX1	COM 6 2 IX1	COM 5 1 IX	COM 5 1 IX
4 0100	BSET2 5 2 DIR	BSET2 5 2 DIR	LSR 5 2 DIR	LSR 5 2 DIR	LSR 6 2 IX1	LSR 6 2 IX1	LSR 5 1 IX	LSR 5 1 IX
5 0101	BCLR2 5 2 DIR	BCLR2 5 2 DIR						
6 0110	BSET3 5 2 DIR	BSET3 5 2 DIR	ROR 5 2 DIR	ROR 5 2 DIR	ROR 6 2 IX1	ROR 6 2 IX1	ROR 5 1 IX	ROR 5 1 IX
7 0111	BCLR3 5 2 DIR	BCLR3 5 2 DIR	ASR 5 2 DIR	ASR 5 2 DIR	ASR 6 2 IX1	ASR 6 2 IX1	ASR 5 1 IX	ASR 5 1 IX
8 1000	BSET4 5 2 DIR	BSET4 5 2 DIR	LSL 5 2 DIR	ASL/LSL 5 2 DIR	LSL 6 2 IX1	ASL/LSL 6 2 IX1	LSL 5 1 IX	ASL/LSL 5 1 IX
9 1001	BCLR4 5 2 DIR	BCLR4 5 2 DIR	ROL 5 2 DIR	ROL 6 2 DIR	ROL 6	ROL 6 2 IX1	ROL 5 1 IX	ROL 5 1 IX
A 1010	BSET5 5 2 DIR	BSET5 5 2 DIR	DEC 5 2 DIR	DEC 6 2 DIR	DEC 6	DEC 6 2 IX1	DEC 5 1 IX	DEC 5 1 IX
B 1011	BCLR5 5 2 DIR	BCLR5 5 2 DIR						
C 1100	BSET6 5 2 DIR	BSET6 5 2 DIR	INC 5 2 DIR	INC 5 2 DIR	INC 6 2 INH	INC 6 2 IX1	INC 5 1 IX	INC 5 1 IX
D 1101	BCLR6 5 2 DIR	BCLR6 5 2 DIR	TST 4 2 DIR	TST 4 2 DIR	TST 6 2 INH	TST 5 2 IX1	TST 4 1 IX	TST 4 1 IX
E 1110	BSET7 5 2 DIR	BSET7 5 2 DIR						
F 1111	BCLR7 5 2 DIR	BCLR7 5 2 DIR	CLR 5 2 DIR	CLR 5 2 DIR	CLR 6 2 INH	CLR 6 2 IX1	CLR 5 1 IX	CLR 5 1 IX

Page 13-10, **Table 13-6. Serial Peripheral Interface Timing (5.0 Vdc),** correct reference at top of table as follows:

From: V_{DD} = 5.0 Vdc ± 10%; V_{SS} = 0 Vdc
(Refer to Figures 13-11 and 13-12.)

To: V_{DD} = 5.0 Vdc ± 10%; V_{SS} = 0 Vdc
(Refer to Figures 13-9 and 13-10.)

Page 13-10, **Table 13-6. Serial Peripheral Interface Timing (5.0 Vdc)**, correct the SPI fall time as follows:

From:

13	Fall Time (20% V_{DD} to 20% V_{DD}, C_L = 200 pF)				

To:

13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF)				

Page 13-11, **Table 13-7. Serial Peripheral Interface Timing (3.3 Vdc)**, correct reference at top of table as follows:

From: V_{DD} = 3.3 Vdc ± 10%; V_{SS} = 0 Vdc
(Refer to Figures 13-11 and 13-12.)

To: V_{DD} = 3.3 Vdc ± 0.3 Vdc; V_{SS} = 0 Vdc
(Refer to Figures 13-9 and 13-10.)

Page 13-11, **Table 13-7. Serial Peripheral Interface Timing (3.3 Vdc)**, correct the SPI fall time as follows:

From:

13	Fall Time (20% V_{DD} to 20% V_{DD}, C_L = 200 pF)				

To:

13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF)				

Page 13-12, a footnote has been added to **Figure 13-9. SPI Master Timing Diagram** figure title as follows:

From: **Figure 13-9. SPI Master Timing Diagram**

To: **Figure 13-9. SPI Master Timing Diagram***

* Refer to **Table 13-6. Serial Peripheral Interface Timing (5.0 Vdc)** and **Table 13-7. Serial Peripheral Interface Timing (3.3 Vdc)** for the timing values corresponding to the circled numbers in the figure above.

Page 13-13, a footnote has been added to **Figure 13-10. SPI Master Timing Diagram** figure title as follows:

From: **Figure 13-10. SPI Master Timing Diagram**

To: **Figure 13-10. SPI Master Timing Diagram***

* Refer to **Table 13-6. Serial Peripheral Interface Timing (5.0 Vdc)** and **Table 13-7. Serial Peripheral Interface Timing (3.3 Vdc)** for the timing values corresponding to the circled numbers in the figure above.

SECTION 15
ORDERING INFORMATION

This section contains instructions for ordering custom-masked ROM MCUs.

15.1 MCU Ordering Forms

To initiate an order for a ROM-based MCU, first obtain the current ordering form for the MCU from a Motorola representative. Submit the following items when ordering MCUs:

- A current MCU ordering form that is **completely filled out** (Contact your Motorola sales office for assistance.)
- A copy of the customer specification if the customer specification deviates from the Motorola specification for the MCU
- Customer's application program on one of the media listed in **15.2 Application Program Media.**

The current MCU ordering form is also available through the Motorola Freeware Bulletin Board Service (BBS). The telephone number is (512) 891-FREE. After making the connection, type bbs in lowercase letters. Then press the return key to start the BBS software.

15.2 Application Program Media

Please deliver the application program to Motorola in one of the following media:

- Macintosh®[1] 3-1/2-inch diskette (double-sided 800K or double-sided high-density 1.4M)
- MS-DOS®[2] or PC-DOS™[3] 3-1/2-inch diskette (double-sided 720K or double-sided high-density 1.44M)
- MS-DOS® or PC-DOS™ 5-1/4-inch diskette (double-sided double-density 360K or double-sided high-density 1.2M)

Use positive logic for data and addresses.

1. Macintosh is a registered trademark of Apple Computer, Inc.
2. MS-DOS is a registered trademark of Microsoft Corporation.
3. PC-DOS is a trademark of International Business Machines Corporation.

When submitting the application program on a diskette, clearly label the diskette with the following information:

- Customer name
- Customer part number
- Project or product name
- File name of object code
- Date
- Name of operating system that formatted diskette
- Formatted capacity of diskette

On diskettes, the application program must be in Motorola's S-record format (S1 and S9 records), a character-based object file format generated by M6805 cross assemblers and linkers.

NOTE

Begin the application program at the first user ROM location. Program addresses must correspond exactly to the available on-chip user ROM addresses as shown in the memory map. **Write $00 in all non-user ROM locations or leave all non-user ROM locations blank**. Refer to the current MCU ordering form for additional requirements. Motorola may request pattern re-submission if non-user areas contain any non-zero code.

If the memory map has two user ROM areas with the same addresses, then write the two areas in separate files on the diskette. Label the diskette with both filenames.

In addition to the object code, a file containing the source code can be included. Motorola keeps this code confidential and uses it only to expedite ROM pattern generation in case of any difficulty with the object code. Label the diskette with the filename of the source code.

15.3 ROM Program Verification

The primary use for the on-chip ROM is to hold the customer's application program. The customer develops and debugs the application program and then submits the MCU order along with the application program.

Motorola inputs the customer's application program code into a computer program that generates a listing verify file. The listing verify file represents the memory map of the MCU. The listing verify file contains the user ROM code and may also contain non-user ROM code, such as self-check code. Motorola sends the customer a computer printout of the listing verify file along with a listing verify form.

To aid the customer in checking the listing verify file, Motorola will program the listing verify file into customer-supplied blank preformatted Macintosh or DOS disks. All original pattern media are filed for contractual purposes and are not returned.

Check the listing verify file thoroughly, then complete and sign the listing verify form and return the listing verify form to Motorola. The signed listing verify form constitutes the contractual agreement for the creation of the custom mask.

15.4 ROM Verification Units (RVUs)

After receiving the signed listing verify form, Motorola manufactures a custom photographic mask. The mask contains the customer's application program and is used to process silicon wafers. The application program cannot be changed after the manufacture of the mask begins. Motorola then produces 10 MCUs, called RVUs, and sends the RVUs to the customer. RVUs are usually packaged in unmarked ceramic and tested to 5 Vdc at room temperature. RVUs are not tested to environmental extremes because their sole purpose is to demonstrate that the customer's user ROM pattern was properly implemented. The 10 RVUs are free of charge with the minimum order quantity. These units are not to be used for qualification or production. RVUs are not guaranteed by Motorola Quality Assurance.

15.5 MCU Order Numbers

Table 15-1 shows the MCU order numbers for the available package types.

Table 15-1. MCU Order Numbers

Package Type	Operating Temperature Range	MC Order Number
40-Pin Plastic Dual In-Line Package (PDIP)	0 °C to 70 °C –40 °C to 85 °C	MC68HC05C9P MC68HC05C9CP
44-Lead Plastic-Leaded Chip Carrier (PLCC)	0 °C to 70 °C –40 °C to 85 °C	MC68HC05C9FN MC68HC05C9CFN
44-Pin Quad Flat Pack (QFP)	0 °C to 70 °C –40 °C to 85 °C	MC68HC05C9FB MC68HC05C9CFB
42-Pin Shrink Dual In-Line Package (SDIP)	0 °C to 70 °C –40 °C to 85 °C	MC68HC05C9B MC68HC05C9CB

NOTES:
1. P = Plastic dual-in-line package (PDIP)
2. FN = Plastic-leaded chip carrier (PLCC)
3. C = Extended temperature range (–40 to +85 °C)
4. B = Shrink dual-in-line package (SDIP)
5. FB = Quad flat pack (QFP)

APPENDIX A
MC68HC705C9

Appendix A introduces the MC68HC705C9, an erasable, programmable, read-only memory (EPROM) version of the MC68HC05C9. The technical data in *MC68HC05C9 Technical Data* applies to the MC68HC705C9 with the exceptions given in this appendix.

A.1 GENERAL DESCRIPTION

A.1.1 Features

- 15,932 Bytes of Erasable, Programmable, Read-Only Memory (EPROM)
- 240 Bytes of Bootstrap ROM

A.1.2 Programmable Options

OR — Option Register **$3FDF**

	Bit 7	6	5	4	3	2	1	Bit 0
	RAM0	RAM1	0	0	0		IRQ	0
RESET:	0	0	0	0	0		0	0

= Unimplemented

Figure A-1. Option Register (OR)

A.1.3 Block Diagram

Figure A-2 shows the block diagram for the MC68HC705C9.

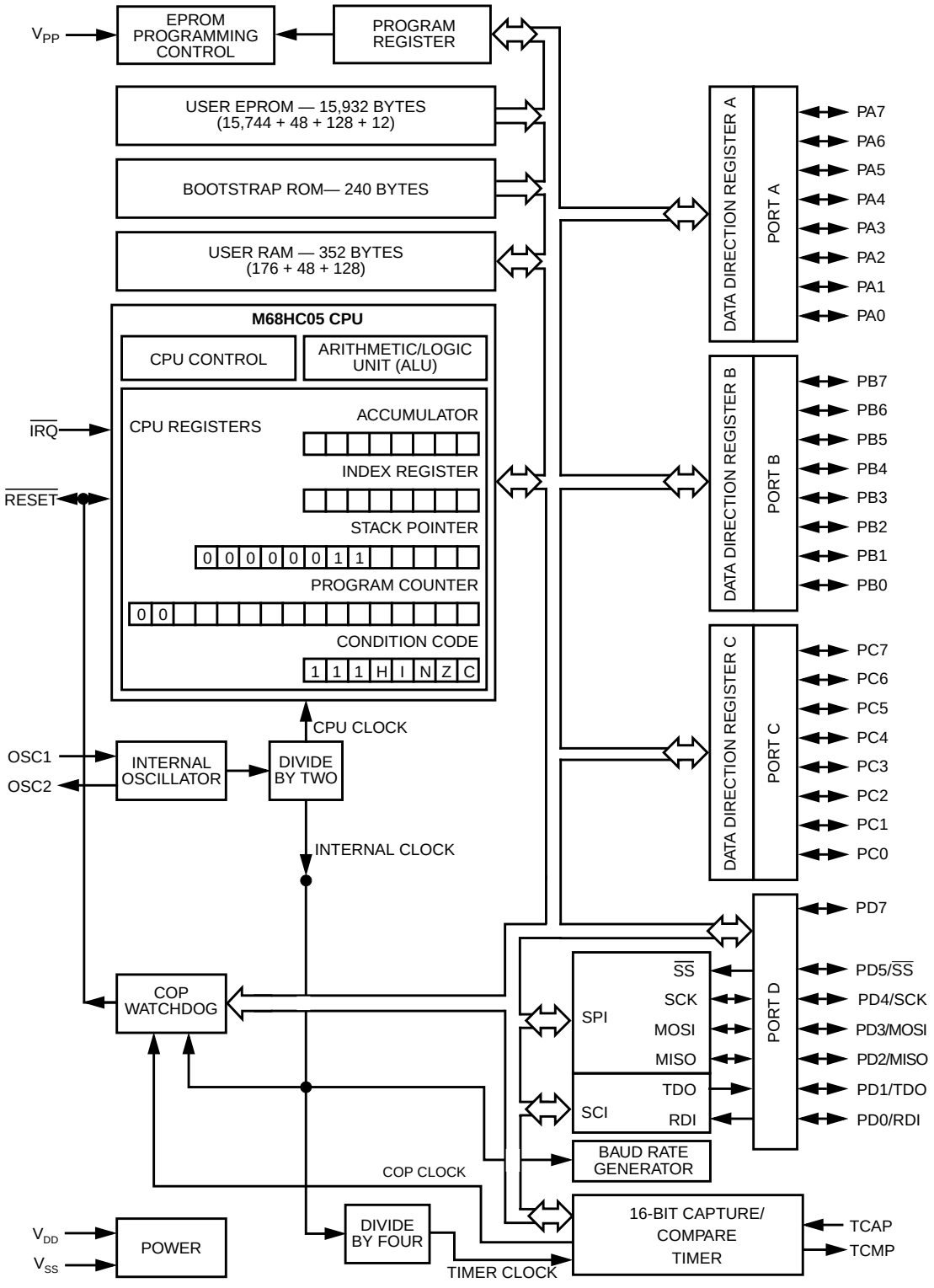


Figure A-2. MC68HC705C9 Block Diagram

A.1.4 Pin Assignments

The MC68HC705C9 is available in the plastic dual in-line package (PDIP) and plastic-leaded chip carrier (PLCC) packages. See **A.5 MECHANICAL SPECIFICATIONS**. Pin assignments are as follows:

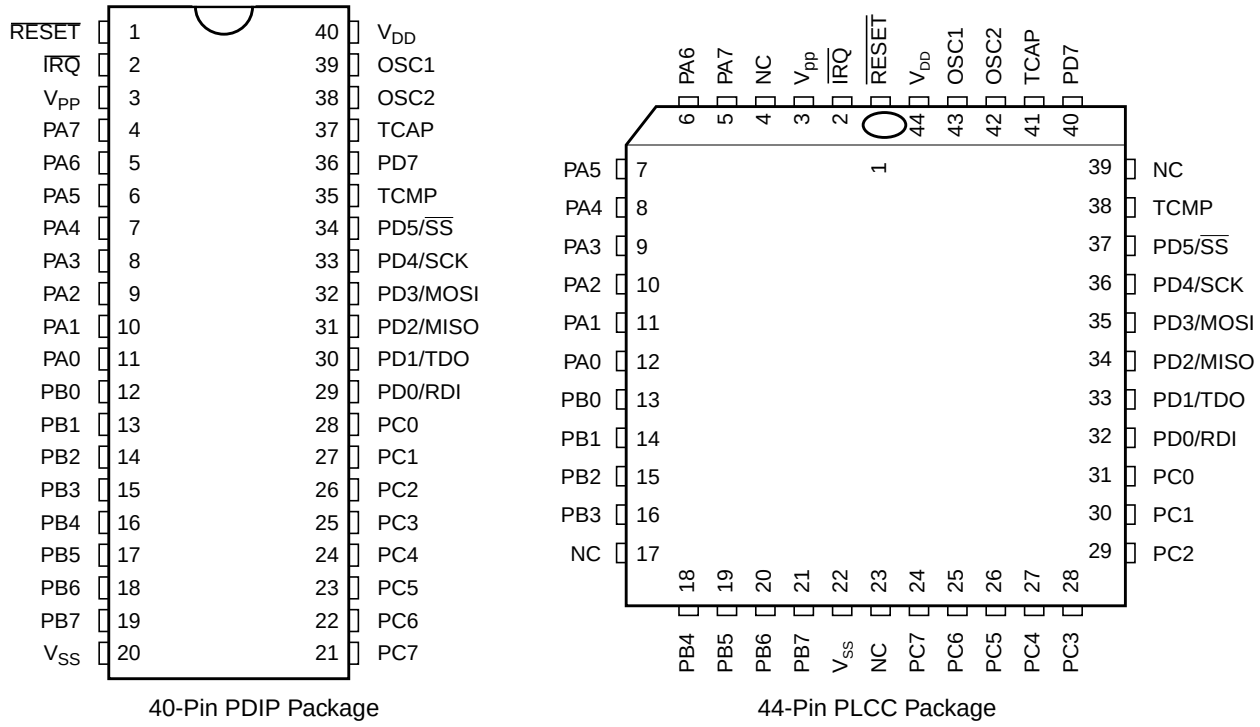


Figure A-3. MC68HC705C9 Pin Assignments

A.1.4.1 V_{PP}

Programming power is supplied to the EPROM through the V_{PP} pin. The nominal programming voltage is 15 volts. The voltage level on the V_{PP} pin (pin 3), shown in Figure A-3, should never fall below V_{DD}.

A.2 Memory

A.2.1 Memory Map and Registers

Figure A-4 is a memory map of the MC68HC705C9.

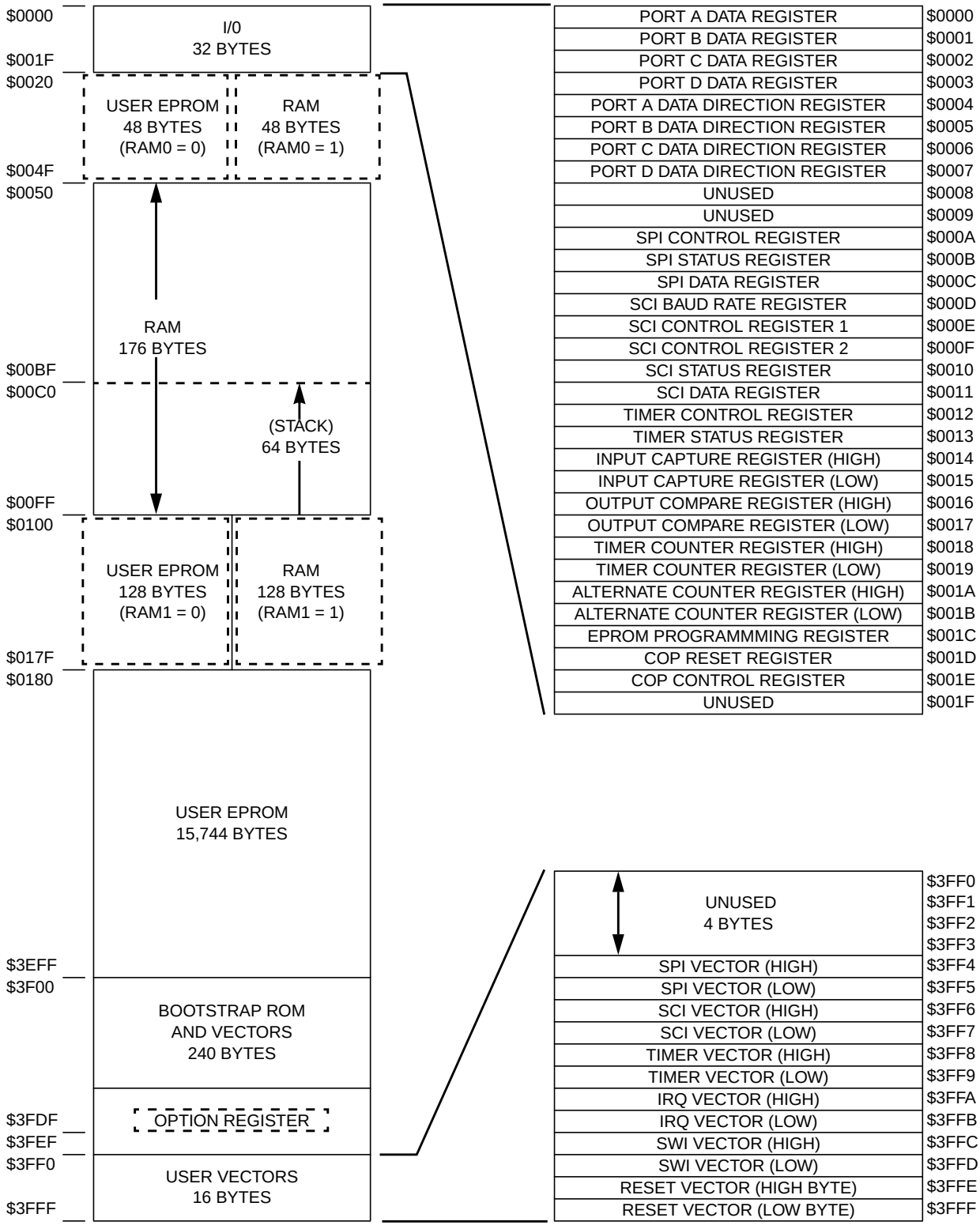


Figure A-4. MC68HC705C9 Memory Map

$0000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Port A Data Register (PORTA)
$0001	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	Port B Data Register (PORTB)
$0002	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	Port C Data Register (PORTC)
$0003	PD7		PD5	PD4	PD3	PD2	PD1	PD0	Port D Data Register (PORTD)
$0004	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0	Data Direction Register A (DDRA)
$0005	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0	Data Direction Register B (DDRB)
$0006	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0	Data Direction Register C (DDRC)
$0007	DDRD7		DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0	Data Direction Register D (DDRD)
$0008									Unused
$0009									Unused
$000A	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR2	SPI Control Register (SPCR)
$000B	SPIF	WCOL		MODF					SPI Status Register (SPSR)
$000C	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0	SPI Data Register (SPDR)
$000D			SCP1	SCP0		SCR2	SCR1	SCR0	SCI Baud Rate Register (BAUD)
$000E	R8	T8		M	WAKE				SCI Control Register 1 (SCCR1)
$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCI Control Register 2 (SCCR2)
$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		SCI Status Register (SCSR)
$0011	SCD7	SCD6	SCD5	SCD4	SCD3	SCD2	SCD1	SCD0	SCI Data Register (SCDR)
$0012	ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL	Timer Control Register (TCR)
$0013	ICF	OCF	TOF	0	0	0	0	0	Timer Status Register (TSR)
$0014	Bit 15	14	13	12	11	10	9	Bit 8	Input Capture Register High (ICRH)
$0015	Bit 7	6	5	4	3	2	1	Bit 0	Input Capture Register Low (ICRL)
$0016	Bit 15	14	13	12	11	10	9	Bit 8	Output Compare Register High (OCRH)
$0017	Bit 7	6	5	4	3	2	1	Bit 0	Output Compare Register Low (OCRL)
$0018	Bit 15	14	13	12	11	10	9	Bit 8	Timer Register High (TRH)
$0019	Bit 7	6	5	4	3	2	1	Bit 0	Timer Register Low (TRL)
$001A	Bit 15	14	13	12	11	10	9	Bit 8	Alternate Timer Register High (ATRH)
$001B	Bit 7	6	5	4	3	2	1	Bit 0	Alternate Timer Register Low (ATRL)
$001C	0	0	LAT	0	0	0	0	PGM	Program Register (PROG)
$001D	Bit 7	6	5	4	3	2	1	Bit 0	COP Reset Register (COPRST)
$001E				COPF	CME	COPE	CM1	CM0	COP Control Register (COPCR)
$001F									Reserved
$3FDF	RAM0	RAM1	0	0	0		IRQ	0	Option Register (OR)

Figure A-5. MC68HC705C9 Register and Control Bit Summary

A.3 EPROM

This section describes how to program the MC68HC705C9.

A.3.1 EPROM Programming

The EPROM can be programmed by either:

- Manipulating the control bits in the EPROM programming register to program the EPROM on a byte-by-byte basis;
- Activating the bootloader ROM to download the contents of an external memory to the on-chip EPROM.

A.3.2 EPROM Program Register (PROG)

This read/write register, shown in Figure A-6, contains two bits used to control the programming of the EPROM bytes. This register is cleared on reset.

PROG — EPROM Program Register **$001C**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	LAT	0	0	0	0	PGM
RESET:	0	0	0	0	0	0	0	0

Figure A-6. Programming Register

LAT – Latch Enable

This read/write bit controls the EPROM array's data and address bus latches to allow programming or normal CPU read operations.

1 = EPROM data and address bus latched for programming on the next byte write cycle

0 = EPROM data and address bus latched for normal CPU operations

PGM – Program

This read/write bit controls the application of the programming voltage V_{PP} to the EPROM array.

1 = V_{PP} on

0 = V_{PP} off

NOTE

The PGM bit can be set only when the EPROM data and address buses are latched, that is, when LAT is set to ones.

Take the following steps to program a byte of EPROM:

1. Apply the programming voltage V_{PP} to the V_{PP} pin
2. Set the LAT bit
3. Write data to the EPROM address
4. Set the PGM bit for a time t_{PROG} to apply to the programming voltage
5. Clear the LAT bit

CAUTION

The V_{PP} pin must be disconnected from V_{PP} (and connected to V_{DD} or left unconnected) before reading the contents of the EPROM.

A.3.3 EPROM Erasing

The erased state of an EPROM byte is $FF. EPROM devices can be erased by exposure to high-intensity ultraviolet (UV) light with a wavelength of 2537 Å. The recommended erasure dosage (UV intensity on a given surface area times exposure time) is 15 Ws/cm^2. UV lamps should be used without shortwave filters, and the EPROM device should be positioned 2.5 cm from the UV source.

A.3.4 Bootloader Mode

The bootloader ROM, located at addresses $3F00–$3FEF, is selected by applying a voltage equal to two times V_{DD} to the $\overline{IRQ}$ pin during reset. The EPROM array is programmed using an industry-standard 16 Kbyte EPROM (27128) via the M68HC05 CPU and software in the on-board bootloader ROM. See **Figure A-7. Bootloader Circuit** for the recommended circuit diagram for the self-programming mode.

The following power-up sequence is essential:

With the MC68HC705C9 installed and the 27128 EPROM device installed in the programming board:

1. Apply the 5 volt supply
2. Apply the high voltage ($2 \times V_{DD}$) to $\overline{IRQ}$
3. Apply the programming voltage to V_{PP}

The above sequence must be reversed to power-down the device.

NOTE

The erased state of the EPROM is $FF.

The logical states of the PD2, PD3, and PD4 pins select the bootloader function, as Table A-1 shows.

Table A-1. Bootloader Function Selection

PD2	PD3	PD4	Function
0	0	0	Program and Verify
0	0	1	Load RAM and Execute
0	1	0	Verify Only
0	1	1	Dump EPROM Contents
1			Execute Program in RAM

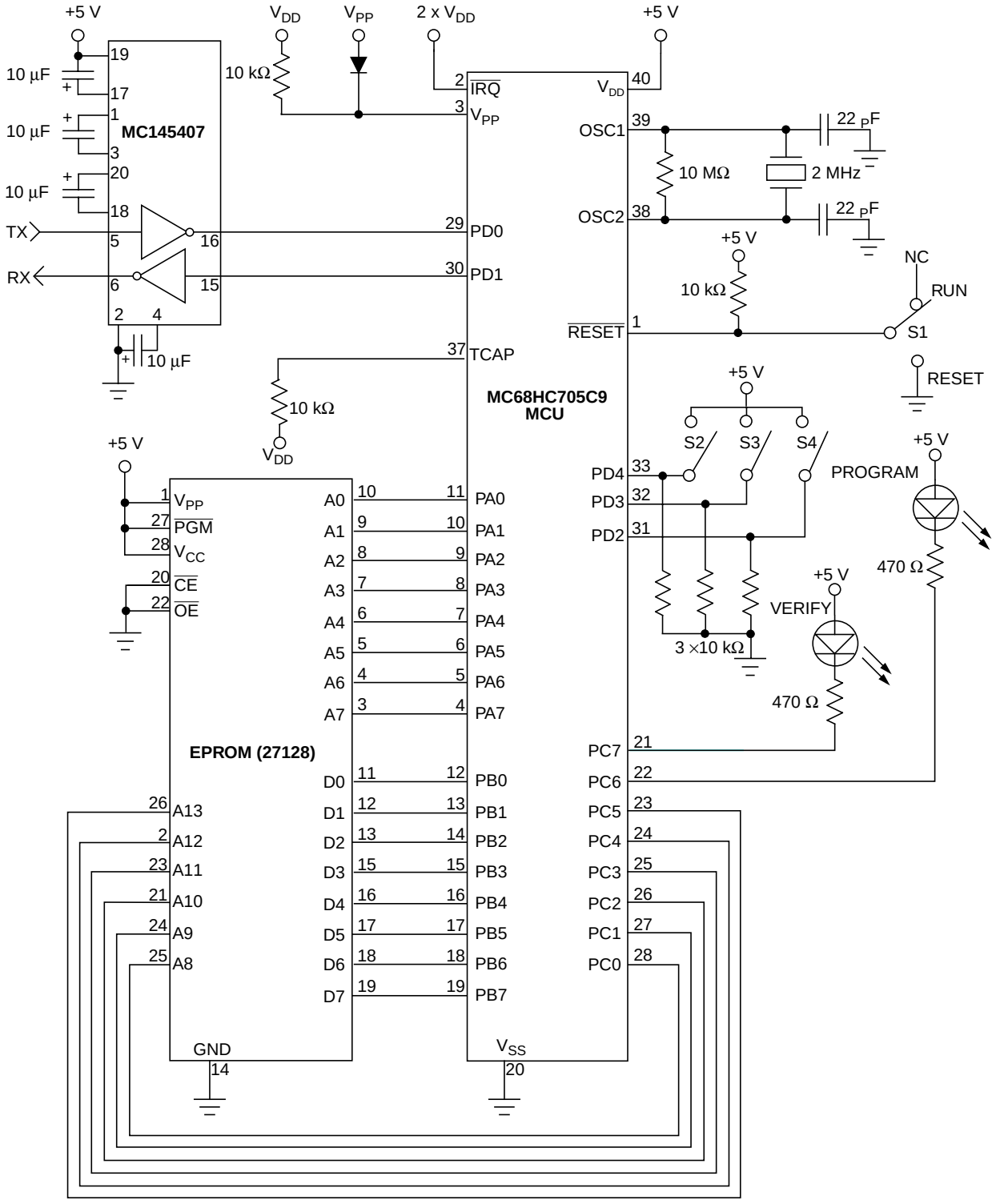


Figure A-7. Bootloader Circuit

A.3.5 Low Power Modes

In STOP mode, the resistor/capacitor (RC) oscillator in the EPROM array is switched off. In WAIT mode, however, the RC oscillator continues to operate, resulting in a higher WAIT I_{DD} than that of the ROM version, the MC68HC05C9.

A.4 ELECTRICAL SPECIFICATIONS

A.4.1 Maximum Ratings

This section contains electrical and timing specifications for the MC68HC705C9.

Table A-2. Maximum Ratings[1]

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to +7.0	V
Input Voltage Normal Operation (Ports, OSC1) $\overline{IRQ}$ and $\overline{RESET}$	V_{IN}	 V_{SS} – 0.3 to V_{DD} + 0.3 V_{SS} – 0.3 to 2 × V_{DD} + 0.3	 V V
Input Voltage V_{PP}	V_{PP}	V_{SS} – 0.3 to 19	V
Storage Temperature Range	T_A	–65 to +150	°C
Current Drain Per Pin (Excluding V_{DD} and V_{SS})[2]	I_D	25	mA

1.Maximum values are not guaranteed operating values. All voltages are with respect to V_{SS}.
2.Maximum drain per pin is for one pin at a time, limited by an external resistor.

A.4.2 Thermal Characteristics

Table A-3. Operating Temperature Range

Rating	Symbol	Value	Unit
Operating Temperature Range	T_A	T_L to T_H –40 to +85	°C

Table A-4. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic Dual In-Line Package (PDIP) Plastic-Leaded Chip Carrier (PLCC)	θ_{JA}	 50 50	°C/W

A.4.3 DC Electrical Characterics

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0, T_A = –40 to + 85 °C)

Table A-5. DC Electrical Characteristics

Characteristic	Symbol	Min	Typ[1]	Max	Unit
Output Voltage I_{LOAD} = +25 µA I_{LOAD} = –25 µA	 V_{OL} V_{OH}	 — V_{DD} – 0.1	 — —	 0.1 —	 V V
Output High Voltage I_{LOAD} = –0.8 mA PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCMP	V_{OH}	V_{DD} – 0.8	—	—	V
Output Low Voltage I_{LOAD} = +1.6 mA PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCMP	V_{OL}	—	—	0.4	V
Input High Voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, $\overline{IRQ}$, $\overline{RESET}$, OSC1, TCAP	V_{IH}	0.7 × V_{DD}	—	—	V
Input Low Voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, $\overline{IRQ}$, $\overline{RESET}$, OSC1, TCAP	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply Current Run[2] WAIT[3] STOP[4]	I_{DD}	 — — —	 5.5 1 —	 9.5 4.0 150	 mA mA µA
I/O Ports Hi-Z Leakage Current PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0	I_{IL}	—	—	±10	µA
Total Port B Sink Current to V_{SS}	I_{SS}	—	—	200	mA
Data Retention Mode Voltage	V_{RM}	—	—	2.0	V
Input Current $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1	I_{IN}	—	—	±1	µA
Capacitance Ports (Input or Output) $\overline{RESET}$, $\overline{IRQ}$	 C_{OUT} C_{IN}	 — —	 — —	 12 8	 pF pF

1. Typical values reflect average measurements at midpoint of voltage range at 25 °C.
2. Run (operating) I_{DD} measured using external square wave clock source (f_{OSC} = 4.0 MHz) with all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
3. WAIT I_{DD} measured using external square wave clock source (f_{OSC} = 4.0 MHz) with all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2. All ports configured as inputs; V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V. Only the timer system active. OSC2 capacitance linearly affects WAIT I_{DD}.
4. STOP I_{DD} measured with OSC1 = V_{DD}. All ports configured as inputs; V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V.

Table A-6. EPROM DC Electrical Characteristics (T_A = 25 °C)

Characteristic	Symbol	Min	Typ[1]	Max	Unit
EPROM					
Programming Voltage	V_{PP}	15	15.5	16	V
Programming Current	I_{PP}	—	2	—	mA
Programming Time	t_{PROG}	4	—	20	ms

1. Typical values reflect average measurements at midpoint of voltage range at 25 °C.

A.4.4 Control Timing

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40 to +85 °C.)

Table A-7. Control Timing

Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency Crystal External Clock	f_{OSC}	 — dc	 4 4	 MHz MHz
Internal Operating Frequency (f_{OSC} ÷ 2) Crystal External Clock	f_{OP}	 — dc	 2 2	 MHz MHz
Internal Clock Cycle Time	t_{CYC}	250	—	ns
Crystal Oscillator Start-Up Time	t_{OXOV}	—	100	ms
$\overline{\text{RESET}}$ Pulse Width Low	t_{RL}	8	—	t_{CYC}
Power-On Reset Delay	f_{PORL}	3968	3968	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	125	—	ns
Interrupt Pulse Period	t_{ILIL}	—[1]	—	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	55	—	ns

1. The minimum period t_{ILIL} should not be less than the number of cycles it takes to execute the interrupt service routine plus 21 t_{CYC}.

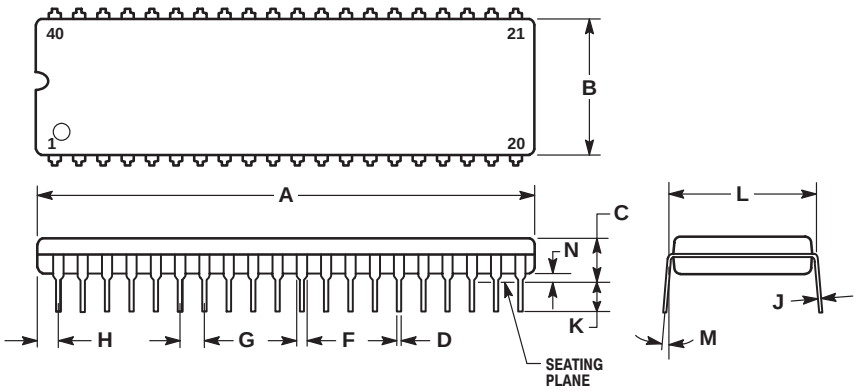
NOTE

The MC68HC705C9 will operate down to dc. However, the power consumption of the EPROM is inversely proportional to frequency. Therefore, at frequencies below f_{OP} = 100 kHz, the total power consumption may exceed the specification limits.

A.5 MECHANICAL SPECIFICATIONS

This section describes the dimensions of the plastic dual-in-line package (PDIP) and plastic-leaded chip carrier package (PLCC).

A.5.1 Plastic Dual-in-Line Package (PDIP)

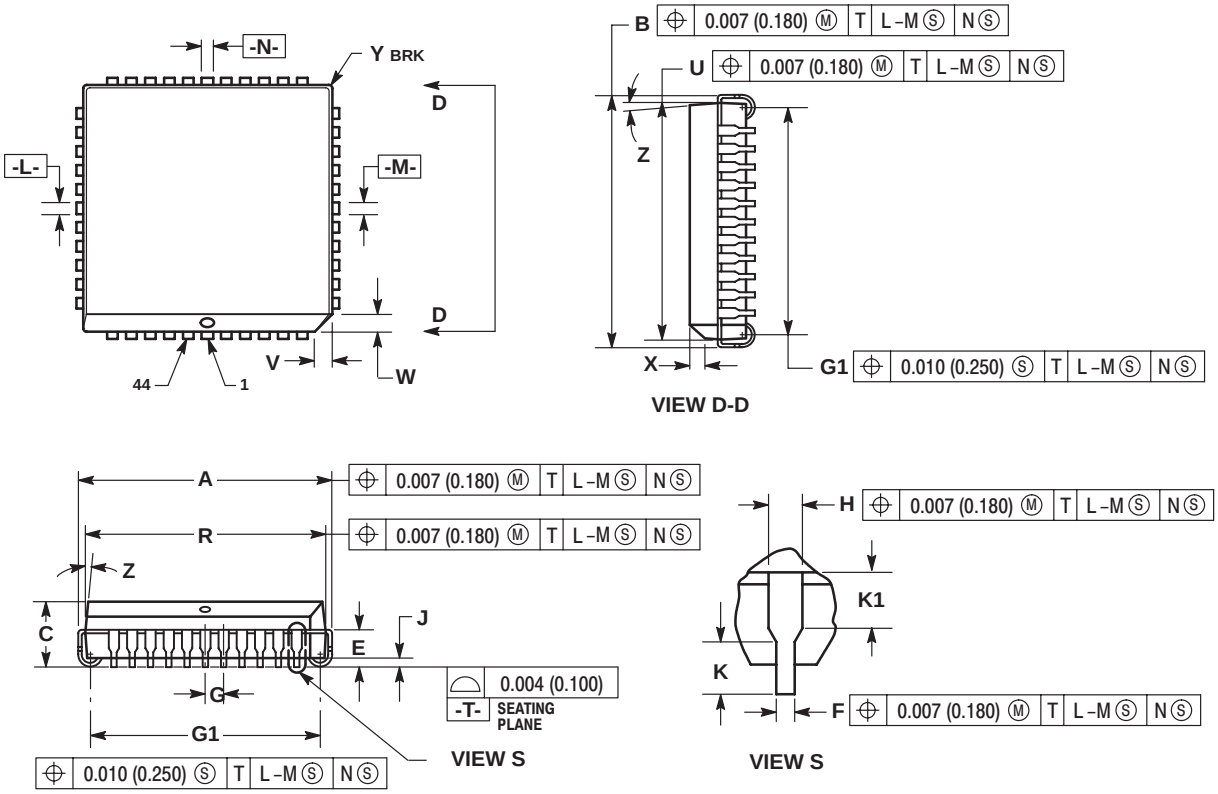


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

Figure A-8. MC68HC705C9P (Case # 711-03)

A.5.2 Plastic-Leaded Chip Carrier (PLCC)



NOTES:
1. DATUMS -L-, -M-, AND -N- ARE DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS (0.010) 0.25 PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	—	1.02	—

Figure A-9. MC68HC705C9FN (Case # 777-02)

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