MC68HC05L9D/H

DragonKat™

8-Bit Microcontroller

MC68HC05L7
MC68HC05L9
MC68HC68L9
MC141510

TECHNICAL
DATA

MC68HC05L7 and MC68HC05L9 are members of the DragonKat™ MCU family designed in Motorola Semiconductor HK Ltd.

MC68HC05L9
MC68HC05L7
MC68HC68L9
MC141510

HCMOS MICROCONTROLLER UNIT

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SECTION 1
INTRODUCTION

1.1 GENERAL

The MC68HC05L9 HCMOS Microcomputer is a member of the M68HC05 Family of low-cost single-chip microcomputers. This 8-bit microcomputer unit (MCU) contains two on-chip oscillators, CPU, RAM, ROM, I/O, timer, serial interface system, liquid crystal display driver circuitry, real time clock, alarm, low voltage inhibit, auto display off, external parallel address, data bus, and a tone generator.

The MC68HC05L7 MCU device is similar to the MC68HC05L9 with several exceptions. It has 60 segments drive, 13 bit address bus and a chip select signal and two I/O ports. Difference information applicable to the MC68HC05L7 MCU is provided in Appendix A of this document.

The MC68HC68L9 and MC141510 are LCD drivers that use with MC68HC05L9 to expand the display capability of MC68HC05L9. The total segment drive of MC68HC68L9 is fifty-five, and MC141510 is one hundred and sixty five. Detail information applicable to MC68HC68L9 and MC141510 are provided in Appendix B and C of this document respectively.

1.2 FEATURES

The following are some of the hardware and software highlights of the MC68HC05L9 single-chip microcomputer.

HARDWARE FEATURES

* 8-bit architecture
* Power saving stop, wait modes
* Low voltage inhibit for data protection
* 176 bytes of on-chip RAM (64 bytes for stack)
* 128 x 5-bit of on-chip display RAM
* 6K bytes of on chip ROM
* 27 bidirectional I/O and 2 input only lines
* LCD driver circuitry with a selection of 1/16 or 1/8 multiplex and 40 segments drive
* Capable to expand to 205 segments drive when connects to 3 MC68HC68L9 or 1 MC141510
* 16-bit address bus
* 8-bit bidirectional data bus
* Internal 16-bit timer
* Serial Communications Interface System
* 2 on-chip oscillators -- 1 RC osc. for MCU and 1 crystal osc. for real time clock and LCD driver
* Self-check mode
* 128-pin QFP or in Die form

SOFTWARE FEATURES

* Similar to MC6800
* 8 x 8 Unsigned Multiply Instruction

SOFTWARE FEATURES (Continued)

* Efficient Use of Program Space
* Versatile Interrupt Handling
* True Bit Manipulation
* Addressing Modes with Index Addressing for Tables
* Efficient Instruction Set
* Memory Mapped I/O
* Two Power-Saving Standby Modes
* Upward Software Compatible with the M146805 CMOS Family

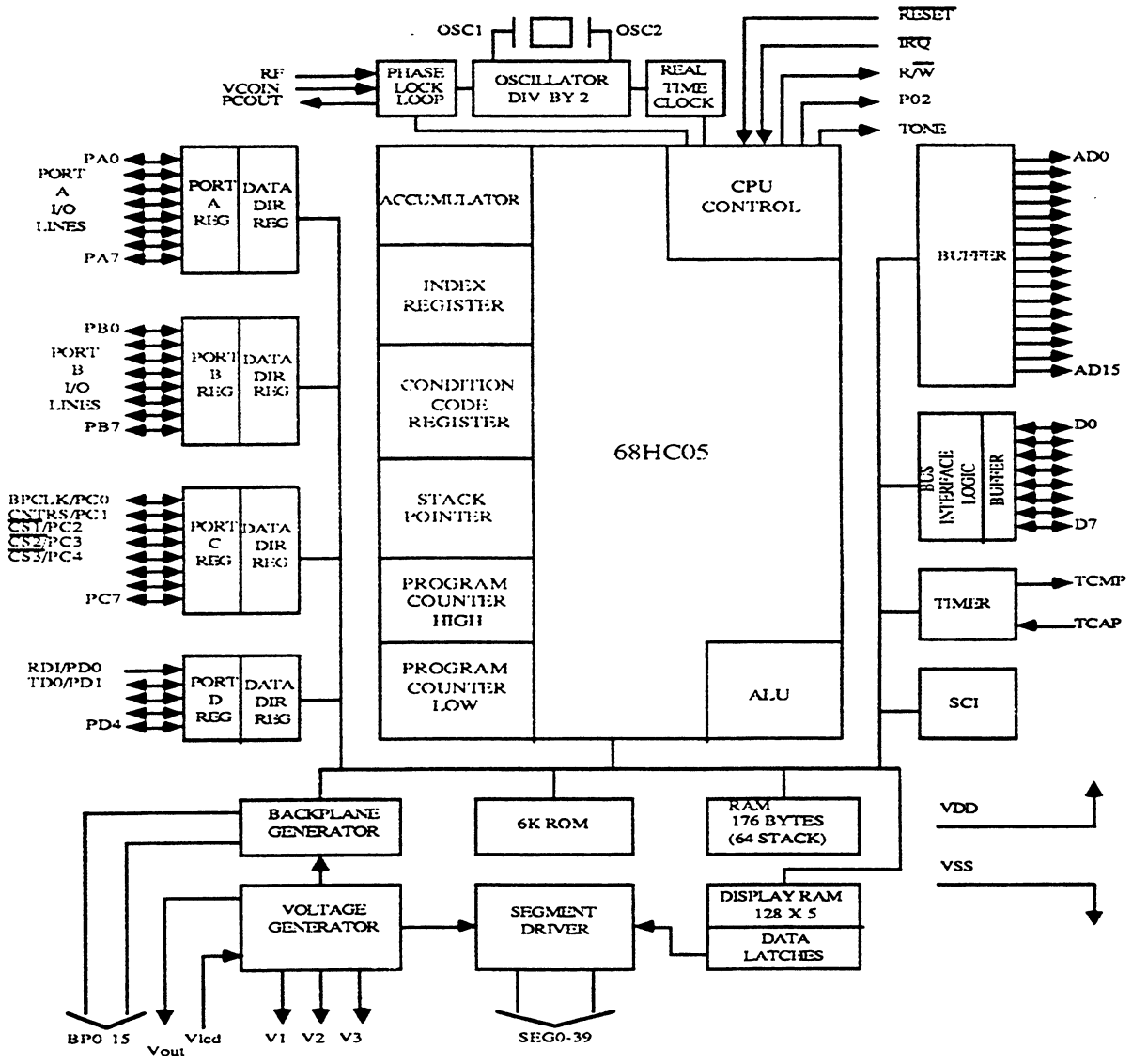


FIG. 1-1 MC68HC05L9 MICROCOMPUTER BLOCK DIAGRAM

SECTION 2
FUNCTIONAL PIN DESCRIPTION, INPUT/OUTPUT PROGRAMMING, MEMORY, CPU REGISTER, AND SELF-CHECK

This section provides a description of the functional pins, input/output programming, memory, CPU registers, and self-check.

2.1 FUNCTIONAL PIN DESCRIPTION

2.1.1 V_{DD} and V_{SS}

Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is ground.

2.1.2 IRQ-

IRQ- is software programmable to provide two different choices of interrupt triggering sensitivity. These options are: 1) negative edge-sensitive triggering only, or 2) negative level-sensitive triggering. The MCU completes the current instruction before it responds to the interrupt request. When the IRQ- pin goes low for at least one tILIH, a logic one is latched internally to signify an interrupt has been requested. When the MCU completes its current instruction, the interrupt latch is tested. If the interrupt latch contains a logic one, and the interrupt mask bit (I bit) in the condition code register is clear, the MCU then begins the interrupt sequence.

If the interrupt is selected to level-sensitive triggering, then the IRQ- input requires an external resistor to VDD for "wire-OR" operation. See **INTERRUPTS** in Section 3 for more detail concerning interrupts.

2.1.3 RESET-

The RESET- input is not required for startup but can be used to reset the MCU internal state and provide an orderly software startup procedure. Refer to **RESETS** in Section 3 for more detail description.

2.1.4 TCAP

The TCAP input controls the input capture feature for the on-chip programmable timer system. Refer to **INPUT CAPTURE REGISTER** in Section 4 for additional information.

2.1.5 TCMP

The TCMP pin provides an output for the output compare feature of the on-chip programmable timer system. Refer to **OUTPUT COMPARE REGISTER** in Section 4 for additional information.

2.1.6 OSC1, OSC2

These pins provide connection to the on chip crystal oscillator. The crystal frequency is 32.768 KHz.

2.1.7 PA0-PA7

These eight I/O lines comprise of port A. The state of any pin is software programmable and all port A lines are configured as input during power on or external reset. Refer to **INPUT/OUTPUT PROGRAMMING** paragraph for a detailed description of I/O programming.

2.1.8 PB0-PB7

These eight I/O lines comprise of port B. The state of any pin is software programmable and all port B lines are configured as input during power on or external reset. Refer to **INPUT/OUTPUT PROGRAMMING** paragraph for a detailed description of I/O programming.

2.1.9 PC0-PC7

These eight I/O lines comprise of port C. The state of any pin is software programmable and all port C lines are configured as input during power on or external reset. PC0-PC4 can be selected either as control signal outputs for the increase of LCD display capability or as general purpose I/O pins. Refer to **INPUT/OUTPUT PROGRAMMING** paragraph for a detailed description of I/O programming.

2.1.10 PD0-PD4

These five lines comprise of port D. PD0 is configured either as a receive data input for serial communication interface or input port, and PD1 is configured either as a transmit data output or input port. PD2-PD4 are general I/O ports. The state of any pin is software programmable (except bit 0-1) and all port D are configured as input during power on or external reset.

2.1.11 P02

This is a bus clock output from the processor that indicates when the data on the external data bus is to be accessed by either the processor or the peripheral.

2.1.12 R/W-

R/W- is the processor output that indicates to peripheral which direction the data is to be passed over the data bus. When R/W-is high and address bus is addressing memory beyond the first 8K bytes, the processor will be reading data from the external peripheral or memory. When R/W- is low , the processor will be writing data to the external peripheral or memory.

2.1.13 AD0-AD15

AD0-AD15 is a 16-bit wide address bus from the processor.

2.1.14 D0-D7

D0-D7 is an 8-bit wide bidirectional data bus used to connect external peripherals and memory to the processor. They will be in high impedence when address bus is selecting the 6K ROM within the MCU.

2.1.15 BP0-BP15

These 16 output lines provide the backplane drive signals to the LCD unit.

2.1.16 SEG0-SEG39

These 40 output lines provide the segment drive signal to the LCD unit.

2.1.17 Vlcd

This input pin provides the power for the LCD driver circuitry.

2.1.18 Vout

This output pin provides the same voltage level as V_{lcd}. It is mainly used as a LCD power supply for MC68HC68L9 or MC141510.

2.1.19 V1, V2, V3

These three pins provide the voltage level for LCD. Refer to **6.2 LIQUID CRYSTAL DISPLAY DRIVER** for a detail description of liquid crystal display driver.

2.1.20 TONE

This output pin provides the audio frequency of either 500 Hz or 2 KHz. Refer to **2.3.1 CONTROL REGISTER** for a detail description of TONE.

2.1.21 RF, VCOIN, PCOUT

These pins provide connections to the on chip RC oscillator. Refer to **6.5 PHASE LOCK LOOP** for a detail description of RF, VCOIN and PCOUT pin.

2.2 INPUT/OUTPUT PROGRAMMING

2.2.1 PARALLEL PORTS

Ports A#, B, C^ and D (PD2-PD4) may be programmed as an input or an output under software control. The direction of the pins is determined by the state of corresponding bit in the port data direction register (DDR). Each 8-bit port has an associated 8-bit data direction register. Any port A, B, C or D (PD2-PD4) pin is configured as an output if its corresponding DDR bit is set to a logic one. A pin is configured as an input if its corresponding DDR bit is cleared to a logic zero. At power-on or reset, all DDRs are cleared, which configure all port A, B, C and D pins as inputs. The data direction registers are capable of being written to or read by the processor. Refer to Figure 2-1 and Table 2-1. During the programmed output state, a read of the data register actually reads the value of the output data latch and not the I/O pin.

When KEYE (bit 4 of $09) is set and port A is configured as an input, there will be ~250 K OHM pull up resistors associate with each pin of port A.

^ PC0-PC4 will be selected as control signal pins when LCD (bit 5 of $0A) is set. Refer to **SECTION 6.2 LIQUID CRYSTAL DISPLAY** for a detailed description of PC0-PC4 configuration when LCD bit is set.

Table 2-1 I/O Pin Functions

R/$\overline{W}$	DDR	I/O Pin Functions
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

2.2.2 FIXED PORT

Port D (PD0-PD1) is a 2-bit fixed input that continually monitors the external pins whenever the SCI system is disabled. During power-on reset or external reset all two bits become valid input ports because all special function output drivers are disabled. For example, with the serial communications interface (SCI) system enable, (RE=TE=1) PD0 and PD1 inputs will read zero. No data register bit is accociated with PD0-PD1.

NOTE
It is recommended that all unused inputs and I/O ports be tied to an appropriate logic level (e.g., either VDD or VSS).

2.2.3 SERIAL PORT (SCI)

The serial communications interface (SCI) uses the port D pins for their functions. The SCI function requires two of the pins (PD0-PD1) for its receive data input (RDI) and transmit data output (TDO) respectively. Refer to **SECTION 5 SERIAL COMMUNICATIONS INTERFACE** for a more detailed discussion.

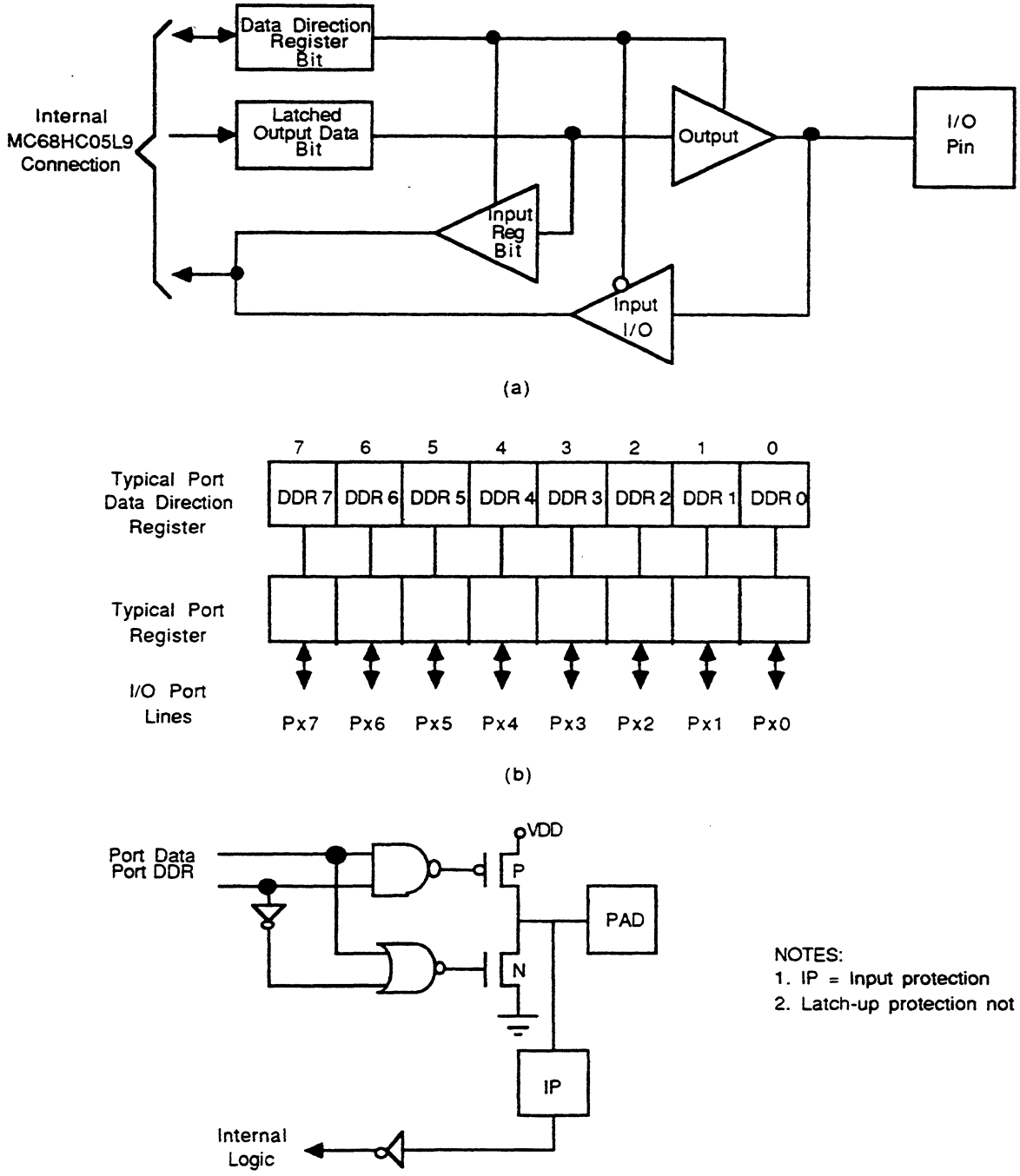


Fig. 2-1 Parallel Port I/O Circuitry

2.3 MEMORY

As shown in Fig. 2-2, the MCU is capable of addressing 64K bytes of memory and I/O registers with its program counter. The first 32 bytes of memory, include 8 bytes for data ports, data direction, 2 bytes for control register, 1 byte for count down register, 2 bytes for alarm register, 10 bytes for timer, 5 bytes for SCI and 3 bytes for real time clock. The next 176 bytes (address $0050-$00FF) are reserved for user and stack. Display RAM occupies 656 x 5 bits, it starts from address $200-$048F. This is only a virtual address space. The physical memory size is 128 x 5 bits ($200-$27F) and the rest of the display RAM area are reserved for MC68HC68L9 or MC141510. Address $0800-$1FFF are areas for the 6144 bytes ROM that include self-check ROM and self-check vectors. Finally, user vectors are located at address $1FF0-$1FFF.

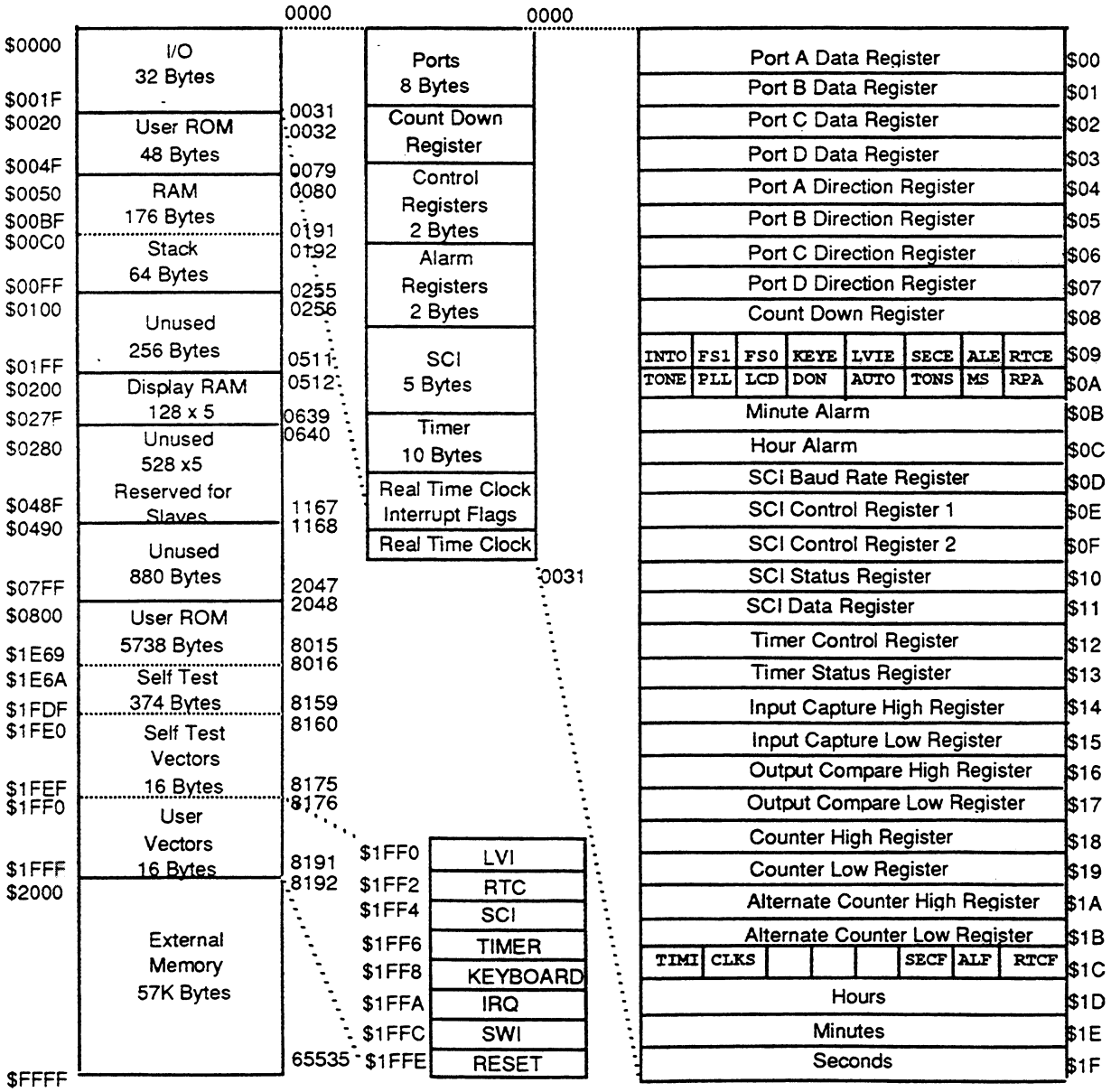


FIG. 2-2 MC68HC05L9 Memory Map

2.3.1 CONTROL REGISTERS

Address $09 and $0A are the control registers to control the special function of the MCU and they are described as follow:

Address $09

RTCE	BIT 0	0 = Real time clock once a day interrupt disable 1 = Real time clock once a day interrupt enable
ALE	BIT1	0 = Alarm interrupt disable 1 = Alarm interrupt enable
SECE	BIT2	0 = Real time clock once a second interrupt disable 1 = Real time clock once a second interrupt enable
LVIE	BIT3	0 = Low voltage inhibit interrupt disable 1 = Low voltage inhibit interrupt enable
KEYE	BIT4	0 = Keyboard interrupt disable 1 = Keyboard interrupt enable
FS1,FS0	BIT6,5	00 = 153 KHz internal bus frequency 01 = 1.22 MHz internal bus frequency 10 = 306 KHz internal bus frequency 11 = 2.44 MHz internal bus frequency
INTO	BIT7	0 = Negative level-sensitive triggering 1 = Negative edge-sensitive triggering

Address $0A

RPA	BIT0	0 = LCD voltage generator total resistance of ~90 K OHM 1 = LCD voltage generator total resistance of ~45 K OHM
MS	BIT1	0 = 1:16 multiplex 1 = 1:8 multiplex
TONS	BIT2	0 = Tone output frequency of 500 Hz 1 = Tone output frequency of 2 KHz
AUTO	BIT3	0 = Disable auto display off feature 1 = Enable auto display off feature
DON	BIT4	0 = Turn off LCD 1 = Turn on LCD
LCD	BIT5	0 = Configure PC0-PC4 as general I/O port 1 = Configure PC0-PC4 as control signal for MC68HC68L9/MC141510

PLLI	BIT6	0 = Indicate PLL is unlocked 1 = Indicate PLL is locked
TONE	BIT7	0 = No audio output at TONE pin 1 = Audio output at TONE pin

All bits in addresses $09 and $0A are readable and writable, except bit 6 of address $0A that is read only. All bits are cleared during power on or external reset.

2.4 CPU REGISTERS

The MC68HC05L9 CPU contains five registers, as shown in the programming model of Fig. 2-3. The interrupt stacking order is shown in Fig. 2-4.

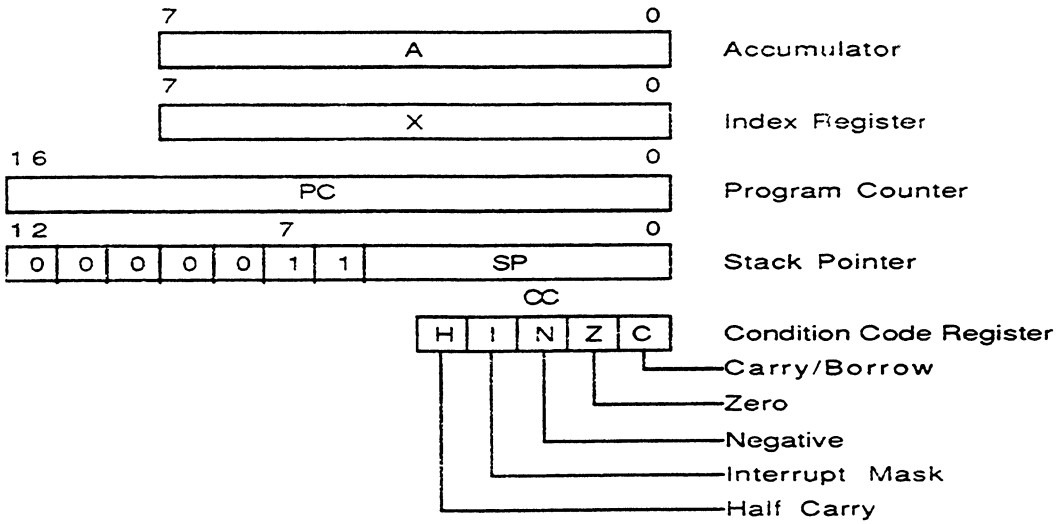


Fig. 2-3 Programming Model

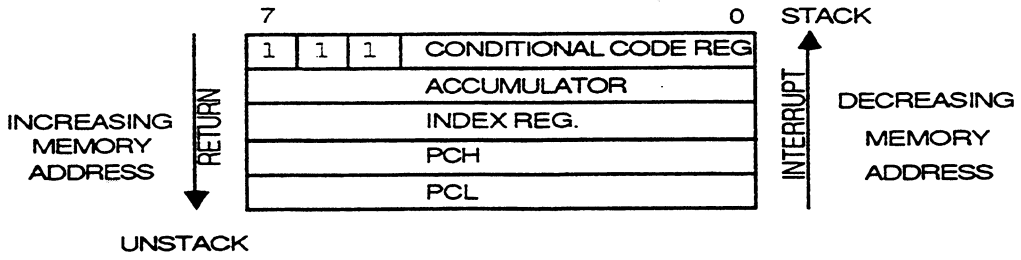


Fig. 2-4 Stacking Order

2.4.1 Accumulator (A)

The accumulator is an 8 bit general purpose register used to hold operands, results of the arithematic calculations, and data manipulation.

2.4.2 Index Register (X)

The X register is an 8-bit register which is used during the index modes of addressing. It provides an 8-bit value which is used to create an effective address. The index register is also used for data manipulations with the read-modify-write type of instructions and as a temporary storage register when not performing addressing operations.

2.4.3 Program Counter (PC)

The program counter is a 16-bit register that contains the address of next instruction to be executed by the processor.

2.4.4 Stack Pointer (SP)

The stack pointer is a 13-bit register containing the address of the next free locations on the push-down/pop-up stack. When accessing memory, the seven most significant bits are permanently configured to 0000011. These seven bits are appended to the six least significant register bits to produce an address within the range of $00FF to $00C0. The stack area of RAM is used to store the return address on subroutine calls and the machine state during interrupts. During external or power-on reset, and during a reset stack pointer (RSP) instruction, the stack pointer is set to its upper limit ($00FF). Nested interrupt and/or subroutines may use up to 64 (decimal) locations. When the 64 locations are exceeded, the stack pointer wraps around and points to its upper limit ($00FF), thus, losing the previously stored information. A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five RAM bytes.

2.4.5 Condition Code Register (CC)

The condition code register is a 5-bit register which indicates the results of the instruction just executed as well as the state of the processor. These bits can be individually tested by a program and specified action taken as a result of their state. Each bit is explained in the following paragraphs.

2.4.5.1 HALF CARRY BIT (H). The H bit is set to one when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. The H bit is useful in binary coded decimal subroutines.

2.4.5.2 INTERRUPT MASK BIT (I). When the I bit is set, all interrupts are disabled. Clearing this bit enables the interrupts. If an external interrupt occurs while the I bit is set, the interrupt is latched and is processed after the I bit is next cleared; therefore, no interrupts are lost because of the I bit being set. An internal interrupt can be lost if it is cleared while the I bit is set (refer to **SECTION 4 PROGRAMMABLE TIMER AND SECTION 5 SERIAL COMMUNICATIONS INTERFACE** for more information).

2.4.5.3 NEGATIVE (N). When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation is negative (bit 7 in the result is a logic one).

2.4.5.4 ZERO (Z). When set, this bit indicates that the result of the last arithematic, logical, or data manipulation is zero.

2.4.5.5 CARRY/BORROW (C). Indicates that a carry or borrow out of the arithematic logic unit (ALU) occurred during the last arithematic operation. This bit is also affected during bit test and branch instructions, shifts, and rotates.

2.5 SELF CHECK

The self-check capability of the MC68HC05L9 MCU provides an internal check to determine if the device is functional. The SELF-CHECK mode is entered if certain conditions are met on the PB0, IRQ and RESET pins. +9.5 volts must be present on the IRQ pin. This value is latched internally on the rising edge of the external RESET pin. Also the state of the PB0 pin is latched internally on the rising edge of external RESET pin. The IRQ pin at +9.5 V and the PB0 is high will place the part in the SELF-CHECK mode. The hold time on the IRQ pin after the external RESET pin is brought high is 2 clock cycles.

Two modes of operations are possible, depending on the state of the PB5 pin :

* SERIAL SELF-CHECK

* PARALLEL SELF-CHECK

2.5.1 SERIAL SELF-CHECK

This mode is entered by setting:

* PB1 = 0, PB4 = 1

* PB5 = 1

This is a bootload routine which downloads program from PC to internal and external SRAM through SCI port, by means of RS232 link at 9600 baud, 8 bit, no parity, full duplex. Program being downloaded should be in binary format and the first byte that is downloaded should have the value to indicate how many additional pages(256 bytes a page) need to be loaded to external SRAM. When this routine is called, 100 bytes will be loaded to RAM address $54-$B7. Depending on the value of the first byte, 256 multiply the value of $54 bytes will be downloaded to external SRAM (starting location depends on the value of $55 : $56).

Locations $50-$53 are reserved for bootload routine and following locations are reserved for interrupt vectors. Three bytes are reserved for each interrupt vector so that a JMP instruction can be stored. See also Fig. 2-5 Serial SELF-CHECK schematic diagram with 8K x 8 bytes external SRAM to store test program.

Interrupt vectors target in RAM for serial SELF-CHECK

$00BE-$00C0	LVI interrupt vector for serial SELF-CHECK
$00C1-$00C3	RTC interrupt vector for serial SELF-CHECK
$00C4-$00C6	SCI interrupt vector for serial SELF-CHECK
$00C7-$00C9	Timer interrupt vector for serial SELF-CHECK
$00CA-$00CC	Keyboard interrupt vector for serial SELF-CHECK
$00CD-$00CF	External interrupt vector for serial SELF-CHECK
$00D0-$00D2	SWI interrupt vector for serial SELF-CHECK

2.5.2 PARALLEL SELF-CHECK

This mode is entered by setting:

* PB1 = 0, PB4 = 1

* PB5 = 0

After reset, the following tests are performed automatically:

I/O - Test ports A, B, C and D
RAM - Counter test for each RAM byte
TIMER - Tracks counter register and checks OCF flag
SCI - Transmission Test; checks for RDRF, TDRF, TC and FE flags
ROM - Exclusive OR with odd 1's parity result
Display Ram - Counter test for each display RAM and display "L9" on LCD
Interrupt - Test external, timer, SCI interrupts

When the part is placed in the SELF-CHECK mode, the SELF-CHECK vector will be fetched and the SELF-CHECK firmware will start to execute. Remark that SELF-CHECK gets its own set of interrupt vectors apart from that of user mode.

Self-check results (using the LEDs as monitors) are shown in Table 2-2.

Table 2-2 Self-Check Results

PC3	PC2	PC1	PC0	REMARKS
1	0	0	1	Bad I/O
1	0	1	0	Bad RAM
1	0	1	1	Bad Timer
1	1	0	0	Bad SCI
1	1	0	1	Bad Display RAM
1	1	1	0	Bad interrupts or IRQ Request
Flashing				Good Device
All Others				Bad Device, Bad Port A, etc.

0 indicates LED on; 1 indicates LED is off.

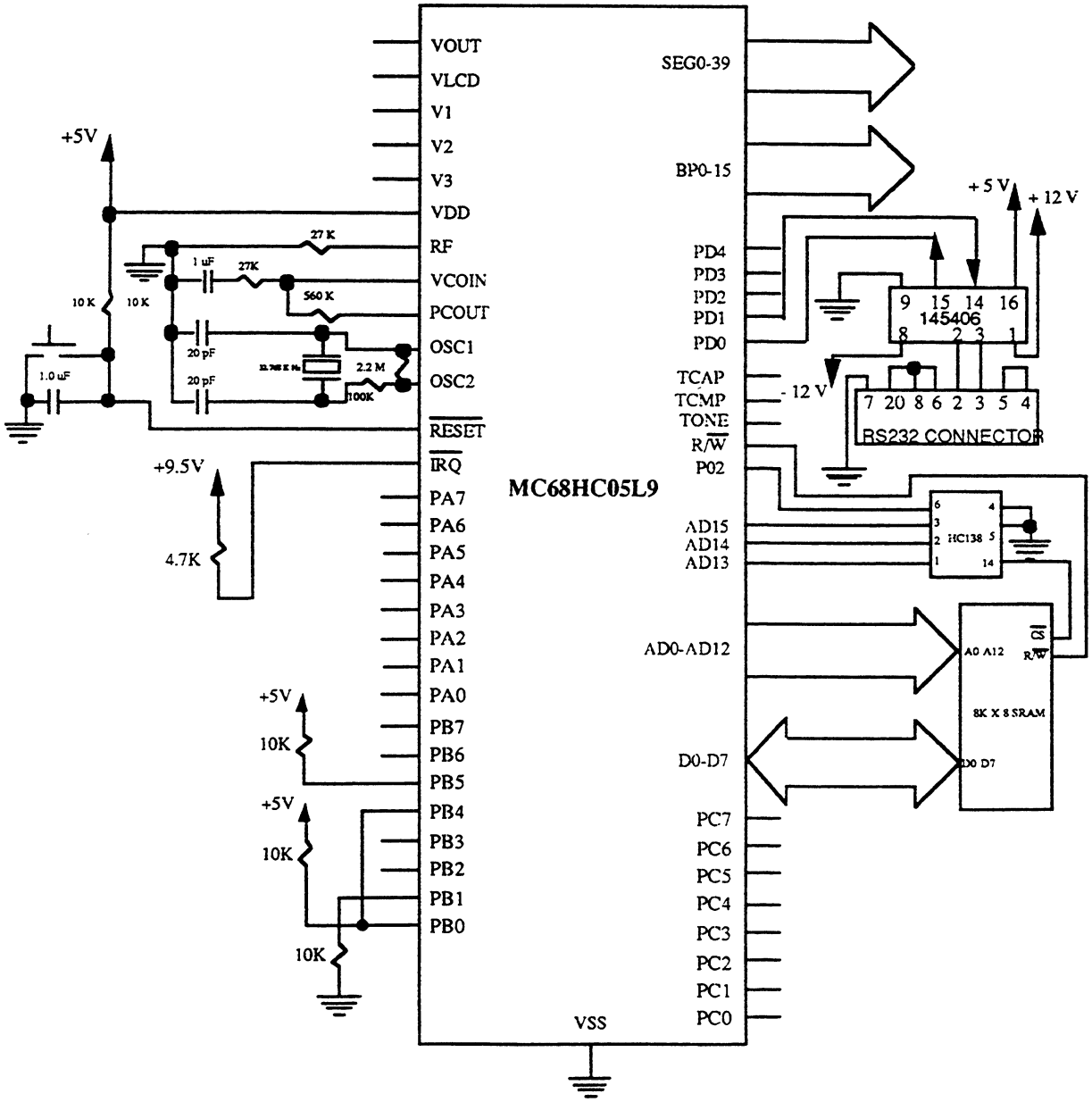


Fig. 2-5 MC68HC05L9 Serial Self-check Schematic

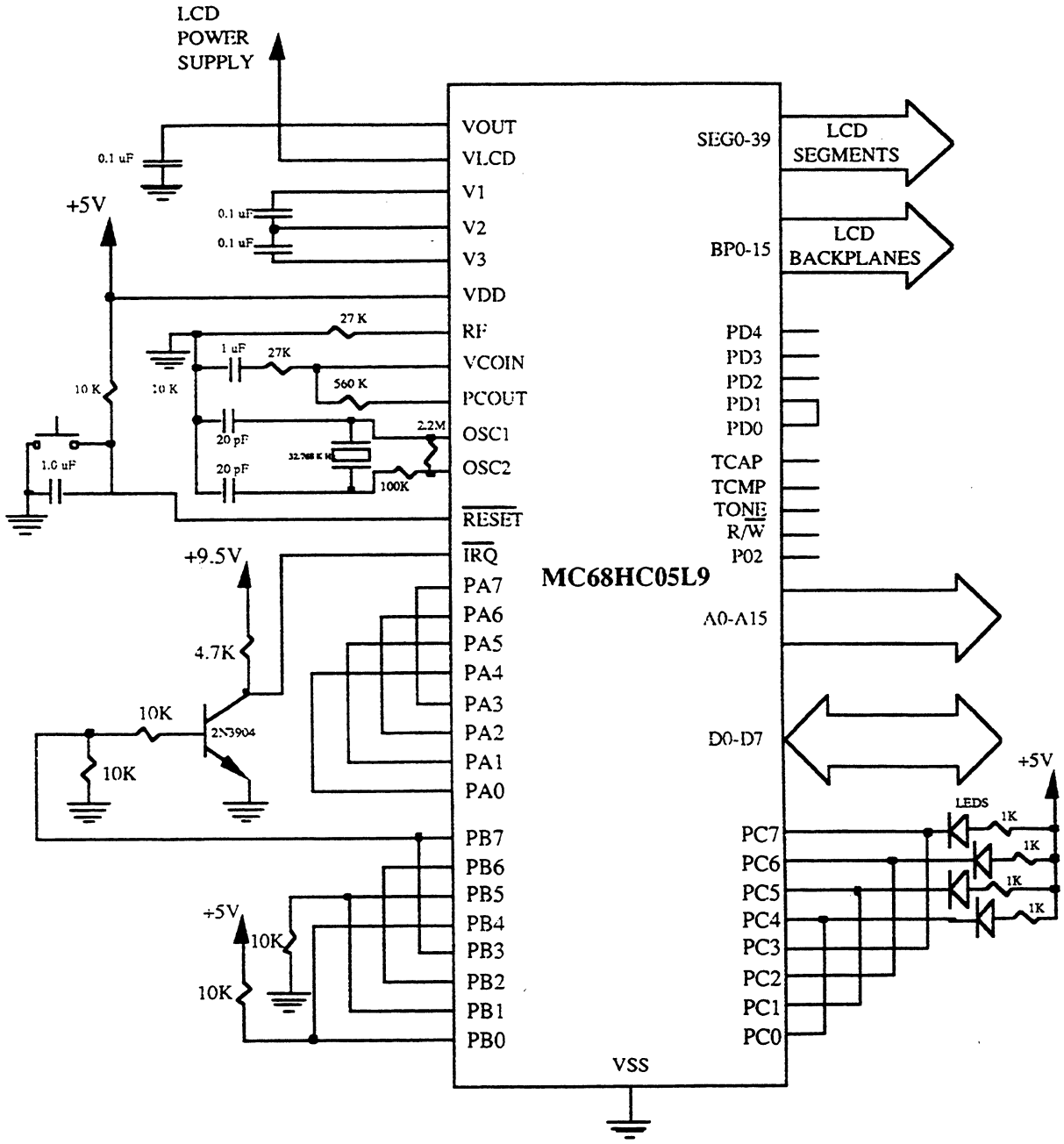


Fig. 2-6 MC68HC05L9 Parallel Self-check Schematic

SECTION 3
RESETS, INTERRUPTS, LOW POWER, AND DATA RETENTION MODES

3.1 RESETS

The MC68HC05L9 has two reset modes; an active low external reset pin (RESET-) and a power-on reset function; refer to Fig. 3-1.

3.1.1 RESET- Pin

The RESET- input pin is used to reset the MCU to provide an orderly software startup procedure. When using the external reset mode, the RESET-pin must stay low for a minimum of one and one half tcyc. The RESET- pin contains an internal Schmitt Trigger as part of its input to improve noise immunity.

3.1.2 Power-On Reset

The power-on reset occurs when a positive transition is detected on VDD. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. There is no provision for a power-down reset. The power-on circuitry provides for a tpor tcyc delay from the time that the oscillator becomes active. If external RESET-pin is low at the end of the tpor tcyc time out, the processor remains in the reset condition until RESET- go high. The user must ensure that VDD has risen to a point where the MCU can operate properly prior to the time the tpor tcyc POR reset cycles have elapsed. If there is doubt, the external RESET- pin should remain low until such time that VDD has risen to the minimum operating voltage specified.

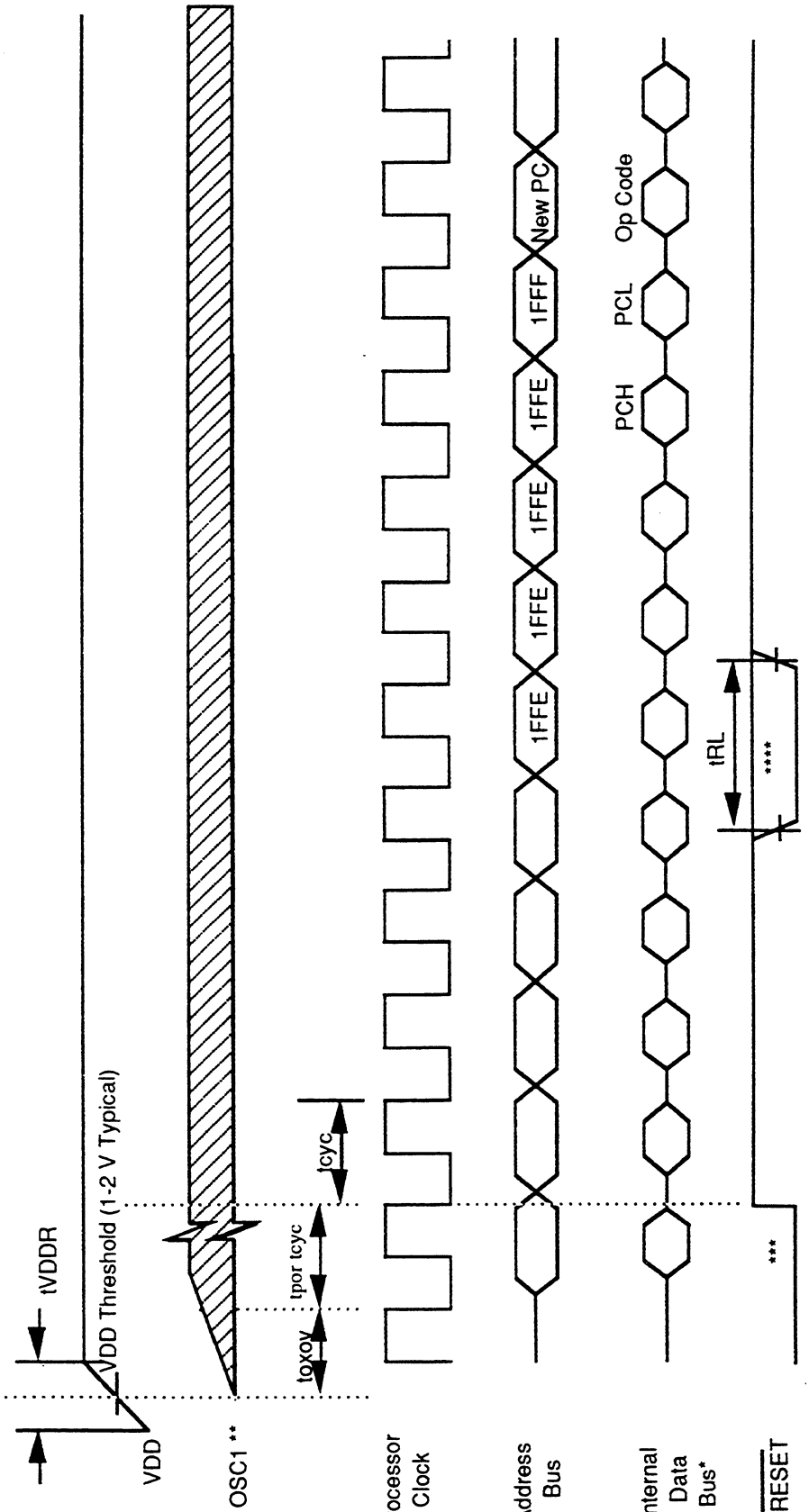
tpor is defined by a user specified mask option as either 16 or 4064 cycles.

Table 3-1 shows the actions of two resets on internal circuits, but not necessarily in order of occurence (X indicates that the condition occurs for the particular reset).

Table 3-1 Reset Action on Internal Circuit

Condition	RESET Pin	Power-On Reset
Timer Prescaler reset to zero state	X	X
Timer counter configures to $FFFC	X	X
Timer output compare (TCMP) bit reset to zero	X	X
All timer interrupt enable bits cleared (ICIE, OCIE, and TOIE) to disable timer interrupts The OLVL timer bit is also cleared by reset	X	X
All data direction registers cleared to zero (input)	X	X
Count Down register are set to three	X	X
Hour and Minute alarm register are set to zero	X	X
Hours, minutes and seconds registers are set to zero	X	X
Configure stack pointer to $00FF	X	X
Force internal address bus to restart vector ($1FFE-$1FFF)	X	X
Set I bit in condition code register to a logic one	X	X
Clear STOP latch	X	X
Clear external interrupt latch	X	X
Clear WAIT latch	X	X
Disable SCI (serial control bits TE=0 and RE=0). Other SCI bits cleared by reset include: TIE, TCIE, RIE, ILIE, RWU, SBK, RDRF, IDLE, OR, NF, and FE	X	X
Set serial status bits TDRE and TC	X	X
Clear all serial interrupt enable bits (TIE, and TCIE)	X	X
Clear SCI prescaler rate control bits SCP0-SCP1	X	X
Keyboard interrupt enable bit is cleared	X	X
RTC interrupt enable bit is cleared. Other RTC bit cleared by reset include: RTCF, ALF, SECF	X	X
LVI interrupt enable bit is cleared	X	X
All bits in address $09, $0A and $1C are cleared	X	X

* Indicate that timeout still occurs



* Internal bus information not available externally.
** OSC1 line is not meant to represent frequency. It is only used to represent time.
*** The reset pin will be pulled low by the POR circuitry until the end of the tpor tcyc.
**** The next rising edge of the processor clock following the rising edge of RESET- initiates the reset sequence.

FIG. 3-1 Power-On reset and RESET-

3.2 INTERRUPTS

The MC68HC05L9 is capable of operating with eight different interrupts, seven hardware and one software. The "I" bit in the Condition Code Register, if set, blocks all interrupts except the software interrupt, SWI. Interrupts such as Timer, RTC, and SCI have several flags which will cause the interrupt. Generally, interrupt flags are found in "read only" status registers (except RTC) while their enables are in associated control registers. They are never mixed in the same register. If the enable bit is "0", it blocks the interrupt from occurring but does not inhibit the flag from being set. RESET clears all enable bits. The general sequence for clearing an interrupt is a software sequence of reading the status register while the flag is set followed by a read or write of an associated register (except RTC). When any of these interrupts occur, and if enabled, normal processing is suspended at the end of the current instruction execution. The state of the machine is pushed onto the stack (see Figure 2-4 for stacking order) and the appropriate vector points to the starting address of the interrupt service routine (see Table 3-2). Also, the interrupt mask bit in the condition code register is set. This masks further interrupts. At the completion of the service routine, the software normally contains an RTI instruction which, when executed, restores the machine state and continues executing the interrupted program. Note that the interrupt mask bit (I bit) will be reset if and only if the corresponding bit stored on the stack is zero.

Table 3-2 Vector Address for Interrupts and Reset

Register	Flag Name	Interrupts	CPU Interrupt	Vector Address
X	X	Reset	RESET	$1FFE-$1FFF
X	X	Software	SWI	$1FFC-$1FFD
X	X	External Interrupt	IRQ	$1FFA-$1FFB
X	X	Keyboard	KEYBOARD	$1FF8-$1FF9
Timer Status	ICF	Input Capture	TIMER	$1FF6-$1FF7
	OCF	Output Compare		
	TOF	Timer Overflow		
SCI Status	TDRE	Transmit Buffer Empty	SCI	$1FF4-$1FF5
	TC	Transmit Complete		
	RDRF	Receive Buffer Full		
	IDLE	Idle Line Detect		
	OR	Overrun		
RTC Status	SECF	Per Second	RTC	$1FF2-$1FF3
	ALF	Alarm		
	RTCF	Per Day		
X	X	Low Voltage Inhibit	LVI	$1FF0-$1FF1

3.2.1 HARDWARE CONTROLLED SEQUENCES

The following three functions are not strictly interrupts, however, they are tied very closely to the interrupts. These functions are RESET, STOP, WAIT.

(a) RESET -The RESET- input pin causes the program to go to its starting address. This address is specified by the contents of memory locations $1FFE and $1FFF. The interrupt mask of the condition code register is also set. Much of the MCU is set to some known state.

(b) STOP - The STOP instruction causes the internal processor clock to be turned off and the processor to "sleep" until an external interrupt (IRQ), RTC, Keyboard, LVI interrupt or RESET occurs. The crystal oscillator will still run if the RTC mask option is selected 'ON'.

(c) WAIT - The WAIT instruction causes all processor clocks to stop, but leaves the Timer and SCI clock running. This "rest" state of the processor can be cleared by RESET, an external interrupt (IRQ), RTC, Keyboard, LVI interrupt, Timer or SCI interrupt. There are no special wait Vectors for these individual interrupts.

3.2.2 SOFTWARE INTERRUPT (SWI)

The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask in the condition code register. The service routine address is specified by the contents of memory location $1FFC and $1FFD.

3.2.3 EXTERNAL INTERRUPT

The IRQ interrupt signal will be explained in this paragraph. If the interrupt mask bit of the condition code register is cleared and a negative edge occurs at the external pin, then the interrupt, IRQ, occurs. A software select option will allow a "low" at the pin to be recognized also. The actual processor interrupt is generated only if the interrupt mask bit of the condition code register is also cleared. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This masks further interrupts until the present one is serviced. The service routine address is specified by the contents of $1FFA and $1FFB. The interrupt logic recognizes negative edge transitions and pulses (special case of negative edges) on the external interrupt line. Figure 3-4 shows both a block diagram and timing for the interrupt line (IRQ) to the processor. The first method is single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the number of cycles required to execute the interrupt service routine plus 21 cycles. Once a pulse occurs, the next pulse should not occur until the MCU software has exited the routine (an RTI occurs). The second configuration shows several interrupt line "wire-ORed" to perform the interrupts at the processor. Thus, if after servicing one interrupt the interrupt line remains low, then the next interrupt is recognized.

NOTE

The internal interrupt latch is cleared in the first part of the service routine; therefore, one (and only one) external interrupt pulse could be latched during t_{ILIL} and serviced as soon as the I bit is cleared.

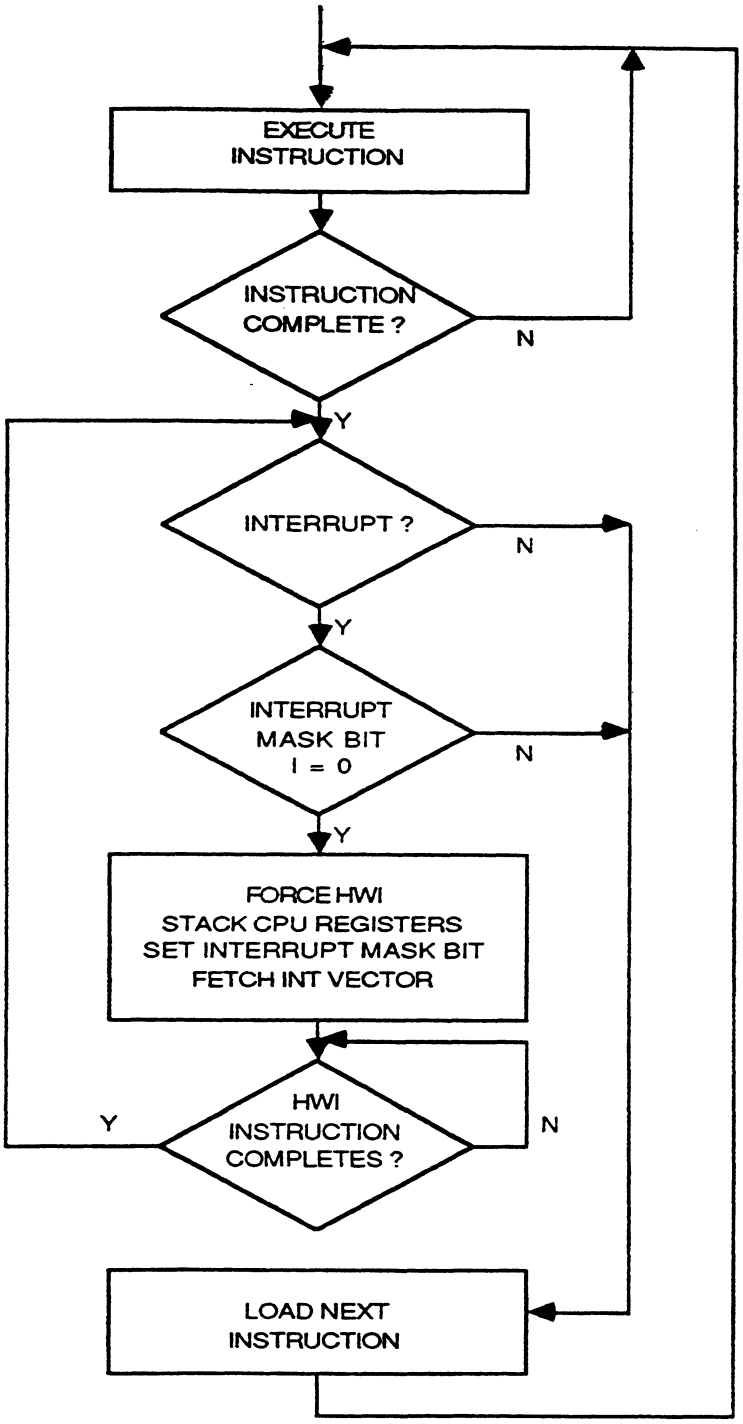


Fig. 3-2 HARDWARE INTERRUPT FLOWCHART

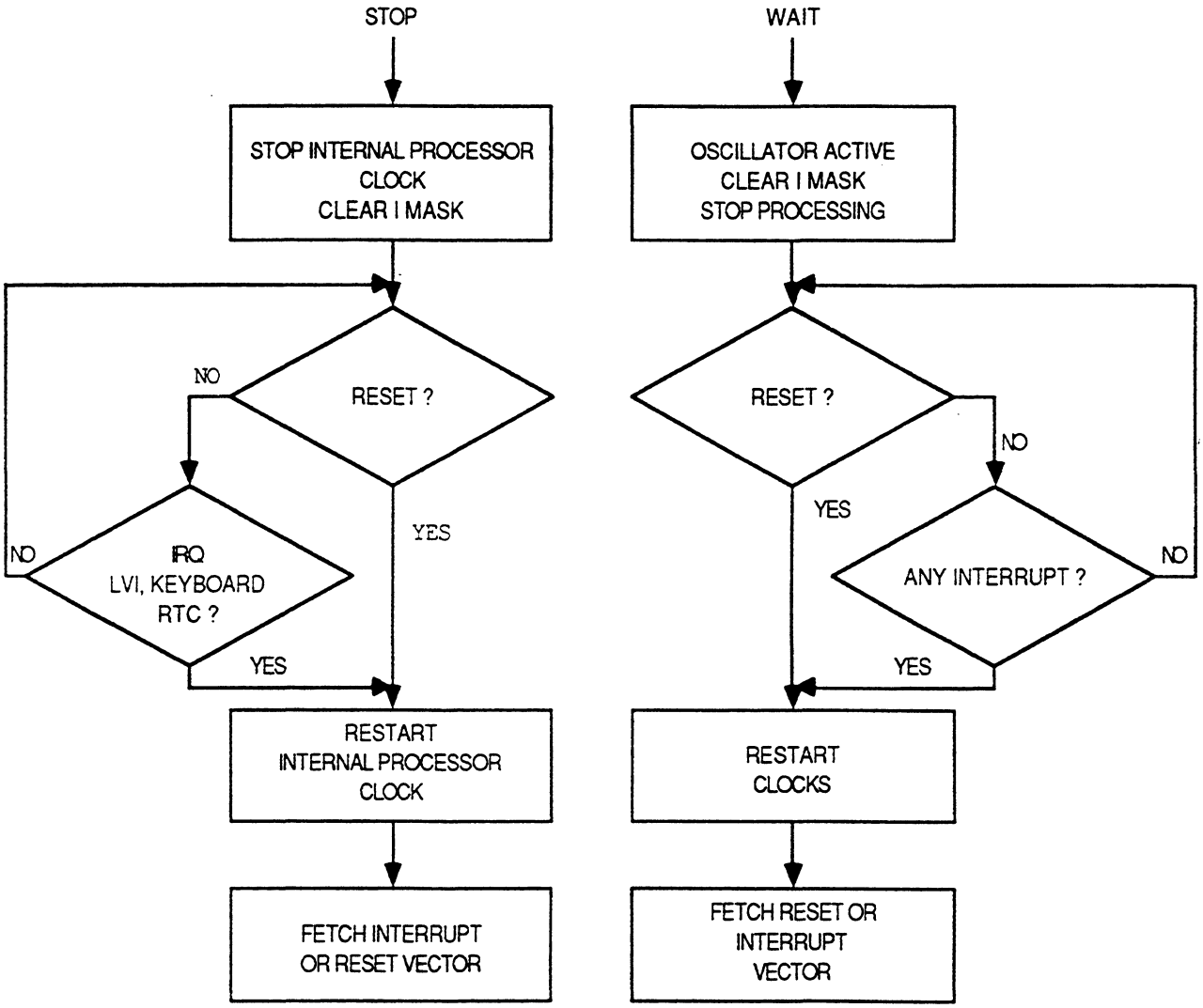
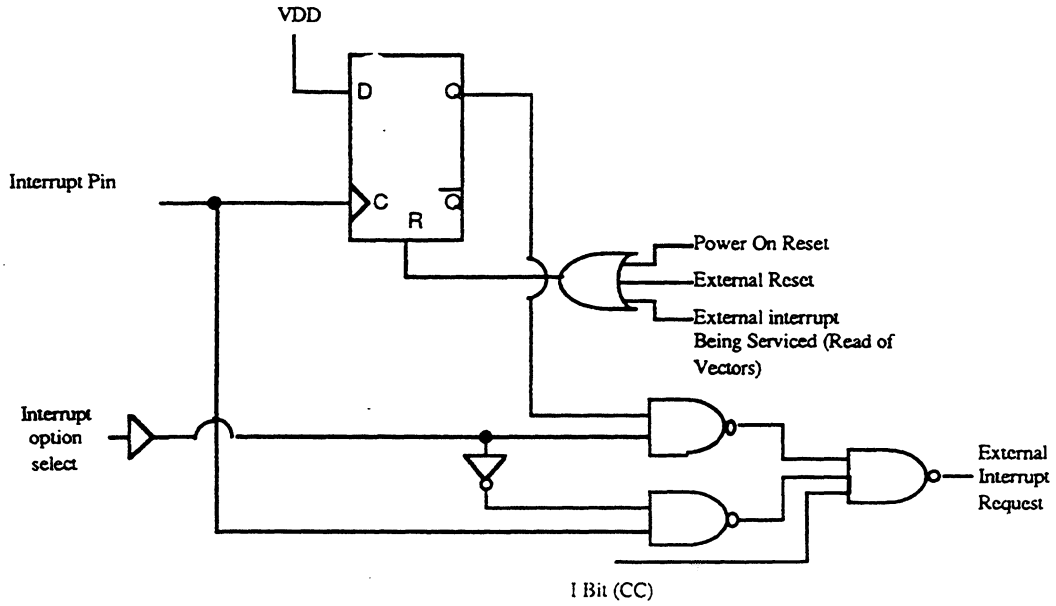
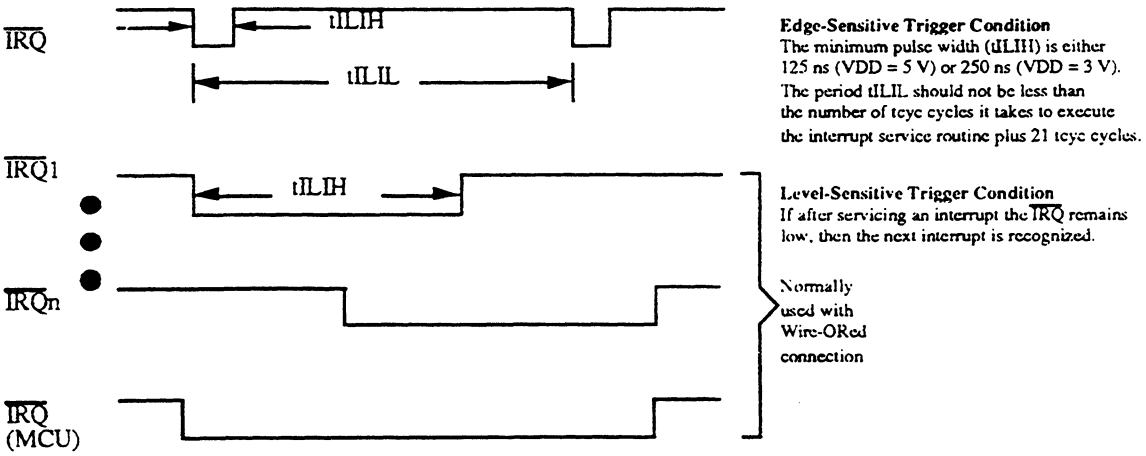


FIG. 3-3 STOP/WAIT FLOWCHARTS



(a) Interrupt Function Diagram



(b) Interrupt Mode Diagram

Fig. 3-4 External Interrupt

3.2.4 TIMER INTERRUPT

The three Timer interrupt flags are found in the three most significant bits of the Timer Status Register (TSR). All three interrupts will vector to the same service routine location.

Each flag bit is defined as follows:

Bit 5 TOF — Timer Overflow Flag - TOD is set during the Counter transition of $FFFF to $0000. It is cleared by reading the TSR (with TOF set) followed by reading the counter least significant byte ($19). Reset does not affect this bit.

Bit 6 OCF — Output Compare Flag - OCF is set when the Output Compare Register matches the Counter Register. It is cleared by reading the TSR (with OCF set) and then accessing the Output Compare Register least significant byte ($17). Reset does not affect this bit.

Bit 7 ICF — Input Capture Flag - ICF is set when a proper edge has been sensed by the input capture edge detector. It is cleared by an CPU read of the TSR (with ICF set) followed by accessing the Input Capture Register least significant byte ($15). Reset does not affect this bit.

All interrupt flags have corresponding enable bits (ICIE, OCIE, and TOIE) found in the Timer Control Register. Reset clears all enable bits preventing an interrupt from occurring. The actual processor interrupt is generated only if the interrupt mask bit of the condition code register is also cleared. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This masks further interrupts until the present one is serviced. The service routine address is specified by the contents of $1FF6 and $1FF7. Refer to **SECTION 4 PROGRAMMABLE TIMER** for additional information about the timer circuitry.

3.2.5 SCI INTERRUPTS

An interrupt in the SCI system will occur when one of the interrupt bits in the SCI Status Register (SCSR) is set, provided the interrupt mask bit of the condition code register is cleared and the enable bit in the SCI Control Register 2 (SCCR2) is enable. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This masks further interrupts until the present one is serviced. The interrupt causes the program counter to vector to memory location $1FF4-$1FF5 in which is stored the service routine's starting address. Software in the serial interrupt service routine must determine the priority and cause of the SCI interrupt by examination of the interrupt flags and status bits located in the SCI Status Register. The general sequence for clearing an interrupt is a software sequence of reading the status register while the flag is set followed by a read or write of an associated register. Refer to **SECTION 5 SERIAL COMMUNICATIONS INTERFACE** for a description of the SCI system and its interrupt.

3.2.6 KEYBOARD INTERRUPT

A keyboard interrupt is enabled when KEYE bit in the control register $09 is set, provided the interrupt mask bit of the condition code register is cleared. When the interrupt (negative edge) is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This masks further interrupts until the present one is serviced. The interrupt causes the program counter to vector to memory location $1FF8 - $1FF9 in which it stored the service routine's starting address. When KEYE bit is set and port A data direction register configures as input port, a ~250 K OHM pull up resistor will associate with each pin of port A. A write to port A resets keyboard interrupt.

Any transition of one of the PORT A pins from 1 to 0 would cause a keyboard interrupt. This interrupt will be latched internally and will not be cleared even if the cause of interrupt pin return to 1 or the KEYE bit is reset to zero. The interrupt flag can only be cleared by performing a 'write' to PORT A. So it is advised that in the keyboard interrupt service routine, the CPU should perform a 'write' to PORT A before it clears the interrupt mask flag or execute an RET instruction.

3.2.7 RTC INTERRUPT

A RTC interrupt is enabled when either RTCE , ALE or SECE bit in the control register $09 is set, provided the interrupt mask bit of the condition code register is cleared. When RTCE bit is set, real time clock will interrupt the CPU once a day. This will occur when hours register in real time clock register changes from twenty-three to zero. When SECE bit is set, real time clock will interrupt CPU once a second. When ALE bit is set, RTC interrupt will occur when the value of hour alarm and hours are equal, and the value of minute alarm and minutes are equal. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This mask further interrupts until the present one is serviced. The interrupt causes the program counter to vector to $1FF2 - $1FF3 in which it stored the service routine's starting address. Interrupt per day, per second or alarm interrupt can be distinguished by RTCF, SECF and ALF flags. In order to reset the interrupt, user is responsible to clear the appropriate flag when execute the interrupt routine. Refer to **SECTION 6.4 REAL TIME CLOCK** for additional information about the Real Time Clock (RTC) interrupt.

3.2.8 LVI INTERRUPT

A LVI interrupt is enabled when the LVIE bit in the control register $09 is set, provided the interrupt mask bit of the condition code register is cleared. When LVIE bit is set, LVI will interrupt the CPU if the following condition is met:

5 volts power supply drop to 3.8 volts (with a tolerance of +/- 15%). The power supply voltage level is sampled once per minute.

When the interrupt is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This mask further interrupts until the present one is serviced. The interrupt causes the program counter to vector to $1FF0 - $1FF1 in which it stored the service routine's starting address.

3.3 LOW POWER MODES

3.3.1 STOP Instruction

The STOP instruction places the MC68HC05L9 in its lowest power consumption mode. In the STOP mode the internal processor clock is turned off, causing all internal processing to be halted; refer to Fig. 3-3. However, if the oscillator in STOP mode mask option is selected 'ON', the crystal oscillator will continue to run and provide clock source to the RTC circuitry. During the STOP mode, the I bit in the condition code register is cleared to enable external interrupt (IRQ), RTC, Keyboard and LVI interrupt. All other registers and memory remain unaltered and all input/output lines remain unchanged. This continues until an external (IRQ), RTC, Keyboard and LVI interrupt, or reset is sensed at which time the internal processor clock is turned on. The external interrupt (IRQ), RTC, Keyboard and LVI interrupt or reset causes the program counter to vector to memory location (depends on the kind of interrupt or reset) which contains the starting address of the interrupt or reset service routine respectively.

The STOP instruction is strongly recommended to be executed within the MC68HC05L9 internal memory address space for lowest power consumption. If the STOP is executed in external memory, a higher current will consume.

3.3.2 WAIT Instruction

The WAIT instruction places the MC68HC05L9 in a low power consumption mode, but the WAIT mode consumes somewhat more power than the STOP mode. In the WAIT mode, the internal clock remains active, and all CPU processing is stopped; however, the programmable timer, serial communications interface system remain active. Refer to Fig. 3-3. During the WAIT mode, the I bit in the condition code register is cleared to enable all interrupts. All other registers and memory remain unaltered and all parallel input/ouptut lines remain unchanged. This continues until any interrupt or reset is sensed. At this time the program counter vectors to the memory location ($1FF0 through $1FFF) which contains the starting address of interrupt or reset service routine.

3.4 DATA RETENTION MODE

The contents of RAM and CPU registers are retained at supply voltages as low as 2.0 Vdc. This is referred to as the data retention mode, where the data is held, but the device is not guaranteed to operate.

SECTION 4
PROGRAMMABLE TIMER

4.1 INTRODUCTION

The timer consists of a 16-bit free-running counter driven by a fixed divide-by-four prescaler. This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from several microseconds to many seconds. Refer to Figure 4-1 for a timer block diagram.

Because the timer has a 16-bit architecture, each specific functional segment (capability) is represented by two registers. These registers contain the high and low byte of that functional segment. Generally, accessing the low byte of a specific timer function allows full control of that function; however, an access of the high byte inhibits that specific timer function until the low byte is also accessed.

NOTE

The I bit in the CCR should be set while manipulating both the high and low byte register of a specific timer function to ensure that an interrupt does not occur.

The programmable timer capabilities are provided by using the following ten addressable 8-bit registers (note the high and low represent the significant of the byte). A description of each register is provided below.

Timer Control Register (TCR) location $12,
Timer Status Register (TSR) location $13,
Input Capture High Register location $14,
Input Capture Low Register location $15,
Output Compare High Register location $16,
Output Compare Low Register location $17,
Counter High Register location $18,
Counter Low Register location $19,
Alternate Counter High Register location $1A, and
Alternate Counter Low Register location $1B.

4.2 COUNTER

The key element in the programmable timer is a 16-bit, free-running counter or counter register, preceded by a prescaler that divides the internal processor clock by four. The prescaler gives the timer a resolution of 3.215 microseconds if the internal bus clock is 1.244 MHz. The counter is incremented during the low portion of the internal bus clock. Software can read the counter at any time without affecting its value.

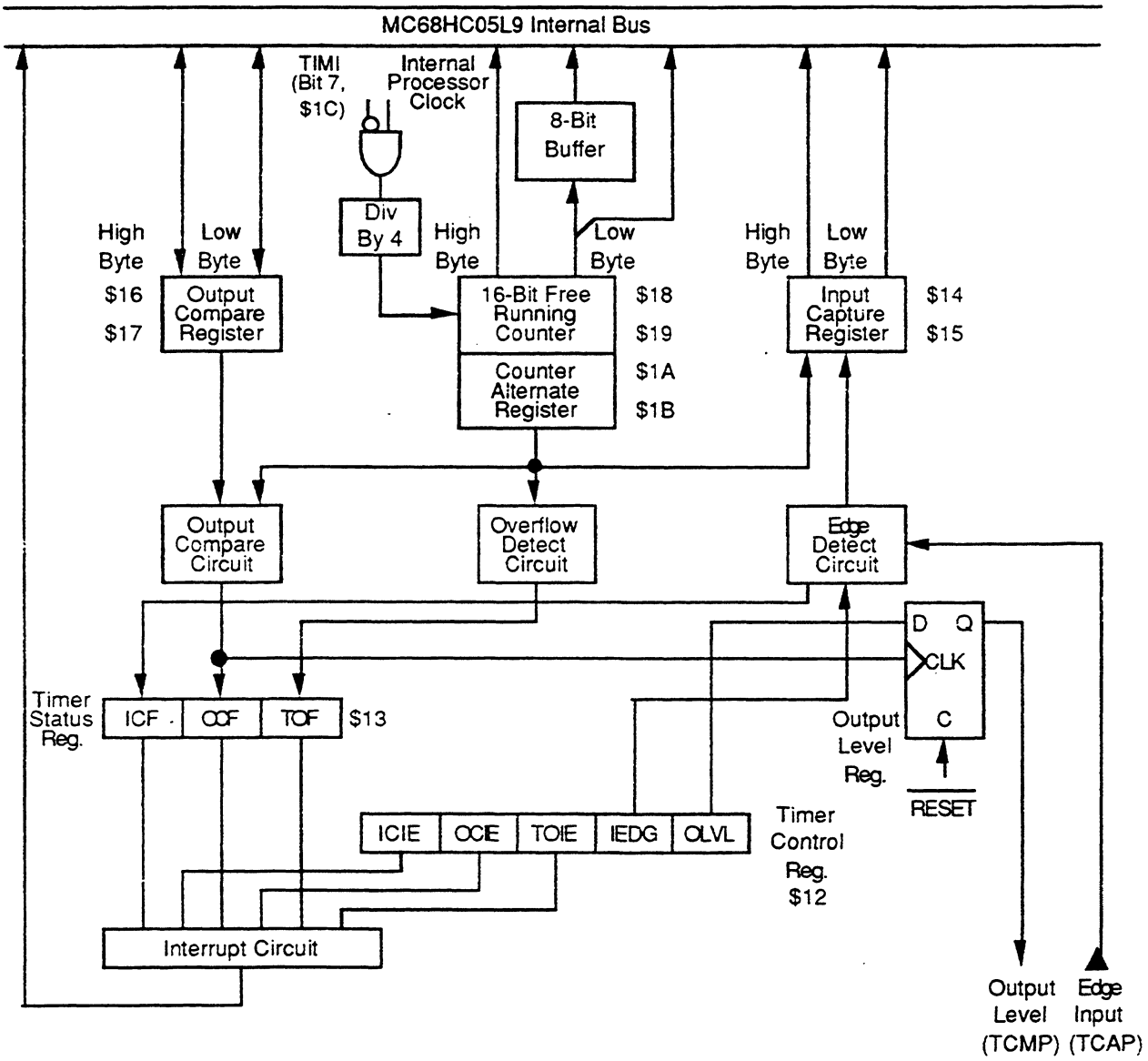
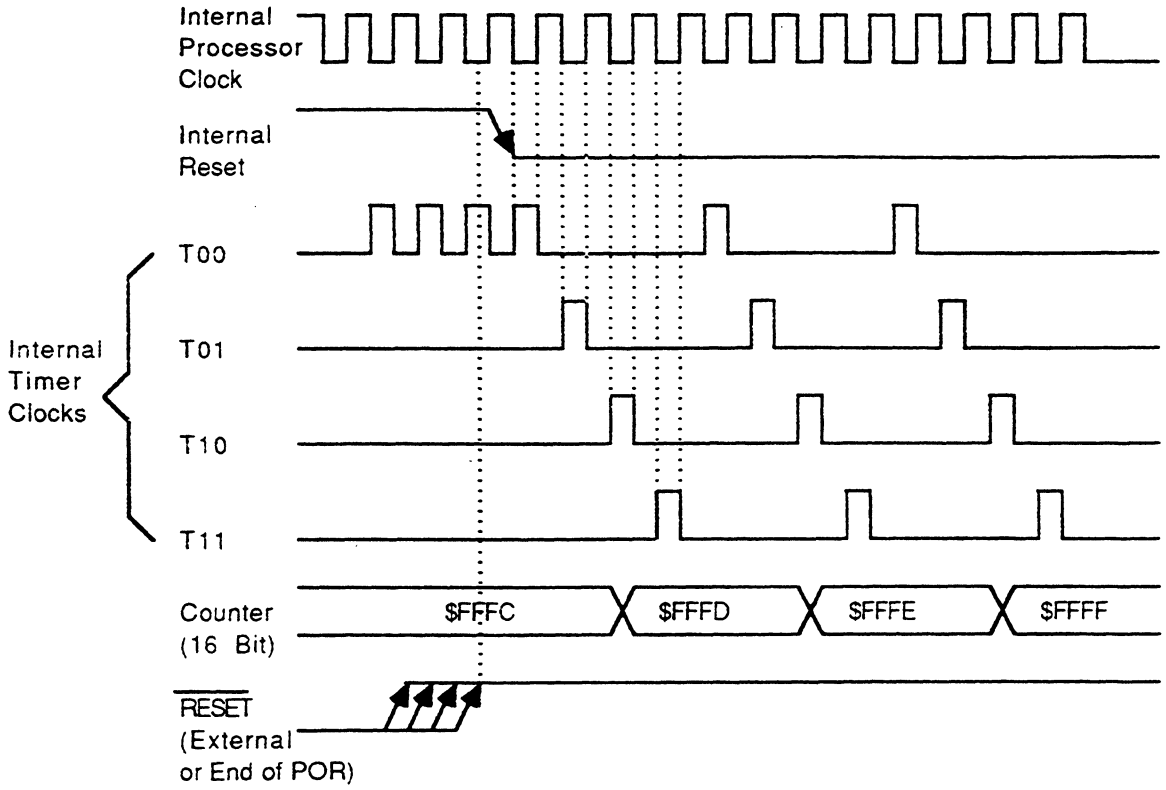
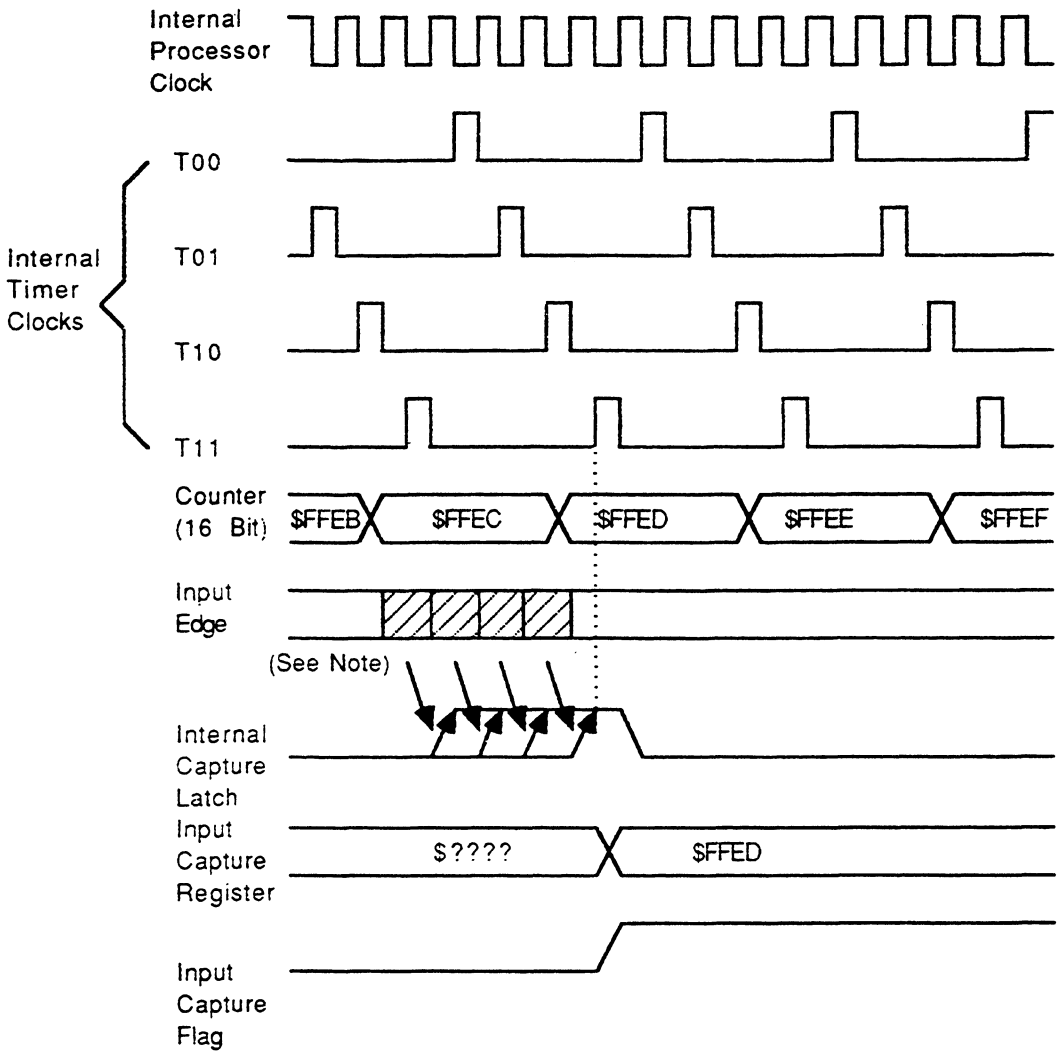


Fig. 4-1 Programmable Timer Block Diagram



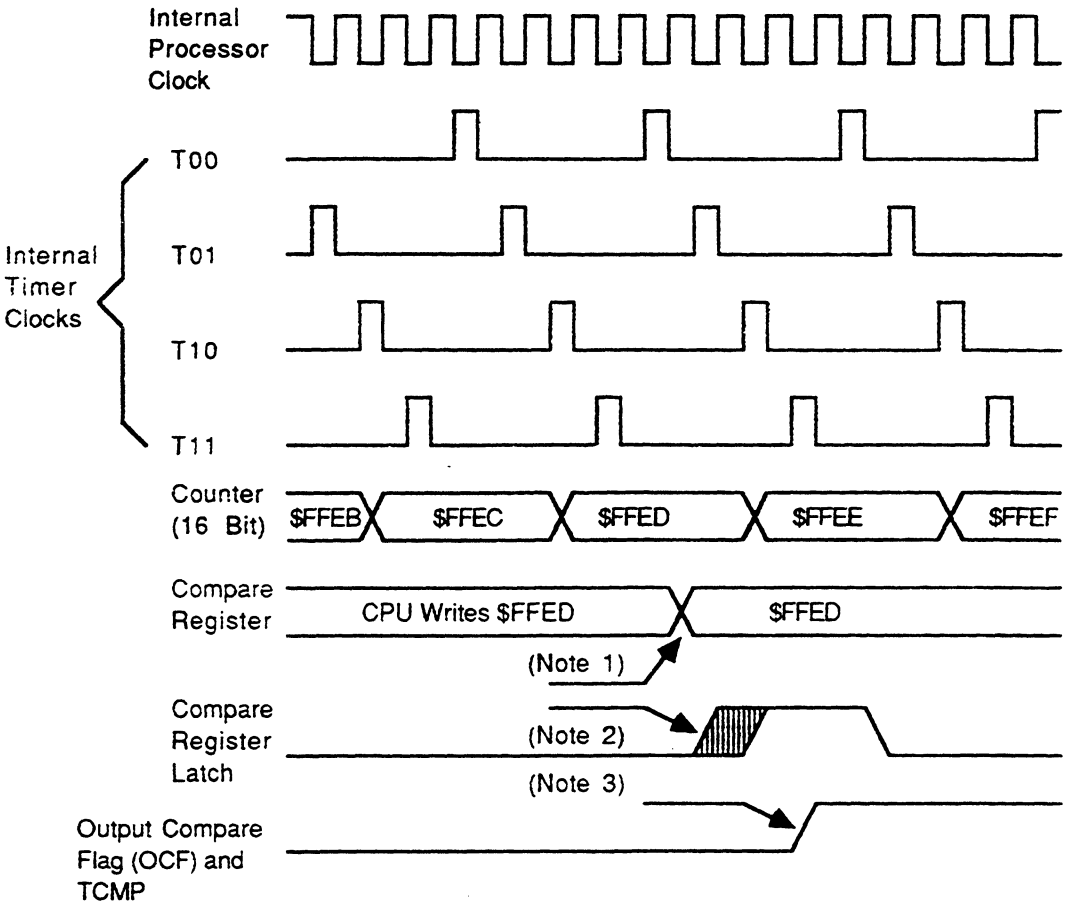
NOTE: The Counter Register and Timer Control Register are the only ones affected by $\overline{\text{RESET}}$

FIG. 4-2 Timer State Timing Diagram For Reset



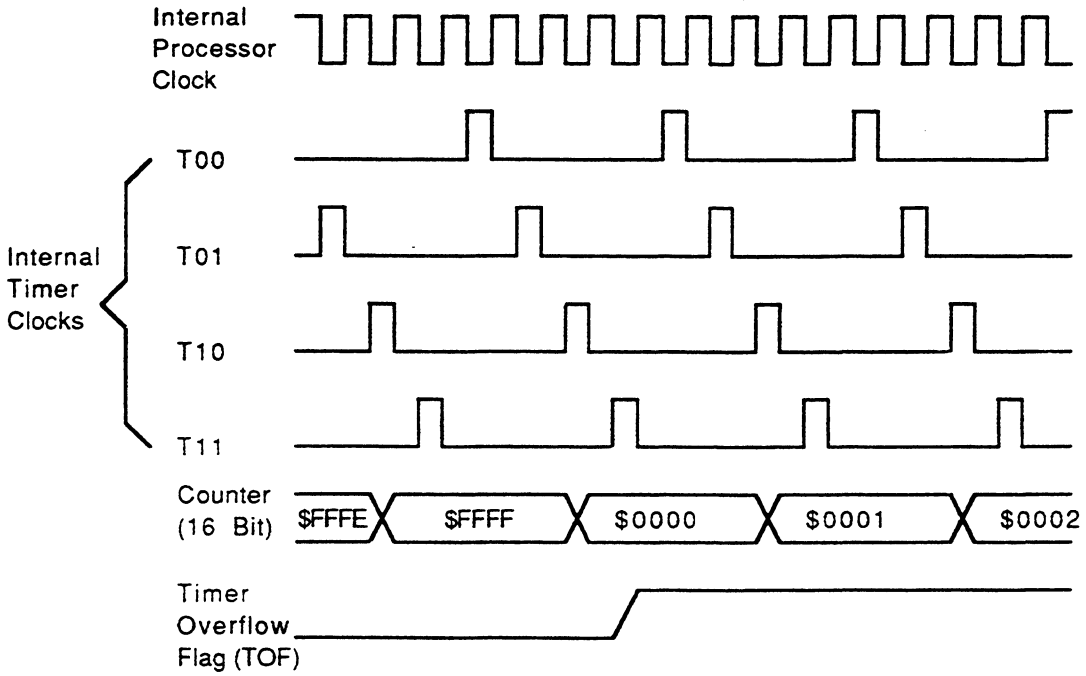
NOTE: If the input edge occurs in the shaded area from one timer state T10 to the other timer state T10 the input capture flag is set during the next state T11.

FIG. 4-3 Timer State Timing Diagram For Input Capture



NOTES: 1. The CPU write to the compare register may take place at any time, but a compare only occurs at timer state T01. Thus, a 4-cycle difference may exist between the write to the compare register and the actual compare.
2. Internal compare takes place during timer state T01.
3. OCF is set at timer state T11 which follows the comparison match ($FFED in this example).

Fig. 4-4 Timer State Timing Diagram For Output Compare



NOTE: The TOF bit is set at timer state T11 (transition of counter from $FFFF to $0000). It is cleared by a read of the timer status register during the internal processor clock high time followed by a read of the counter low register.

Fig. 4-5 Timer State Diagram For Timer Overflow

The double-byte, free-running counter can be read from either of two locations, $18-$19 (counter register) or $1A-$1B (counter alternate register). A read from only the least significant byte (LSB) of the free-running counter ($19, $1B) receives the count value at the time of the read. If a read of the free-running counter or counter alternate register first addresses the most significant byte (MSB) ($18, $1A), the LSB ($19, $1B) is transferred to a buffer. This buffer value remains fixed after the first MSB read, even if the user reads the MSB several times. This buffer is accessed when reading the free-running counter or counter alternate register LSB ($19 or $1B) and, thus, completes a read sequence of the total counter value. In reading either the free-running counter or counter alternate register, if the MSB is read, the LSB must also be read to complete the sequence.

The counter alternate register differs from the counter register in one respect: a read of the counter register MSB can clear the timer overflow flag (TOF). Therefore, the counter alternate register can be read at any time without the possibility of missing timer overflow interrupts due to clearing of the TOF.

The free-running counter is configured to $FFFC during reset and is always a read-only register. During a power-on reset, the counter is also preset to $FFFC and begins running after the oscillator start-up delay. Because the free-running counter is 16 bits preceded by a fixed divide-by-four prescaler, the value in the free-running counter repeats every 262,144 internal bus clock cycles. When the counter rolls over from $FFFF to $0000, the TOF bit is set. An interrupt can also be enabled when counter rollover occurs by setting its interrupt enable bit (TOIE).

In some particular timing control applications it may be desirable to reset the 16-bit free running counter under software control. When the low byte of the counter ($19 or $1B) is written to, the counter is configured to its reset value ($FFFC).

The divide-by-4 prescaler is also reset and the counter resumes normal counting operation. All of the flags and enable bits remain unaltered by this operation. If access has previously been made to the high byte of the free running counter ($18 or $1A), then the reset counter operation terminates the access sequence.

4.3 OUTPUT COMPARE REGISTER

The 16-bit output compare register is made up of two 8-bit registers at locations $16 (MSB) and $17 (LSB). The output compare register is used for several purposes, such as indicating when a period of time has elapsed. All bits are readable and writable and are not altered by the timer hardware or reset. If the compare function is not needed, the two bytes of the output compare register can be used as storage locations.

The output compare register contents are compared with the contents of the free-running counter continually, and if a match is found, the corresponding output compare flag (OCF) bit is set and the corresponding output level (OLVL) bit is clocked to an output level register. The output compare register values and the output level bit should be changed after each successful comparison to establish a new elapsed timeout. An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit (OCIE) is set.

After a processor write cycle to the output compare register containing the MSB ($16), the output compare function is inhibited until the LSB ($17) is also written. The user must write both bytes (locations) if the MSB is written first. A write made only to the LSB ($17) will not inhibit the compare function. The free-running counter is updated every four internal bus clock cycles. The minimum time required to update the output compare register is a function of the program rather than the internal hardware.

The processor can write to either byte of the output compare register without affecting the other byte. The output level (OLVL) bit is clocked to the output level register regardless of whether the output compare flag (OCF) is set or clear.

4.4 INPUT CAPTURE REGISTER

Two 8-bit registers, which make up the 16-bit input capture register, are read-only and are used to latch the value of the free-running counter after the corresponding input capture edge detector senses a defined transition. The level transition which triggers the counter transfer is defined by the corresponding input edge bit (IEDG). Reset does not affect the contents of the input capture register.

The result obtained by an input capture will be one more than the value of the free-running counter on the rising edge of the internal bus clock preceding the external transition. This delay is required for internal synchronization. Resolution is one count of the free-running counter, which is four internal bus clock cycles.

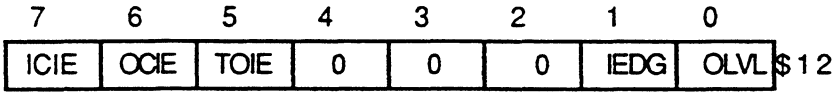
The free-running counter contents are transferred to the input capture register on each proper signal transition regardless of whether the input capture flag (ICF) is set or clear. The input capture register always contains the free-running counter value that corresponds to the most recent input capture.

After a read of the input capture register ($14) MSB, the counter transfer is inhibited until the LSB ($15) is also read. This characteristic causes the time used in the input capture software routine and its interaction with the main program to determine the minimum pulse period.

A read of the input capture register LSB ($15) does not inhibit the free-running counter transfer since they occur on opposite edges of the internal bus clock.

4.5 TIMER CONTROL REGISTER (TCR)

The TCR is a read/write register containing five control bits. Three bits control interrupts associated with each of the three flag bits found in the timer status register (discussed below). The other two bits control: 1) which edge is significant to the input capture edge detector (ie., negative or positive), and 2) the next value to be clocked to the output level register in response to a successful output compare. The timer control register and the free running counter are the only sections of the timer affected by reset. The TCMP pin is forced low during external reset and stays low until a valid compare changes it to high. The timer control register is illustrated below by a definition of each bit.



B7, ICIE — If the input capture interrupt enable (ICIE) bit is set, a timer interrupt is enable when the ICF status flag (in the timer status register) is set. If the ICIE bit is cleared, the interrupt is inhibited. The ICIE bit is cleared by reset.

B6, OCIE — If the output compare interrupt enable (OCIE) bit is set, a timer interrupt is enabled whenever the OCF status flag is set. If the OCIE bit is cleared, the interrupt is inhibited. The OCIE bit is cleared by reset.

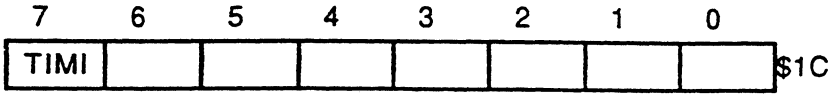
B5, TOIE — If the timer overflow interrupt enable (TOIE) bit is set, a timer interrupt is enabled whenever the TOF status flag (in the timer status register) is set. If the TOIE bit is cleared, the interrupt is inhibited. The TOIE bit is cleared by reset.

B1, IEDG — The value of the input edge (IEDG) bit determines which level transition on TCAP pin will trigger a free running counter transfer to the input capture register. Reset does not affect the IEDG bit.

0 = negative edge
1 = positive edge

B0, OLVL — The value of the output level (OLVL) bit is clocked into the output level register by the next successful output compare and will appear at TCMP pin. This bit and the output level register are cleared by reset.

0 = low output
1 = high output



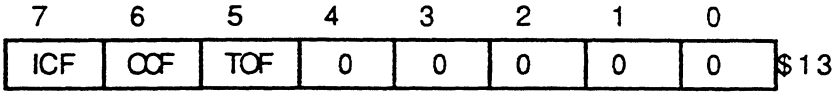
B7, TIMI — When this bit is set, timer is inhibit. This bit is cleared by power on reset or external reset.

4.6 TIMER STATUS REGISTER (TSR)

The TSR is a read-only register containing three status flag bits. These three bits indicate the following:

1. A proper transition has taken place at TCAP pin with an accompanying transfer of the free running counter contents to the input capture register,
2. A match has been found between the free running counter and the output compare register, and
3. A free running counter transition from $FFFF to $0000 has been sensed (timer overflow).

The timer status register is illustrated below followed by a definition of each bit. Refer to timing diagrams shown in Figures 4-2, 4-3, and 4-4 for timing relationship to the timer status register bits.



B7, ICF — The input capture flag (ICF) is set when a proper edge has been sensed by the input capture edge detector. It is cleared by a processor access of the timer status register (with ICF set) followed by accessing the low byte ($15) of the input capture register. Reset does not affect the input compare flag.

B6, OCF — The output compare flag (OCF) is set when the output compare register contents matches the contents of the free running counter. The OCF is cleared by accessing the timer status register (with OCF set) and then accessing the low byte ($17) of the output compare register. Reset does not affect the output compare flag.

B5, TOF — The timer overflow flag (TOF) bit is set by transition of the free running counter from $FFFF to $0000. It is cleared by accessing the timer status register (with TOF set) followed by an access of the free running counter least significant byte ($19). Reset does not affect the TOF bit.

Accessing the timer status register satisfies the first condition required to clear status bits. The remaining step is to access the register corresponding to the status bit.

A problem can occur when using the timer overflow function and reading the free-running counter at random times to measure an elapsed time. Without incorporating the proper precautions into software, the timer overflow flag could unintentionally be cleared if: 1)The timer status register is read or written when TOF is set, and 2)The LSB of the free-running counter is read but not for the purpose of servicing the flag. The counter alternate register at address $1A and $1B contains the same value as the free-running counter (at address $18 and $19); therefore, this alternate register can be read at any time without affecting the timer overflow flag in the timer status register.

During STOP and WAIT instructions, the programmable timer functions as follows: during the wait mode, the timer continues to operate normally and may generate an interrupt to trigger the CPU out of the wait state; during the stop mode, the timer holds at its current state, retaining all data, and resumes operation from this point when external interrupt (IRQ), RTC, Keyboard or LVI interrupt is received.

SECTION 5
SERIAL COMMUNICATIONS INTERFACE (SCI)

5.1 INTRODUCTION

A full-duplex asynchronous SCI is provided with a standard NRZ format and a variety of baud rates. The SCI transmitter and receiver are functionally independent but use the same data format and baud rate. The terms baud and bit rate are used synonymously in the following description.

5.1.1 SCI TWO-WIRE SYSTEM FEATURES

* Standard NRZ (mark/space) format
* Advanced error detection method includes noise detection for noise duration of up to 1/16 bit time
* Full-duplex operation (simultaneous transmit and receive)
* Software programmable for different baud rates
* Software-selectable word length (eight or nine bit words)
* Separate transmitter and receiver enable bits
* SCI may be interrupt driven
* Four separate interrupt conditions

5.1.2 SCI RECEIVER FEATURES

* Receiver wake-up function (idle or address bit)
* Idle line detect
* Framing error detect
* Noise detect
* Overrun detect
* Receiver data register full flag

5.1.3 SCI TRANSMITTER FEATURES

* Transmit data register empty flag
* Transmit complete flag
* Break send

Any SCI two-wire system requires receive data in (RDI) and transmit data out (TDO).

5.2 DATA FORMAT

Receive data in (RDI) or transmit data out (TDO) is the serial data presented between the internal data bus and the output pin (TDO) and between the input pin (RDI) and the internal data bus. Data format is as shown for the NRZ in Fig. 5-1 and must meet the following criteria:

1. A high level indicates a logic one and a low level indicates a logic zero.
2. The idle line is in a high (logic one) state prior to transmission/reception of a message.
3. A start bit (logic zero) is transmitted/received indicating the start of a message.
4. The data is transmitted and received least-significant-bit first.
5. A stop bit (high in the tenth or eleventh bit position) indicates the byte is complete.
6. A break is defined as the transmission or reception of a low (logic zero) for some multiple of the data format.

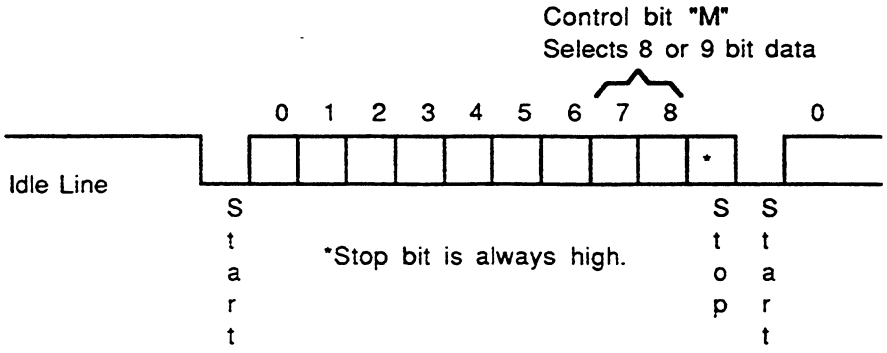


FIG. 5-1 Data Format

5.3 WAKE-UP FEATURE

In a typical multiprocessor configuration, the software protocol will usually identify the addressee(s) at the beginning of the message. To permit uninterested MPUs to ignore the remainder of the message, a wake-up feature is included, whereby all further SCI receiver flag (and interrupt) processing can be inhibited until its data line returns to the idle state. An SCI receiver is re-enabled by an idle string of at least ten (or eleven) consecutive ones. Software for the transmitter must provide for the required idle string between consecutive messages and prevent it from occurring within messages.

A second wake-up method is available in which sleeping SCI receivers can be awakened by a logic one in the high-order bit of a received character.

5.4 RECEIVE DATA IN

Receive data in (RDI) is the serial data which is presented from the input pin via the SCI to the receive data register (RDR). While waiting for a start bit, the receiver samples the input at a rate 16 times higher than the set baud rate. This increased rate is referred to as the RT rate. When the input (idle) line is detected low, it is tested for three more sample times. If at least two of these three samples detect a logic low, a valid start bit is assumed to be detected. If in two or more samples, a logic high is detected, the line is assumed to be idle. The receive clock generator is controlled by the baud rate register (see Fig. 5-6 and 5-7); however, the SCI is synchronized by the start bit independent of the transmitter.

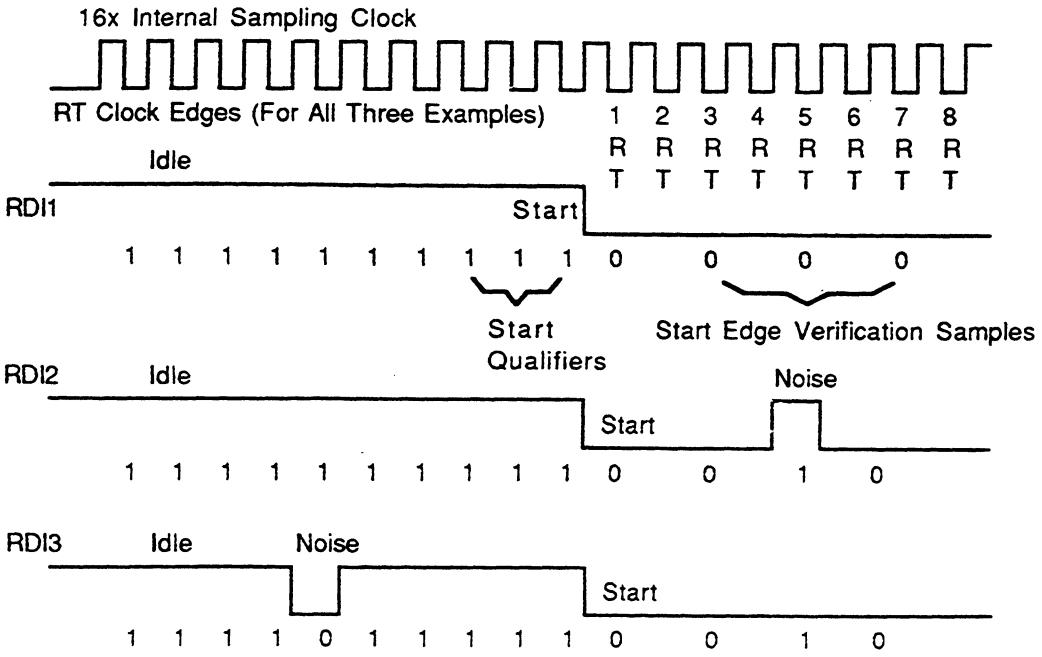


FIG. 5-2 Example of Start-Bit Sampling Technique

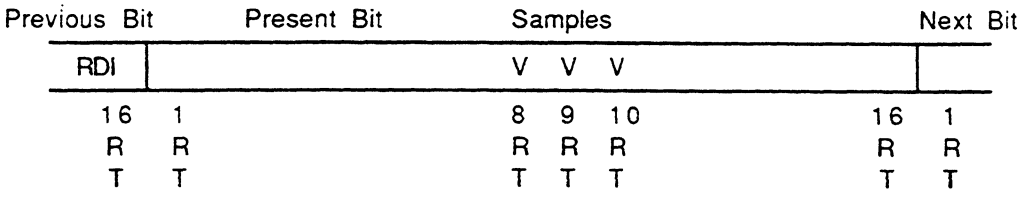


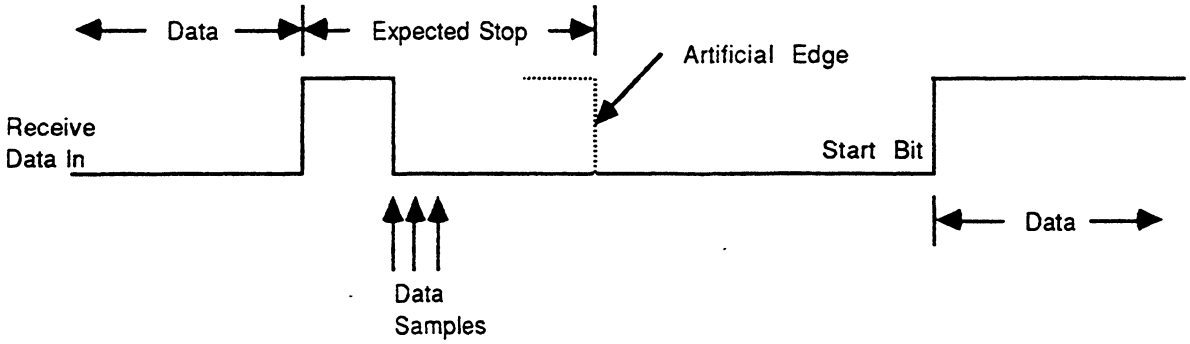
FIG. 5-3 Sampling Technique Used on All Bits

Once a valid start bit is detected, the start bit, each data bit, and the stop bit are each sampled three times. The value of the bit is determined by voting logic, which takes the value of a majority of samples. A noise flag is set when all three samples on a valid start bit, data bit, or stop bit do not agree. A noise flag is also set when the start verification samples do not agree.

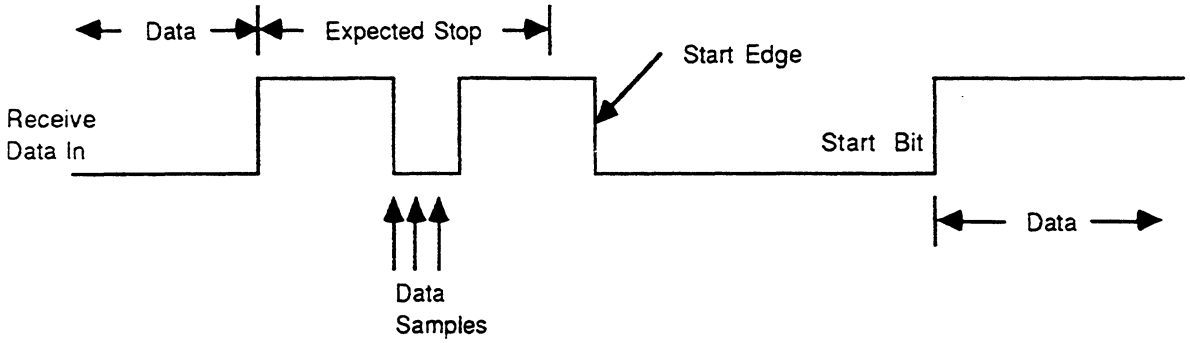
5.5 START BIT DETECTION FOLLOWING A FRAMING ERROR

If there has been a framing error (FE) without detection of a break (10 zeros for 8-bit format or 11 zeros for a 9-bit format), the circuit continues to operate as if there actually were a stop bit, and the start edge will be placed artificially. The last bit received in the data shift register is inverted to a logic one, and the three logic-one start qualifiers (shown in Fig. 5-2) are forced into the sample shift register during the interval when detection of a start bit is anticipated (see Fig. 5-4); therefore, the start bit will be accepted no sooner than it is anticipated.

If the receiver detects that a break (RDRF=1, FE=1, receiver data register=$00) produced the framing error, the start bit will not be artificially induced, and the receiver must actually receive a logic one before start. See Fig. 5-5.



(a) Case 1, Receive Line Low During Artificial Edge



(b) Case 2, Receive Line High During Start Edge

FIG. 5-4 SCI Artificial Start Following A Framing Error

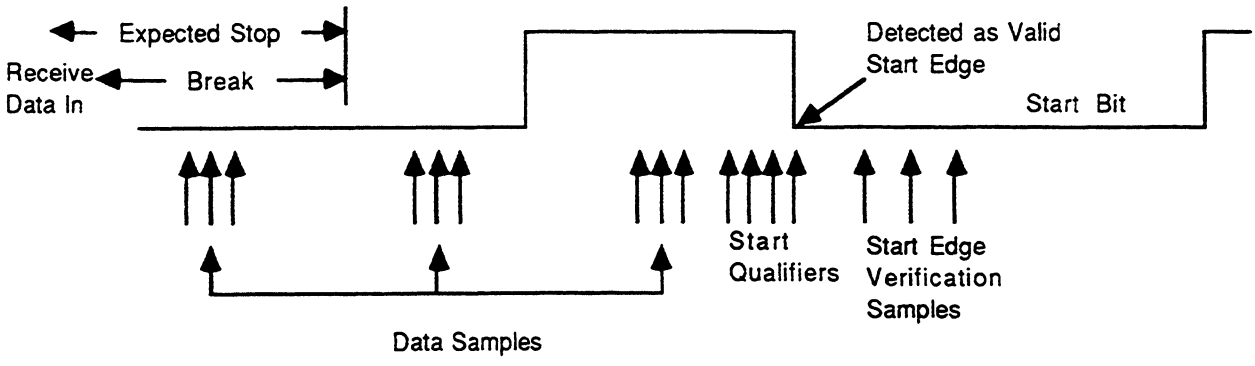
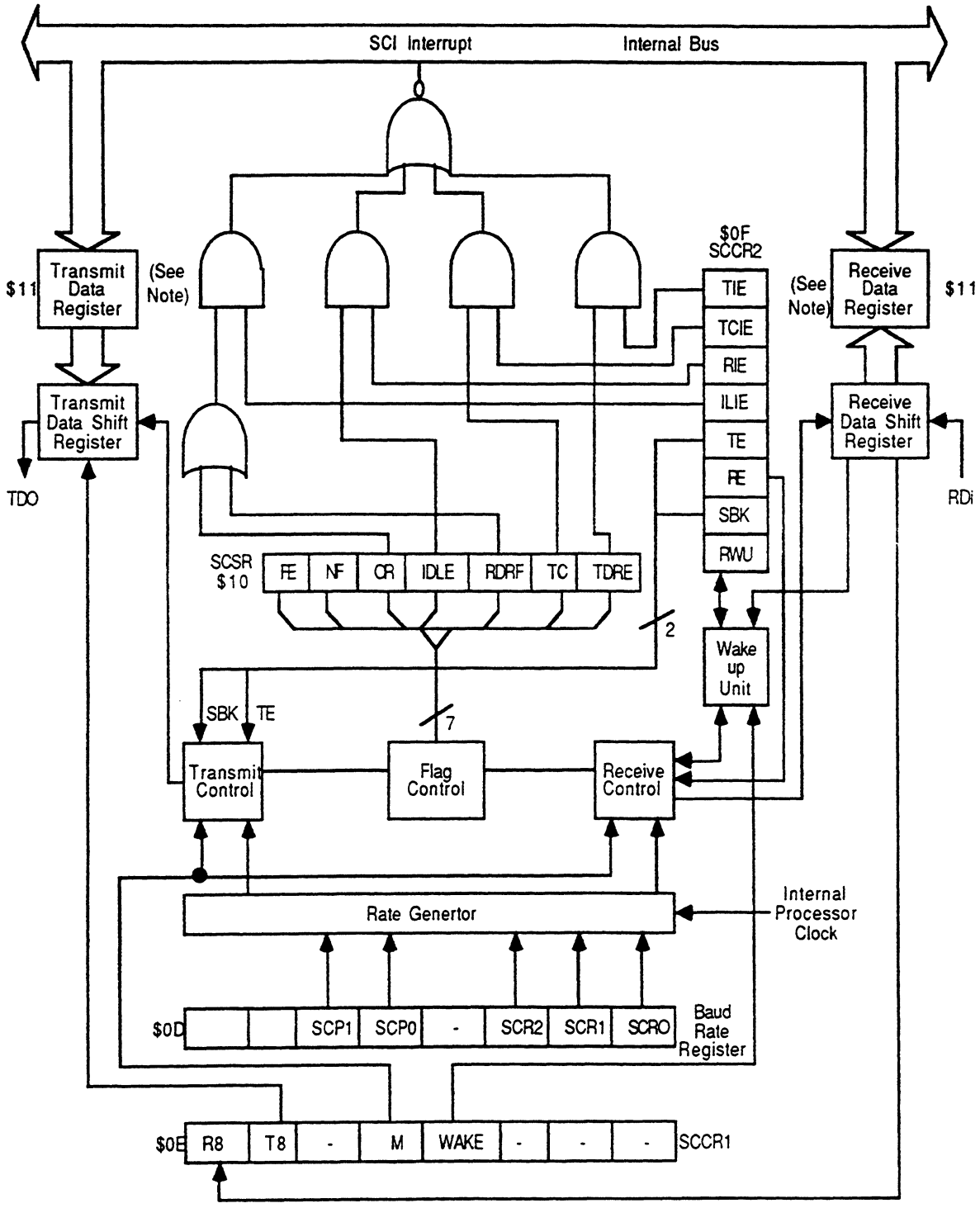


FIG. 5-5 SCI Start Bit Following A Break



NOTE: The Serial Data Communications Data Register (SCDAT) is controlled by the R/W signal. It is the transmit data register when written and received data register when read.

Fig. 5-6 Serial Communications Interface Block Diagram

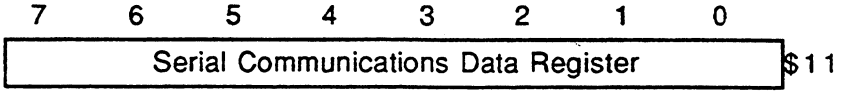
5.6 TRANSMIT DATA OUT (TDO)

Transmit data out is the serial data which is presented from the internal data bus via the SCI and then to the output pin. Data format is as discussed above and shown in Fig. 5-1. The transmitter generates a bit time by using a derivative of the RT clock, thus producing a transmission rate equal to 1/16 that of the receiver sample clock.

5.7 REGISTERS

There are five registers used in the SCI; the internal configuration of these registers is discussed in the following paragraphs. A block diagram of the SCI system is shown in Fig. 5-6.

5.7.1 Serial Communications Data Register (SCDAT)

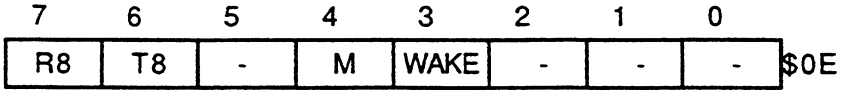


The serial communications data register performs two functions in the serial communications interface; i.e. it acts as the receive data register when it is read and as the transmit data register when it is written. Fig. 5-6 shows this register as two separate registers, namely: the receive data register (RDR) and the transmit data register (TDR). As shown in Fig. 5-6, the TDR (transmit data register) provides the parallel interface from the internal data bus to the transmit shift register and the receive data register (RDR) provides the interface from the receive shift register to the internal data bus.

When SCDAT is read, it becomes the receive data register and contains the last byte of data received. The receive data register, represented above, is a read-only register containing the last byte of data received from the shift register for the internal data bus. The RDRF bit (receive data register full bit in the serial communications status register) is set to indicate that a byte has been transferred from the input serial shift register to the serial communications data register. The transfer is synchronized with the receiver bit rate clock (from the receive control) as shown in Fig. 5-6. All data is received least-significant-bit first.

When SCDAT is written, it becomes the transmit data register and contains the next byte of data to be transmitted. The transmit data register, also represented above, is a write-only register containing the next byte of data to be applied to the transmit shift register from the internal data bus. As long as the transmitter is enabled, data stored in the serial communications data register is transferred to the transmit shift register (after the current byte in the shift register has been transmitted). The transfer from the SCDAT to the transmit shift register is synchronized with the bit rate clock (from the transmit control) as shown in Fig. 5-6. All data is transmitted least-significant-bit first.

5.7.2 Serial Communications Control Register 1 (SCCR1)



The serial communications control register 1 (SCCR1) provides the control bits which: 1) determine the word length (either 8 or 9 bits), and 2) selects the method used for the wake-up feature. Bits 6 and 7 provide a location for storing the ninth bit for longer bytes.

B7, R8 — If the M bit is a one, then this bit provides a storage location for the ninth bit in the receive data byte. Reset does not affect this bit.

B6, T8 — If the M bit is a one, then this bit provides a storage location for the ninth bit in the transmit data byte. Reset does not affect this bit.

B4, M — The option of the word length is selected by the configuration of this bit and is shown below. Reset does not affect this bit.
0 = 1 start bit, 8 data bits, 1 stop bit
1 = 1 start bit, 9 data bits, 1 stop bit

B3, WAKE — This bit allows the user to select the method for receive "wake up". If the WAKE bit is a logic zero, an idle line condition will "wake up" the receiver. If the WAKE bit is set to a logic one, the system acknowledges an address bit (most significant bit). The address bit is dependent on both the WAKE bit and the M bit level (table shown below). (Additionally, the receiver does not use the wake-up feature unless the RWU control bit in serial communications control register 2 is set as discussed below.) Reset does not affect this bit.

Wake	M	Method of Receiver "Wake-Up"
0	X	Detection of an idle line allows the next data byte received to cause the receive data register to fill and produce an RDRF flag.
1	0	Detection of a received one in the eighth data bit allows an RDRF flag and associated error flags.
1	1	Detection of a received one in the ninth data bit allows an RDRF flag and associated error flags.

5.7.3 Serial Communications Control Register 2 (SCCR2)

7	6	5	4	3	2	1	0	
TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	$0F

The serial communications control register 2 (SCCR2) provides the control bits which: individually enable/disable the transmitter or receiver, enable the system interrupts, and provide the wake-up enable bit and a "send break code" bit. Each of these bits is described below. (The individual flags are discussed in the 5.7.4 Serial Communications Status Register).

B7, TIE — When the transmit interrupt enable bit is set, the SCI interrupt occurs provided TDRE is set (see Fig. 5-6). When TIE is cleared, the TDRE interrupt is disabled. Reset clears the TIE bit.

B6, TCIE — When the transmission complete interrupt enable bit is set, the SCI interrupt occurs provided TC is set (see Fig. 5-6). When TCIE is clear, the TC interrupt is disabled. Reset clears the TCIE bit.

B5, RIE — When the receive interrupt enable bit is set, the SCI interrupt occurs provided OR is set or RDRF is set (see Fig. 5-6). When RIE is cleared, the OR and RDRF interrupts are disabled. Reset clears the RIE bit.

B4, ILIE — When the idle line interrupt enable bit is set, the SCI interrupt occurs provided IDLE is set (see Fig. 5-6). When ILIE is cleared, the IDLE interrupt is disabled. Reset clears the ILIE bit.

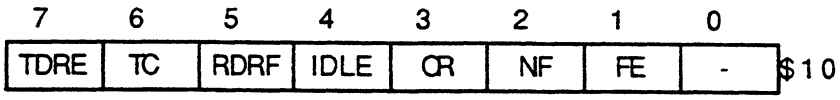
B3, TE — When the transmit enable bit is set, the transmit shift register output is applied to the TDO line. Depending on the state of control bit M in serial communications control register 1, a preamble of 10 (M=0) or 11 (M=1) consecutive ones is transmitted when software sets the TE bit from a cleared state. If a transmission is in progress, and TE is written to a zero, then the transmitter will wait until after the present byte has been transmitted before placing the TDO pin in the idle high-impedance state. If the TE bit has been written to a zero and then set to a one before the current byte is transmitted, the transmitter will wait until that byte is transmitted and will then initiate transmission of a new preamble. After the preamble is transmitted, and provided the TDRE bit is set (no new data to transmit), the line remains idle (driven high while TE = 1); otherwise, normal transmission occurs. This function allows the user to "neatly" terminate a transmission sequence. After loading the last byte in the serial communications data register and receiving the interrupt from TDRE, indicating the data has been transferred into the shift register, the user should clear TE. The last byte will then be transmitted and the line will go idle (high impedance). Reset clears the TE bit.

B2, RE — When the receive enable bit is set, the receiver is enabled. When RE is cleared, the receiver is disabled and all of the status bits associated with the receiver (RDRF, IDLE, OR, NF, and FE) are inhibited. Reset clears the RE bit.

B1, RWU — When the receiver wake-up bit is set, it enables the "wake up" function. The type of "wake up" mode for the receiver is determined by the WAKE bit discussed above (in the SCCR1). When the RWU bit is set, no status flags will be set. Flags which were set previously will not be cleared with RWU is set. If the WAKE bit is cleared, RWU is cleared after receiving 10 (M=0) or 11 (M=1) consecutive ones. Under these conditions, RWU cannot be set if the line is idle. If the WAKE bit is set, RWU is cleared after receiving an address bit. The RDRF flag will then be set and the address byte will be stored in the receiver data register. Reset clears the RWU bit.

B0, SBK — When the send break bit is set the transmitter sends zeros in some number equal to a multiple of the data format bits. If the SBK bit is toggled set and clear, the transmitter sends 10 (M=0) or 11 (M=1) zeros and then reverts to idle or sending data. The actual number of zeros sent when SBK is toggled depends on the data format set by the M bit in the serial communications control register 1; therefore, the break code will be synchronous with respect to the data stream. At the completion of the break code, the transmitter sends at least one high bit to guarantee recognition of a valid start bit. Reset clears the SBK bit.

5.7.4 Serial Communications Status Register (SCSR)



The serial communications status register (SCSR) provides inputs to the interrupt logic circuits for generation of the SCI system interrupt. In addition, a noise flag bit and a framing error bit are also contained in the SCSR.

B7, TDRE The transmit data register empty bit is set to indicate that the contents of the serial communications data register have been transferred to the transmit serial shift register. If the TDRE bit is clear, it indicates that the transfer has not yet occurred and a write to the serial communications data register will overwrite the previous value. The TDRE bit is cleared by accessing the serial communications status register (with TDRE set), followed by writing to the serial communications data register. Data can not be transmitted unless the serial communications status register is accessed before writing to the serial communications data register to clear the TDRE flag bit. Reset sets the TDRE bit.

B6, TC The transmit complete bit is set at the end of a data frame, preamble, or break condition if:

1. TE = 1, TDRE = 1, and no pending data, preamble, or break is to be transmitted; or
2. TE = 0, and the data preamble, or break (in the transmit shift register) has been transmitted.

The TC bit is a status flag which indicates that one of the above conditions has occurred. The TC bit is cleared by accessing the serial communications status register (with TC set), followed by writing to the serial communications data register. It does not inhibit the transmitter function in any way. Reset sets the TC bit.

B5, RDRF When the receive data register full bit is set, it indicates that the receiver serial shift register is transferred to the serial communications data register. If multiple errors are detected in any one received word, the NF, FE, and RDRF bits will be affected as appropriate during the same clock cycle. The RDRF bit is cleared when the serial communications status register is accessed (with RDRF set) followed by a read of the serial communications data register. Reset clears the RDRF bit.

B4, IDLE When the idle line detect bit is set, it indicates that a receiver idle line is detected (receipt of a minimum number of ones to constitute the number of bits in the byte format). The minimum number of ones needed will be 10 (M=0) or 11 (M=1). This allows a receiver that is not in the wake-up mode to detect the end of a message, detect the preamble of a new message, or to resynchronize with the transmitter. The IDLE bit is cleared by accessing the serial communications status register (with IDLE set) followed by a read of the serial communications data register. The IDLE bit will not be set again until after an RDRF has been set; i.e., a new idle line occurs. The IDLE is not set by an idle line when the receiver "wakes up" from the wake-up mode. Reset clears the IDLE bit.

B3, OR — When the overrun error bit is set, it indicates that the next byte is ready to be transferred from the receive shift register to the serial communications data register when it is already full (RDRF it is set). Data transfer is then inhibited until the RDRF bit is cleared. Data in the serial communications data register is valid in this case, but additional data received during an overrun condition (including the byte causing overrun) will be lost. The OR bit is cleared when the serial communications status register is accessed (with OR set), followed by a read of the serial communications data register. Reset clears the OR bit.

B2, NF — The noise flag bit is set if there is noise on a "valid" start bit or if there is noise on any of the data bits or if there is noise on the stop bit. It is not set by noise on the idle line nor by invalid (false) start bits. If there is noise, the NF bit is not set until the RDRF flag is set. Each data bit is sampled three times as described above in RECEIVE DATA IN and shown in Fig. 5-3. The NF bit represents the status of the byte in the serial communications data register. For the byte being received (shifted in) there will also be a "working" noise flag the value of which will be transferred to the NF bit when the serial data is loaded into the serial communications data register. The NF bit does not generate an interrupt because the RDRF bit gets set with NF and can be used to generate the interrupt. The NF bit is cleared when the serial communications status register is accessed (with NF set), followed by a read of the serial communications data register. Reset clears the NF bit.

B1, FE — The framing error bit is set when the byte boundaries in the bit stream are not synchronized with the receiver bit counter (generated by a "lost" stop bit). The byte is transferred to the serial communications data register and the RDRF bit is set. The FE bit does not generate an interrupt because the RDRF bit is set at the same time as FE and can be used to generate the interrupt. Note that if the byte received causes a framing error and it will also cause an overrun if transferred to the serial communications data register, then the overrun bit will be set, but not the framing error bit, and the byte will not be transferred to the serial communications data register. The FE bit is cleared when the serial communications status register is accessed (with FE set) followed by a read of the serial communications data register. Reset clears the FE bit.

5.7.5 Baud Rate Register

7	6	5	4	3	2	1	0	
-	-	SCP1	SCP0	-	SCR2	SCR1	SCR0	$0D

The baud rate register provides the means for selecting different baud rates which may be used as the rate control for the transmitter and receiver. The SCP0-SCP1 bits function as a prescaler for the SCR0-SCR2 bits. Together, these five bits provide multiple, baud rate combinations for a given internal processor clock frequency.

B5, SCP1
B4, SCP0 — These two bits in the baud rate register are used as a prescaler to increase the range of standard baud rates controlled by the SCR0-SCR2 bits. A table of the prescaler internal processor clock division versus bit levels is provided below. Reset clears SCP1-SCP0 bit (divide-by-one).

SCP1	SCP0	Internal Processor Clock Divide By
0	0	1
0	1	3
1	0	4
1	1	13

B2, SCR2
B1, SCR1
B0, SCR0

These three bits in the baud rate register are used to select the baud rates of both the transmitter and receiver. A table of baud rates versus bit levels is shown below. Reset does not affect the SCR2-SCR0 bits.

SCR2	SCR1	SCR0	Prescaler Output Divide By
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

The diagram of Fig. 5-7 and Tables 5-1 and 5-2 illustrate the divided chain used to obtain the baud rate clock (transmit clock). Note that there is a fixed rate divide-by-16 between the receive clock (RT) and the transmit clock (Tx). The actual divider chain is controlled by the combined SCP0-SCP1 and SCR0-SCR2 bits in the baud rate register as illustrated. All divided frequencies shown in the first table represent the final transmit clock (the actual baud rate) resulting from the internal processor clock division shown in the "divide-by" column only (prescaler division only). The second table illustrates how the prescaler output can be further divided by action of the SCI select bits (SCR0-SCR2). For example, assume that a 9600 Hz baud rate is required with a 2.4576 MHz PLL output clock. In this case the prescaler bits (SCP0-SCP1) could be configured as a divide-by-one or a divide-by-four. If a divide-by-four prescaler is used, then the SCR0-SCR2 bits must be configured as a divide-by-two. This results in a divide-by-128 of the internal processor clock to produce a 9600 Hz baud rate clock. Using the same PLL output clock, the 9600 baud rate can be obtained with a prescaler divide-by-one and the SCR0-SCR2 bits configured for a divide-by-eight.

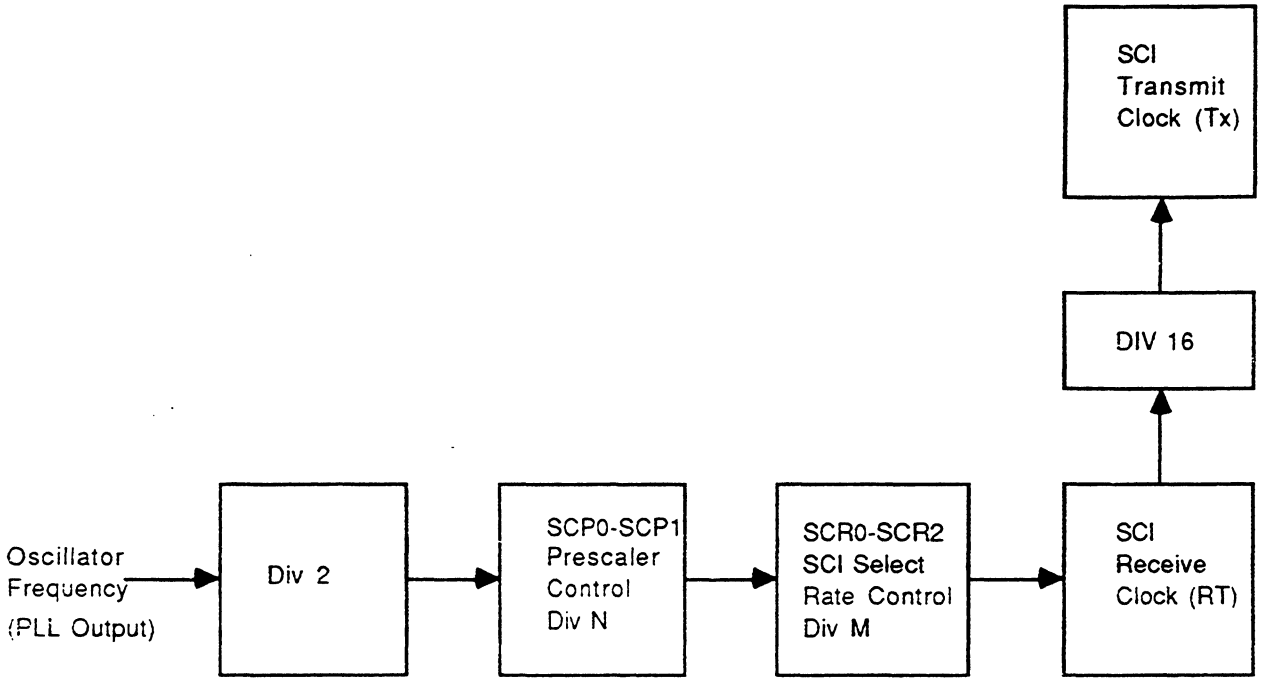


FIG. 5-7 Rate Generator Division

Table 5-1 Prescaler Highest Baud Rate Frequency Output

SCP Bit		Clock* Divided By	PLL Output Clock Frequency MHz			
1	0		4.9125	2.4576	0.6144	0.3072
0	0	1	153.5 KHz	76.80 KHz	19.20 KHz	9.60 KHz
0	1	3	51.17 KHz	25.60 KHz	6.40 KHz	3.20 KHz
1	0	4	38.38 KHz	19.20 KHz	4.80 KHz	2.40 KHz
1	1	13	11.81 KHz	5.907 KHz	1.477 KHz	0.74 KHz

* The Clock in the "Clock Divided By" column is the internal processor clock.

NOTE: The divided frequencies shown in Table 5-1 represent baud rates which are the highest transmit baud rate (Tx) that can be obtained by a specific clock frequency and only using the prescaler division. Lower baud rate may be obtained by providing a further division using the SCI rate select bits as shown below for some representative prescaler outputs.

Table 5-2 Transmit Baud Rate Output For a Given Prescaler Output

SCR Bits			Divide	Representative Highest Prescaler Baud Rate Output			
2	1	0	By	153.5 KHz	76.80 KHz	19.20 KHz	9600 Hz
0	0	0	1	153.5 KHz	76.80 KHz	19.20 KHz	9600 Hz
0	0	1	2	76.80 KHz	38.40 KHz	9600 Hz	4800 Hz
0	1	0	4	38.40 KHz	19.20 KHz	4800 Hz	2400 Hz
0	1	1	8	19.20 KHz	9600 Hz	2400 Hz	1200 Hz
1	0	0	16	9600 Hz	4800 Hz	1200 Hz	600 Hz
1	0	1	32	4800 Hz	2400 Hz	600 Hz	300 Hz
1	1	0	64	2400 Hz	1200 Hz	300 Hz	150 Hz
1	1	1	128	1200 Hz	600 Hz	150 Hz	75 Hz

NOTE: Table 5-2 illustrates how the SCI select bits can be used to provide lower transmitter baud rates by further dividing the prescaler output frequency. The four examples are only representative samples. In all cases, the baud rates shown are transmit baud rates (transmit clock) and the receiver clock is 16 times higher in frequency than the actual baud rate.

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SECTION 6
LIQUID CRYSTAL DISPLAY DRIVER, AUTO DISPLAY OFF REAL TIME CLOCK, PHASE LOCKED LOOP AND LOW VOLTAGE INHIBIT

6.1 INTRODUCTION

This section contains a description of liquid crystal display driver, auto display off, real time clock, and phase lock loop.

6.2 LIQUID CRYSTAL DISPLAY DRIVER

Liquid crystal display driver consists of the following circuitry:

CONTROL LOGIC provides the control signals for display synchronization.

DISPLAY RAM which stores the display data, and each bit of the display RAM is one to one corresponding to the pixel of the LCD. Display RAM is 5 bits word, readable and writable, and is located at address $200-$27F.

LCD DATA LATCH is used to latch data from the display RAM.

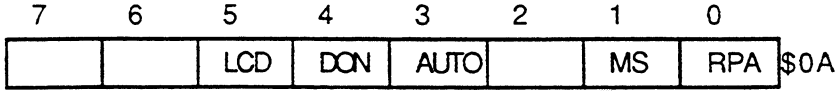
VOLTAGE GENERATOR consists of voltage divider which provides the appropriate voltage levels for backplane and segment driver.

BACKPLANE DRIVER provides the backplane drive signal to the LCD. It can be selected either as 1:16 or 1:8 multiplex.

SEGMENT DRIVER provides the require signals that represent 40 bits of data within the LCD data latch to be displayed.

LCD driver clock is derived from the 32KHz oscillator and frame frequency of LCD driver is 62.5 Hz.

There are several bits in the control register ($0A) which are used to control the operation of the LCD driver and they are explained in the following paragraphs:



RPA BIT 0 When this bit is cleared, voltage generator (Fig 9.1) consists of four serial resistors with total resistance of 90 K ohm. When larger LCD panel is used, either this bit can be set to one to provide a 45 K ohm resistor or external resistors are connected in parallel to pins Vout, V1, V2 and V3 to provide more current for the LCD panel. Resistors value between R1, R2, R3 and R4 are recommended to be R1=R4, R2=R3 and R1=3R2 in order to obtain 1:5 bias LCD driving waveform. The setting of resistance value is determined by considering of the

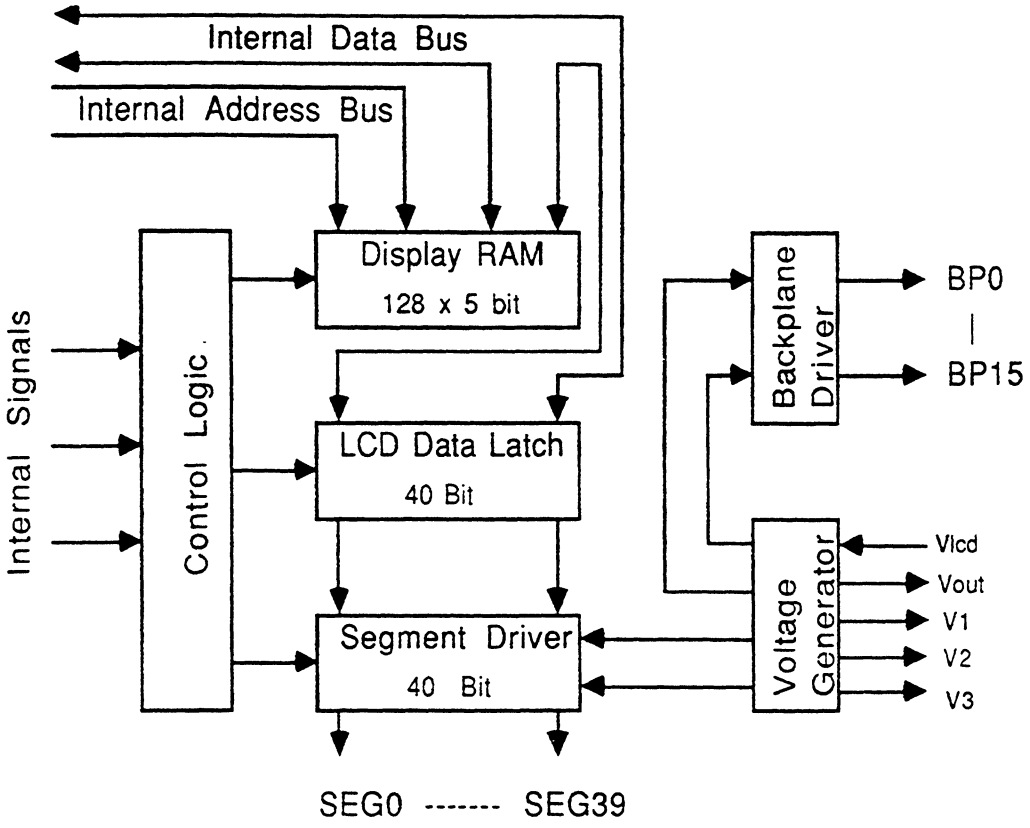


FIG. 6.1 LCD Driver - Functional Block Diagram

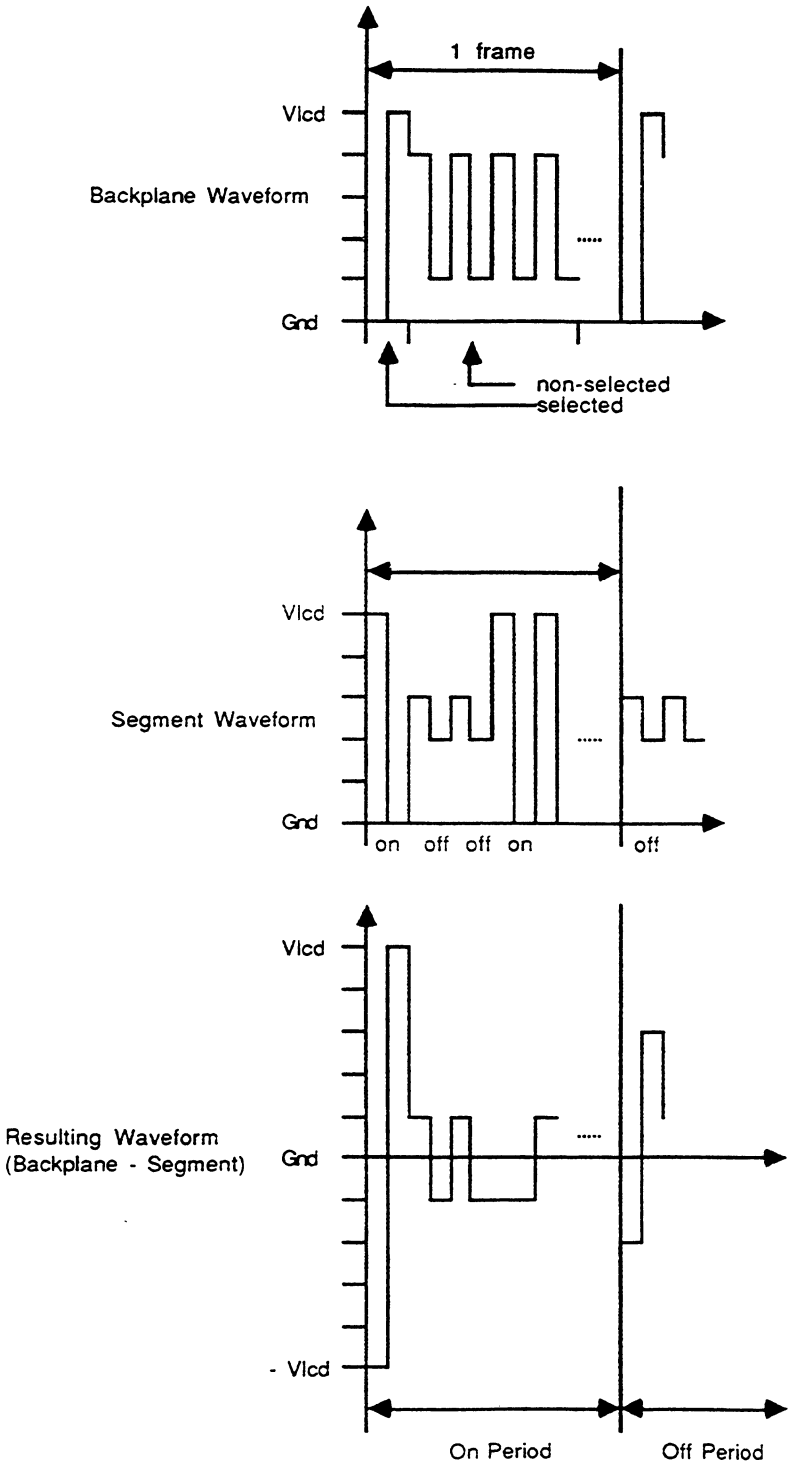


FIG. 6.2 Backplane and Segment Waveform

margin and power consumption. Since driving waveform (backplane and segment) is distorted due to charge/discharge current applying to the liquid crystal display load. It is efficient to connect a 0.1 uF capacitor to the resistors in parallel. This bit is cleared during power on or external reset.

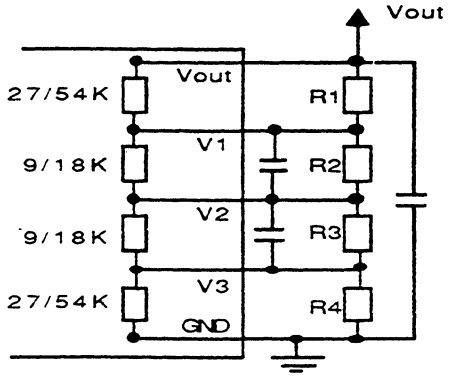


FIG. 6.3 Voltage Generator

MS BIT 1 When this bit is cleared, LCD driver is 1:16 multiplex, setting this bit changes the LCD driver to 1:8 multiplex. Each bit of the display RAM is one to one corresponding to the pixel on the LCD and the following example shows how to display character "A" and "B" on a 1:16 multiplex LCD. This bit is cleared during power on or external reset.

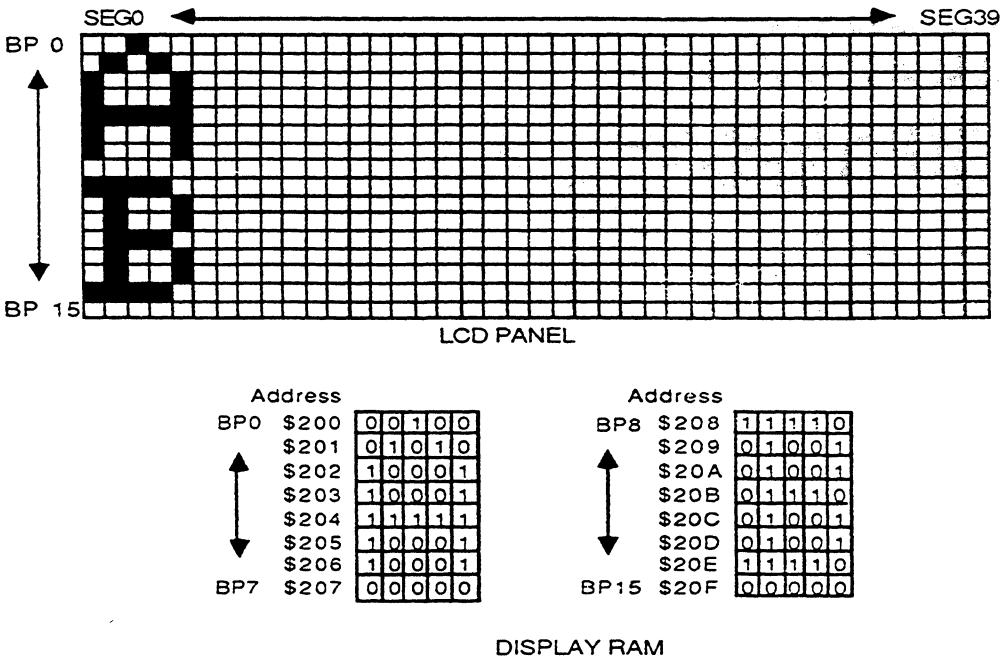


FIG. 6.4 Relation between display RAM Data and Display

AUTO BIT 3 This bit controls whether the auto display off feature is selected or not. When this bit is set, LCD will be turned off after CPU executes STOP instruction. The amount of time that is required for LCD to turn off after execute the STOP instruction depending on the value in the count down register. If this bit is cleared, there is no auto display off feature. This bit is cleared during power on or external reset.

DON BIT 4 This is the bit which controls the on/off of the LCD and is cleared during power on or external reset. LCD will not turn on if this bit is cleared. This is the bit which can be cleared by the auto display off feature. When auto display off feature is selected and count down register reaches zero, DON bit is cleared. In order to turn on the LCD again, a one has to be written into this bit. For example:

*LCD is turned off after execute the STOP instruction when auto display off feature is selected.

```
BSET    3,$0A       Select auto display off feature.
BSET    4,$0A       Turn on LCD.
STOP                Enter stop mode to conserve power.
```

(LCD will turn off when the count down register reaches zero)

*MCU waked up by interrupt or reset.

```
BSET    4,$0A       LCD is turned off by the auto display off feature, so turns it
                    back on.
```

LCD BIT 5 This bit is used to select PC0-PC4 (Port C) as control signal pins when MC68HC05L9 is connected to MC68HC68L9 or MC141510 (slave LCD driver). After this bit is set, a delay of maximum one millisecond is required for 1:16 multiplex before PC0-PC4 can communicate with slave LCD driver, and a delay of maximum of two millisecond is required for 1:8 multiplex. Pins configuration of PC0-PC4 is as follow:

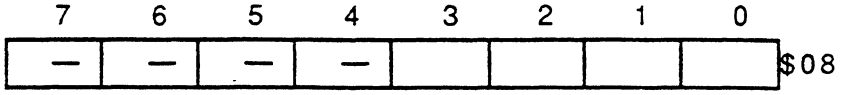
LCD	PC4	PC3	PC2	PC1	PC0
0	I/O	I/O	I/O	I/O	I/O
1	CS3	CS2	CS1	CNTRS	BPCLK

BPCLK : 2 KHz clock (1:16 multiplex) or 1 KHz clock (1:8 multiplex).
CNTRS : Periodic reset clock.
CS1 : Select (active low) display RAM address $280-$32F (slave 1).
CS2 : Select (active low) display RAM address $330-$3DF (slave 2).
CS3 : Select (active low) display RAM address $3E0-$48F (slave 3).

When switch function of PC0 - PC4 from I/O to slave control, the PC0 - PC4 pins will remain as I/O function for another one to two milliseconds depends on the multiplex ratio before the change over. Bus contention problem could arise if the data in the corresponing data register bit PC2 to PC4 were previousely written as zero. A good practice to avoid this problem would be either to configure PC0 - PC4 as input pin before the change over or to perform a 'write' to the corresponing bit of PC0 - PC4 in data register with data one.

6.3 AUTO DISPLAY OFF

Address $08 represents the count down register which is used for the auto display off feature. This register represents the amount of time (in minute) that has to elapse before the LCD is turned off. This is a 4 bits register with default value equal to three during power on or external reset. When MCU is waked up from STOP mode, this register will resume to previous value. Degree of accuracy of the count down register is -59 seconds and maximum elapse time is 15 minutes.

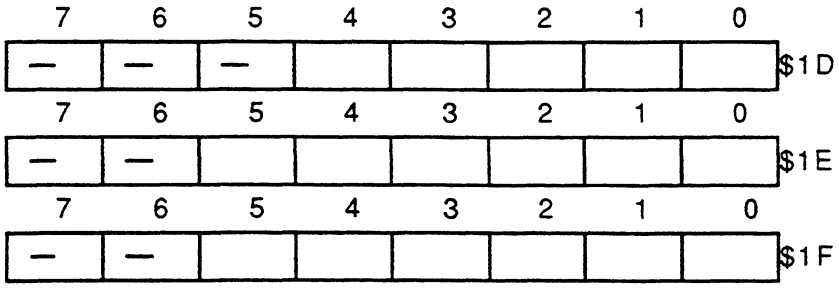


6.4 REAL TIME CLOCK

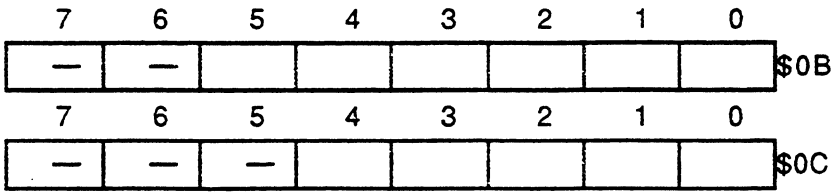
Real time clock is a mask programmable option (Crystal oscillator in STOP mode) which can be either enabled or disabled. Real time clock consists of three binary counters which divide down the clock source from the 32 KHz oscillator. There are three bits in control register ($09) and three bits in address ($1C) which associate to the operation of the real time clock. Three locations are reserved for real time clock, and they are address $1D that represents hours, address $1E that represents minutes and address $1F that represents seconds.

As the hour, minute and second counters are not inhibited to count during being written by CPU, it may happen that the CPU want to set the time to 15:00:00 at the instant when the RTC counters is at the value of 3:59:59. After writing the hour counter to the value of 15, it may immediately advance to the value of 16 as the RTC may advance ahead of the CPU writing to the minute counter. Then the result is that 16:00:00 is set instead of 15:00:00. So it is always suggested to write to the RTC counters only after detecting a change of second interrupt flag so that there is approximately 1 sec for the CPU to write to the RTC counter before the next RTC counter advance. This can be done by either CPU reading the SECOND INTERRUPT flag until it changes from 0 to 1 or by enabling the SECOND INTERRUPT so that the CPU only writes to the counter after it is interrupted by the RTC.

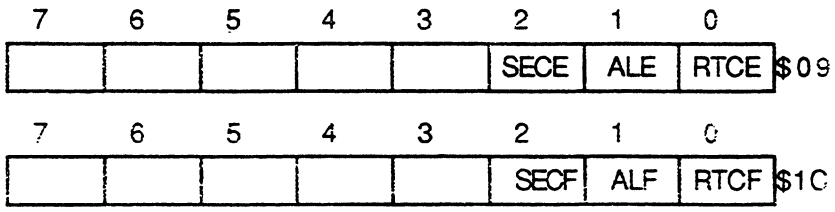
Also reading the RTC counter may have the same problem if the RTC counter advances between the reading of the RTC counters. So it is better to read the RTC counters only after a change of second interrupt flag is detected.



There are two locations associated with the alarm registers. They are address $0B which represents the minute of the alarm and address $0C which represents the hour of the alarm. These two registers contain random data when power up.



Corresponding to the real time clock, there are three interrupts, and they are controlled by the following bits:



RTCE BIT 0 When this bit is set, real time clock interrupts CPU once a day, RTCF (bit 0 of address $1C) is the bit which indicates whether an once a day interrupt has just occurred. After serving this interrupt, user is responsible to clear this bit (RTCF), otherwise the CPU will keep on serving this once a day interrupt when a new RTC interrupt occurs (even there is no once a day interrupt occurs). Both RTCE and RTCF bits are cleared during power on or external reset.

ALE BIT 1 When this bit is set, real time clock interrupts CPU whenever the value of real time clock matches the value of alarm registers. ALF (bit 1 of address $1C) is the bit to indicate whether this is a real time clock interrupt caused by the matching of the value of real time clock and the alarm registers. After serving this interrupt, user is responsible to clear this bit (ALF), otherwise the CPU will keep on serving this alarm interrupt when a new RTC interrupt occurs (even there is no alarm interrupt occurs). Both ALE and ALF bits are cleared during power on or external reset. A write to the hour/minute registers ($1D, 1E) or alarm hour/minute register ($0B,0C) will reset the ALE bit to zero.

The ALF is set at the time when the second counter advances while the value programmed in the alarm hour and alarm minute register matches the value of the hour and minute counter respectively. This means that for example an alarm time of 3:45 is programmed in the alarm registers, then the RTC will start to set the alarm flag at the the time 3:45:01 and continues to do so until 3:46:00. This means that there is one second delay in the generation of the alarm interrupt to the CPU and the CPU can only clear the alarm interrupt one minute after the alarm time. If the CPU clear the alarm flag too early, say at 3:45:15, then the alarm flag will be set again at 3:45:16.

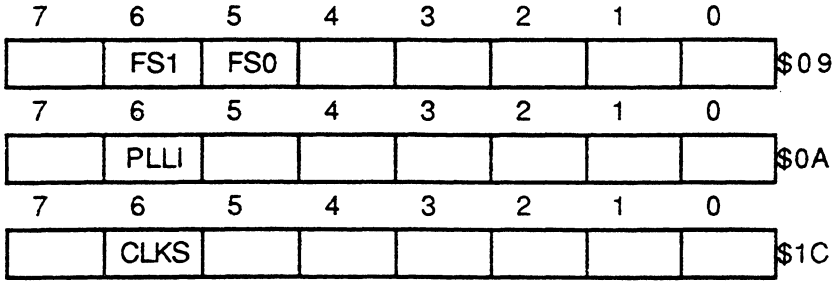
SECE BIT 2 When this bit is set, real time clock interrupts CPU once a second, SECF (bit 2 of address $1C) is the bit which indicates whether an once a second interrupt has just occurred. After serving this interrupt, user is responsible to clear this bit (SECF), otherwise the CPU will keep on serving this once a second interrupt when a new RTC interrupt occurs (even there is no once a second interrupt occurs). Both SECE and SECF bits are cleared during power on or external reset.

Following is an example showing how to use the real time clock interrupt:

```
*Main program
        BSET    0,$09       Enable RTC (once a day) interrupt.
        BSET    1,$09       Enable RTC (alarm) interrupt.
        BSET    2,$09       Enable RTC (once a second) interrupt.
        STOP                MCU execute STOP instruction for power
                            conservation.

*Real time clock interrupt service routine
        BRSET   0,$1C,ODAY  This bit is set indicating this is an once a day RTC
                            interrupt.
        BRSET   1,$1C,ALINT This bit is set indicating this is a RTC interrupt caused
                            by a match of alarm registers and real time clock
                            registers.
        BRSET   2,$1C,OSEC  This bit is set indicating this is an once a second RTC
                            interrupt.
ODAY    BCLR    0,$1C       Clear this bit so that this once a day interrupt will not be
                            recognized as a new one on next RTC interrupt.
        JSR     OADAY       Once a day interrupt service routine

        BRSET1,$1C,ALINT    This bit is set indicating alarm interrupt also occurs at
                            the same time.
        BRSET2,$1C,OSEC     This bit is set indicating once a second RTC interrupt
                            also occurs at the same time.
RTCR    RTI

ALINT   BCLR    1,$1C       Clear this bit so that this alarm interrupt will not be
                            recognized as a new one on next RTC interrupt
        JSR     ALARM       Alarm service interrupt routine.
        BRSET   2,$1C,OSEC  This bit is set indicating once a second interrupt also
                            occurs at the same time.
        BRA     RTCR        Return from interrupt.

OSEC    BCLR    2,$1C       Clear this bit so that this once a second interrupt will not
                            be recognized as a new one on next RTC interrupt.
        JSR     OASEC       Once a second interrupt service routine.
        BRA     RTCR        Return from interrupt.
```

6.5 PHASE LOCK LOOP

System clock can be either obtained from the 32KHz oscillator or from PLL. During power on or external reset, MCU system clock comes from the 32KHz clock. Setting bit 6 of address $1C selects PLL clock for the CPU. PLL clock frequency depends on FS1,FS0 (bit 6,5 of location $09). When FS1 and FS0 are set, a 4.9 MHz clock is output from the PLL. A 0.306 MHz clock is output when FS1 and FS0 are cleared. Phase Lock Loop Indicator (PLLI, Bit 6 of address $0A) is a read only bit which indicates an accurate clock is ready when set to one. The accuracy of clock is checked every millisecond. It takes 1 ms to reset PLLI by unstable clock and 16 ms to set PLLI by stable clock. FS1, FS0 and bit 6 of address $1C are cleared during power on or external reset.



FS1	FS0	PLL Output Clock Frequency	P02 (Internal Bus Frequency)
0	0	0.306 MHz	0.153 MHz
0	1	2.448 MHz	1.244 MHz
1	0	0.612 MHz	0.306 MHz
1	1	4.896 MHz	2.448 MHz

CLKS (bit 6 of address $1C) is the bit to select CPU clock either coming from the phase lock loop or from the 32 KHz clock. During power on or external reset, this bit is clear to indicate that CPU clock is from the 32K Hz clock. And following is an example of how to use the PLL to obtain an accurate CPU clock.

```
BSET    6,$1C     Select PLL clock for CPU.
BSET    5,$09     Select 1.244 MHz as internal bus frequency.
BRCLR   6,$0A,*   Wait until PLL flag reset from previously stable state
BRSET   6,$0A,*   Wait until PLL clock is stable.
JMP     SERVE     Clock is stable now, go to perform jobs that require accurate
                  frequency (such as SCI and Timer).
```

The PLL consists of an on chip VCO, a phase comparator and programmable divide-by-N counter. An external filter is required to filter the phase comparator output to provide a DC signal to control the VCO frequency (Fig. 6.5).

The phase comparator compares the rising edge of a 1 KHz reference signal dervied from the 32 KHz crystal clock to the rising edge of the VCO clock after being divided by the divide-by-N counter. When there is phase different between the two signals, the phase comparator output will adjust the DC level input to the VCO to change the VCO frequency (Fig. 6.6) The divide-by-N counter can be programmed to divide by different rates to obtain 4 different VCO frequencies which are 307.2 KHz, 614.4 KHz, 2.4576 MHz and 4.9152 MHz.

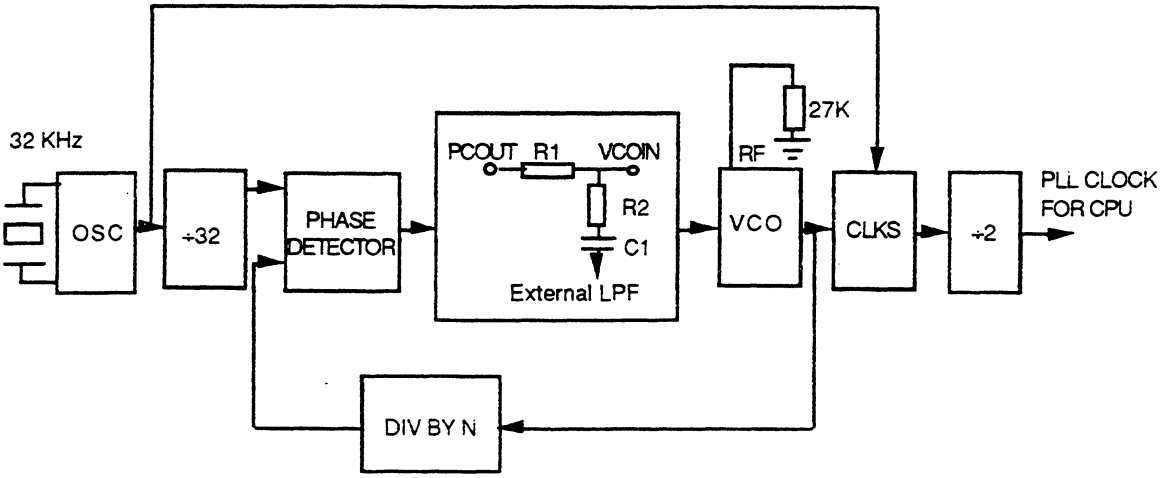


FIG. 6.5 PHASE LOCK LOOP BLOCK DIAGRAM

6.5.1 LOW PASS FILTER/VCO

Pin PCOUT is the phase detector output and used to connect to the input of an external low pass filter. A second order filter is recommended as shown in Fig. 6.5. Pin VCOIN is the D.C. input of the on-chip VCO. It is connected to the output of the LPF.

Pin RF is used to connect a resistor to ground. The resistor is used to control the charging current of the VCO. A value of 27K is suggested.

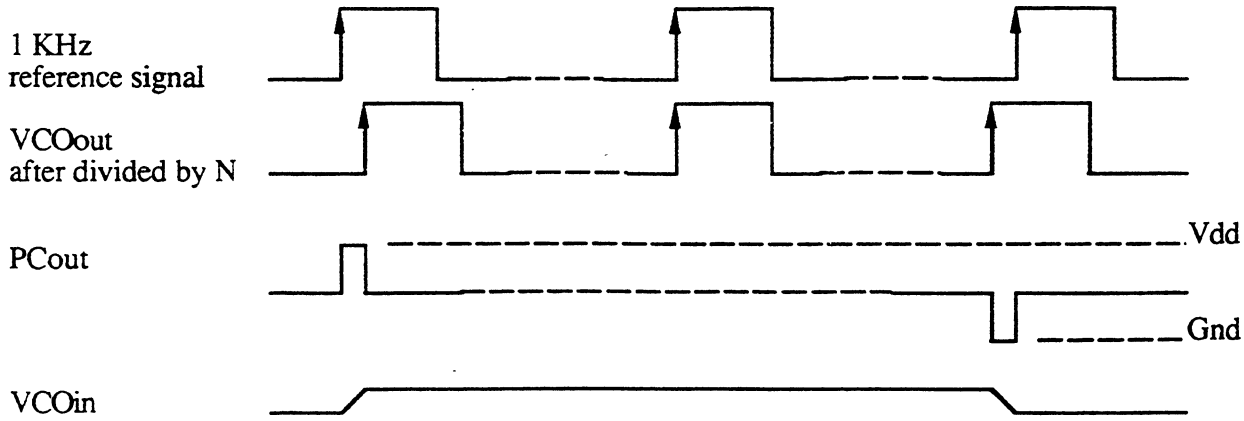
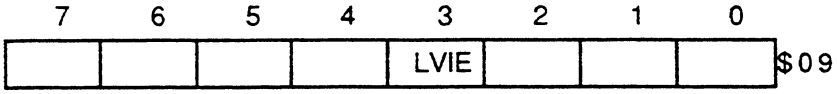


Fig. 6.6 Typical Waveforms for PLL

6.6 LOW VOLTAGE INHIBIT

Low Voltage Inhibit is a feature to allow CPU to take action for its data base protection due to a drop of voltage supply. If LVIE = 1, an interrupt to the CPU occurs when voltage supply level drops below 3.8 volts (with a tolerance of +/- 15 %). A fraction of supply voltage and an internal voltage reference are fed to the input of a voltage comparator once per minute. When the supply voltage drops below a triggering level, the comparator output will change state to interrupt the CPU (Fig. 6.7). During power on or external reset, low voltage inhibit is disabled.



LVIE = 0 Low Voltage Inhibit Interrupt disable
LVIE = 1 Low Voltage Inhibit Interrupt enable

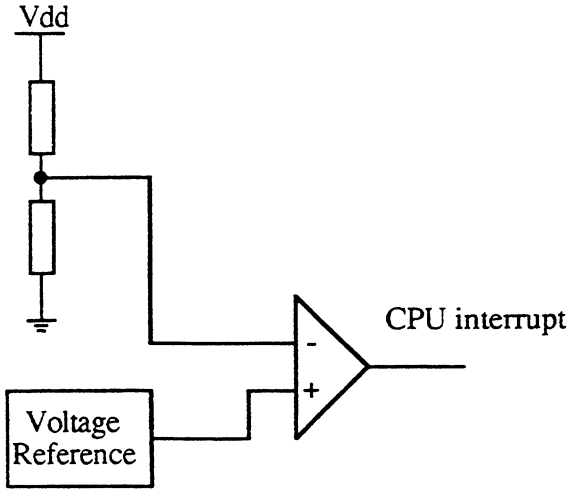


Fig. 6.7 Low Voltage Interrupt

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SECTION 7
EFFECTS OF STOP AND WAIT MODES ON THE TIMER, REAL TIME CLOCK AND SERIAL SYSTEM

7.1 INTRODUCTION

The STOP and WAIT instructions have different effects on the programmable timer and serial communications interface (SCI) system. These different effects are discussed separately below.

7.2 STOP MODE

When the processor executes the STOP instruction, the internal processor clock is turned off. This halts all internal CPU processing including the operation of the programmable timer and serial communications interface. The only way for the MCU to "wake up" from the stop mode is by receipt of an interrupt (logic low on IRQ pin, LVI, KEYBOARD or REAL TIME CLOCK(RTC)) or by the detection of a reset (logic low on RESET pin or a power-on reset). The effects of the stop mode on each of the MCU systems (Timer, RTC, SCI) are described separately.

7.2.1 Timer During Stop Mode

When the MCU enters the stop mode, the timer counter stops counting (the internal processor clock is stopped) and remains at that particular count value until the stop mode is exited by an interrupt (if exited by reset the counter is forced to $FFFC). If the stop mode is exited by an external interrupt on the IRQ pin, interrupt from LVI, KEYBOARD or RTC, then the counter resumes from its stop value as if nothing had happened. Another feature of the programmable timer, in the stop mode, is that if at least one valid input capture edge occurs at the TCAP pin, the input capture detect circuitry is armed. This action does not set any timer flags or "wake up" the MCU, but when the MCU does "wake up" there will be an active input capture flag (and data) from that first valid edge which occurred during stop mode. If the stop mode is exited by an external reset (logic low on RESET pin), then no such input capture flag or data action takes place even if there was a valid input capture edge (at the TCAP pin) during MCU stop mode.

7.2.2 SCI During Stop Mode

When the MCU enters the stop mode, the baud rate generator which drives the receiver and transmitter is shut down. This essentially stops all SCI activity. The receiver is unable to receive and transmitter is unable to transmit. If the STOP instruction is executed during a transmitter transfer, that transfer is halted. When the stop mode is exited, that particular transmission resumes (if the exit mode is the result of an external low on the IRQ pin, interrupt from LVI, KEYBOARD or RTC). Since the previous transmission resumes after an IRQ, LVI, KEYBOARD or RTC interrupt stop mode exit, the user should ensure that the SCI transmitter is in the idle state when the STOP instruction is executed. If the receiver is receiving data when STOP instruction is executed, received data sampling is stopped (baud rate generator stops) and the rest of the data is lost. For the above reasons, all SCI transactions should be in the idle state when the STOP instruction is executed.

7.2.3 RTC During Stop Mode

Since RTC runs on a 32 KHz clock, stop instruction has no effect on the RTC (If RTC option is chosen).

7.3 WAIT MODE

When the MCU enters the wait mode, the CPU clock is halted. All CPU action is suspended; however, the timer and SCI system remain active. In fact an interrupt from the timer, LVI, KEYBOARD, RTC or SCI (in addition to a logic low on the IRQ or RESET pins) causes the processor to exit the wait mode. Since the systems mentioned above operate as they do in the normal mode, only a general discussion of the wait mode is provided below.

The wait mode power consumption depends on how many systems are active. The power consumption will be the highest when all the system (timer, and SCI) are active. If a non-reset exit from the wait mode is performed (eg. timer overflow interrupt exit), the state of the remaining systems will be unchanged. If a reset exit from the wait mode is performed all the systems revert to the disabled reset state.

SECTION 8
INSTRUCTION SET AND ADDRESSING MODES

8.1 INSTRUCTION SET

The MCU has a set of 62 basic instructions. They can be divided into five different types: register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type.

This MCU uses all the instructions available in the M146805 CMOS Family plus one more: the unsigned multiply (MUL) instruction. This instruction allows unsigned multiplication of the contents of the accumulator (A) and the index register (X). The high-order product is then stored in the index register, and the low-order product is stored in the accumulator. A detailed definition of the MUL instruction is shown below.

Operation: X:A <---- X*A

Description: Multiplies the eight bits in the index register by the eight bits in the accumulator to obtain a 16-bit unsigned number in the concatenated accumulator and index register.

Condition Codes:

H : Cleared
I : Not affected
N : Not affected
Z : Not affected
C : Cleared

Source Form(s): MUL

Addressing Mode	Cycles	Bytes	Opcode
Inherent	11	1	$42

8.1.1 REGISTER/MEMORY INSTRUCTIONS

Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to the following instruction list.

Function	Mnemonic
Load A from Memory	LDA
Load X from Memory	LDX
Store A in Memory	STA
Store X in Memory	STX
Add Memory to A	ADD
Add Memory and Carry to A	ADC
Subtract Memory	SUB
Subtract Memory from A with Borrow	SBC
AND Memory to A	AND
OR Memory with A	ORA
Exclusive OR Memory with A	EOR
Arithmetic Compare A with Memory	CMP
Arithmetic Compare X with Memory	CPX
Bit Test Memory with A (Logical Compare)	BIT
Jump Unconditional	JMP
Jump to Subroutine	JSR

8.1.2 READ-MODIFY-WRITE INSTRUCTIONS

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read-modify-write sequence since it does not modify the value. Refer to the following list of instructions.

Function	Mnemonic
Increment	INC
Decrement	DEC
Clear	CLR
Complement	COM
Negate (2's Complement)	NEG
Rotate Left Thru Carry	ROL
Rotate Right Thru Carry	ROR
Logical Shift Left	LSL
Logical Shift Right	LSR
Arithmetic Shift Right	ASR
Test for Negative or Zero	TST
Multiply	MUL

8.1.3 BRANCH INSTRUCTIONS

This set of instructions branches if a particular condition is met; otherwise, no operation is performed. Branch instructions are two-byte instructions. Refer to the following list for branch instructions.

Function	Mnemonic
Branch Always	BRA
Branch Never	BRN
Branch if Higher	BHI
Branch if Lower or Same	BLS
Branch if Carry Clear	BCC
Branch if Higher or Same	BHS
Branch if Carry Set	BCS
Branch if Lower	BLO
Branch if Not Equal	BNE
Branch if Equal	BEQ
Branch if Half Carry Clear	BHCC
Branch if Half Carry Set	BHCS
Branch if Plus	BPL
Branch if Minus	BMI
Branch if Interrupt Mask Bit is Clear	BMC
Branch if Interrupt Mask Bit is Set	BMS
Branch if Interrupt Line is Low	BIL
Branch if Interrupt Line is High	BIH
Branch to Subroutine	BSR

8.1.4 BIT MANIPULATION INSTRUCTIONS

The MCU is capable of setting or clearing any bit which resides in the first 256 bytes of the memory space except for bit 6 of location $0A, which is read only, serial communications status register ($10), timer status register ($13), and timer input capture register ($14-$15). An additional feature allows the software to test and branch on the state of any bit within the first 256 locations. The bit set, bit clear, and bit test and branch functions are all implemented with a single instruction. For the test and branch instructions, the value of the bit tested is automatically placed in the carry bit of the condition code register. Refer to the following list for bit manipulation instructions.

Function	Mnemonic
Branch if Bit n is Set	BRSET n (n = 0...7)
Branch if Bit n is Clear	BRCLR n (n = 0...7)
Set Bit n	BSET n (n = 0...7)
Clear Bit n	BCLR n (n = 0...7)

8.1.5 CONTROL INSTRUCTIONS

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to the following list for control instructions.

Function	Mnemonic
Transfer A to X	TAX
Transfer X to A	TXA
Set Carry Bit	SEC
Clear Carry Bit	CLC
Set Interrupt Mask Bit	SEI
Clear Interrupt Mask Bit	CLI
Software Interrupt	SWI
Return from Subroutine	RTS
Return from Interrupt	RTI
Reset Stack Pointer	RSP
No-Operation	NOP
Stop	STOP
Wait	WAIT

8.2 ADDRESSING MODES

The MC68HC05L9 uses ten different addressing modes to provide the programmer with an opportunity to optimize the code to all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables, and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions, while the longest instructions (three bytes) permit accessing tables throughout memory. Short absolute (direct) and long absolute (extended) addressing are also included. One and two byte direct addressing permits jump instructions to reach all memory.

The term "effective address" (EA) is used in describing the various addressing modes, and is defined as the byte address to or from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described in the following paragraphs. Parentheses are used to indicate "contents of" the location or register referred to; e.g., (PC) indicates the contents of the location pointed to by the PC. An arrow indicates "is replaced by", and a colon indicates concatenation of two bytes. For additional details and graphical illustrations, refer to the M6805 HMOS/M146805 CMOS Family Microcomputer/Microprocessor User's Manual.

8.2.1 Inherent

In inherent instructions, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, and no other arguments, are included in this mode.

8.2.2 Immediate

In immediate addressing, the operand is contained in the byte immediately following the opcode. Immediate addressing is used to access constants which do not change during program execution (e.g. a constant used to initialize a loop counter).

EA = PC + 1; PC <-- PC + 2

8.2.3 Direct

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two-byte instruction. This includes all on-chip RAM and I/O registers, and 48 bytes of on chip ROM. Direct addressing is efficient in both memory and time.

EA = (PC + 1); PC <-- PC + 2
Address Bus High <-- 0; Address Bus Low <-- (PC + 1)

8.2.4 Extended

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing modes are capable of referencing arguments anywhere in memory with a single three-byte instruction. When using the Motorola assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the most efficient addressing mode.

EA = (PC + 1):(PC + 2); PC <-- PC + 3
Address Bus High <-- (PC + 1); Address Bus Low <-- (PC + 2)

8.2.5 Indexed, No Offset

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is used to move a pointer through a table or to address a frequently referenced RAM or I/O location.

EA = X; PC <-- PC + 1
Address Bus High <-- 0; Address Bus Low <-- X

8.2.6 Indexed, 8-Bit Offset

Here the EA is obtained by adding the contents of the byte following the opcode to that of the index register; therefore, the operand is located anywhere within the lowest 511 memory locations. For example, this mode of addressing is useful for selecting the mth element in a n element table. All instructions are only two bytes. The content of the index register (X) is not changed. The content of (PC + 1) is an unsigned 8-bit integer. One byte offset indexing permits look-up tables to be easily accessed in either RAM or ROM.

EA = X + (PC + 1); PC <-- PC + 2
Address Bus High <-- K; Address Bus Low <-- X + (PC + 1)

where:
K = The carry from the addition of X + (PC + 2)

8.2.7 Indexed, 16-Bit Offset

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed 8-bit offset, except that this three-byte instruction allows tables to be anywhere in memory (e.g., jump tables in ROM). As with direct and extended, the M6805 assembler determines the most efficient form of indexed offset; 8- or 16-bit. The content of the index register is not changed.

EA = X + (PC + 1):(PC + 2); PC <-- PC + 3
Address Bus High <-- (PC + 1) + K; Address Bus Low <-- X + (PC + 2)

where:
K = The carry from the addition of X + (PC + 2)

8.2.8 Relative

Relative addressing is only used in branch instructions. In relative addressing, the content of the 8-bit signed byte following the opcode (the offset) is added to the PC if and only if the branch condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is limited to the range of -126 to +129 bytes from the branch instruction opcode location. The Motorola assembler calculates the proper offset and checks to see if it is within the span of the branch.

EA = PC + 2 + (PC + 1); PC <-- EA if branch taken;
otherwise, EA = PC <-- PC + 2

8.2.9 Bit Set/Clear

Direct addressing and bit addressing are combined in instructions which set and clear individual memory and I/O bits. In the bit set and clear instructions, the byte is specified as a direct address in the location following the opcode. The first 256 addressable locating are thus accessed. The bit to be modified within that byte is specified in the first three bits of the opcode. The bit set and clear instructions occupy two bytes, one for the opcode (including the bit number) and the other to address the byte which contains the bit of interest.

EA = (PC + 1); PC <-- PC + 2
Address Bus High <-- 0; Address Bus Low <-- (PC + 1)

8.2.10 Bit Test and Branch

Bit test and branch is a combination of direct addressing, bit set/clear addressing, and relative addressing. The actual bit to be tested, within the byte, is specified within the low order nibble of the opcode. The address of the data byte to be tested is located via a direct address in the location following the opcode byte (EA1). The signed relative 8-bit offset is in the third byte (EA2) and is added to the PC if the specified bit is set or cleared in the specified memory location. This single three-byte instruction allows the program to branch based on the condition of any bit in the first 256 locations of memory.

EA1 = (PC +1)
Address Bus High <-- 0; Address Bus Low <-- (PC + 1)
EA2 = PC + 3 + (PC + 2); PC <-- EA2 if branch taken;
otherwise, PC <-- PC + 3

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SECTION 9
ELECTRICAL CHARACTERISTICS

9.1 INTRODUCTION

This section contains the electrical specifications of MC68HC05L9.

9.2 MAXIMUM RATINGS
(Voltages Referenced to VSS)

Ratings	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 to +7.0	V
Input Voltage	Vin	VSS-0.3 to VDD +0.3	V
Self-Check Mode ($\overline{IRQ}$ Pin Only)	Vin	VSS-0.3 to 2xVDD + 0.3	V
Current Drain Per Pin Excluding VDD and VSS	I	25	mA
Operating Temperature Range	TA	0 to 70	°C
Storage Temperature Range	Tstg	-65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedence circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < or = (Vin or Vout) < or = VDD. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either VSS or VDD).

9.3 DC ELECTRICAL CHARACTERISTICS

(VDD = 5.0 Vdc + or - 10 %, VSS = 0 Vdc,
Temperature range = 0 to 70 deg. C)

Characteristics	Symbol	Min	Typ		Max	Unit
Output Voltage, Iload < or = 10.0 uA	VOL VOH	- VDD-0.1	- -		0.1 -	V V
Output High Voltage (Iload =1.6 mA) PA0-PA7, PB0-PB7, PC0-PC7, PD1-PD4, TCMP, TONE, P02, R/W, D0-D7, AD0-AD15	VOH	VDD-0.8	-		-	V
Output Low Voltage (Iload = 1.6 mA) PA0-PA7, PB0-PB7, PC0-PC7, PD1-PD4, TCMP, TONE, P02, R/W, D0-D7, AD0-AD15	VOL	-	-		0.4	V
Input High Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD4, TCAP, IRQ, RESET, OSC1, D0-D7	VIH	0.7xVDD	-		VDD	V
Input Low Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD4, TCAP, IRQ, RESET, OSC1, D0-D7	VIL	VSS	-		0.2xVDD	V
Data Retention Mode	VRM	2.0	-		-	V
Supply Current	VDD		5.0V	5.5V	5.5V	
Run (2.45MHZ) (1.22MHZ) (306KHZ) (153KHZ)	IDD IDD IDD IDD	- - - 	7.0 3.5 0.9 0.5	8.0 4.0 1.1 0.6	12 6 1.8 1.0	mA mA mA mA
Wait (2.45MHZ) (1.22MHZ) (306KHZ) (153KHZ)	IDD IDD IDD IDD	- - - 	1.0 0.6 0.25 0.2	1.2 0.7 0.35 0.25	2.0 1.2 0.6 0.5	mA mA mA mA
Stop (16KHZ) (NO CLOCK)	IDD IDD	- -	16 2	18 3	30 12	uA uA
I/O Ports Hi-Z Leakage Current PA0-PA7, PB0-PB7, PC0-PC7, PD1-PD4	IIL	-	-		±10	uA
Input Current TCAP, IRQ, RESET, PD0, OSC1	Iin	-	-		±1	uA
Capacitance Ports (as Input or Output), D0-D7, AD0-AD15, P02, TONE, R/W RESET, IRQ, TCAP, OSC1, PD0-PD4	Cout Cin	- -	- -		12 8	pF pF

9.4 DC ELECTRICAL CHARACTERISTICS

(VDD = 3.0 Vdc + or - 10 %, VSS = 0 Vdc
Temperature range = 0 to 70 deg. C)

Characteristics	Symbol	Min	Typ		Max	Unit
Output Voltage, Iload < or = 10.0 uA	VOL VOH	- VDD-0.1	- -		0.1 -	V V
Output High Voltage (Iload =0.4 mA) PA0-PA7, PB0-PB7, PC0-PC7, PD1-PD4, TCMP, TONE, P02, R/$\overline{W}$, D0-D7, AD0-AD15	VOH	VDD-0.3	-		-	V
Output Low Voltage (Iload = 0.4 mA) PA0-PA7, PB0-PB7, PC0-PC7, PD1-PD4, TCMP, TONE, P02, R/$\overline{W}$, D0-D7, AD0-AD15	VOL	-	-		0.3	V
Input High Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD4, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1, D0-D7	VIH	0.7xVDD	-		VDD	V
Input Low Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD4, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1, D0-D7	VIL	VSS	-		0.2xVDD	V
Data Retention Mode	VRM	2.0	-		-	V
Supply Current	VDD		3.0V	3.3V	3.3V	
Run (1.22MHZ) (306KHZ) (153KHZ)	IDD IDD IDD	- -	1.8 500 300	2.0 700 400	3.0 900 500	mA uA uA
Wait (1.22MHZ) (306KHZ) (153KHZ)	IDD IDD IDD	- - -	250 100 80	300 130 100	500 200 150	uA uA uA
Stop (16KHZ) (NO CLOCK)	IDD IDD	- -	8.5 1	10 2	20 8	uA uA
I/O Ports Hi-Z Leakage Current PA0-PA7, PB0-PB7, PC0-PC7, PD1-PD4	IIL	-	-		$\pm$10	uA
Input Current $\overline{TCAP}$, $\overline{IRQ}$, $\overline{RESET}$, PD0, OSC1	Iin	-	-		$\pm$1	uA
Capacitance Ports (as Input or Output), D0-D7, AD0-AD15, P02, TONE, R/$\overline{W}$ $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1, PD0-PD4	Cout Cin	- -	- -		12 8	pF pF

9.5 LCD DRIVER DC ELECTRICAL CHARACTERISTICS

(Vlcd=6.0Vdc, Vss=0Vdc, TA=0 to 70 deg. C, see Figure 9.1)						
Num	**Characteristic**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Slave LCD Voltage Suppiy, Iload=100uA	Vout	5.975	-	6.0	V
2	V1 (high)	V1h	5.975	-	6.0	V
3	V2 (high)	V2h	4.7	-	4.8	V
4	V3 (high)	V3h	3.5	-	3.6	V
5	V1 (low)	V1l	2.3	-	2.4	V
6	V2 (low)	V2l	1.1	-	1.2	V
7	V3 (low)	V3l	0.0	-	0.05	V
(Vlcd=3.0Vdc, Vss=0Vdc, TA=0 to 70 deg. C, see Figure 9.1)						
1	Slave LCD Voltage Supply, Iload<=10uA	Vout	2.975	-	3.0	V
2	V1 (high)	V1h	2.975	-	3.0	V
3	V2 (high)	V2h	2.35	-	2.4	V
4	V3 (high)	V3h	1.75	-	1.8	V
5	V1 (low)	V1l	1.15	-	1.2	V
6	V2 (low)	V2l	0.55	-	0.6	V
7	V3 (low)	V3l	0.0	-	0.025	V

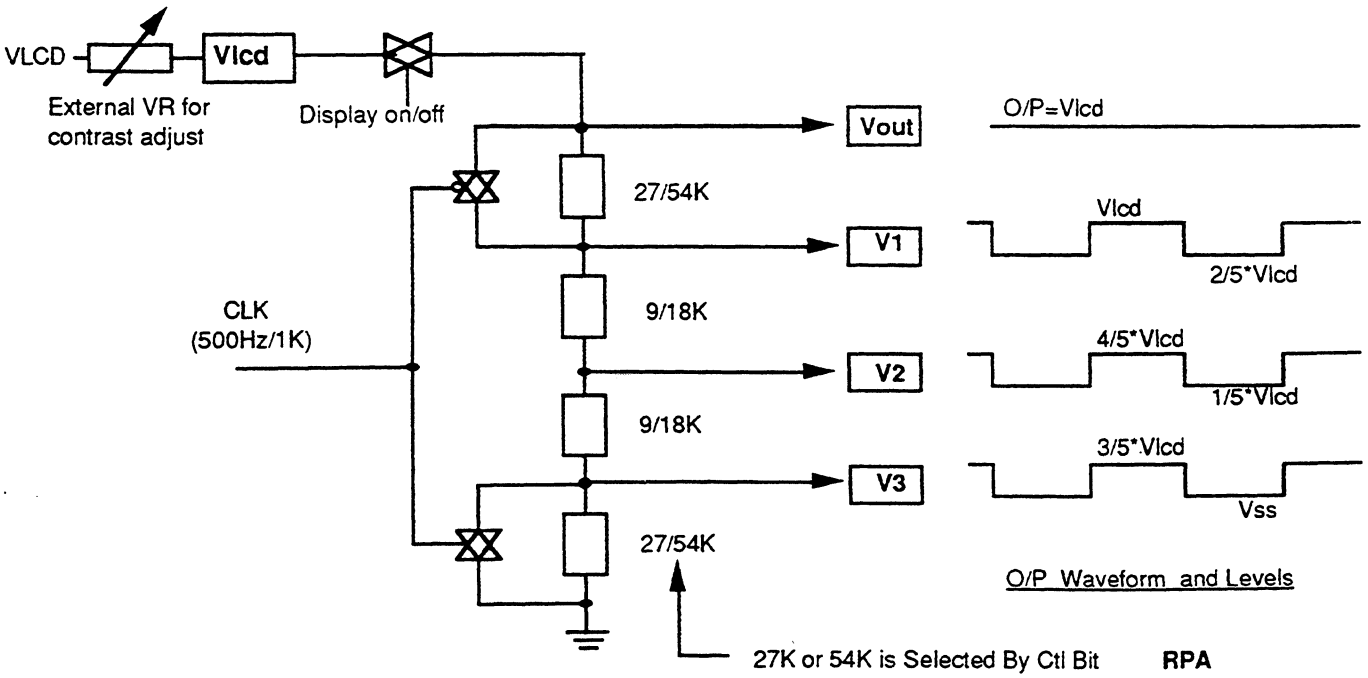


Fig 9.1 LCD Voltage Generator

9.6 BUS TIMING

(Vdd=5.0Vdc+-10%, Vss=0Vdc, TA=0 to 70 deg.C, see Figure 9.2)

Num	Characteristic	Symbol	153KHz		2.45MHz		Unit
			Min	Max	Min	Max	
1	Cycle Time	tcyc	6536	-	408	-	nS
2	Pulse Width, P02 Low	P02l	3185	-	188	-	nS
3	Pulse Width, P02 High	P02h	3185	-	188	-	nS
4	P02 Rise Time	tr	-	25	-	25	nS
5	P02 Fall Time	tf	-	18	-	18	nS
6	Address Delay Time from P02 fall	tad	-	55	-	55	nS
7	Address Hold Time from P02 rise	tah	0	-	0	-	nS
8	R/W Delay Time from P02 fall	trwd	-	55	-	55	nS
9	R/W Hold Time from P02 rise	trwh	0	-	0	-	nS
10	Write Data Delay Time	tddw	-	20	-	20	nS
11	Write Data Hold Time	tdhw	10	-	10	-	nS
12	Read Data Set Up Time	tdsr	30	-	30	-	nS
13	Read Data Hold Time	tdhr	30	-	30	-	nS

NOTES:
1. Full test loads are applied during all dc electrical tests and ac timing measurements.
2. During ac timing measurement, inputs are driven to 0.4 volts and Vdd-0.8volts while timing measurements are taken at the 20% and 70% Vdd points.
3. Osc1 is forced with a 50% duty cycle input clock.

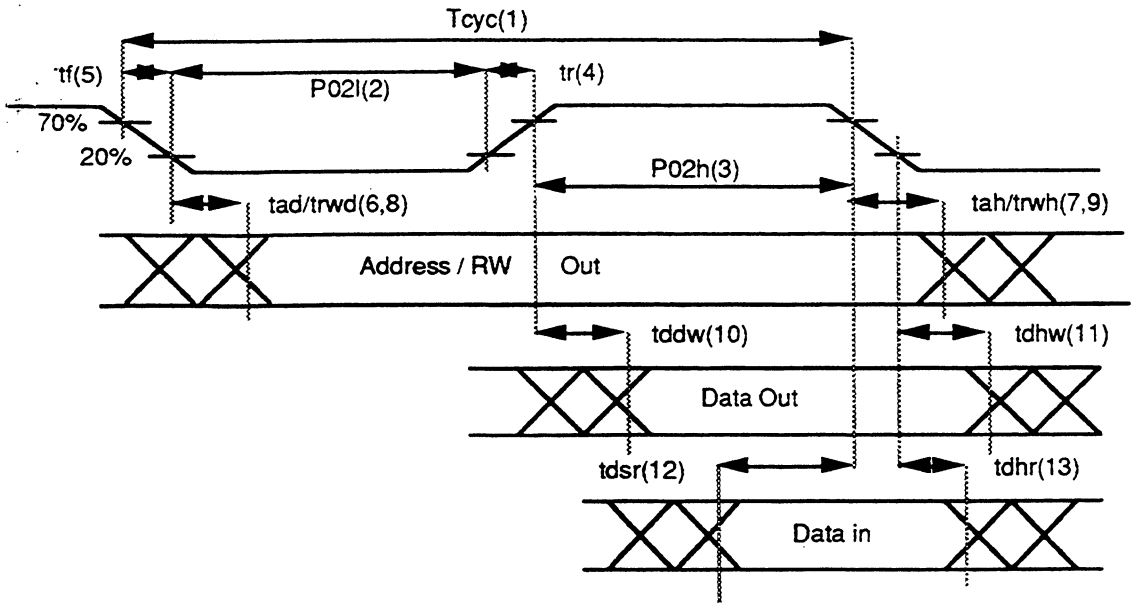


Fig 9.2 Bus timing

9.7 PORT/SLAVE SELECT CTL TIMING (Vdd=5.0Vdc+-10%, Vss=0Vdc, TA=0 to 70 deg. C, see Figure 9.3)

Num	Characteristic	Symbol	153KHz		2.45MHz		Unit
			Min	Max	Min	Max	
1	Cycle Time	tcyc	6536	-	408	-	nS
2	Port Data In Setup Time	tpdsu	100	-	100	-	nS
3	Port Data In Hold Time	tpdh	700	-	50	-	nS
4	Port Data Write Delay Time	tpwd	-	45	-	45	nS
5	$\overline{CS}$1,2,3 Output Delay	tcsd	-	80	-	80	nS
6	Backplane Clock (1/16 multiplex)	bpclk	2048	-	2048	-	Hz
	(1/8 multiplex)		1024	-	1024	-	
7	Slave Counter Reset	cntr	64	-	64	-	Hz

NOTES:1. Full test loads are applied during all dc electrical tests and ac timing measurements.
2. During ac timing measurement, inputs are driven to 0.4 volts and Vdd-0.8volts while timing measurements are taken at the 20% and 70% Vdd points.
3. Osc1 is forced with a 50% duty cycle input clock.
4. The CS- becomes low when the Slave1, 2 or 3 memory space is being addressed.
5. Accuracy of backplane clock and counter reset depends on OSC Xtal 32.768KHz accuracy.

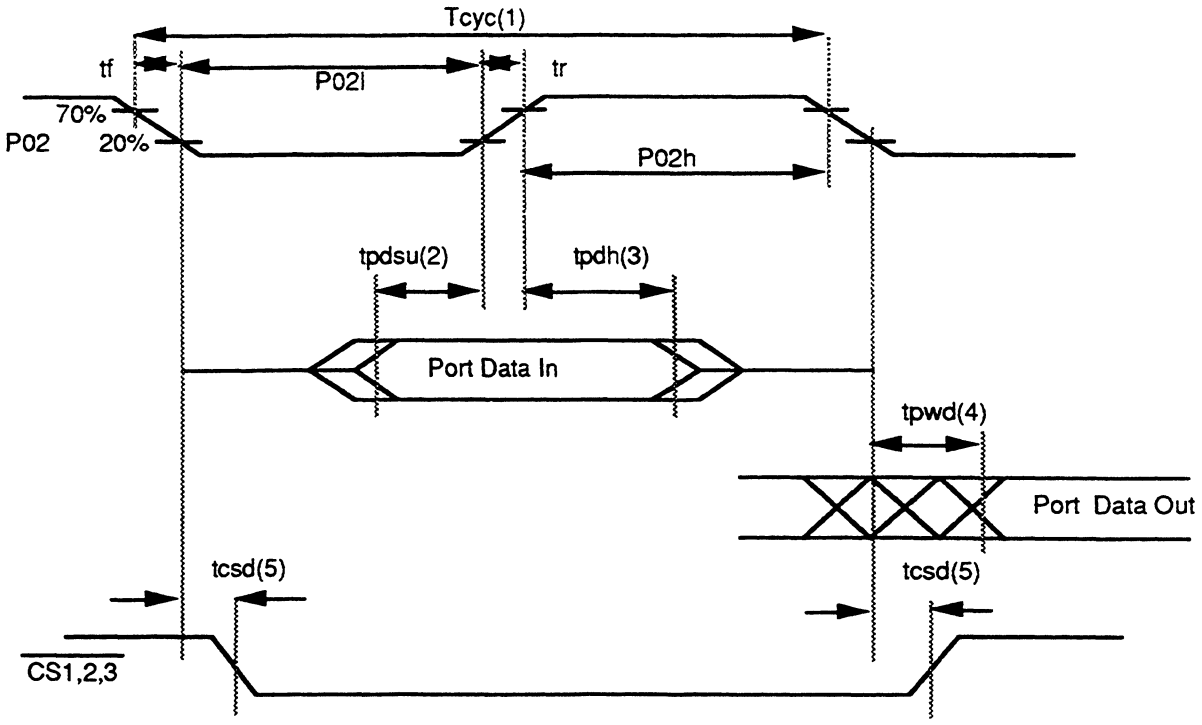
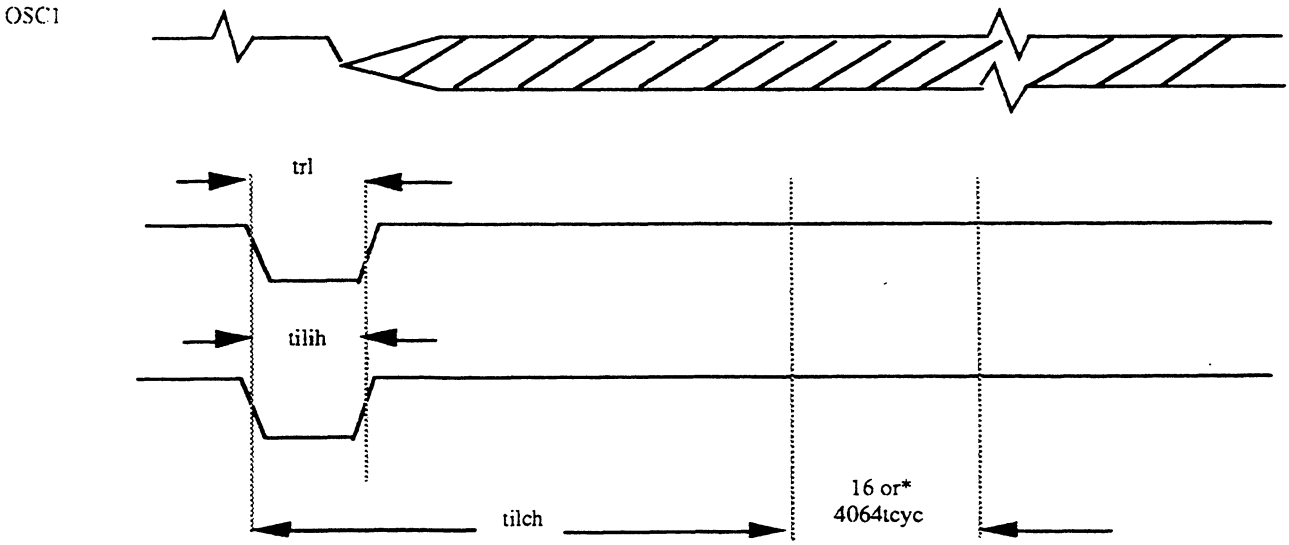


Fig 9.3 Port/Slave CS- timing

9.8 CONTROL TIMING

(Vdd=5.0Vdc+-10%, Vss=0Vdc, TA=0 to 70 deg. C, see Figure 9.4)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation — Crystal	fosc	-	32.768	KHz
Internal Operating Frequency — Crystal Selected	fop	-	16.384	KHz
Internal Operating Frequency — Phase Lock Loop Selected	fop	0.153	2.45	MHz
Cycle Time	tcyc	408	-	nS
Crystal Oscillator Startup Time	toxov	-	500	mS
Stop Recovery Startup Time	tilch	-	500	mS
Reset Pulse Width	trl	1.5	-	tcyc
Timer — Resolution	tresl	4.0	-	tcyc
Timer — Input Capture Pulse Width	tih,til	125	-	nS
Interrupt Pulse Width Low	tilih	125	-	nS



*Select by Mask Option

Fig 9.4 Stop Recovery Timing Diagram

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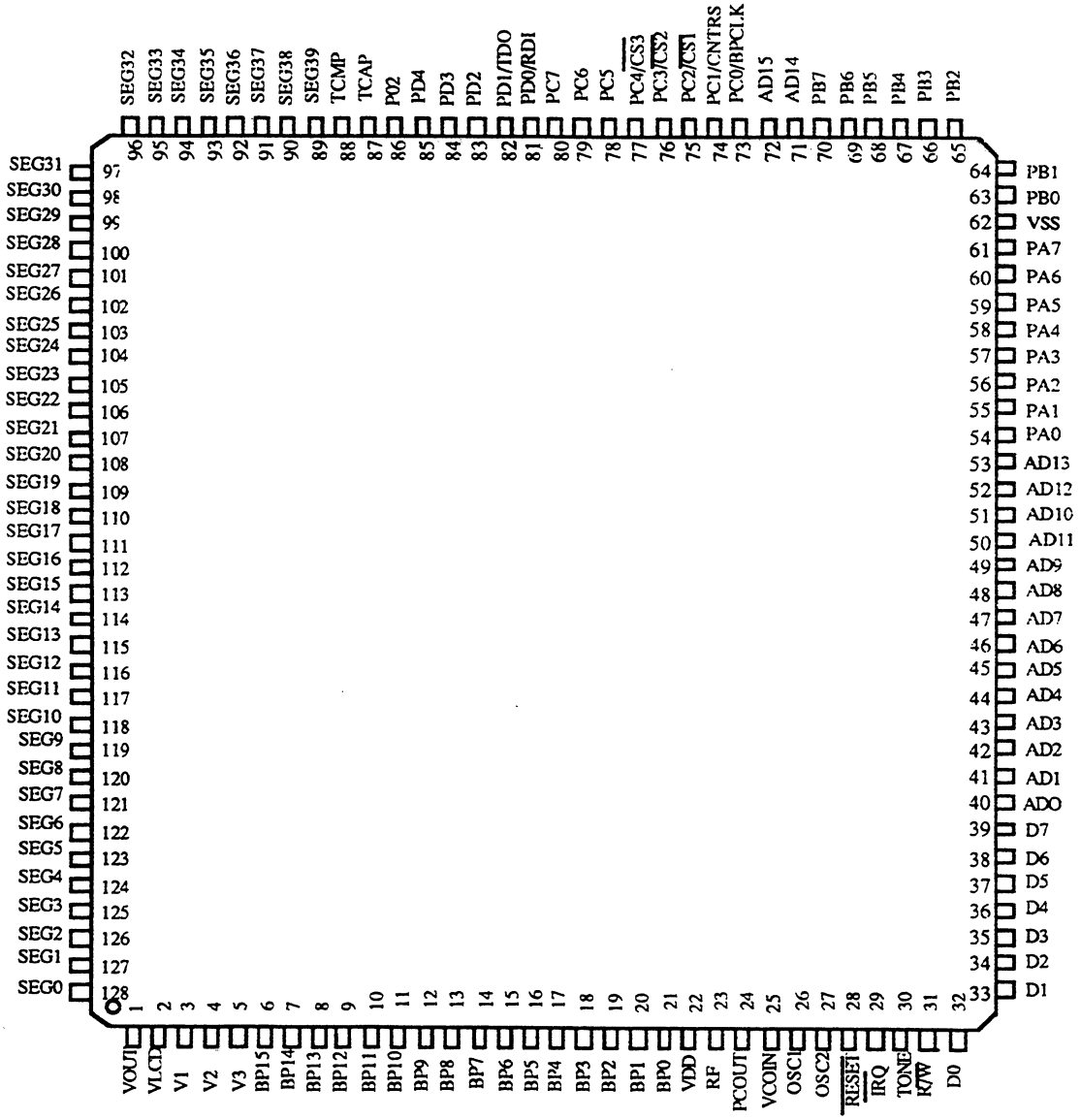
SECTION 10
MECHANICAL DATA

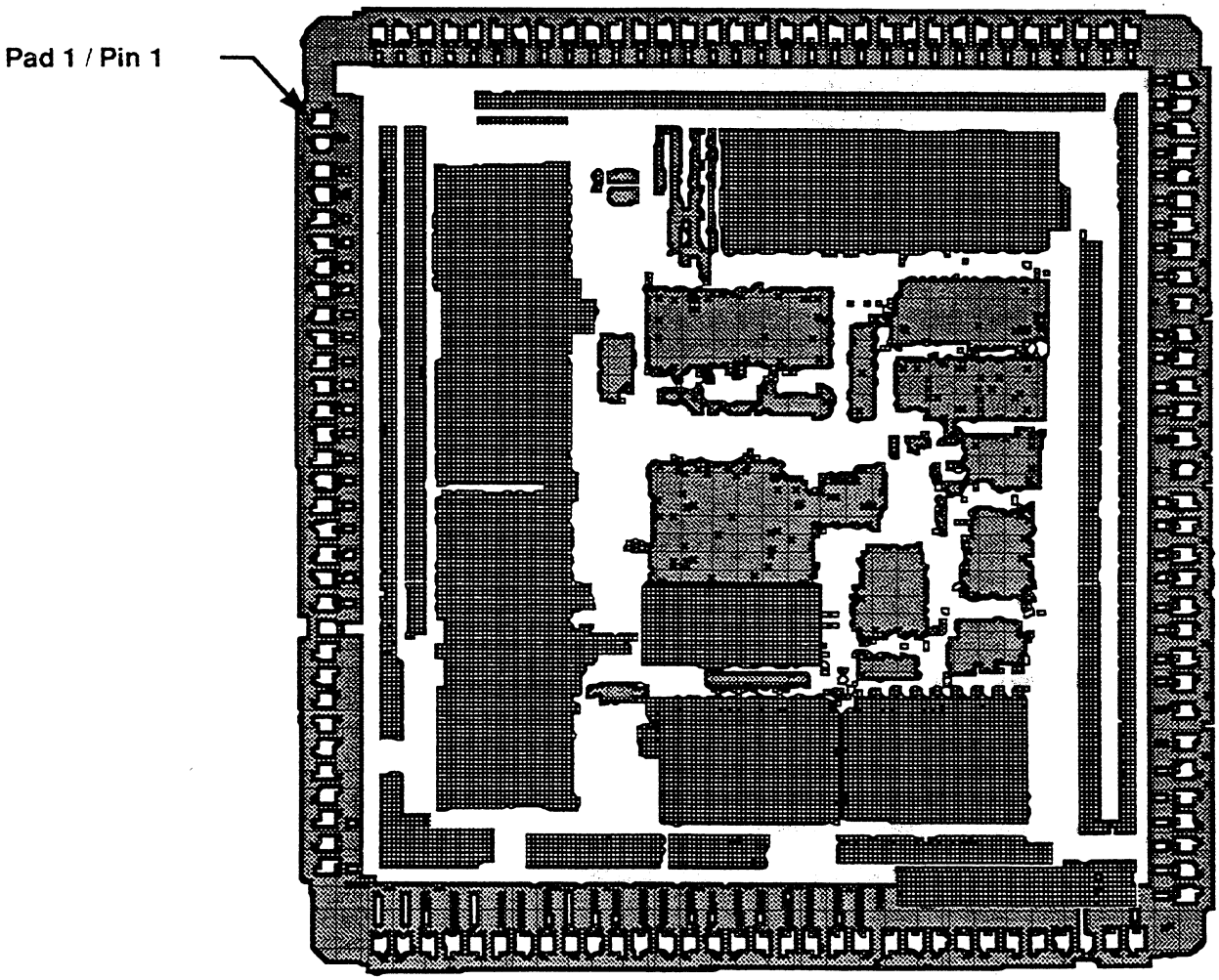
This section contains the pin assignment for the MC68HC05L9 microcomputer.

10.1 PIN ASSIGNMENT

128 PIN QFP



10.2 Bond Pad Diagram



Note 1: Pin # and Pad # are the same

Note 2: Silicon substrate can either be grounded or left open

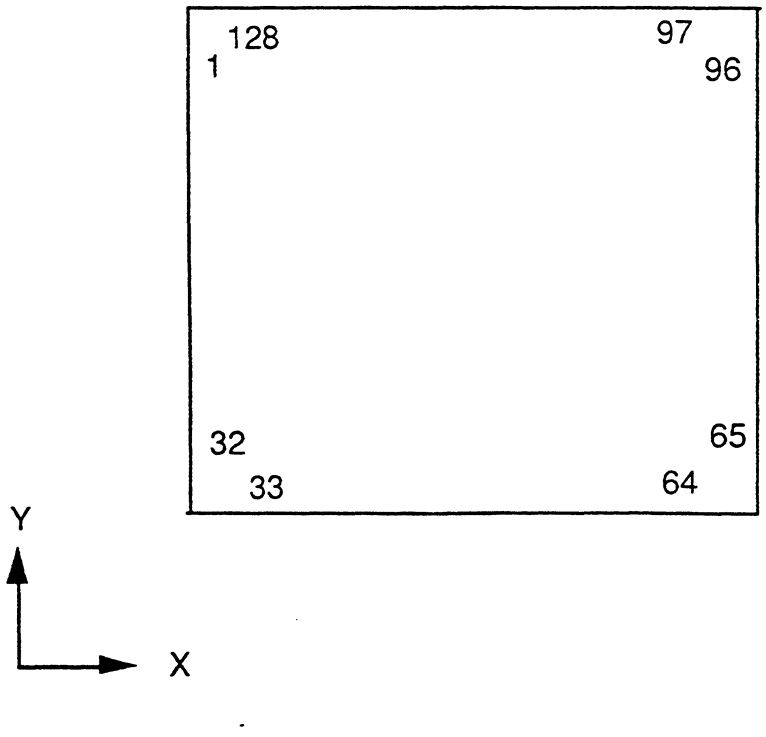
10.3 Bond Pad Coordinates (All units in um)

HC05L9 and HC05L7 are with the same coordinates

PIN NO.	X	Y
1	235	5441.5
2	235	5291.5
3	235	5125.5
4	235	4971.5
5	235	4821.5
6	235	4671.5
7	235	4521.5
8	235	4371.5
9	235	4221.5
10	235	4071.5
11	235	3921.5
12	235	3771.5
13	235	3621.5
14	235	3471.5
15	235	3321.5
16	235	3171.5
17	235	3021.5
18	235	2871.5
19	235	2721.5
20	235	2571.5
21	235	2421.5
22	235	2263.5
23	235	2113.5
24	235	1963.5
25	235	1813.5
26	235	1663.5
27	235	1513.5
28	235	1363.5
29	235	1213.5
30	235	1063.5
31	235	913.5
32	235	763.5
33	554	278.5
34	704	278.5
35	854	278.5
36	1004	278.5
37	1154	278.5
38	1304	278.5
39	1454	278.5
40	1604	278.5
41	1754	278.5
42	1904	278.5
43	2054	278.5
44	2204	278.5
45	2354	278.5
46	2504	278.5
47	2654	278.5
48	2804	278.5
49	2954	278.5

50	3104	278.5
51	3254	278.5
52	3404	278.5
53	3554	278.5
54	3727	278.5
55	3877	278.5
56	4027	278.5
57	4177	278.5
58	4327	278.5
59	4477	278.5
60	4627	278.5
61	4777	278.5
62	4927	278.5
63	5077	278.5
64	5227.5	278.5
65	5554.5	559
66	5554.5	709.5
67	5554.5	859.5
68	5554.5	1009.5
69	5554.5	1159.5
70	5554.5	1337.5
71	5554.5	1514.5
72	5554.5	1716.5
73	5554.5	1893.5
74	5554.5	2043.5
75	5554.5	2220.5
76	5554.5	2370.5
77	5554.5	2547.5
78	5554.5	2697.5
79	5554.5	2874.5
80	5554.5	3024.5
81	5554.5	3221
82	5554.5	3419
83	5554.5	3596
84	5554.5	3746
85	5554.5	3923
86	5554.5	4073
87	5554.5	4269.5
88	5554.5	4441.5
89	5554.5	4619.5
90	5554.5	4769.5
91	5554.5	4919.5
92	5554.5	5069.5
93	5554.5	5219.5
94	5554.5	5369.5
95	5554.5	5519.5
96	5554.5	5669.5
97	5227.5	5970
98	5077.5	5970
99	4927.5	5970
100	4777.5	5970
101	4627.5	5970
102	4477.5	5970
103	4327.5	5970
104	4177.5	5970

105	4027.5	5970
106	3877.5	5970
107	3727.5	5970
108	3577.5	5970
109	3427.5	5970
110	3277.5	5970
111	3127.5	5970
112	2977.5	5970
113	2827.5	5970
114	2677.5	5970
115	2527.5	5970
116	2377.5	5970
117	2227.5	5970
118	2077.5	5970
119	1927.5	5970
120	1777.5	5970
121	1627.5	5970
122	1477.5	5970
123	1327.5	5970
124	1177.5	5970
125	1027.5	5970
126	877.5	5970
127	727.5	5970
128	577.5	5970



APPENDIX A
MC68HC05L7

The MC68HC05L7 microcomputer unit (MCU) device is similar to the MC68HC05L9 device with few exceptions. These exceptions include 60 segments drive, incapable to connect to MC68HC68L9 or MC14150, 13-bit address bus and a low active chip select signal pin which selects address $2000-$3FFF. Fifteen I/O ports with PB2 and PB3 that can be selected as RDI and TDO. Since TCAP and TCMP does not exist in MC68HC05L7, all features of timer system that incorporate with TCAP and TCMP pins does not exist in MC68HC05L7. The entire data sheet of the MC68HC05L9 MCU applies to the MC68HC05L7 with the exceptions mentioned above. Figure A-1 illustrates the MC68HC05L7 block diagram and figure A-2 illustrates the MC68HC05L7 memory map.

A.1 INTRODUCTION

Information contained in **SECTION 1 INTRODUCTION** (general information, features, and block diagram) of this document applies to the MC68HC05L7 device except to the areas described in the following paragraphs.

A.1.1 Features

* 192 x 5 bit of on-chip display RAM
* 15 bidirectional I/O lines
* LCD driver circuitry with a selection of 1/16 or 1/8 multiplex and 60 segments drive
* Incapable to connect to MC68HC68L9 or MC141510
* 13 bit address bus

A.2 FUNCTIONAL PIN DESCRIPTION, INPUT/OUTPUT PROGRAMMING, MEMORY, CPU REGISTER, AND SELF-CHECK

Information contained in **SECTION 2 FUNCTIONAL PIN DESCRIPTION, INPUT/OUTPUT PROGRAMMING, MEMORY, CPU REGISTERS AND SELF-CHECK** of this document applies to the MC68HC05L7 MCU device except for the areas described in the following paragraphs.

FUNCTIONAL PIN DESCRIPTION

Pin PB7, PC0-PC7, PD0-PD4, P02, AD13-AD15, TCAP, TCMP, VOUT do not exist in MC68HC05L7. And the followings are additional pins that exist in MC68HC05L7.

A.2.1 CS-

CS- is an active low output used to select the external 8K x 8 memory. It selects memory address $2000-$3FFF.

A.2.2 SEG0-SEG59

These 60 output lines provide the segment drive signal to the LCD unit.

A.2.3 INPUT/OUTPUT PROGRAMMING

Port B (PB2-PB3) are used both as a general I/O port or SCI port. Bit 2 of $0F (receive enable) selects PB2 either as an I/O port or receive data input (RDI) and Bit 3 of $0F (transmit enable) selects PB3 either as I/O port or transmit data output. Following is how this two pins are configured:

RE (bit 2 of $0F)	PB2	TE (bit 3 of $0F)	PB3
1	RDI	1	TDO
0	I/O	0	I/O

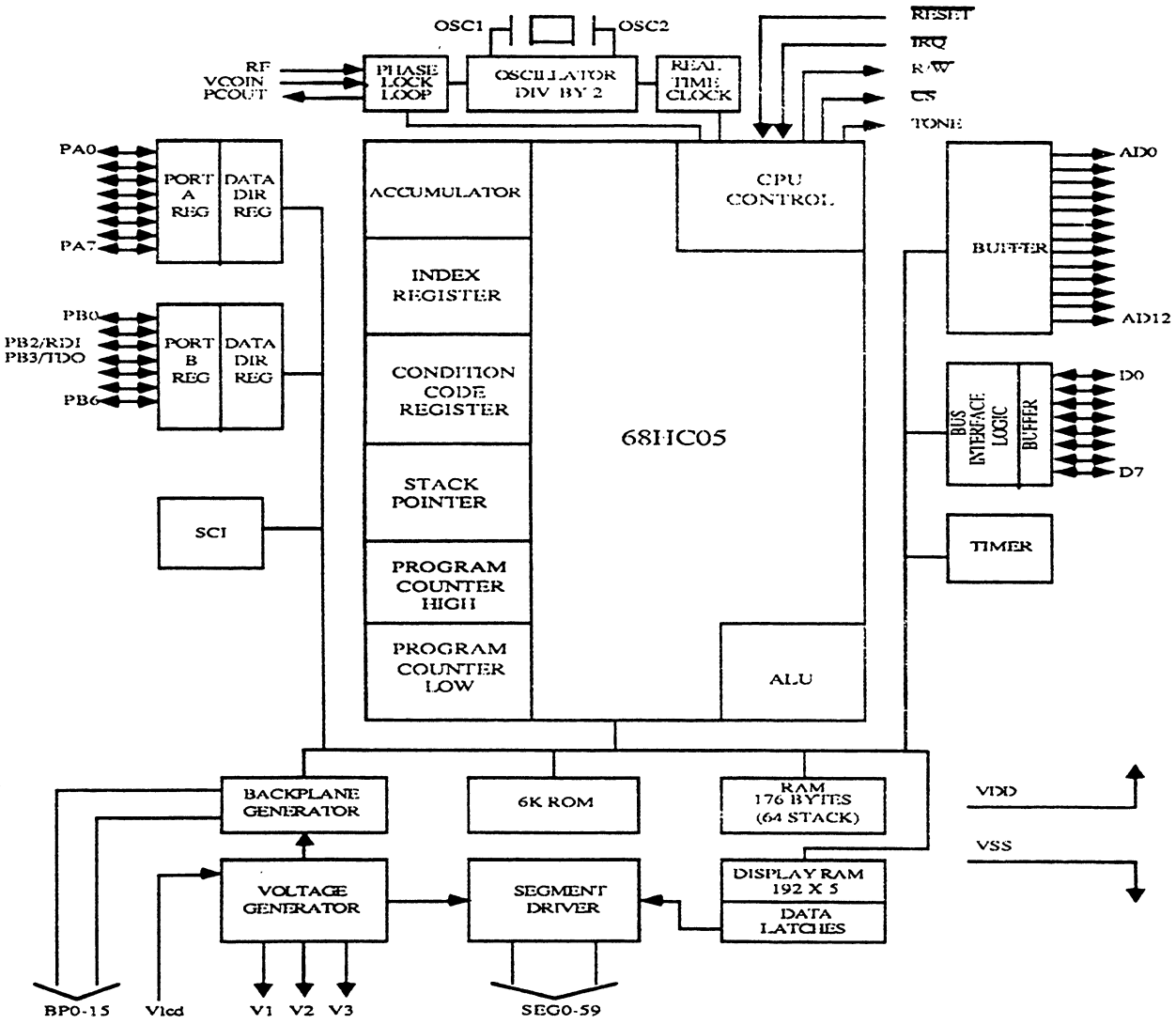


FIG. A-1 MC68HC05L7 MICROCOMPUTER BLOCK DIAGRAM

A.2.4 Memory

Fig. A-2 illustrates the MC68HC05L7 MCU device address map. As shown, display RAM is 192 x 5 bit; port C and port D, LCD bit of $0A, input capture high and input capture low register do not exist in MC68HC05L7. Finally, MC68HC05L7 is capable to address to 16 K bytes of memory.

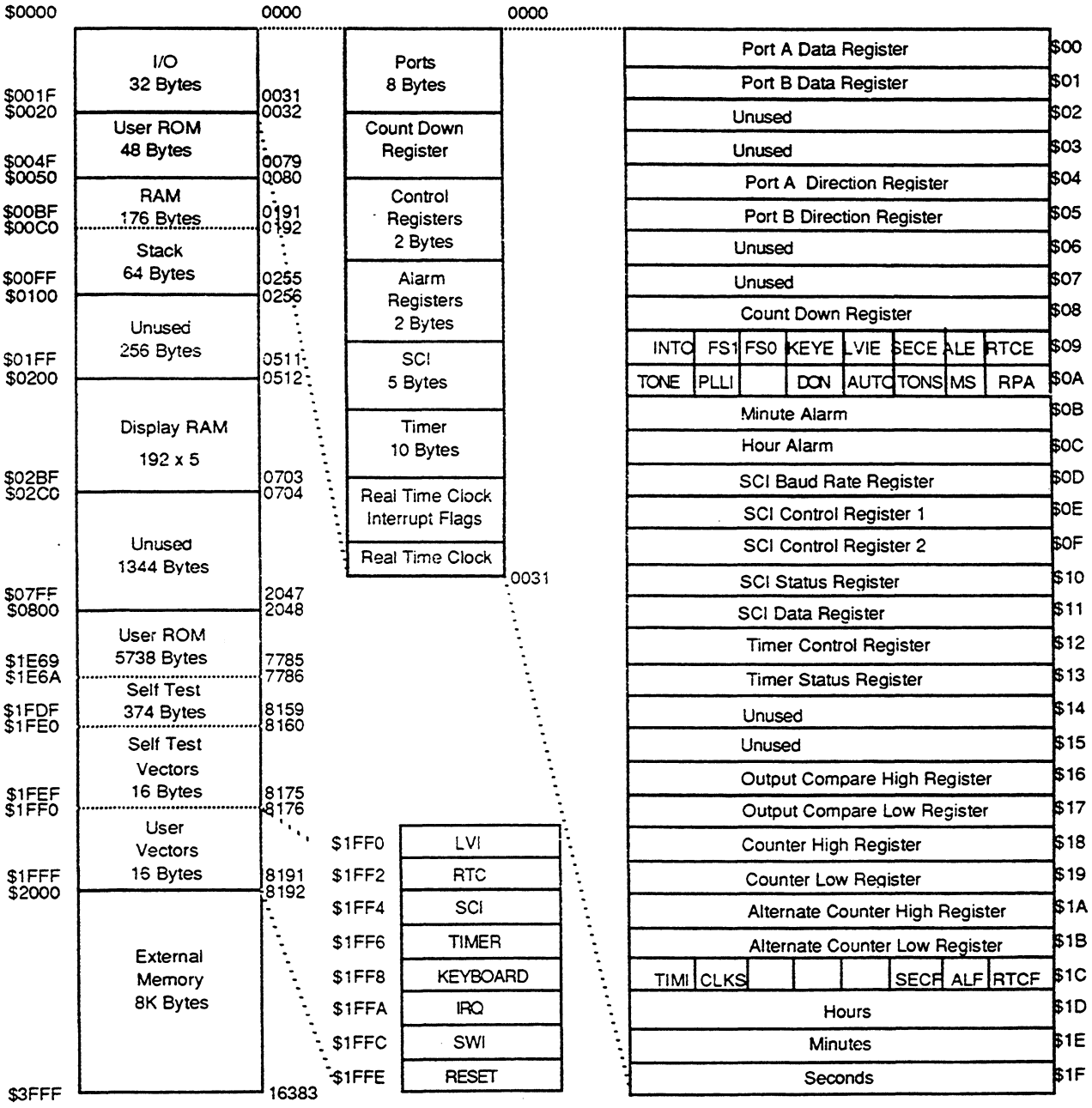
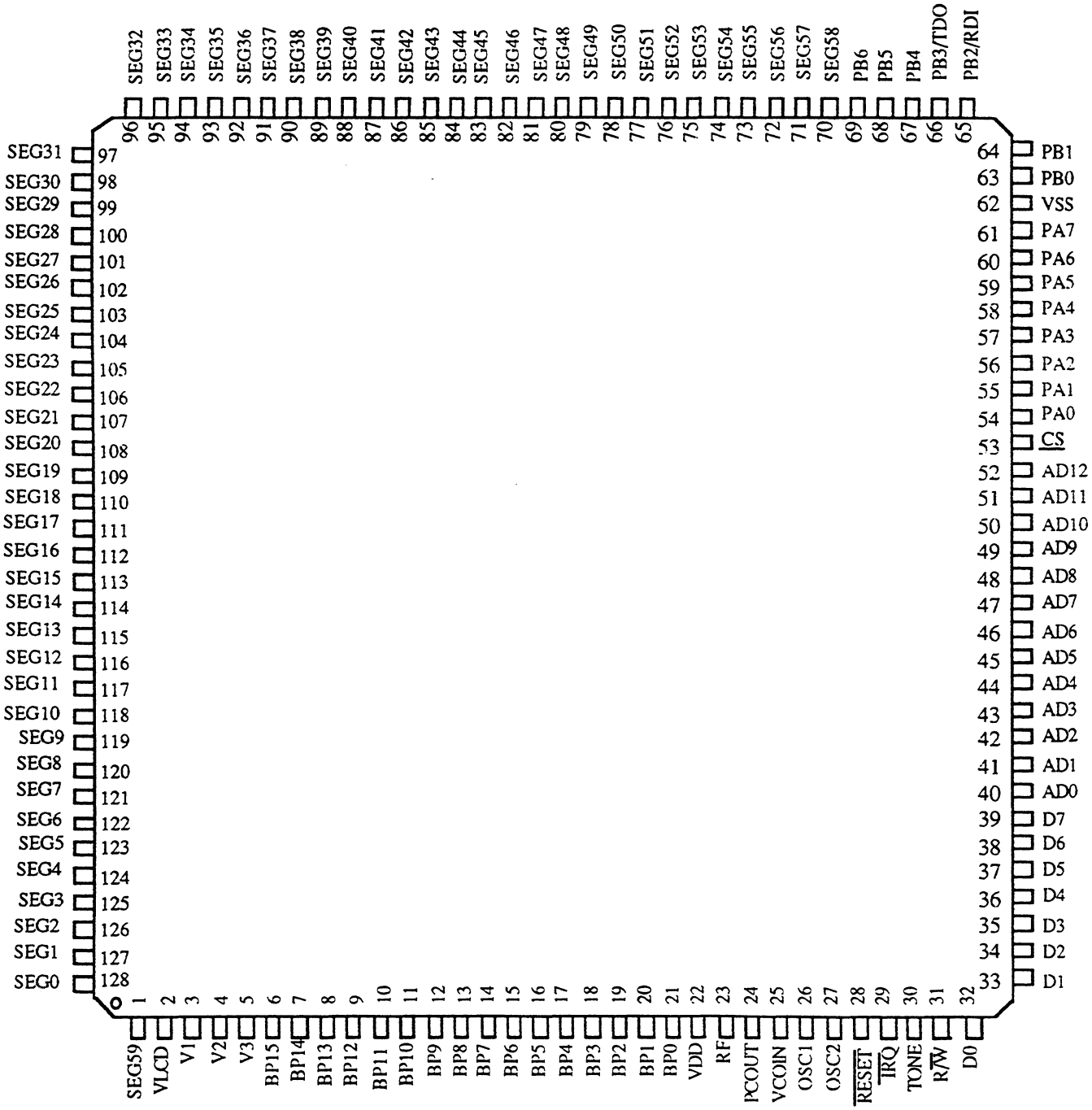


FIG. A-2 MC68HC05L7 Memory Map

A.3 PIN ASSIGNMENT

MC68HC05L7 MCU device pin assignments are identified below.

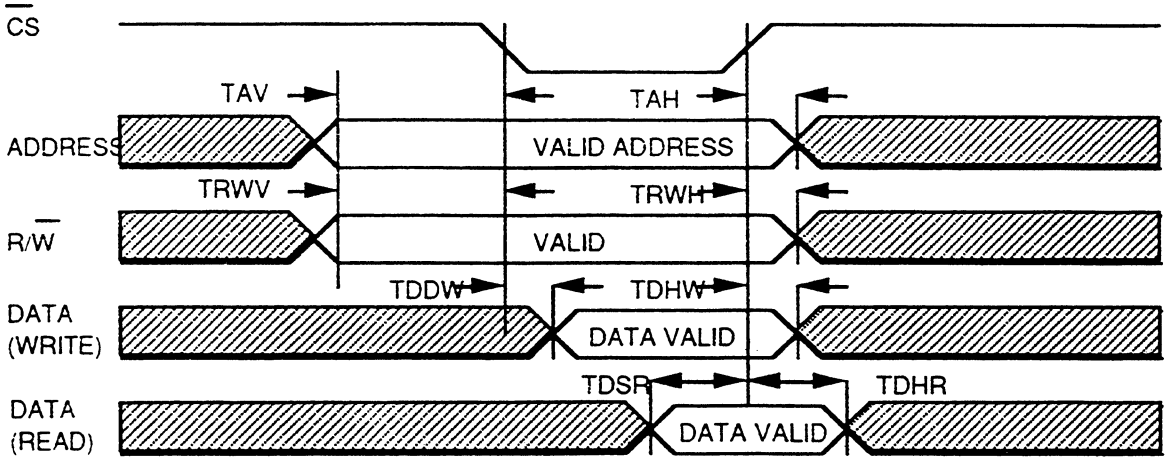
128-Pin QFP



A.4 BUS TIMING

Vdd = 5.0 Vdc +/-10%, Vss = 0 Vdc, TA = 0 to 70 deg C, Frequency = 2.45 MHZ

Characteristics	Symbol	Max	Min	Unit
Address vaild before $\overline{CS}$ fall	TAV	—	160	ns
Address hold from $\overline{CS}$ rise	TAH	—	0	ns
R/$\overline{W}$ Valid before $\overline{CS}$ fall	TRWV	—	160	ns
R/$\overline{W}$ hold from $\overline{CS}$ rise	TRWH	—	0	ns
Write data delay	TDDW	40	—	ns
Write data hold	TDHW	—	20	ns
Read data setup	TDSR	—	40	ns
Read data hold	TDHR	—	20	ns



Note: $\overline{CS}$ is driven low when address is within $2000-$3FFF and will held low for half bus cycle time.

Fig. A-3 MC68HC05L7 Bus Timing

APPENDIX B
MC68HC68L9

B.1 GENERAL

This is a LCD driver HCMOS chip. This HCMOS chip consists of 176 x 5 bit display RAM and is used with MC68HC05L9.

B.1.1 FEATURES

* 176 x 5-bit static RAM (display RAM)
* 55 LCD driving segments
* 8-bit address bus
* 5-bit bidirectional data bus
* 1:5 Bias
* 1:8 or 1: 16 multiplex
* 80-pin QFP or in Die form

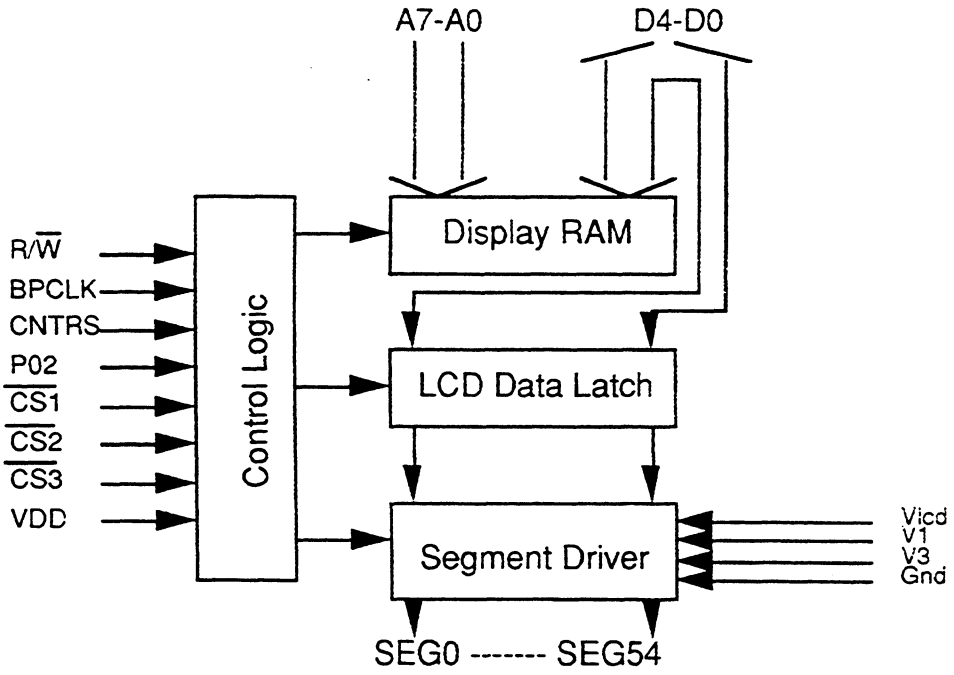


FIG. B-1 MC68HC68L9 Functional Block Diagram

B.2 FUNCTIONAL PIN DESCRIPTION

B.2.1 VDD and VSS

Power is supplied to the driver using these two pins. VDD is power and VSS is ground.

B.2.2 Vlcd, V1, V3

These input pins provide the voltage level for the segment driver and are connected to the Vout, V1 and V3 pins of MC68HC05L9.

B.2.3 D0-D4

Five bit wide bidirectional data bus which are connected to the D0-D4 of MC68HC05L9.

B.2.4 A0-A7

Eight bit wide address bus for addressing the display RAM and are connected to A0-A7 of MC68HC05L9.

B.2.5 CNTRS

A periodic active high output from MC68HC05L9 to MC68HC68L9 for timing synchronization. This pin is connected to PC1 of MC68HC05L9.

B.2.6 BPCLK

A 2 KHz (1:16 multiplex) or 1 KHz (1:8 multiplex) 50% duty cycle signal which provides the required frame frequency for the segment driver. This pin is connected to PC0 of MC68HC05L9.

B.2.7 P02

A bus clock input that is used for data bus timing synchronization. This pin is connected to P02 of MC68HC05L9.

B.2.8 SEG0-54

These 55 output lines provide the segment drive signal to the LCD panel. They are all grounded while display is turned off.

B.2.9 CS1-

This is an active low input for chip selection. When this pin is connected to CS1- of MC68HC05L9, it represents this chip is selected for display RAM address $280-$32F (with the condition that CS2- and CS3- is connected to VDD).

B.2.10 CS2-

This is an active low input for chip selection. When this pin is connected to CS2- of MC68HC05L9, it represents this chip is selected for display RAM address $330-$3DF (with the condition that CS1- and CS3- is connected to VDD).

B.2.11 CS3-

This is an active low input for chip selection. When this pin is connected to CS3- of MC68HC05L9, it represents this chip is selected for display RAM address $3E0-$48F (with the condition that CS1- and CS2- is connected to VDD).

B.2.12 R/W-

This input pin is connected to the MC68HC05L9 R/W- output to control the read and write of the display ram data.

B.3 ELECTRICAL CHARACTERISTICS

B.3.1 MAXIMUM RATINGS
(Voltages Referenced to VSS)

Ratings	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 to +7.0	V
Input Voltage	Vin	VSS-0.3 to VDD +0.3	V
Current Drain Per Pin Excluding VDD and VSS	I	25	mA
Operating Temperature Range	TA	0 to 70	°C
Storage Temperature Range	Tstg	-65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedence circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < or = (Vin or Vout) < or = VDD. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either VSS or VDD).

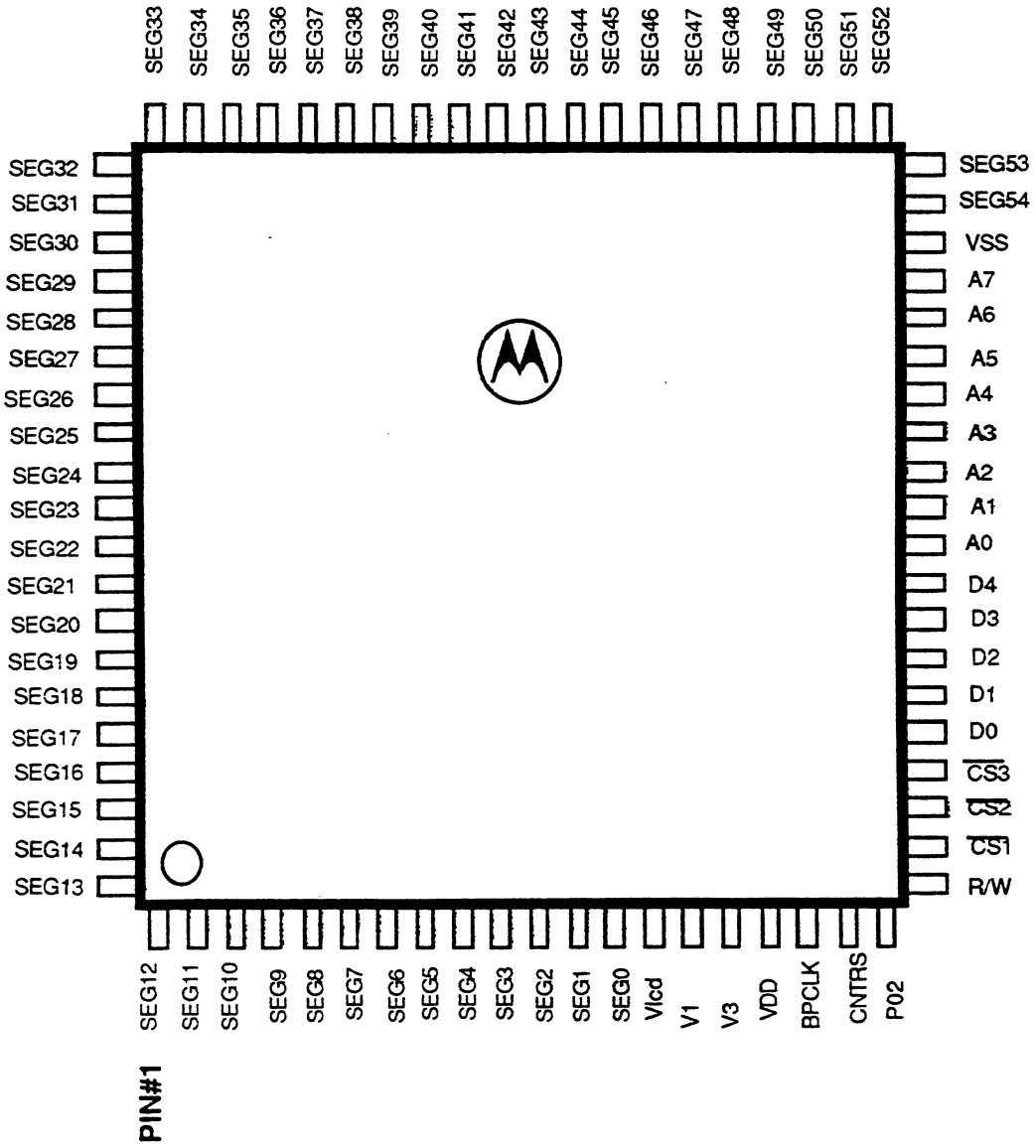
B.3.2 DC ELECTRICAL CHARACTERISTICS (TA = 0 to 70 deg. c)

Characteristics	Symbol	Min	Typ		Max	Unit
Input High Voltage R/W, BPCLK, CNTRS, P02 CS1, CS2, CS3, AD7-AD0, D4-D0	VIH	0.7xVDD	-		VDD	V
Input Low Voltage R/W, BPCLK, CNTRS, P02 CS1, CS2, CS3, AD7-AD0, D4-D0	VIL	VSS	-		0.2xVDD	V
Data Retention	VR	2.0	-		-	V
Input Current R/W, P02, AD7-AD0, D4-D0	Iin	-	-		±1	uA
Capacitance R/W, BPCLK, CNTRS, P02 CS1, CS2, CS3, AD7-AD0, D4-D0	Cin	- -	- -		8	pF
Internal Pull Up Resistance CS1, CS2, CS3	Rup	-	1		-	M Ohm
Internal Pull Down Resistance BPCLK, CNTRS	Rdn	-	1		-	M Ohm
Supply Current TYPICAL VDD = 5.0V	VDD		5.0V	5.5V	5.5V	
RUN (2.45MHZ)	IDD	-	280	330	400	uA
(1.22MHZ)	IDD	-	145	170	220	uA
(306KHZ)	IDD	-	50	60	100	uA
(153KHZ)	IDD	-	32	40	50	uA
STOP	IDD	-	3	4	5	uA
LCD	ILCD*	-	30	50	80	nA
TYPICAL VDD = 3.0V	VDD		3.0V	3.3v	3.3V	
RUN (1.22MHZ)	IDD	-	74	83	100	uA
(306KHZ)	IDD	-	20	23	50	uA
(153KHZ)	IDD	-	8	13	20	uA
STOP	IDD	-	1.6	4	4	uA
LCD	ILCD*	-	60	100	100	nA

*Note: ILCD is measured under zero loading (no LCD panel is connected)

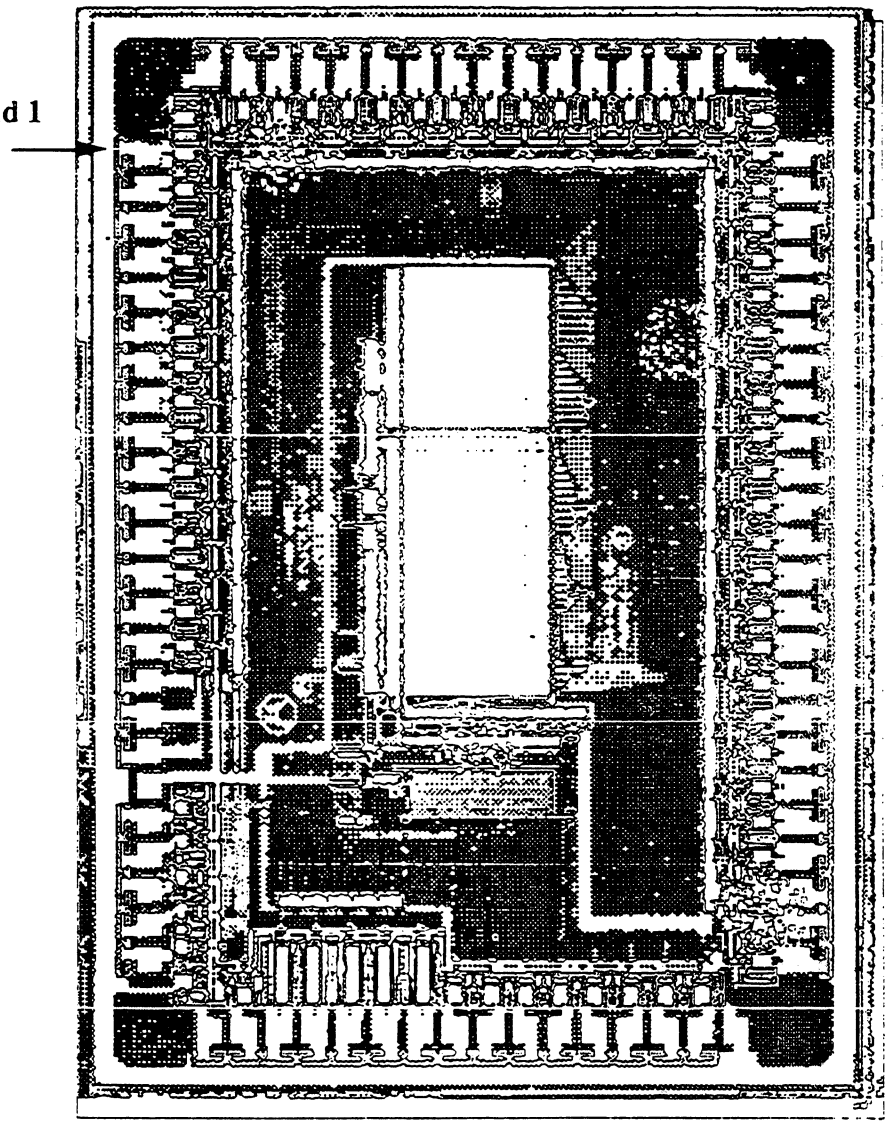
B.4 PIN ASSIGNMENT

80 Pins QFP



MC68HC68L9FU PIN ASSIGNMENT

B.5 BOND PAD DIAGRAM



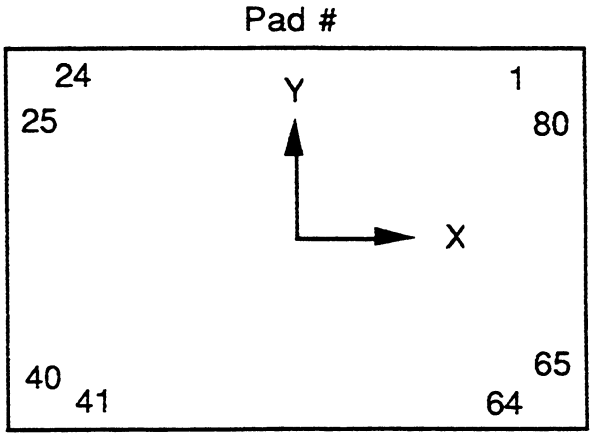
Note: Pad number and Pin number is DIFFERENT.

B.6 BOND PAD COORDINATE (all units in um)

PADNO.	PINNO.	X	Y
1	79	1657.75	1387
2	80	1500.75	1387
3	1	1350.75	1387
4	2	1200.75	1387
5	3	1050.75	1387
6	4	900.75	1387
7	5	750.75	1387
8	6	600.75	1387
9	7	450.75	1387
10	8	300.75	1387
11	9	150.75	1387
12	10	0.75	1387
13	11	-149.25	1387
14	12	-299.25	1387
15	13	-449.25	1387
16	14	-599.25	1387
17	15	-749.25	1387
18	16	-899.25	1387
19	17	-1049.25	1387
20	18	-1199.25	1387
21	19	-1349.25	1387
22	20	-1499.25	1387
23	21	-1649.25	1387
24	22	-1799.25	1387
25	23	-2096	1130.25
26	24	-2096	980.25
27	25	-2096	830.25
28	26	-2096	680.25
29	27	-2096	530.25
30	28	-2096	380.25
31	29	-2096	230.25
32	30	-2096	80.25
33	31	-2096	-69.75

34	32	-2096	-219.75
35	33	-2096	-369.75
36	34	-2096	-519.75
37	35	-2096	-669.75
38	36	-2096	-819.75
39	37	-2096	-969.75
40	38	-2096	-119.75
41	39	-1799.25	-1378.5
42	40	-1649.25	-1378.5
43	41	-1499.25	-1378.5
44	42	-1349.25	-1378.5
45	43	-1199.25	-1378.5
46	44	-1049.25	-1378.5
47	45	-899.25	-1378.5
48	46	-749.25	-1378.5
49	47	-599.25	-1378.5
50	48	-449.25	-1378.5
51	49	-299.25	-1378.5
52	50	-149.25	-1378.5
53	51	0.75	-1378.5
54	52	150.75	-1378.5
55	53	300.75	-1378.5
56	54	450.75	-1378.5
57	55	600.75	-1378.5
58	56	750.75	-1378.5
59	57	900.75	-1378.5
60	58	1050.75	-1378.5
61	59	1200.75	-1378.5
62	60	1350.75	-1378.5
63	61	1500.75	-1378.5
64	62	1650.75	-1378.5
65	63	1988.5	-1120.75
66	64	1988.5	-970.75
67	65	1988.5	820.75
68	66	1988.5	-670.75
69	67	1988.5	-520.75
70	68	1988.5	-370.75
71	69	1988.5	-220.75

72	70	1988.5	-70.75
73	71	1988.5	79.25
74	72	1988.5	229.25
75	73	1988.5	379.25
76	74	1988.5	529.25
77	75	1988.5	679.25
78	76	1988.5	829.25
79	77	1988.5	977.25
80	78	1988.5	1129.25



APPENDIX C
MC141510

C.1 GENERAL

This HCMOS LCD Driver is to combine three 68HC68L9 drivers into one and using TAB technology. It has 165 segment outputs operating at 1/8 or 1/16 duty with built-in 528 x 5 display RAM.

C.1.1 FEATURES

* Direct interface with MC68HC05L9
* 528 x 5 static display RAM
* 165 LCD driving segment outputs
* 8 bit address bus
* 5 bit bidirectional data bus
* 1:5 Bias
* 1:8 or 1:16 multiplex
* 194 pins TAB or die form (5 mil pad pitch)

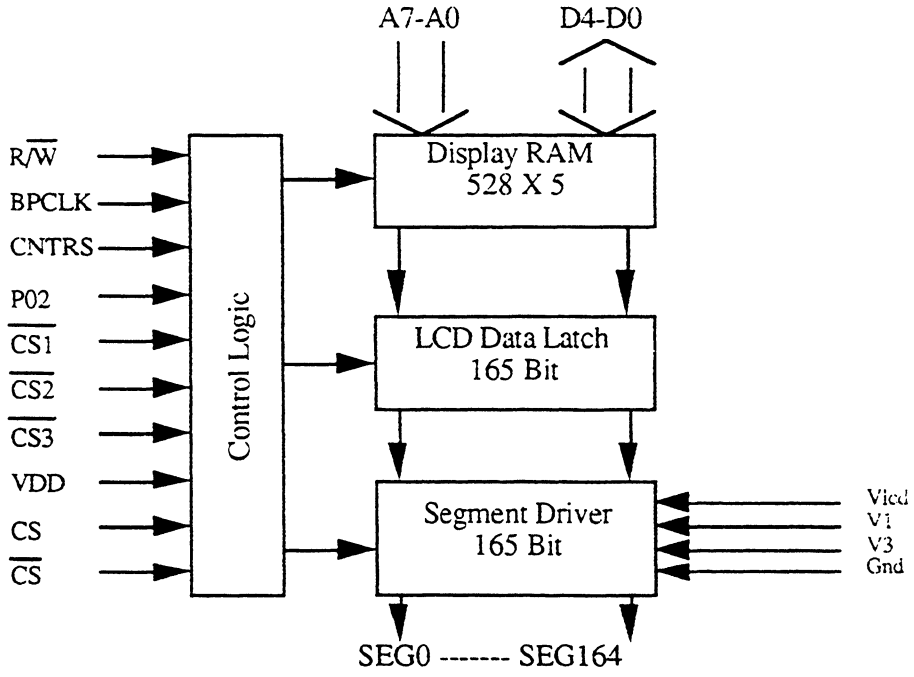


FIG. C.1 Functional Block Diagram

C.2. FUNCTIONAL PIN DESCRIPTION

C.2.1 VDD and VSS

Power is supplied to the driver using these two pins. VDD is power and VSS is ground.

C.2.2 Vlcd, V1, V3

These input pins provide the voltage level for the segment driver and are connected to the Vout, V1 and V3 pins of MC68HC05L9.

C.2.3 D0-D4

Five bit wide bidirectional data bus which are connected to the D0-D4 of MC68HC05L9.

C.2.4 A0-A7

Eight bit wide address bus for addressing the display RAM and are connected to A0-A7 of MC68HC05L9.

C.2.5 CNTRS

A periodic active high is output from MC68HC05L9 for timing synchronization. This pin is connected to PC1 of MC68HC05L9.

C.2.6 BPCLK

A 2 KHz (1:16 multiplex) or 1 KHz (1:8 multiplex) 50% duty cycle signal which provides the required frame frequency for the segment driver. This pin is connected to PC0 of MC68HC05L9.

C.2.7 P02

A bus clock input that is used for data bus timing synchronization. This pin is connected to P02 of MC68HC05L9.

C.2.8 SEG0-164

These 165 output lines provide the segment drive signal to the LCD panel. They are all grounded while display is turned off.

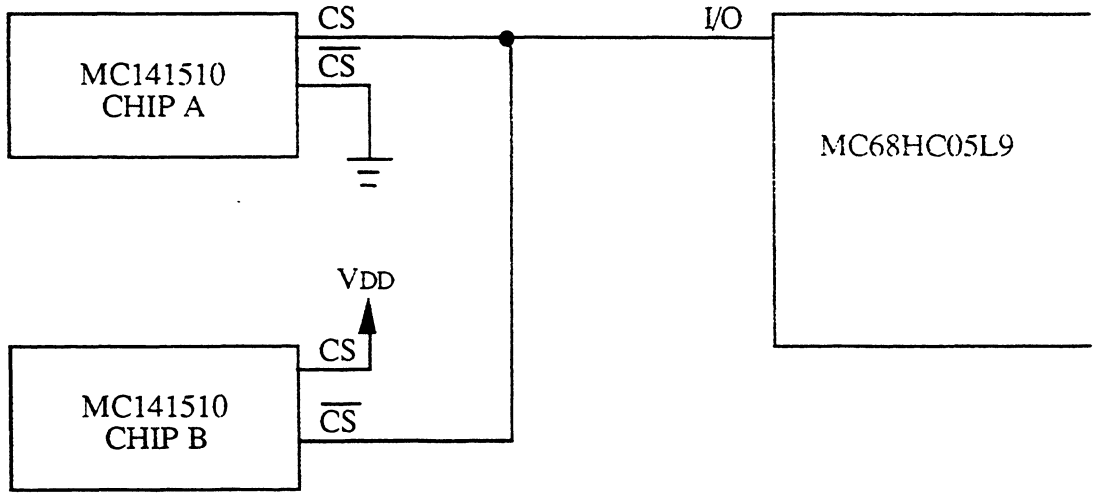
C.2.9 $\overline{CS1}$,$\overline{CS2}$,$\overline{CS3}$

These are active low inputs for chip selection of display RAM address. They should be connected to CS1, CS2 and CS3 of MC68HC05L9 respectively.

	SELECTED RAM ADDRESS
$\overline{CS1}$	$280-$32F
$\overline{CS2}$	$330-$3DF
$\overline{CS3}$	$3E0-$48F

C.2.10 CS, $\overline{CS}$

To enable the chip, both pins should be true.



I/O PIN = 1 CHIP A IS SELECTED

I/O PIN = 0 CHIP B IS SELECTED

C.3. ELECTRICAL CHARACTERISTICS

C.3.1 MAXIMUM RATINGS
(Voltages Referenced to VSS)

Ratings	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 to +7.0	V
Input Voltage	Vin	VSS-0.3 to VDD +0.3	V
Current Drain Per Pin Excluding VDD and VSS	I	25	mA
Operating Temperature Range	TA	0 to 70	°C
Storage Temperature Range	Tstg	-65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedence circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < or = (Vin or Vout) < or = VDD. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either VSS or VDD).

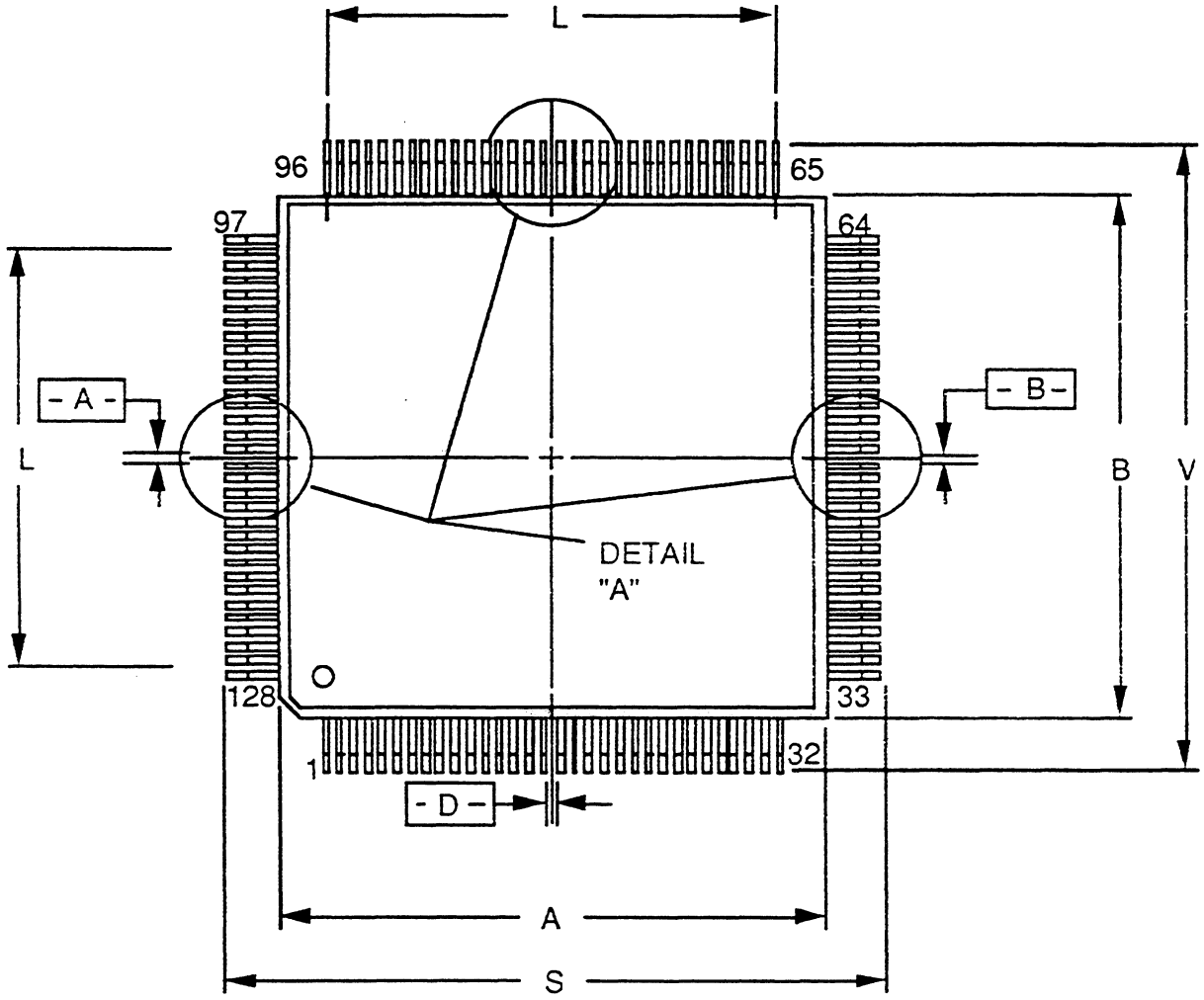
C.3.2 DC ELECTRICAL CHARACTERISTICS

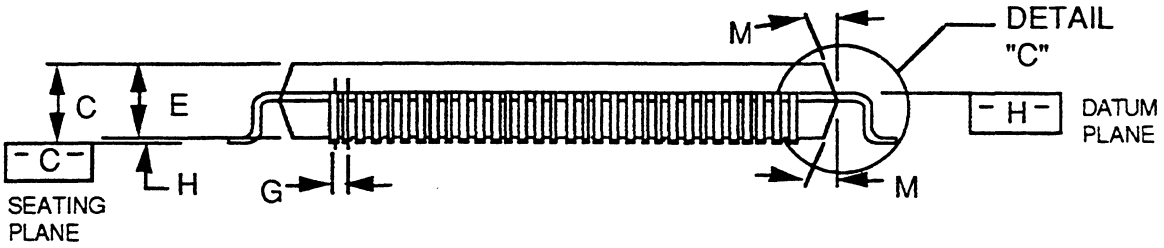
Characteristics	Symbol	Min	Typ	Max	Unit
Input High Voltage R/W, BPCLK, CNTRS, P02 $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, AD7-AD0, D4-D0	VIH	0.7xVDD	-	VDD	V
Input Low Voltage R/W, BPCLK, CNTRS, P02 $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, AD7-AD0, D4-D0	VIL	VSS	-	0.2xVDD	V
Data Retention	VR	2.0	-	-	V
Input Current R/W, P02, AD7-AD0, D4-D0	Iin	-	-	±1	uA
Capacitance R/W, BPCLK, CNTRS, P02 $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, AD7-AD0, D4-D0	Cin	- -	- -	8	pF
Internal Pull Up Resistance $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$	Rup	-	1	-	M Ohm
Internal Pull Down Resistance BPCLK, CNTRS	Rdn	-	1	-	M Ohm

APPENDIX D

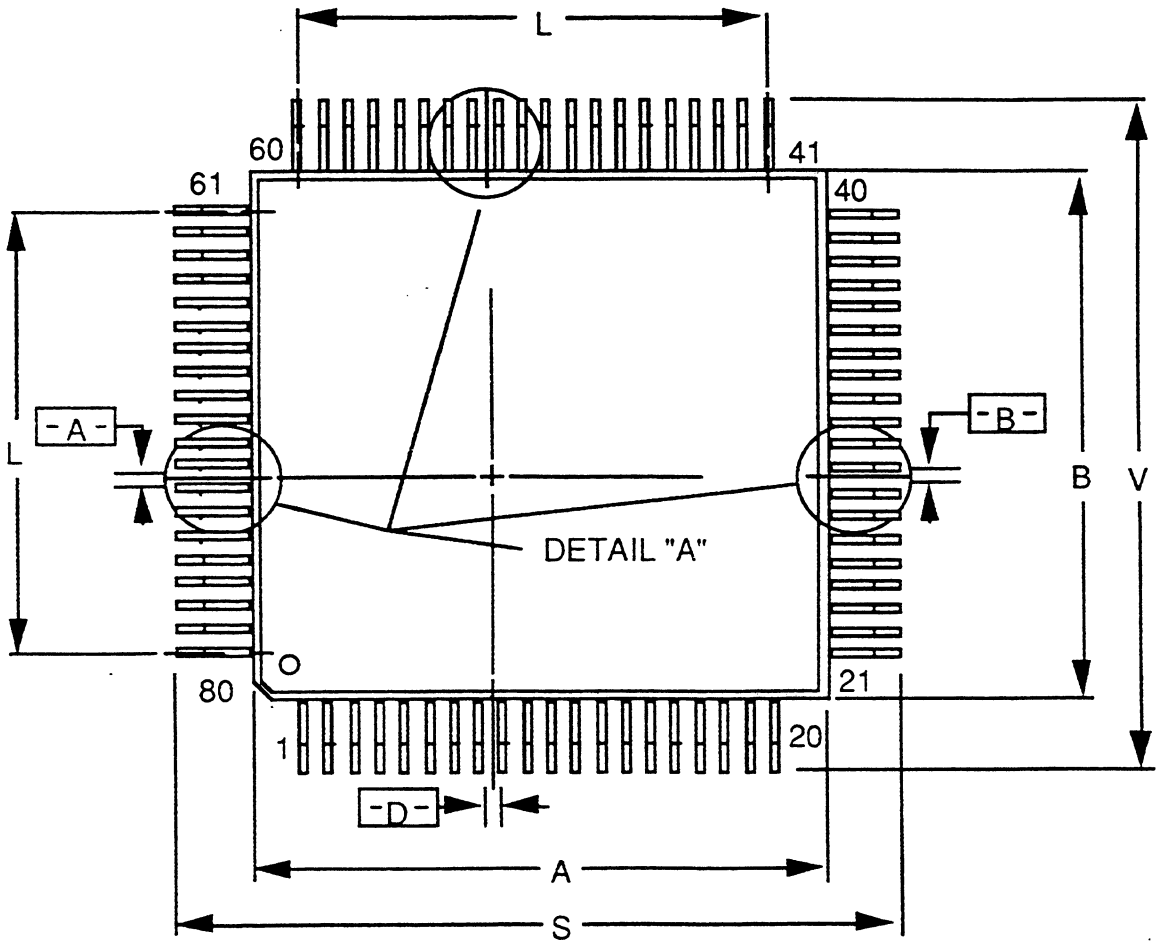
PACKAGE DIMENSIONS

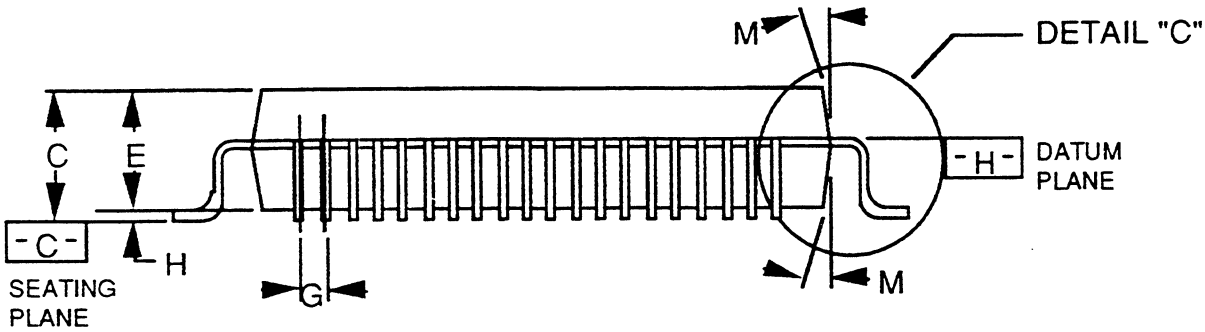
MC68HC05L7/L9

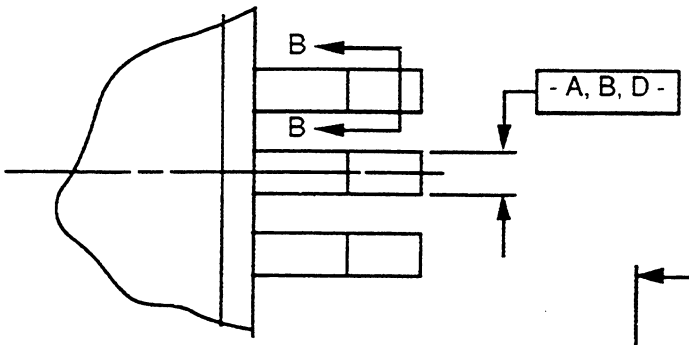




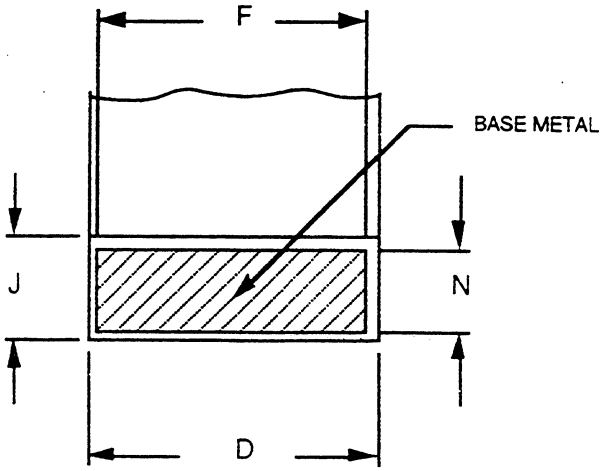
MC68HC68L9



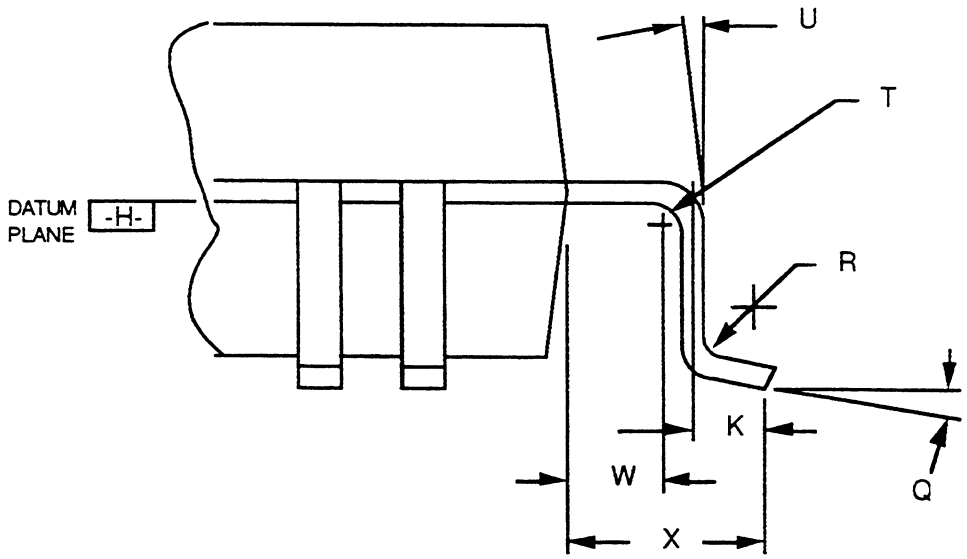




DETAIL "A"



SECTION B-B



DETAIL "C"

Dimension of 80/128 QFP

NOTES :

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION : MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25(.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND DETERMINED AT THE DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS MIN	MAX
A	27.61	28.11
B	27.61	28.11
C	---	---
D	0.31	0.46
E	3.39	3.59
F	---	
G	0.8 BSC	
H	0.3	0.15
J	---	
K	1.1	0.51
L	---	
M	---	
N	---	
Q	---	
R	---	
S	31.9	32.5
T	---	
U	---	
V	31.9	32.5
W	---	
X	---	

128 PIN QFP

DIM	MILLIMETERS MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5	10
N	0.13	0.17
Q	---	7
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0 min	---
V	16.95	17.45
W	0.40 NOM	
X	1.6 REF	

80 PIN QFP

APPENDIX E

E.1 MONITOR PART

E.1.1 ORDER PART NUMBER

Device	Package	P/N	Remark
MC68HC05L9	128QFP	MC68HC05L9FT1	OSC off in 'STOP' mode
	128QFP	MC68HC05L9FT2	OSC on in 'STOP' mode
	DIE	MCC68HC05L9D1	OSC off in 'STOP' mode
	DIE	MCC68HC05L9D2	OSC on in 'STOP' mode
MC68HC05L7	128QFP	MC68HC05L7FT1	OSC off in 'STOP' mode
	128QFP	MC68HC05L7FT2	OSC on in 'STOP' mode
	DIE	MCC68HC05L7D1	OSC off in 'STOP' mode
	DIE	MCC68HC05L7D2	OSC on in 'STOP' mode

E.1.2 EXTERNAL PROGRAM ACCESS

PB6 (PIN 69) has to be 'HIGH' from power-on reset and remain 'HIGH' for full operation.

With this set up arrangement interrupt vectors will be divert to below addresses:

3FE8 - 3FEA	LVI
3FFB - 3FED	RTC
3FEE - 3FF0	SCI
3FF1 - 3FF3	TIMER
3FF4 - 3FF6	KEYBOARD
3FF7 - 3FF9	IRQ
3FFA - 3FFC	SWI
3FFD - 3FFF	RESET

Each interrupt vector will then consist of three consecutive bytes. The first byte is the 'JUMP' instruction and the next two bytes will be the 16 bit address vector.

E.1.3 MONITOR MODE

For the monitor part to be running in the monitor mode, the PB6 (PIN 69) will need to be held 'LOW" from power-on reset.

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Freescale Semiconductor, Inc.

MC68HC05L7 MCU ORDERING FORM

Date_____ Customer PO Number_____

Customer Company_____

Application _____ End Equipment _____

Address_____

City_____ State_____ Zip_____

Country_____

Phone_____ Extention_____

Customer Contact Person _____

Customer Part Number _____
(12 Charaters Maximum - If Applicable)

Temperature Range

- ☐ 0 to +70 deg.C for package
- ☐ -40 to +85 deg.C for package
- ☐ 25 deg. C for dice

Package type

- ☐ 128-pin QFP
- ☐ Die

Operation Bus Frequency

- ☐ 153 KHz
- ☐ 306 KHz
- ☐ 1.22 MHz
- ☐ 2.45 MHz

On-Chip Function Used

- ☐ Timer
- ☐ LVI
- ☐ SCI
- ☐ RTC

Voltage Supply (+/- 10%)

- ☐ +5.0 V
- ☐ *+3.0 V

Mask Options

1. Crystal Oscillator in 'STOP' Mode
   - ☐ Running (RTC option)
   - ☐ Stop

2. POR & STOP RECOVERY CYCLES
   - ☐ 16**
   - ☐ 4064

* 3.0V is not guaranteed at 2.45 MHz bus frequency operation.
** Longer delay is needed through external R-C reset circuit for the crystal OSC to become stable from POR. Mask option of OSC stops in 'STOP' mode is not recommended if this option is chosen

Special Electrical Provisions : _____
(Customer specifications required.)

Device to be tested to Motorola data sheet specifications. Customer part number, if used as part of marking, is for reference purposes only.

_____
(SIGNATURE)

Device to be tested to customer specifications.(Customer specifications required.)

_____
(SIGNATURE)

ONLY ONE SIGNATURE IS REQUIRED TO PROCESS THIS ORDERING FORM.

MC68HC05L9 MCU ORDERING FORM

Date_____ Customer PO Number_____

Customer Company_____

Application _____ End Equipment _____

Address_____

City_____ State_____ Zip_____

Country_____

Phone_____ Extention_____

Customer Contact Person _____

Customer Part Number _____
(12 Charaters Maximum - If Applicable)

Temperature Range

- ☐ 0 to +70 deg.C for package
- ☐ -40 to +85 deg.C for package
- ☐ 25 deg. C for dice

Package type

- ☐ 128-pin QFP
- ☐ Die

Operation Bus Frequency

- ☐ 153 KHz
- ☐ 306 KHz
- ☐ 1.22 MHz
- ☐ 2.45 MHz

On-Chip Function Used

- ☐ Timer
- ☐ LVI
- ☐ SCI
- ☐ RTC

Voltage Supply (+/- 10%)

- ☐ +5.0 V
- ☐ *+3.0 V

Mask Options

1. Crystal Oscillator in 'STOP' Mode
   - ☐ Running (RTC option)
   - ☐ Stop

2. POR & STOP RECOVERY CYCLES
   - ☐ 16**
   - ☐ 4064

* 3.0V is not guaranteed at 2.45 MHz bus frequency operation.
** Longer delay is needed through external R-C reset circuit for the crystal OSC to become stable from POR. Mask option of OSC stops in 'STOP' mode is not recommended if this option is chosen

Special Electrical Provisions : _____
(Customer specifications required.)

Device to be tested to Motorola data sheet specifications. Customer part number, if used as part of marking, is for reference purposes only.

_____
(SIGNATURE)

Device to be tested to customer specifications.(Customer specifications required.)

_____
(SIGNATURE)

ONLY ONE SIGNATURE IS REQUIRED TO PROCESS THIS ORDERING FORM.

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