MC68HC05P9/D

HC05

MC68HC05P9

TECHNICAL
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MC68HC05P9

HCMOS MICROCONTROLLER UNIT

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SECTION 1
INTRODUCTION

The MC68HC05P9 high-density complementary metal-oxide semiconductor (HCMOS) microcontroller unit (MCU) is a member of the popular M68HC05 Family of microcontrollers. This high-performance, low-cost MCU is a complete system on a single chip. The MCU features include the following:

1.1 Features

- Popular M68HC05 Central Processor Unit (CPU)
- Memory-Mapped Input/Output (I/O) Registers
- 2112 Bytes of User ROM including 16 User Vector Locations
- 128 Bytes of Static RAM (SRAM)
- 20 Bidirectional I/O Pins and One Input-Only Pin
- Synchronous Serial I/O Port (SIOP)
- Fully Static Operation (No Minimum Clock Speed)
- On-Chip Oscillator with Crystal/Ceramic Resonator Connections
- 16-Bit Capture/Compare Timer
- Self-Check Mode
- Four-Channel 8-bit A/D Converter
- Power-Saving STOP, WAIT, and Data Retention Modes
- Single 3.3-Volt to 5.0-Volt Power Requirement
- 8 × 8 Unsigned Multiply Instruction
- 28-Pin Dual-in-Line Package (DIP)
- 28-Pin Small Outline Integrated Circuit (SOIC)

The following mask options are available:

- Edge-Sensitive or Edge- and Level-Sensitive External Interrupt Trigger
- Most Significant Bit (MSB) First or Least Significant Bit (LSB) First Serial Data Format
- Computer Operating Properly (COP) Watchdog Timer

Figure 1-1 shows the structure of the MC68HC05P9 MCU.

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1.2 Structure

Figure 1-1 shows the architecture of the MC68HC05P9 MCU.

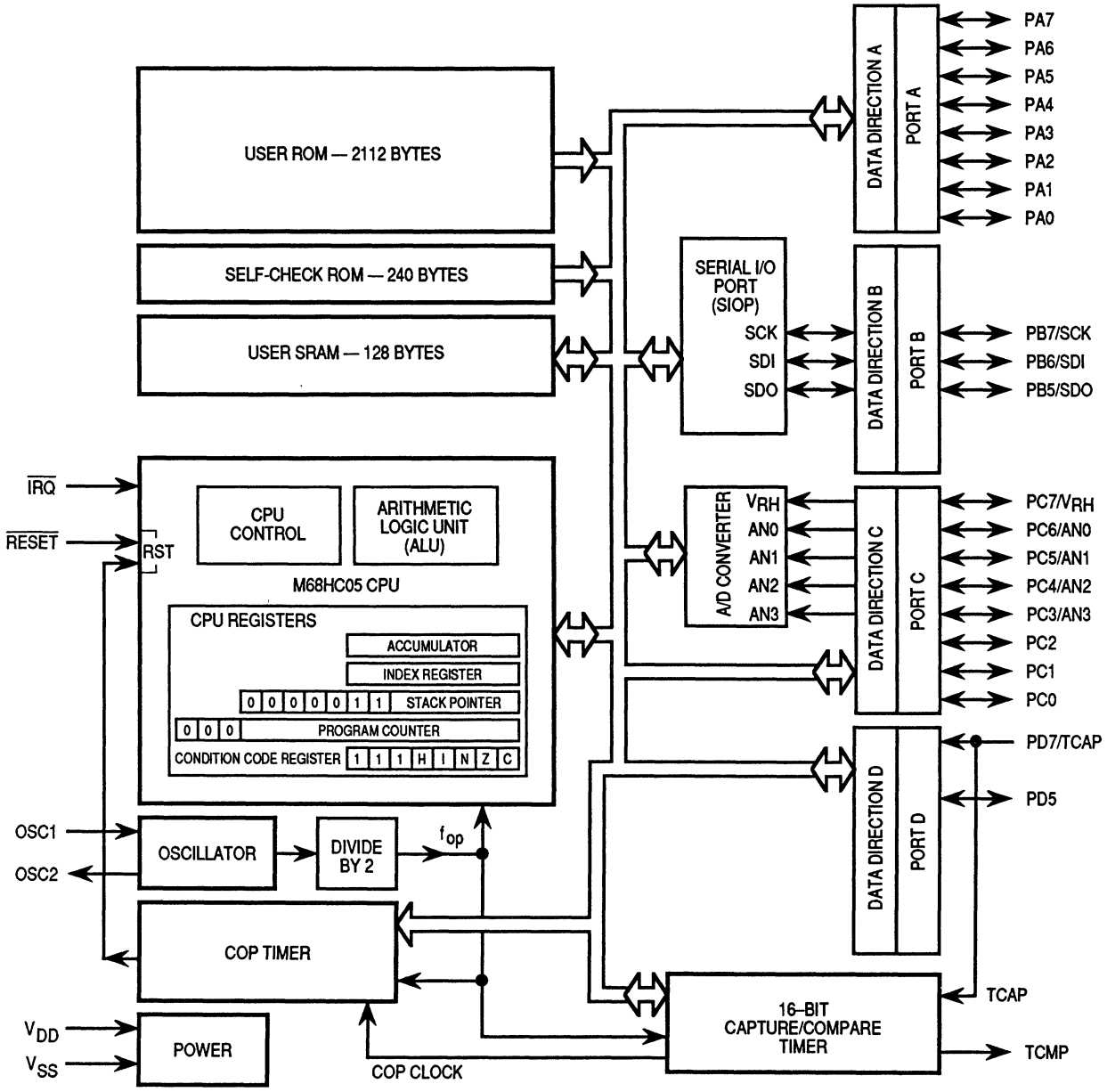

Figure 1-1. MC68HC05P9 Block Diagram

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SECTION 2
PIN DESCRIPTIONS

Section 2 details the MC68HC05P9 pin assignments and describes the function of each pin.

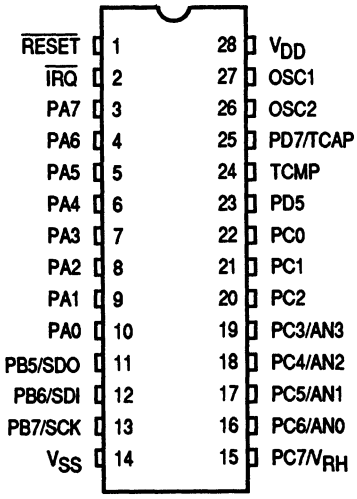

Figure 2-1. Pin Assignments

2.1 V_{DD} and V_{SS}

Power is supplied to the MCU through V_{DD} and V_{SS}. V_{DD} is the power supply, and V_{SS} is ground. The MCU operates from a single 5-volt (nominal) power supply.

Very fast signal transitions occur on the MCU pins. The short rise and fall times place very high short-duration current demands on the power supply. To prevent noise problems, take special care to provide good power supply bypassing at the MCU. Use bypass capacitors with good high-frequency characteristics, and position them as close to the MCU as possible. Bypassing requirements vary, depending on how heavily the MCU pins are loaded.

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2.2 OSC1 and OSC2

OSC1 and OSC2 are the control connections for the on-chip oscillator. The OSC1 and OSC2 pins can accept the following:

- A crystal (Refer to Figure 2-2.)
- A ceramic resonator (Refer to Figure 2-2.)
- An external clock signal (Refer to Figure 2-3.)

The frequency, f_{osc}, of the oscillator or external clock source is divided by two to produce the internal operating frequency, f_{op}.

2.2.1 Crystal

The circuit in Figure 2-2 shows a typical crystal oscillator circuit for an AT-cut, parallel resonant crystal. Follow the crystal supplier's recommendations, as the crystal parameters determine the external component values required to provide maximum stability and reliable start-up. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances. Mount the crystal and components as close as possible to the pins for start-up stabilization and to minimize output distortion.

2.2.2 Ceramic Resonator

In cost-sensitive applications, use a ceramic resonator in place of the crystal. Use the circuit in Figure 2-2 for a ceramic resonator, and follow the resonator manufacturer's recommendations, as the resonator parameters determine the external component values required for maximum stability and reliable starting. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances.

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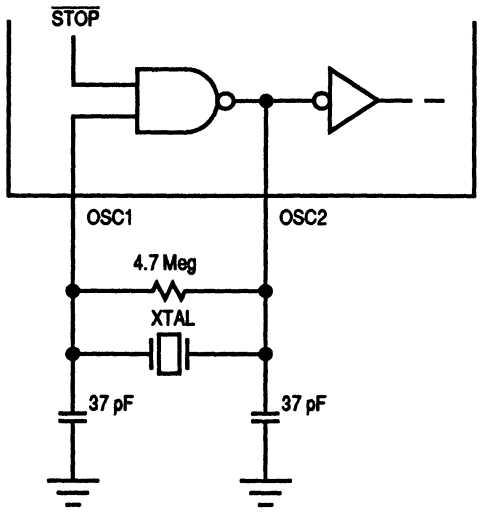

Figure 2-2. Crystal/Ceramic Resonator Connections

2.2.3 External Clock

An external clock from another CMOS-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in Figure 2-3.

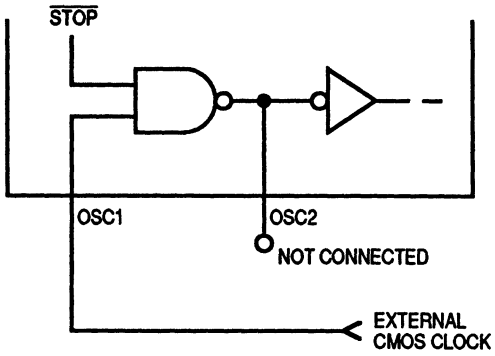

Figure 2-3. External Clock Source Connections

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2.3 $\overline{\text{RESET}}$

A logical zero on the $\overline{\text{RESET}}$ pin forces the MCU to a known start-up state. (Refer to **4.1 Resets** for more information.)

2.4 $\overline{\text{IRQ}}$ (External Interrupt Request)

$\overline{\text{IRQ}}$ is a dual-purpose pin with the following functions:

- Applying asynchronous external interrupts (Refer to **4.2 Interrupts**.)
- Putting the MCU in self-check mode. (Refer to **9.1 Self-Check Circuit**.)

2.5 TCMP (Timer Compare)

The output compare feature of the capture/compare timer uses the TCMP pin for output. (Refer to **SECTION 6 CAPTURE/COMPARE TIMER** for more information.)

2.6 Parallel I/O

The MCU's 20 I/O pins form four I/O ports. Each I/O pin is programmable as an input or an output. The contents of the data direction register (DDR) determine the data direction for the port. Writing a logical one to a DDR bit enables the output buffer for that pin; a logical zero disables the output buffer. A reset initializes all implemented DDR bits to logical zero to put the pins in the input mode.

NOTE

Connect any unused inputs and I/O pins to an appropriate logical level (e.g., either V_{DD} or V_{SS}). Although the I/O ports do not require termination for proper operation, termination is recommended to reduce the possibility of electrostatic damage.

A reset does not initialize the four port data registers. The port data registers for ports A, B, C, and D are at addresses $0000, $0001, $0002, and $0003, respectively. To avoid undefined levels, write the data registers before writing the DDR bits.

When a pin is programmed as an output, reading the associated port bit actually reads the value of the output data latch and not the voltage on the pin itself. When a pin is programmed as an input, reading the port bit reads the voltage

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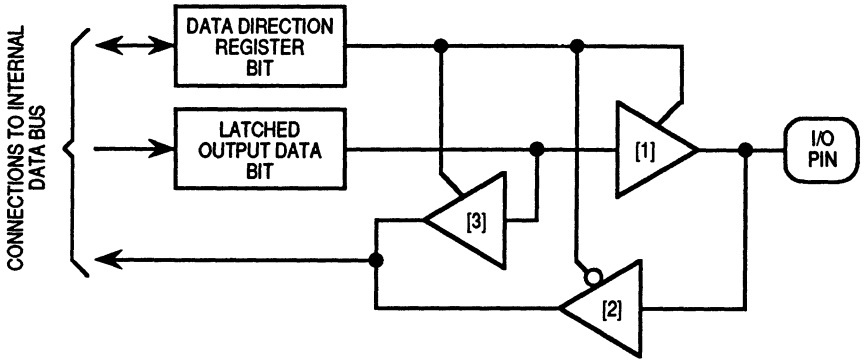
level on the I/O pin. The output data latch can always be written, regardless of the state of its DDR bit. (Refer to Figure 2-4 for typical port circuitry, and to Table 2-1 for a summary of I/O pin functions.)



[1] This output buffer enables the latched output to drive the pin when DDR bit is 1 (output mode).
[2] This input buffer is enabled when DDR bit is 0 (input mode).
[3] This input buffer is enabled when DDR bit is 1 (output mode).

Figure 2-4. Parallel I/O Port Circuit

Table 2-1. I/O Pin Functions

R/$\overline{W}$	DDR	I/O Pin Functions
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch, which drives the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in output mode. The output data latch is read.

NOTE: R/$\overline{W}$ is an internal signal.

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2.6.1 Port A

PA7–PA0 form an 8-bit general-purpose bidirectional I/O port. The contents of data direction register A (DDRA) determine whether each pin is an input or an output. Figure 2-5 shows the port A data register and DDRA.

PORTA — Port A Data Register **$0000**

	Bit 7	6	5	4	3	2	1	Bit 0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	PORT DATA REGISTER NOT CHANGED BY RESET							

DDRA — Data Direction Register A **$0004**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
RESET:	0	0	0	0	0	0	0	0

Figure 2-5. Port A Data Register and DDRA

DDRA7–DDRA0 — Port A Data Direction Bits

These read/write bits determine whether the PA7–PA0 pins are inputs or outputs.

1 = Corresponding port pin configured as output
0 = Corresponding port pin configured as input

2.6.2 Port B and Serial I/O Port (SIOP)

PB7/SCK (serial clock), PB6/SDI (serial data input), and PB5/SDO (serial data output) form a 3-bit shared function I/O port. Port B can be either the SIOP or a general-purpose I/O port. Figure 2-6 shows the port B data register and data direction register B (DDRB). Bits 4–0 of these registers are not implemented.

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PORTB — Port B Data Register **$0001**

	Bit 7	6	5	4	3	2	1	Bit 0
	PB7/SCK	PB6/SDI	PB5SDO	0	0	0	0	0
RESET:	PORT DATA REGISTER NOT CHANGED BY RESET							

DDRB — Data Direction Register B **$0005**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRB7	DDRB6	DDRB5	1	1	1	1	1
RESET:	0	0	0	0	0	0	0	0

Figure 2-6. Port B Data Register and DDRB

DDRB7–DDRB5 — Port B Data Direction Bits

These read/write bits determine whether the PB7–PB5 pins are inputs or outputs.

1 = Corresponding port pin configured as output
0 = Corresponding port pin configured as input

The SIOP is a three-wire master/slave system. When the SIOP is enabled, SCK serves as a clock output in master mode or as a clock input in slave mode. SDI is the serial data input, and SDO is the serial data output. User software can change the settings of DDRB7–5 to override these defaults if necessary.

A factory-set mask option selects either an MSB first or an LSB first SIOP data format.

Use these same pins as a general-purpose I/O port when the SIOP system is disabled. DDRB7–5 determine the data direction through the port B pins (input or output).

2.6.3 Port C and Analog-to-Digital Converter

Port C, as an 8-bit shared function port, shares five of its pins with the analog-to-digital (A/D) converter. When the A/D converter is not enabled, PC7–PC0 form an 8-bit general-purpose bidirectional I/O port. The contents of data direction register C (DDRC) determine whether each pin is an input or an output.

When the A/D converter is enabled, PC7 becomes V_{RH}, and PC6–PC3 become AN3–AN0 (analog inputs 3–0). The values of CH1 and CH0 in the A/D status

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and control register (ADSCR) select one of the four pins as the input to the A/D converter. When the A/D converter is enabled, a digital read of port C gives a logical zero from the selected analog input pin. A digital read of port C's remaining pins gives their correct digital values. V_{RH} is the positive (high) reference voltage for the A/D converter. V_{SS} is the negative (low) reference voltage. A reset turns off the A/D converter and configures port C as a general-purpose I/O port. (Refer to **SECTION 8 ANALOG-TO-DIGITAL CONVERTER.**)

PORTC — Port C Data Register **$0002**

	Bit 7	6	5	4	3	2	1	Bit 0
	PC7/VRH	PC6/AN0	PC5/AN1	PC4/AN2	PC3/AN3	PC2	PC1	PC0
RESET:	PORT DATA REGISTER NOT CHANGED BY RESET							

DDRC — Data Direction Register C **$0006**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
RESET:	0	0	0	0	0	0	0	0

Figure 2-7. Port C Data Register and DDRC

DDRC7–DDRC0 — Port C Data Direction Bits

These read/write bits determine whether the PC7–PC0 pins are inputs or outputs.

1 = Corresponding port pin configured as output
0 = Corresponding port pin configured as input

2.6.4 Port D and Timer Capture (TCAP)

PD7/TCAP and PD5 form a 2-bit special function I/O port. The PD7/TCAP pin serves as both the edge-detecting input capture line for the capture/compare timer and as a general-purpose digital input. PD7/TCAP can be used as a digital input even when the timer is using it as the input capture pin. There is no output driver associated with the PD7/TCAP pin. PD5 is a general-purpose digital I/O pin whose direction is controlled by bit 5 of data direction register D (DDRD). Figure 2-8 shows the port D data register and DDRD.

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PORTD — Port D Data Register **$0003**

	Bit 7	6	5	4	3	2	1	Bit 0
	PD7/TCAP	0	PD5	1	0	0	0	0
RESET:	PORT DATA REGISTER NOT CHANGED BY RESET							

DDRD — Data Direction Register D **$0007**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	DDRD5	0	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Figure 2-8. Port D Data Register and DDRD

DDRD5 — Port D Data Direction Bit

This read/write bit determines whether the PD5 pin is an input or an output.

1 = PD5 configured as output

0 = PD5 configured as input

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SECTION 3
CENTRAL PROCESSOR UNIT

This section describes the registers, instruction set, and addressing modes of the M68HC05 central processor unit (CPU). The STOP and WAIT modes, initiated by software instructions, are also described here.

The M68HC05 CPU executes all instructions of the earlier M6805 and M146805 instruction sets and is upgraded to include an 8 × 8 bit unsigned multiply instruction.

3.1 CPU Registers

The CPU contains the following registers:

- Accumulator (A)
- Index register (X)
- Stack pointer (SP)
- Program counter (PC)
- Condition code register (CCR)

These registers are hard-wired within the CPU and are not part of the memory map. Figure 3-1 is a block diagram of the MC68HC05 CPU.

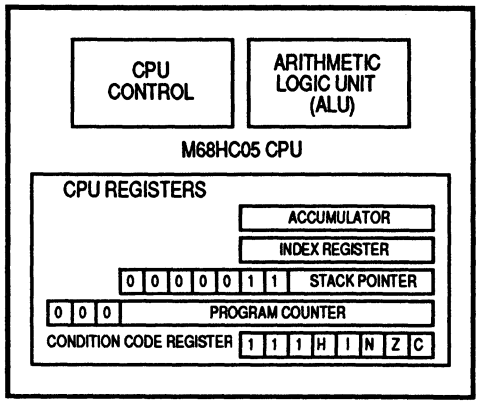

Figure 3-1. CPU Block Diagram

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Figure 3-2 shows the five CPU registers.

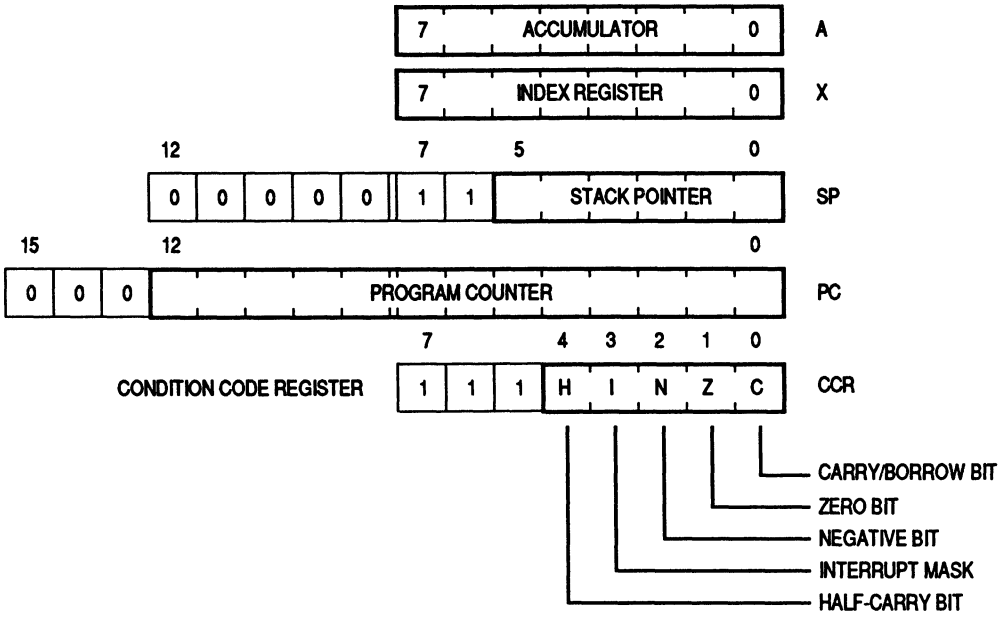

Figure 3-2. Programming Model

3.1.1 Accumulator (A)

The accumulator is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and results of arithmetic and nonarithmetic operations. (Refer to Figure 3-3.)

Figure 3-3. Accumulator (A)

3.1.2 Index Register (X)

The 8-bit index register can perform two functions:

- Indexed addressing
- Temporary storage

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In indexed addressing with no offset, the index register contains the low byte of the operand address, and the high byte is assumed to be $00. In indexed addressing with an 8-bit offset, the CPU finds the operand address by adding the index register contents to an 8-bit immediate value. In indexed addressing with a 16-bit offset, the CPU finds the operand address by adding the index register contents to a 16-bit immediate value. (Refer to **3.3 Addressing Modes**.)

The index register can also serve as an auxiliary accumulator for temporary storage. (Refer to Figure 3-4.)

Figure 3-4. Index Register (X)

3.1.3 Stack Pointer (SP)

The stack pointer is a 13-bit register that contains the address of the next free location on the stack. During a reset or after the reset stack pointer (RSP) instruction, the stack pointer contents are set to $FF. The address in the stack pointer is decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the seven most significant bits of the stack pointer are permanently set to 0000011. (Refer to Figure 3-5.) These seven bits are appended to the six least significant register bits to produce an address within the range of $00FF–$00C0. Subroutines and interrupts may use up to 64 locations. If 64 locations are exceeded, the stack pointer wraps around and writes over the previously stored information. A subroutine call occupies two locations on the stack; an interrupt uses five locations.

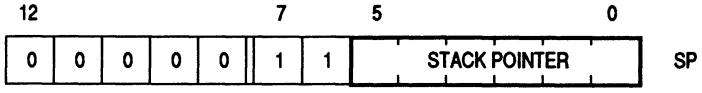

Figure 3-5. Stack Pointer (SP)

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3.1.4 Program Counter (PC)

The program counter is a 13-bit register that contains the address of the next instruction or operand to be fetched. Because addresses are often 16-bit values, the program counter may be thought of as having three additional upper bits that are always zeros. (Refer to Figure 3-6.)

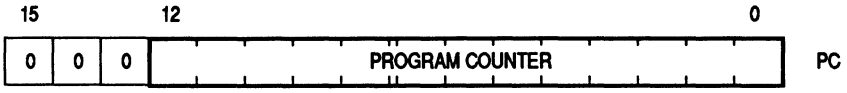

Figure 3-6. Program Counter (PC)

Normally, the address in the program counter increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, and interrupt operations load the program counter with an address other than that of the next sequential location.

3.1.5 Condition Code Register (CCR)

The 5-bit condition code register uses four bits to indicate the results of the instruction just executed. A fifth bit is the interrupt mask. (Refer to Figure 3-7.) These bits can be individually tested by a program, allowing specific actions as a result of their states. Consider the condition code register as having three additional upper bits that are always ones.

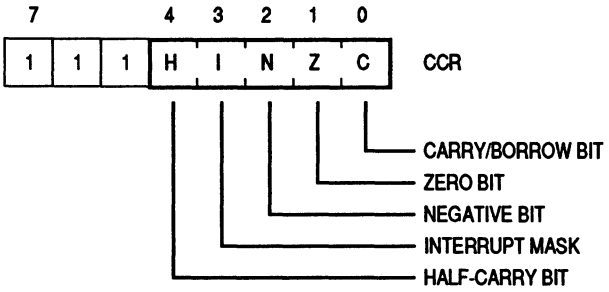

Figure 3-7. Condition Code Register (CCR)

The following paragraphs explain the functions of the lower five bits of the condition code register.

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3.1.5.1 Half-Carry Bit (H Bit)

When the half-carry bit is set, it means that a carry occurred between bits 3 and 4 of the accumulator during the last ADD or ADC operation. The half-carry bit is required for binary-coded decimal (BCD) arithmetic operations.

3.1.5.2 Interrupt Mask (I Bit)

When the interrupt mask is set, timer interrupts and external interrupts are disabled. Interrupts are enabled when the interrupt mask is cleared. When an interrupt occurs, the interrupt mask is automatically set after the CPU registers are saved on the stack, but before the interrupt vector is fetched. If an interrupt occurs while the interrupt mask is set, the interrupt is latched. Normally, the interrupt is processed as soon as the interrupt mask is cleared.

A return from interrupt (RTI) instruction pulls the CPU registers from the stack, restoring the interrupt mask to its cleared state. After any reset, the interrupt mask is set and can only be cleared by a software instruction.

3.1.5.3 Negative Bit (N Bit)

The negative bit is set when the result of the last arithmetic operation, logical operation, or data manipulation was negative. (Bit 7 of the result was a logical one.)

The negative bit can also be used to check an often-tested flag by assigning the flag to bit 7 of a register or memory location. Loading the accumulator with the contents of that register or location then sets or clears the negative bit according to the state of the flag.

3.1.5.4 Zero Bit (Z Bit)

The zero bit is set when the result of the last arithmetic operation, logical operation, or data manipulation was zero.

3.1.5.5 Carry/Borrow Bit (C Bit)

The carry/borrow bit is set when a carry out of bit 7 of the accumulator occurred during the last arithmetic operation, logical operation, or data manipulation. The carry/borrow bit is also set or cleared during bit test and branch instructions and during shifts and rotates.

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3.2 Arithmetic/Logic Unit (ALU) and CPU Control

The ALU performs the arithmetic and logical operations defined by the instruction set.

The binary arithmetic circuits decode the instruction and set up the ALU for the desired function. Most binary arithmetic is based on the addition algorithm, carrying out subtraction as negative addition. Multiplication is not performed as a discrete instruction but as a chain of addition and shift operations within the ALU. The multiply instruction (MUL) requires 11 internal processor cycles to complete this chain of operations.

The CPU control circuitry sequences the logic elements of the ALU to carry out the required operations.

3.3 Addressing Modes

The CPU uses eight addressing modes for flexibility in accessing data. These addressing modes define the manner in which the CPU finds the data required to execute an instruction. The eight addressing modes are as follows:

- Inherent
- Immediate
- Direct
- Extended
- Indexed, no offset
- Indexed, 8-bit offset
- Indexed, 16-bit offset
- Relative

3.3.1 Inherent

The inherent addressing mode is used for instructions with no operand (e.g. STOP) and for some of the instructions that act on data in the CPU registers (e.g. CLRA). No memory address is required for inherent instructions. Inherent instructions are one byte long. Table 3-1 lists the instructions to use in the inherent addressing mode.

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Table 3-1. Inherent Addressing Instructions

Instruction	Mnemonic
Arithmetic Shift Left	ASLA, ASLX
Arithmetic Shift Rght	ASRA, ASRX
Clear Carry Bit	CLC
Clear Interrupt Mask	CLI
Clear	CLRA, CLRX
Complement	COMA, COMX
Decrement	DECA, DECX
Increment	INCA, INCX
Logical Shift Left	LSLA, LSLX
Logical Shift Right	LSRA, LSRX
Multiply	MUL
Negate	NEGA, NEGX
No Operation	NOP
Rotate Left through Carry	ROLA, ROLX
Rotate Right through Carry	RORA, RORX
Reset Stack Pointer	RSP
Return from Interrupt	RTI
Return from Subroutine	RTS
Set Carry Bit	SEC
Set Interrupt Mask	SEI
Enable $\overline{\text{IRQ}}$ and Stop Oscillator	STOP
Software Interrupt	SWI
Transfer Accumulator to Index Register	TAX
Test for Negative or Zero	TSTA, TSTX
Transfer Index Register to Accumulator	TXA
Enable Interrupt and Halt Processor	WAIT

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3.3.2 Immediate

The immediate addressing mode is used for instructions that contain a value to be used in an operation with the value in the accumulator or index register. No memory address is required for immediate instructions. The operand is contained in the byte immediately following the opcode. These are two-byte instructions, one for the opcode and one for the immediate data byte. Table 3-2 lists the instructions to use in the immediate addressing mode.

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Table 3-2. Immediate Addressing Instructions

Instruction	Mnemonic
Add with Carry	ADC
Add	ADD
Logical AND	AND
Bit Test Memory with Accumulator	BIT
Compare Accumulator with Memory	CMP
Compare Index Register with Memory	CPX
Exclusive OR Memory with Accumulator	EOR
Load Accumulator from Memory	LDA
Load Index Register from Memory	LDX
Inclusive OR	ORA
Subtract with Carry	SBC
Subtract	SUB

3.3.3 Direct

The direct addressing mode allows the access data within the first 256 bytes of memory with a single two-byte instruction. In the direct addressing mode, the low byte of the operand's address is contained in the byte following the opcode. The high byte of the address is assumed to be $00. Most direct instructions take two bytes, one for the opcode and one for the operand's address. BRSET and BRCLR are three-byte instructions that use direct addressing to access the operand and relative addressing to specify a branch destination. Table 3-3 lists the instructions to use in the direct addressing mode.

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Table 3-3. Direct Addressing Instructions

Instruction	Mnemonic
Add with Carry	ADC
Add	ADD
Logical AND	AND
Arithmetic Shift Left	ASL
Arithmetic Shift Right	ASR
Clear Bit in Memory	BCLR
Bit Test Memory with Accumulator	BIT
Branch if Bit n Is Clear	BRCLR
Branch if Bit n Is Set	BRSET
Set Bit in Memory	BSET
Clear	CLR
Compare Accumulator with Memory	CMP
Complement	COM
Compare Index Register with Memory	CPX
Decrement	DEC
Exclusive OR Memory with Accumulator	EOR
Increment	INC
Jump	JMP
Jump to Subroutine	JSR
Load Accumulator from Memory	LDA
Load Index Register from Memory	LDX
Logical Shift Left	LSL
Logical Shift Right	LSR
Negate	NEG
Inclusive OR	ORA
Rotate Left through Carry	ROL
Rotate Right through Carry	ROR
Subtract with Carry	SBC
Store Accumulator in Memory	STA
Store Index Register in Memory	STX
Subtract	SUB
Test for Negative or Zero	TST

NOTE: ASL = LSL

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3.3.4 Extended

The extended addressing mode allows the access of data in any memory location with a single three-byte instruction. In the extended addressing mode, the high and low bytes of the operand's address are contained in the two bytes following the opcode. Extended instructions take three bytes, one for the opcode and two for the operand's address.

When using the Motorola assembler, the user does not need to specify whether an instruction uses direct or extended addressing. The assembler automatically selects the shortest form of the instruction. Table 3-4 lists the instructions that can be used in the extended addressing mode.

Table 3-4. Extended Addressing Instructions

Instruction	Mnemonic
Add with Carry	ADC
Add	ADD
Logical AND	AND
Bit Test Memory with Accumulator	BIT
Compare Accumulator with Memory	CMP
Compare Index Register with Memory	CPX
Exclusive OR Memory with Accumulator	EOR
Jump	JMP
Jump to Subroutine	JSR
Load Accumulator from Memory	LDA
Load Index Register from Memory	LDX
Inclusive OR	ORA
Subtract with Carry	SBC
Store Accumulator in Memory	STA
Store Index Register in Memory	STX
Subtract	SUB

3.3.5 Indexed, No Offset

The indexed, no offset addressing mode is used to access data with variable addresses within the first 256 memory locations. The CPU finds the low byte of the operand's conditional address by reading the contents of the index register. The high byte is assumed to be $00. These instructions are only one byte long. The indexed, no offset mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location. Table 3-5 lists the instructions that can be used in the indexed, no offset addressing mode.

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3.3.6 Indexed, 8-Bit Offset

The indexed, 8-bit offset addressing mode permits the access of data with variable addresses within the first 511 memory locations. The CPU finds the operand's conditional address by adding the unsigned contents of the index register to the unsigned byte following the opcode. This addressing mode is useful for selecting the kth element in an n-element table. The table can begin anywhere within the first 256 memory locations and could extend as far as location 510 ($01FE). With this two-byte instruction, k would typically be in the index register, and the address of the beginning of the table would be in the byte following the opcode. Table 3-5 lists the instructions to use in the indexed, 8-bit offset addressing mode.

3.3.7 Indexed, 16-Bit Offset

The indexed, 16-bit offset addressing mode is used to access data with variable addresses at any location in memory. The CPU finds the operand's conditional address by adding the unsigned contents of the 8-bit index register to the 16-bit unsigned word formed by the two bytes following the opcode. The first byte after the opcode is the high byte of the 16-bit offset; the second byte is the low byte. This addressing mode can be used in a manner similar to indexed, 8-bit offset, but this three-byte instruction allows tables to be anywhere in memory.

As with direct and extended addressing, the Motorola assembler determines the shortest form of indexed addressing. Table 3-5 lists the instructions that can be used in the indexed, 16-bit offset addressing mode.

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Table 3-5. Indexed Addressing Instructions

Instruction	Mnemonic	No Offset	8-Bit Offset	16-Bit Offset
Add with Carry	ADC	√	√	√
Add	ADD	√	√	√
Logical AND	AND	√	√	√
Arithmetic Shift Left	ASL	√	√	
Arithmetic Shift Right	ASR	√	√	
Bit Test Memory with Accumulator	BIT	√	√	√
Clear	CLR	√	√	
Compare Accumulator with Memory	CMP	√	√	√
Complement	COM	√	√	
Compare Index Register with Memory	CPX	√	√	√
Decrement	DEC	√	√	
Exclusive OR Memory with Accumulator	EOR	√	√	√
Increment	INC	√	√	
Jump	JMP	√	√	√
Jump to Subroutine	JSR	√	√	√
Load Accumulator from Memory	LDA	√	√	√
Load Index Register from Memory	LDX	√	√	√
Logical Shift Left	LSL	√	√	
Logical Shift Right	LSR	√	√	
Negate	NEG	√	√	
Inclusive OR	ORA	√	√	√
Rotate Left through Carry	ROL	√	√	
Rotate Right through Carry	ROR	√	√	
Subtract with Carry	SBC	√	√	√
Store Accumulator in Memory	STA	√	√	√
Store Index Register in Memory	STX	√	√	√
Subtract	SUB	√	√	√
Test for Negative or Zero	TST	√	√	

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3.3.8 Relative

The relative addressing mode is used only for branch instructions and bit test and branch instructions. The CPU finds the conditional branch destination by adding the signed byte following the opcode to the contents of the program counter if the branch condition is true. If the branch condition is not true, the program counter goes to the next instruction. To branch either forward or backward, the offset is a signed, twos complement byte that gives a branching range of –127 to +128 bytes from the address of the next location after the branch instruction.

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The programmer does not need not calculate the offset when using the Motorola assembler, as it calculates the proper offset and verifies that it is within the span of the branch. Table 3-6 lists the instructions that can be used in the relative addressing mode.

Table 3-6. Relative Addressing Instructions

Instruction	Mnemonic
Branch if Carry Clear	BCC
Branch if Carry Set	BCS
Branch if Equal	BEQ
Branch if Half-Carry Clear	BHCC
Branch if Half-Carry Set	BHCS
Branch if Higher	BHI
Branch if Higher or Same	BHS
Branch if Interrupt Line is High	BIH
Branch if Interrupt Line Is Low	BIL
Branch if Lower	BLO
Branch if Lower or Same	BLS
Branch if Interrupt Mask is Clear	BMC
Branch if Minus	BMI
Branch if Interrupt Mask Is Set	BMS
Branch if Not Equal	BNE
Branch if Plus	BPL
Branch Always	BRA
Branch if Bit n Is Clear	BRCLR
Branch if Bit n Is Set	BRSET
Branch Never	BRN
Branch to Subroutine	BSR

3.4 Instruction Set

This MCU uses all the instructions available in the M146805 CMOS Family plus the unsigned multiply (MUL) instruction. The MUL instruction allows unsigned multiplication of the contents of the accumulator and the index register. The high-order product is then stored in the index register, and the low-order product is stored in the accumulator.

The MCU instructions can be divided into five basic types:

- Register/memory
- Read-modify-write
- Jump/branch
- Bit manipulation
- Control

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3.4.1 Register/Memory Instructions

Most of these instructions use two operands. One operand is in either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. Use most register/memory instructions in the following addressing modes:

- Immediate
- Direct
- Extended
- Indexed, no offset
- Indexed, 8-bit offset
- Indexed, 16-bit offset

Table 3-7 lists the register/memory instructions.

Table 3-7. Register/Memory Instructions

Instruction	Mnemonic
Load Accumulator from Memory	LDA
Load Index Register from Memory	LDX
Store Accumulator in Memory	STA
Store Index Register in Memory	STX
Add Memory to Accumulator	ADD
Add Memory and Carry to Accumulator	ADC
Subtract Memory	SUB
Subtract Memory from Accumulator with Borrow	SBC
AND Memory with Accumulator	AND
OR Memory with Accumulator	ORA
Exclusive OR Memory with Accumulator	EOR
Arithmetic Compare Accumulator with Memory	CMP
Arithmetic Compare Index Register with Memory	CPX
Bit Test Memory with Accumulator (Logical Compare)	BIT
Multiply	MUL

3.4.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read-modify-write sequence because it does not write a replacement value. Use read-modify-write instructions in the following addressing modes:

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- Inherent
- Direct
- Indexed, no offset
- Indexed, 8-bit offset

Table 3-8 lists the read-modify-write instructions.

Table 3-8. Read-Modify-Write Instructions

Instruction	Mnemonic
Increment	INC
Decrement	DEC
Clear	CLR
Complement	COM
Negate (Twos Complement)	NEG
Rotate Left through Carry	ROL
Rotate Right through Carry	ROR
Logical Shift Left	LSL
Logical Shift Right	LSR
Arithmetic Shift Right	ASR
Test for Negative or Zero	TST

3.4.3 Jump/Branch Instructions

Jump instructions allow the CPU to interrupt the normal sequence of the program counter. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Jump instructions can be used in the following addressing modes:

- Direct
- Extended
- Indexed, no offset
- Indexed, 8-bit offset
- Indexed, 16-bit offset

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Branch instructions allow the CPU to interrupt the normal sequence of the program counter when a test condition is met. If the test condition is not met, the branch is not performed. All branch instructions are used in the relative addressing mode.

Bit test and branch instructions cause a branch based on the condition of any readable bit in the first 256 memory locations. These three-byte instructions use a combination of direct addressing and relative addressing. The direct address of the byte to be tested is in the byte following the opcode. The third byte is the signed offset byte. The CPU finds the conditional branch destination by adding the third byte to the program counter if the specified bit tests true. The bit to be tested and its condition (set or clear) is part of the opcode. The span of branching is from –128 to +127 from the address of the next location after the branch instruction. The CPU also transfers the tested bit to the carry/borrow bit (C bit) of the condition code register.

Table 3-9 lists the jump and branch instructions.

Table 3-9. Jump and Branch Instructions

Instruction	Mnemonic
Branch Always	BRA
Branch Never	BRN
Branch if Bit n of M = 0	BRCLR
Branch if Bit n of M = 1	BRSET
Branch if Higher	BHI
Branch if Lower or Same	BLS
Branch if Carry Clear	BCC
Branch if Higher or Same	BHS
Branch if Carry Set	BCS
Branch if Lower	BLO
Branch if Not Equal	BNE
Branch if Equal	BEQ
Branch if Half-Carry Clear	BHCC
Branch if Half-Carry Set	BHCS
Branch if Plus	BPL
Branch if Minus	BMI
Branch if Interrupt Mask Clear	BMC
Branch if Interrupt Mask Set	BMS
Branch if Interrupt Line Low	BIL
Branch if Interrupt Line High	BIH
Branch to Subroutine	BSR
Jump Unconditional	JMP
Jump to Subroutine	JSR

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3.4.4 Bit Manipulation Instructions

The CPU can set or clear any writable bit in the first 256 bytes of memory. Port registers, port data direction registers, timer registers, and on-chip RAM locations are in the first 256 bytes of memory. The CPU can also test and branch based on the state of any bit in any of the first 256 memory locations. Bit manipulation instructions are used in the direct addressing mode. Table 3-10 lists these instructions.

Table 3-10. Bit Manipulation Instructions

Instruction	Mnemonic
Set Bit n	BSET n (n = 0 . . . 7)
Clear Bit n	BCLR n (n = 0 . . . 7)
Branch if Bit n of M = 0	BRCLR
Branch if Bit n of M = 1	BRSET

3.4.5 Control Instructions

These register reference instructions control CPU operation during program execution. Control instructions, listed in Table 3-11, are used in the inherent addressing mode.

Table 3-11. Control Instructions

Instruction	Mnemonic
Transfer Accumulator to Index Register	TAX
Transfer Index Register to Accumulator	TXA
Set Carry Bit	SEC
Clear Carry Bit	CLC
Set Interrupt Mask	SEI
Clear Interrupt Mask	CLI
Software Interrupt	SWI
Return from Subroutine	RTS
Return from Interrupt	RTI
Reset Stack Pointer	RSP
No Operation	NOP
Stop	STOP
Wait	WAIT

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3.4.6 Instruction Set Summary

Table 3-12 shows all MC68HC05P9 instructions in all possible addressing modes. For each instruction, the operand construction and the execution time in internal clock cycles (t_{cyc}) are shown. One internal clock cycle equals two oscillator input cycles. The following legend summarizes the symbols and abbreviations used in Table 3-12.

Abbreviations and Symbols

A	–	Accumulator
C	–	Carry/borrow bit in condition code register
CCR	–	Condition code register
dd	–	Address of operand in direct addressing mode (1 byte)
dd rr	–	Address (dd) of operand and offset (rr) of branch instruction for bit test instructions
DIR	–	Direct addressing mode
ee ff	–	High (ee) and low (ff) bytes of offset in indexed, 16-bit offset addressing mode (2 bytes)
EXT	–	Extended addressing mode
ff	–	Offset byte in indexed, 8-bit offset addressing mode (1 byte)
H	–	Half-carry bit in condition code register
hh ll	–	High (hh) and low (ll) bytes of operand address in extended addressing mode (2 bytes)
I	–	Interrupt mask in condition code register
ii	–	Operand byte for immediate addressing mode
IMM	–	Immediate addressing mode
INH	–	Inherent addressing mode
IX	–	Indexed, no offset addressing mode
IX1	–	Indexed, 8-bit offset addressing mode
IX2	–	Indexed, 16-bit offset addressing mode
M	–	Any memory location (1 byte)
N	–	Negative bit in condition code register
n	–	Any bit (7,6,5 . . . 0)
opr	–	Operand byte
PC	–	Program counter
PCH	–	Program counter high byte
PCL	–	Program counter low byte
REL	–	Relative addressing mode
rel	–	Offset byte for relative addressing mode
rr	–	Offset byte of branch instruction
SP	–	Stack pointer
X	–	Index register
Z	–	Zero bit in condition code register

↕	–	Set if true; clear if not true	–( )	–	Negation (twos complement)
–	–	Not affected	+	–	Inclusive OR
?	–	If	⊕	–	Exclusive OR
0	–	Cleared (logical zero)	$\overline{\quad}$	–	NOT
1	–	Set (logical one)	×	–	Multiplication
( )	–	Contents of	+	–	Addition
←	–	Is loaded with	–	–	Subtraction
•	–	AND	:	–	Concatenated with

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Table 3-12. Instruction Set (Sheet 1 of 4)

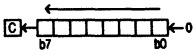
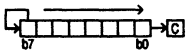
Source Form(s)	Operation	Description	Addressing Mode for Operand	Machine Coding (hexadecimal) Opcode	Machine Coding (hexadecimal) Operand	Cycles	Condition Code H	I	N	Z	C
ADC opr	Add with carry	A ← (A) + (M) + C	IMM	A9	ii	2	↕	–	↕	↕	↕
			DIR	B9	dd	3					
			EXT	C9	hh ll	4					
			IX2	D9	ee ff	5					
			IX1	E9	ff	4					
			IX	F9		3					
ADD opr	Add without carry	A ← (A) + (M)	IMM	AB	ii	2	↕	–	↕	↕	↕
			DIR	BB	dd	3					
			EXT	CB	hh ll	4					
			IX2	DB	ee ff	5					
			IX1	EB	ff	4					
			IX	FB		3					
AND opr	Logical AND	A ← (A) • (M)	IMM	A4	ii	2	–	–	↕	↕	–
			DIR	B4	dd	3					
			EXT	C4	hh ll	4					
			IX2	D4	ee ff	5					
			IX1	E4	ff	4					
			IX	F4		3					
ASL opr	Arithmetic shift left		DIR	38	dd	5	–	–	↕	↕	↕
ASLA			INH	48		3					
ASLX			INH	58		3					
ASL opr			IX1	68	ff	6					
ASL opr			IX	78		5					
ASR opr	Arithmetic shift right		DIR	37	dd	5	–	–	↕	↕	↕
ASRA			INH	47		3					
ASRX			INH	57		3					
ASR opr			IX1	67	ff	6					
ASR opr			IX	77		5					
BCC rel	Branch if carry bit clear	? C = 0	REL	24	rr	3	–	–	–	–	–
BCLR n opr	Clear bit n	Mn ← 0	DIR (b0)	11	dd	5	–	–	–	–	–
			DIR (b1)	13	dd	5					
			DIR (b2)	15	dd	5					
			DIR (b3)	17	dd	5					
			DIR (b4)	19	dd	5					
			DIR (b5)	1B	dd	5					
			DIR (b6)	1D	dd	5					
			DIR (b7)	1F	dd	5					
BCS rel	Branch if carry bit set	? C = 1	REL	25	rr	3	–	–	–	–	–
BEQ rel	Branch if equal	? Z = 1	REL	27	rr	3	–	–	–	–	–
BHCC rel	Branch if half carry bit clear	? H = 0	REL	28	rr	3	–	–	–	–	–
BHCS rel	Branch if half carry bit set	? H = 1	REL	29	rr	3	–	–	–	–	–
BHI rel	Branch if higher	? C + Z = 0	REL	22	rr	3	–	–	–	–	–
BHS rel	Branch if higher or same	? C = 0	REL	24	rr	3	–	–	–	–	–
BIH rel	Branch if $\overline{IRQ}$ pin high	? $\overline{IRQ}$ = 1	REL	2F	rr	3	–	–	–	–	–
BIL rel	Branch if $\overline{IRQ}$ pin low	? $\overline{IRQ}$ = 0	REL	2E	rr	3	–	–	–	–	–
BIT rel	Bit test accumulator contents with memory contents	(A) • (M)	IMM	A5	ii	2	–	–	↕	↕	–
			DIR	B5	dd	3					
			EXT	C5	hh ll	4					
			IX2	D5	ee ff	5					
			IX1	E5	ff	4					
			IX	F5		3					
BLO rel	Branch if lower	? C = 1	REL	25	rr	3	–	–	–	–	–
BLS rel	Branch if lower or same	? C + X = 1	REL	23	rr	3	–	–	–	–	–
BMC rel	Branch if interrupt mask clear	? I = 0	REL	2C	rr	3	–	–	–	–	–
BMI rel	Branch if minus	? N = 1	REL	2B	rr	3	–	–	–	–	–
BMS rel	Branch if interrupt mask set	? I = 0	REL	2D	rr	3	–	–	–	–	–
BNE rel	Branch if not equal	? Z = 0	REL	26	rr	3	–	–	–	–	–
BPL rel	Branch if plus	? N = 0	REL	2A	rr	3	–	–	–	–	–

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Table 3-12. Instruction Set (Sheet 2 of 4)

Source Form(s)	Operation	Description	Addressing Mode for Operand	Machine Coding (hexadecimal)		Cycles	Condition Code				
				Opcode	Operand		H	I	N	Z	C
BRA rel	Branch always	? 1 = 1	REL	20	rr	3	–	–	–	–	–
BRCLR n opr rel	Branch if bit n clear	? Mn = 0	DIR (b0)	01	dd rr	5	–	–	–	–	↕
			DIR (b1)	03	dd rr	5					
			DIR (b2)	05	dd rr	5					
			DIR (b3)	07	dd rr	5					
			DIR (b4)	09	dd rr	5					
			DIR (b5)	0B	dd rr	5					
			DIR (b6)	0D	dd rr	5					
			DIR (b7)	0F	dd rr	5					
BRN rel	Branch never	? 1 = 0	REL	21	rr	3	–	–	–	–	–
BRSET n opr rel	Branch if bit n set	? Mn = 1	DIR (b0)	00	dd rr	5	–	–	–	–	↕
			DIR (b1)	02	dd rr	5					
			DIR (b2)	04	dd rr	5					
			DIR (b3)	06	dd rr	5					
			DIR (b4)	08	dd rr	5					
			DIR (b5)	0A	dd rr	5					
			DIR(b6)	0C	dd rr	5					
			DIR (b7)	0E	dd rr	5					
BSET n opr	Set bit n	Mn ← 1	DIR (b0)	10	dd	5	–	–	–	–	–
			DIR (b1)	12	dd	5					
			DIR (b2)	14	dd	5					
			DIR (b3)	16	dd	5					
			DIR (b4)	18	dd	5					
			DIR (b5)	1A	dd	5					
			DIR (b6)	1C	dd	5					
			DIR (b7)	1E	dd	5					
BSR rel	Branch to subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1 PC ← (PC) + rel	REL	AD	rr	6	–	–	–	–	–
CLC	Clear carry bit	C ← 0	INH	98		2	–	–	–	–	0
CLI	Clear interrupt mask	I ← 0	INH	9A		2	–	0	–	–	–
CLR opr	Clear register	M ← $00	DIR	3F	dd	5	–	–	0	1	–
CLRA		A ← $00	INH	4F		3					
CLRX		X ← $00	INH	5F		3					
CLR opr		M ← $00	IX1	6F	ff	6					
CLR opr		M ← $00	IX	7F		5					
CMP opr	Compare accumulator contents with memory contents	(A) – (M)	IMM	A1	ii	2	–	–	↕	↕	↕
			DIR	B1	dd	3					
			EXT	C1	hh ll	4					
			IX2	D1	ee ff	5					
			IX1	E1	ff	4					
			IX	F1		3					
COM opr	Complement register contents (ones complement)	M ← $\overline{M}$ = $FF – (M)	DIR	33	dd	5	–	–	↕	↕	1
COMA		A ← $\overline{A}$ = $FF – (A)	INH	43		3					
COMX		X ← $\overline{X}$ = $FF – (X)	INH	53		3					
COM opr		M ← $\overline{M}$ = $FF – (M)	IX1	63	ff	6					
COM opr		M ← $\overline{M}$ = $FF – (M)	IX	73		5					
CPX opr	Compare index register contents with memory contents	(X) – (M)	IMM	A3	ii	2	–	–	↕	↕	↕
			DIR	B3	dd	3					
			EXT	C3	hh ll	4					
			IX2	D3	ee ff	5					
			IX1	E3	ff	4					
			IX	F3		3					
DEC opr	Decrement register contents	M ← (M) – 1	DIR	3A	dd	5	–	–	↕	↕	–
DECA		A ← (A) – 1	INH	4A		3					
DECX		X ← (X) – 1	INH	5A		3					
DEC opr		M ← (M) – 1	IX1	6A	ff	6					
DEC opr		M ← (M) – 1	IX	7A		5					

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Table 3-12. Instruction Set (Sheet 3 of 4)

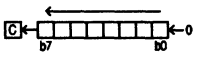
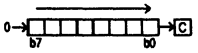
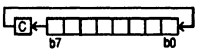
Source Form(s)	Operation	Description	Addressing Mode for Operand	Machine Coding (hexadecimal) Opcode	Machine Coding (hexadecimal) Operand	Cycles	Condition Code H	I	N	Z	C
EOR opr	Exclusive OR accumulator contents with memory contents	A ← (A) ⊕ (M)	IMM	A8	ii	2	–	–	↕	↕	–
			DIR	B8	dd	3					
			EXT	C8	hh ll	4					
			IX2	D8	ee ff	5					
			IX1	E8	ff	4					
			IX	F8		3					
INC opr	Increment memory or register contents	M ← (M) + 1	DIR	3C	dd	5	–	–	↕	↕	–
INCA		A ← (A) + 1	INH	4C		3					
INCX		X ← (X) + 1	INH	5C		3					
INC opr		M ← (M) + 1	IX1	6C	ff	6					
INC opr		M ← (M) + 1	IX	7C		5					
JMP opr	Unconditional jump	PC ← jump address	DIR	BC	dd	2	–	–	–	–	–
			EXT	CC	hh ll	3					
			IX2	DC	ee ff	4					
			IX1	EC	ff	3					
			IX	FC		2					
JSR opr	Jump to subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← conditional address	DIR	BD	dd	5	–	–	–	–	–
			EXT	CD	hh ll	6					
			IX2	DD	ee ff	7					
			IX1	ED	ff	6					
			IX	FD		5					
LDA opr	Load accumulator with memory contents	A ← (M)	IMM	A6	ii	2	–	–	↕	↕	–
			DIR	B6	dd	3					
			EXT	C6	hh ll	4					
			IX2	D6	ee ff	5					
			IX1	E6	ff	4					
			IX	F6		3					
LDX opr	Load index register with memory contents	X ← (M)	IMM	AE	ii	2	–	–	↕	↕	–
			DIR	BE	dd	3					
			EXT	CE	hh ll	4					
			IX2	DE	ee ff	5					
			IX1	EE	ff	4					
			IX	FE		3					
LSL opr	Logical shift left		DIR	38	dd	5	–	–	↕	↕	↕
LSLA			INH	48		3					
LSLX			INH	58		3					
LSL opr			IX1	68	ff	6					
LSL opr			IX	78		5					
LSR opr	Logical shift right		DIR	34	dd	5	–	–	0	↕	↕
LSRA			INH	44		3					
LSRX			INH	54		3					
LSR opr			IX1	64	ff	6					
LSR opr			IX	74		5					
MUL	Unsigned multiply	X : A ← (X) × (A)	INH	42		11	0	–	–	–	0
NEG opr	Negate memory or register contents (twos complement)	M ← –(M) = $00 – (M)	DIR	30	dd	5	–	–	↕	↕	↕
NEGA		A ← –(A) = $00 – (A)	INH	40		3					
NEGX		X ← –(X) = $00 – (X)	INH	50		3					
NEG opr		M ← –(M) = $00 – (M)	IX1	60	ff	6					
NEG opr		M ← –(M) = $00 – (M)	IX	70		5					
NOP	No operation		INH	9D		2	–	–	–	–	–
ORA opr	Inclusive OR accumulator contents with memory contents	A ← (A) + (M)	IMM	AA	ii	2	–	–	↕	↕	–
			DIR	BA	dd	3					
			EXT	CA	hh ll	4					
			IX2	DA	ee ff	5					
			IX1	EA	ff	4					
			IX	FA		3					
ROL opr	Rotate left through carry		DIR	39	dd	5	–	–	↕	↕	↕
ROLA			INH	49		3					
ROLX			INH	59		3					
ROL opr			IX1	69	ff	6					
ROL opr			IX	79		5					

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Table 3-12. Instruction Set (Sheet 4 of 4)

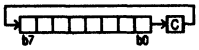
Source Form(s)	Operation	Description	Addressing Mode for Operand	Machine Coding (hexadecimal) Opcode	Machine Coding (hexadecimal) Operand	Cycles	Condition Code H	I	N	Z	C
ROR opr	Rotate right through carry		DIR	36	dd	5	–	–	↕	↕	↕
RORA			INH	46		3					
RORX			INH	56		3					
ROR opr			IX1	66	ff	6					
ROR opr			IX	76		5					
RSP	Reset stack pointer	SP ← $00FF	INH	9C		2	From Stack				
RTI	Return from interrupt	SP ← (SP) + 1; pull (CCR) SP ← (SP) + 1; pull (A) SP ← (SP) + 1; pull (X) SP ← (SP) + 1; pull (PCH) SP ← (SP) + 1; pull (PCL)	INH	80		9	↕	↕	↕	↕	↕
RTS	Return from subroutine	SP ← (SP) + 1; pull (PCH) SP ← (SP) + 1; pull (PCL)	INH	81		6	–	–	–	–	–
SBC opr	Subtract memory contents and carry bit from accumulator contents	A ← (A) – (M) – C	IMM	A2	ii	2	–	–	↕	↕	↕
			DIR	B2	dd	3					
			EXT	C2	hh ll	4					
			IX2	D2	ee ff	5					
			IX1	E2	ff	4					
			IX	F2		3					
SEC	Set carry bit	C ← 1	INH	99		2	–	–	–	–	1
SEI	Set interrupt mask	I ← 1	INH	9B		2	–	1	–	–	–
STA opr	Store accumulator contents in memory	M ← (A)	DIR	B7	dd	4	–	–	↕	↕	–
			EXT	C7	hh ll	5					
			IX2	D7	ee ff	6					
			IX1	E7	ff	5					
			IX	F7		4					
STOP	Enable $\overline{IRQ}$; stop oscillator		INH	8E		2	–	0	–	–	–
STX opr	Store index register contents in memory	M ← (X)	DIR	BF	dd	4	–	–	↕	↕	–
			EXT	CF	hh ll	5					
			IX2	DF	ee ff	6					
			IX1	EF	ff	5					
			IX	FF		4					
SUB opr	Subtract memory contents from accumulator contents	A ← (A) – (M)	IMM	A0	ii	2	–	–	↕	↕	↕
			DIR	B0	dd	3					
			EXT	C0	hh ll	4					
			IX2	D0	ee ff	5					
			IX1	E0	ff	4					
			IX	F0		3					
SWI	Software interrupt	PC ← (PC) + 1; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1; push (X) SP ← (SP) – 1; push (A) SP ← (SP) – 1; push (CCR) SP ← (SP) – 1; I ← 1 PCH ← ($xFFC) PCL ← ($xFFD) (Vector fetch)	INH	83		10	–	1	–	–	–
TAX	Transfer accumulator contents to index register	X ← (A)	INH	97		2	–	–	–	–	–
TST opr	Test memory, accumulator, or index register contents for negative or zero	(M) – $00	DIR	3D	dd	4	–	–	↕	↕	0
TSTA			INH	4D		3					
TSTX			INH	5D		3					
TST opr			IX1	6D	ff	5					
TST opr			IX	7D		4					
TXA	Transfer index register contents to accumulator	A ← (X)	INH	9F		2	–	–	–	–	–
WAIT	Enable interrupts; halt CPU		INH	8F		2	–	0	–	–	–

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Table 3-13 is an opcode map for the MC68HC05P9 instructions.

Table 3-13. Opcode Map

	Bit Manipulation		Branch	Read-Modify-Write					Control		Register/Memory						
	DIR	DIR	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
HI / LO	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	HI / LO
0 0000	5 BRSET0 3 DIR	5 BSET0 2 DIR	3 BRA 2 REL	5 NEG 2 DIR	3 NEGA 1 INH		6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0 0000
1 0001	5 BRCLR0 3 DIR	5 BCLR0 2 DIR	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1 0001
2 0010	5 BRSET1 3 DIR	5 BSET1 2 DIR	3 BHI 2 REL		11 MUL 1 INH						2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2 0010
3 0011	5 BRCLR1 3 DIR	5 BSCLR1 2 DIR	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3 0011
4 0100	5 BRSET2 3 DIR	5 BSET2 2 DIR	3 BCC 2 REL	5 LSR 2 DIR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4 0100
5 0101	5 BRCLR2 3 DIR	5 BCLR2 2 DIR	3 BCS 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5 0101
6 0110	5 BRSET3 3 DIR	5 BSET3 2 DIR	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6 0110
7 0111	5 BRCLR3 3 DIR	5 BCLR3 2 DIR	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7 0111
8 1000	5 BRSET4 3 DIR	5 BSET4 2 DIR	3 BHCC 2 REL	5 LSL 2 DIR	3 LSLA 1 INH	3 LSLX 1 INH	6 LSL 2 IX1	5 LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8 1000
9 1001	5 BRCLR4 3 DIR	5 BCLR4 2 DIR	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9 1001
A 1010	5 BRSET5 3 DIR	5 BSET5 2 DIR	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 INH	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A 1010
B 1011	5 BRCLR5 3 DIR	5 BCLR5 2 DIR	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B 1011
C 1100	5 BRSET6 3 DIR	5 BSET6 2 DIR	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 INH	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C 1100
D 1101	5 BRCLR6 3 DIR	5 BCLR6 2 DIR	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	6 TST 2 INH	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D 1101
E 1110	5 BRSET7 3 DIR	5 BSET7 2 DIR	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E 1110
F 1111	5 BRCLR7 3 DIR	5 BCLR7 2 DIR	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 INH	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F 1111

ABBREVIATIONS FOR ADDRESSING MODES

INH	Inherent	REL	Relative
IMM	Immediate	IX	Indexed, No Offset
DIR	Direct	IX1	Indexed, 8-Bit Offset
EXT	Extended	IX2	Indexed, 16-Bit Offset

LEGEND

	F 1111	High Byte of Opcode in Hexadecimal High Byte of Opcode in Binary
Number of Cycles Opcode Mnemonic Number of Bytes/Addressing Mode	3 SUB 1 IX	0 Low Byte of Opcode in Hexadecimal 0000 Low Byte of Opcode in Binary

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3.5 Low-Power Modes

The following paragraphs describe the STOP and WAIT modes. (Refer also to **5.2 Data-Retention Mode**.)

3.5.1 STOP Mode

The STOP instruction places the MCU in its lowest power-consumption mode. In STOP mode, the internal oscillator turns off, halting all internal processing, including capture/compare timer operation and computer operating properly (COP) timer operation. (Refer to Figure 3-8.)

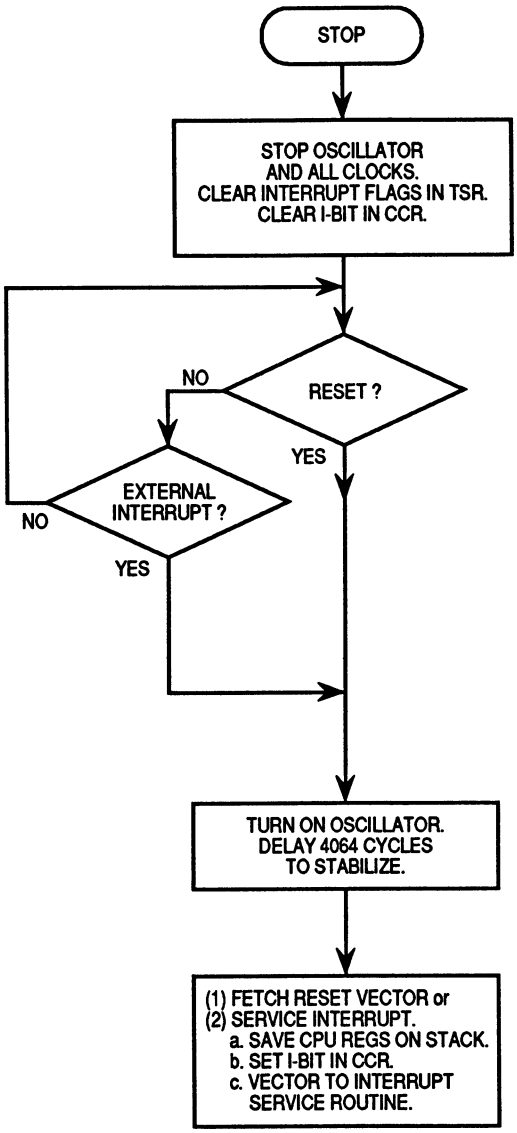

Figure 3-8. STOP Function Flowchart

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During STOP mode, the input capture interrupt enable bit (ICIE), the output compare interrupt enable bit (OCIE), and the timer overflow interrupt enable bit (TOIE) in the timer control register (TCR) are cleared to remove any pending timer interrupt requests and to disable any further timer interrupts. The interrupt mask (I-bit) in the condition code register is cleared to enable external interrupts. All other registers and memory locations remain unchanged. All I/O lines remain unchanged. The MCU can be brought out of STOP mode only by an external interrupt or a reset. An external interrupt automatically loads the program counter with the contents of $1FFA and $1FFB, the locations of the vector address of the interrupt service routine. A reset automatically loads the program counter with the contents of $1FFE and $1FFF, the locations of the vector address of the reset service routine.

3.5.2 WAIT Mode

The WAIT instruction places the MCU in an intermediate power-consumption mode. All CPU action stops, but the capture/compare timer remains active. If the A/D converter is enabled, it is also active in WAIT mode. An interrupt from the capture/compare timer can cause the MCU to exit WAIT mode. (Refer to Figure 3-9.)

The COP timer is not disabled in WAIT mode. To prevent a COP timer reset, exit from WAIT and reset the COP timer before timeout.

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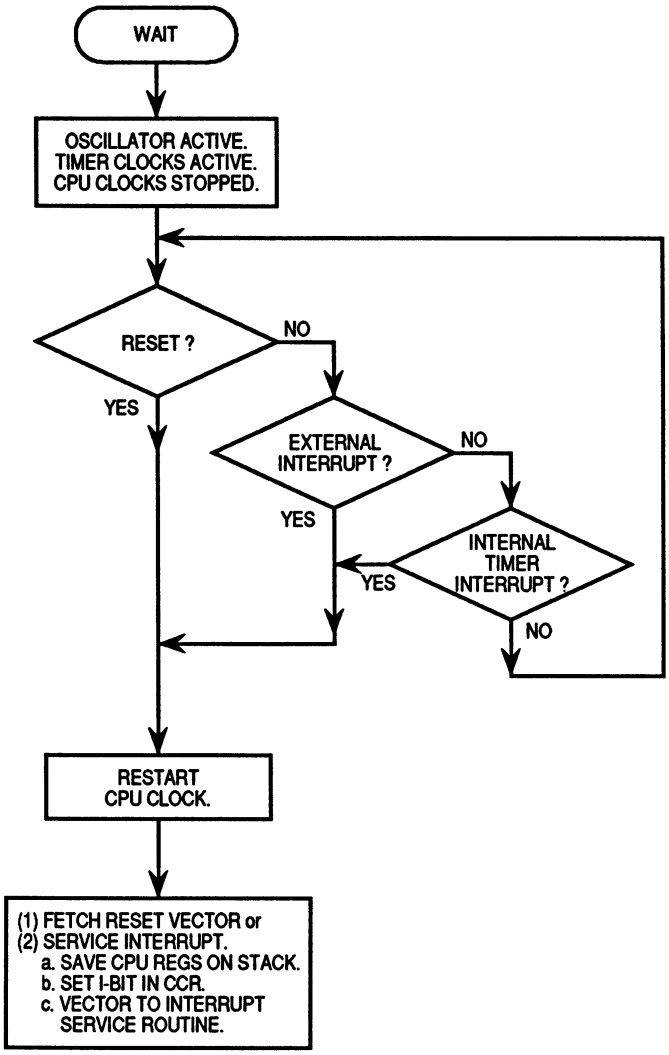

Figure 3-9. WAIT Function Flowchart

During WAIT mode, the interrupt mask (I bit) in the condition code register is cleared to enable interrupts. All other registers, memory locations, and I/O lines remain in their previous states.

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SECTION 4
RESETS AND INTERRUPTS

This section describes CPU resets and interrupts.

4.1 Resets

A reset immediately stops execution of the current instruction. A reset forces the program counter to a known starting address and forces certain control and status bits to known conditions. The CPU can be reset in the following ways:

- Initial power-up (power-on reset)
- An external, logical zero signal on the reset pin ($\overline{\text{RESET}}$)
- Timeout of the computer operating properly (COP) timer

NOTE

The current instruction is the one already fetched and under operation.

The following internal actions occur as a result of a reset:

- All implemented data direction register bits are cleared to logical zero, so the corresponding I/O pins become high-impedance inputs.
- The stack pointer is loaded with $FF.
- The interrupt mask (I-bit) is set, inhibiting interrupts.
- The capture/compare timer clock divider stages are reset. The capture/compare timer is loaded with $FFFC. The output compare bit (TCMP) and the output level bit (OLVL) are cleared. All capture/compare timer interrupt enable bits (ICIE, OCIE, and TOIE) are cleared to disable timer interrupts.
- The STOP latch is cleared to enable MCU clocks.
- The WAIT latch is cleared to wake the CPU from the WAIT mode.
- On exit from reset, the program counter is loaded with the user-defined reset vector address; the high byte of the program counter is loaded with the contents of location $1FFE, and the low byte of the program counter is loaded from location $1FFF.

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4.1.1 Power-On Reset (POR)

A positive transition on V_{DD} generates a power-on reset, which is strictly for power-up conditions. It cannot be used to detect drops in power supply voltage.

A 4064 t_{cyc} (internal clock cycle) delay after the oscillator becomes active allows the clock generator to stabilize. If the $\overline{\text{RESET}}$ pin is at logical zero at the end of 4064 t_{cyc}, the CPU remains in the reset condition until $\overline{\text{RESET}}$ goes to logical one.

4.1.2 External Reset ($\overline{\text{RESET}}$)

The CPU is reset when a logical zero is applied to the $\overline{\text{RESET}}$ pin for a period of one and one-half internal clock cycles (t_{cyc}). The $\overline{\text{RESET}}$ input consists of a Schmitt trigger that senses the logic level at the $\overline{\text{RESET}}$ pin.

$\overline{\text{RESET}}$ is an input-only pin and does not become active (go to logical zero) when a power-on reset or COP timer reset is generated.

4.1.3 Computer Operating Properly (COP) Reset

As a factory-set mask option, the MCU contains a COP timer that automatically times out if not cleared within a specific time by a program sequence. The COP timer system is used to detect software errors. When the COP timer times out, a reset is generated. The COP system is implemented with an 18-stage ripple counter that provides a timeout period of 64 ms at an internal clock rate of 2 MHz. A COP timeout resets and reinitializes the CPU in the same fashion as a power-on reset or external reset. A COP timer reset is prevented by writing a logical zero to bit 0 (COPR) of the COP register at location $1FF0. Writing a logical zero to COPR resets the COP timer and begins the timeout period again.

The write-only COP register is used to prevent a COP timer reset. This location contains user-defined ROM data. Figure 4-1 shows the COP register.

COP — Computer Operating Properly Register **$1FF0**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	—	—	—	—	—	COPR
RESET:	—	—	—	—	—	—	—	0

Figure 4-1. COP Register

COPR — COP Reset

Periodically writing a logical zero to COPR prevents the COP timer from resetting the CPU.

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4.2 Interrupts

An interrupt temporarily stops normal processing so that some unusual event can be processed. Unlike a reset, an interrupt does not stop the current instruction. An interrupt is considered pending until the current instruction is complete. There are three types of CPU interrupts:

- External interrupt — If the interrupt mask (I bit) is a logical zero, and the external interrupt pin ($\overline{\text{IRQ}}$) goes to logical zero, then the CPU recognizes an external interrupt.
- Capture/compare timer interrupt — When the interrupt mask is a logical zero, the CPU can recognize interrupts from the capture/compare timer. A timer interrupt is serviced if one of the three timer interrupt flags (ICF, OCF, or TOF) is set to logical one while its corresponding timer interrupt enable bit (ICIE, OCIE, or TOIE) is a logical one. The timer interrupt flags are in the timer status register (TSR); the timer interrupt enable bits are in the timer control register (TCR). (Refer to **SECTION 6 CAPTURE/COMPARE TIMER**.)
- Software interrupt — The software interrupt is an instruction that is executed regardless of the state of the interrupt mask.

The following internal actions occur as a result of an interrupt:

- CPU register contents are stored on the stack in the order PCL, PCH, X, A, CCR.
- The interrupt mask (I-bit) is automatically set to prevent additional interrupts.
- An interrupt vector that causes processing to continue at the starting address of the interrupt routine is fetched.
- The RTI (return from interrupt) instruction causes the register contents to be recovered from the stack in the order CCR, A, X, PCH, PCL. Normal processing resumes.

Figure 4-2 shows the stacking and recovery sequence.

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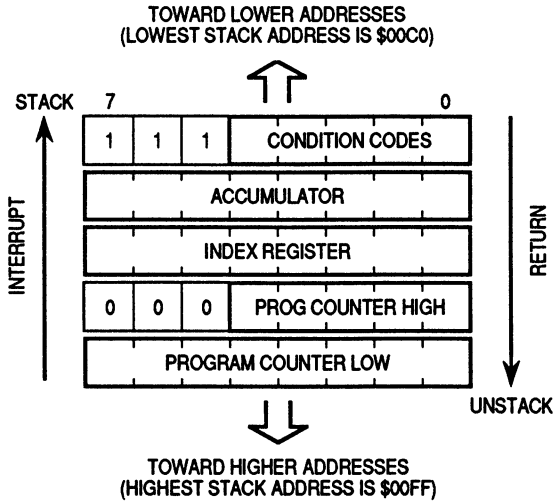

Figure 4-2. Interrupt Stacking Order

As each instruction is completed, the CPU checks for the presence of enabled external interrupt requests and enabled timer interrupt requests. For an external interrupt request to be recognized, the interrupt mask (I-bit) in the CCR must be a logical zero. If the interrupt mask is set or if no qualified interrupt request is pending, the CPU fetches and executes the next program instruction.

For a capture/compare timer interrupt request to be recognized, the interrupt mask must be a logical zero, and one of the timer interrupt enable bits (ICIE, OCIE, or TOIE) in the timer control register must be a logical one. If the interrupt mask is set or if no qualified interrupt request is pending, the CPU fetches and executes the next program instruction.

If both an external interrupt and a capture/compare timer interrupt are pending at the end of an instruction execution, the external interrupt is serviced first.

A software interrupt (SWI) is executed as an instruction, regardless of the state of the interrupt mask. Figure 4-3 shows how interrupts relate to normal instruction execution. CPU control logic determines the sequence of operations.

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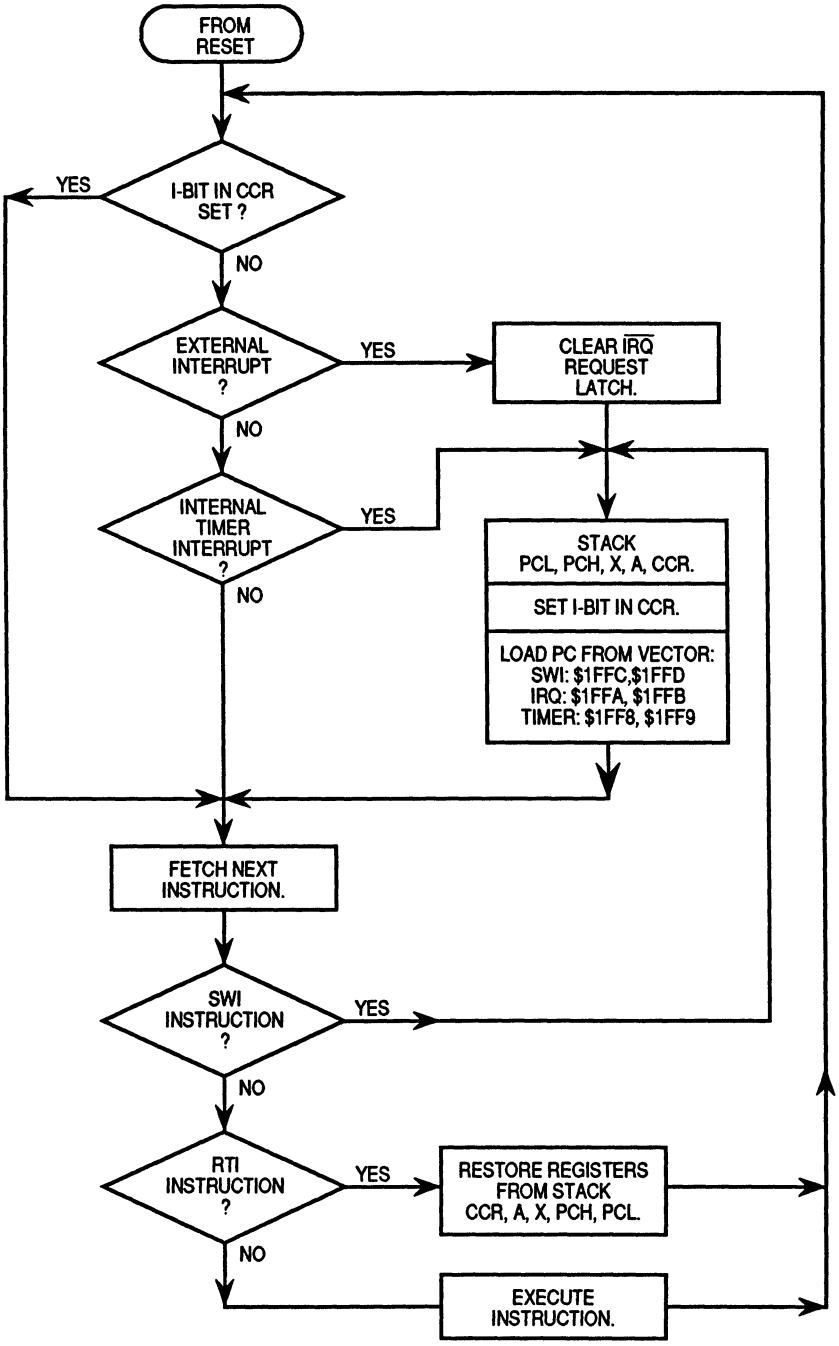

Figure 4-3. Reset and Interrupt Flowchart

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4.2.1 External Interrupt ($\overline{IRQ}$)

The CPU recognizes an external interrupt when the external interrupt pin ($\overline{IRQ}$) goes to a logical zero while the interrupt mask (I-bit) is a logical zero. A small synchronization delay occurs, and a logical one is latched internally to signify that an external interrupt is requested. When the CPU completes its current instruction, the interrupt latch is tested. If the interrupt latch contains a logical one, and if the interrupt mask in the condition code register is a logical zero, the CPU then begins the interrupt sequence. The current state of the CPU is pushed onto the stack, and the interrupt mask is set to inhibit further interrupts until the present one is serviced. The address of the external interrupt service routine is contained in memory locations $1FFA and $1FFB.

Either an edge and level sensitive external interrupt trigger or an edge sensitive only external interrupt trigger is available as a factory-set mask option. Figure 4-4 shows the internal logic of the interrupt trigger sensitivity option. The interrupt latch is cleared while the interrupt vector is being fetched. During the interrupt service routine, a new external interrupt request can be initiated and latched. As soon as the interrupt mask is cleared (usually during the return from interrupt), the latched request is recognized and serviced.

The level sensitive trigger option allows multiple external interrupt sources to be wire-ORed to the $\overline{IRQ}$ pin. As long as any source is holding the $\overline{IRQ}$ pin at logical zero, an external interrupt request is considered to be pending.

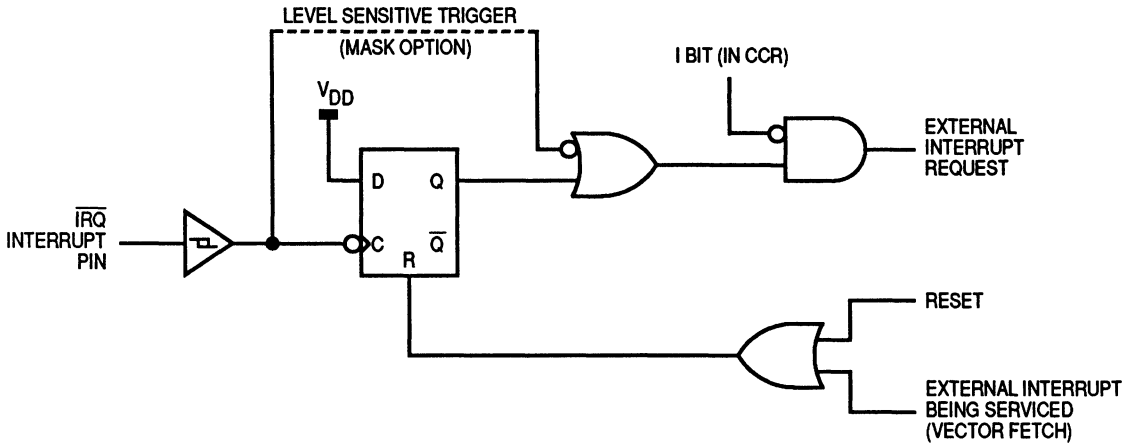

Figure 4-4. External Interrupt Logic

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4.2.2 Software Interrupt (SWI)

The SWI instruction is executed regardless of the state of the interrupt mask (I-bit) in the condition code register. The address of the SWI interrupt service routine is in memory locations $1FFC and $1FFD.

4.2.3 Capture/Compare Timer Interrupt

Three interrupts can be generated by the timer when the interrupt mask is a logical zero. When one of the three timer interrupt flags in the timer control and status register is at logical one, and the corresponding timer interrupt enable flag in the timer control register is at logical one, the CPU recognizes a timer interrupt. (Refer to **SECTION 6 CAPTURE/COMPARE TIMER** for more information.) All three of the timer interrupts use the same interrupt vector at $1FF8 and $1FF9.

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SECTION 5
MEMORY

Section 5 describes the organization of the on-chip memory. The MC68HC05P9 MCU can address 8K bytes of memory space.

5.1 Memory Map

The program counter normally advances one address at a time through the on-chip memory, reading the instructions and data necessary to execute the program. The ROM portion of memory holds program instructions, user-defined vectors, and service routines. The RAM portion of memory holds variable data. Input/output (I/O) registers are memory-mapped so that the CPU can access their locations in the same way it accesses any other memory location.

Figure 5-1 is a memory map of the MCU. Refer to Figure 5-2 for a more detailed memory map of the 32-byte I/O register and status and control register area.

5.1.1 Input/Output (I/O) Section

The first 32 addresses of the memory space, $0000–$001F, are defined as the I/O section. These are the addresses of the I/O data, status, and control registers.

5.1.2 RAM

The MCU has 128 bytes of fully static read-write memory for storage of variable and temporary data during program execution. The top 64 RAM addresses ($00C0–$00FF) serve as the stack. The CPU uses the stack to save CPU register contents before processing an interrupt or subroutine call. The stack pointer decrements during pushes and increments during pulls.

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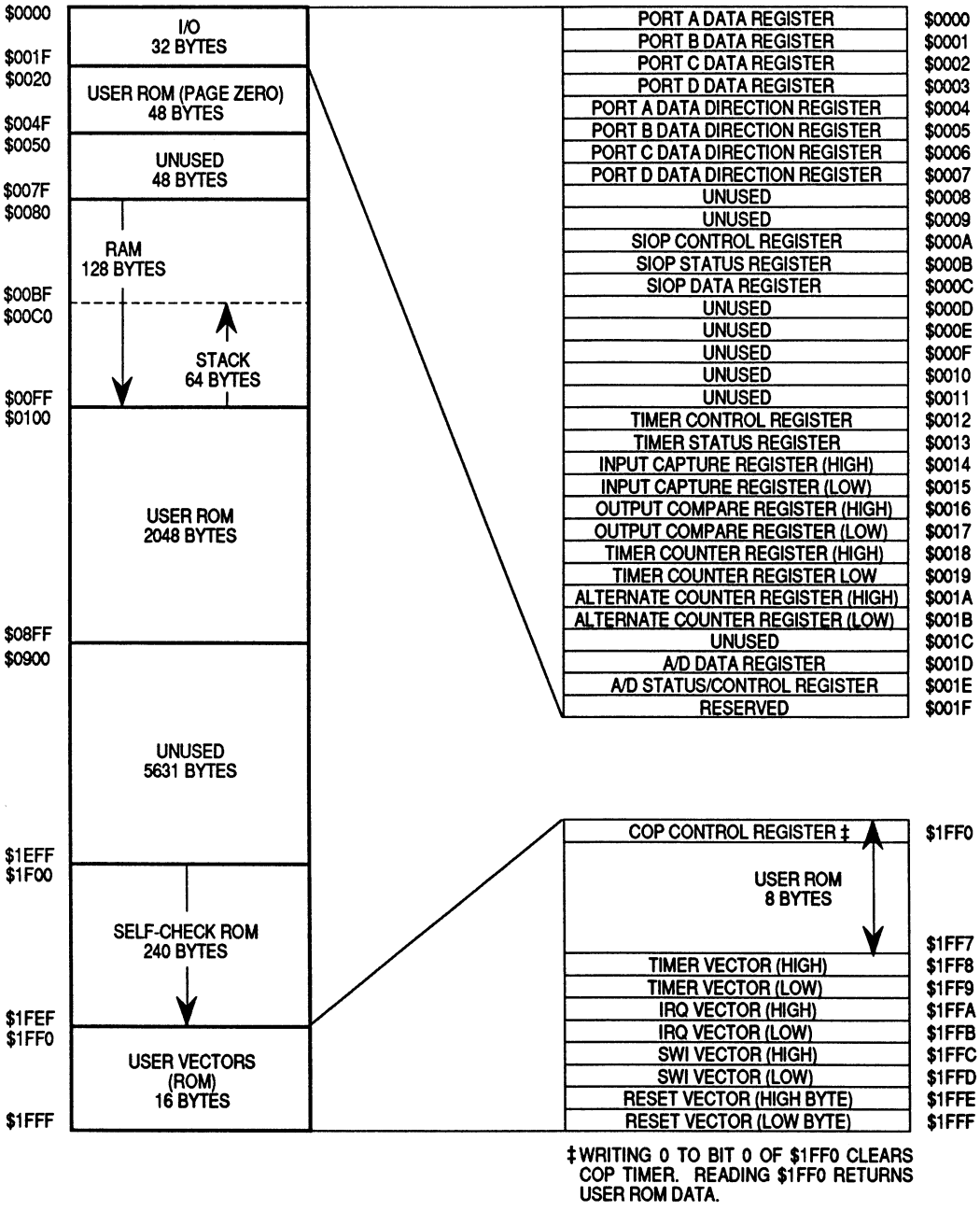

Figure 5-1. Memory Map

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	Bit 7	6	5	4	3	2	1	Bit 0	
$0000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$0001	PB7/SCK	PB6/SDI	PB5/SDO	0	0	0	0	0	PORTB
$0002	PC7/V_{RH}	PC6/AN0	PC5/AN1	PC4/AN2	PC3/AN3	PC2	PC1	PC0	PORTC
$0003	PD7/TCAP	0	PD5	1	0	0	0	0	PORTD
$0004	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0	DDRA
$0005	DDRB7	DDRB6	DDRB5	1	1	1	1	1	DDRB
$0006	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0	DDRC
$0007	0	0	DDRD5	0	0	0	0	0	DDRD
$0008	—	—	—	—	—	—	—	—	UNUSED
$0009	—	—	—	—	—	—	—	—	UNUSED
$000A	0	SPE	0	MSTR	0	0	0	0	SCR
$000B	SPIF	DCOL	0	0	0	0	0	0	SSR
$000C	Bit 7	6	5	4	3	2	1	Bit 0	SDR
$000D	—	—	—	—	—	—	—	—	UNUSED
$000E	—	—	—	—	—	—	—	—	UNUSED
$000F	—	—	—	—	—	—	—	—	UNUSED
$0010	—	—	—	—	—	—	—	—	UNUSED
$0011	—	—	—	—	—	—	—	—	UNUSED
$0012	ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL	TCR
$0013	ICF	OCF	TOF	0	0	0	0	0	TSR
$0014	Bit 15	14	13	12	11	10	9	Bit 8	ICR (HIGH)
$0015	Bit 7	6	5	4	3	2	1	Bit 0	ICR (LOW)
$0016	Bit 15	14	13	12	11	10	9	Bit 8	OCR (HIGH)
$0017	Bit 7	6	5	4	3	2	1	Bit 0	OCR (LOW)
$0018	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (HIGH)
$0019	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (LOW)
$001A	Bit 15	14	13	12	11	10	9	Bit 8	ALTCNT (HIGH)
$001B	Bit 7	6	5	4	3	2	1	Bit 0	ALTCNT (LOW)
$001C	—	—	—	—	—	—	—	—	UNUSED
$001D	Bit 7	6	5	4	3	2	1	Bit 0	ADDR
$001E	CCF	ADRC	ADON	0	0	0	CH1	CH0	ADSCR
$001F	—	—	—	—	—	—	—	—	RESERVED
$1FF0	—	—	—	—	—	—	—	COPR	COP

Figure 5-2. I/O Registers

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NOTE

Using the stack area for data storage or as a temporary work area requires care to prevent data from being overwritten during stacking from an interrupt or subroutine call.

5.1.3 ROM

On-chip user ROM includes 48 bytes at addresses $0020–$004F, 2048 bytes at $0100–$08FF, and 16 bytes at $1FF0–$1FFF that contain user-defined vectors for servicing interrupts and resets.

The 240 bytes at $1F00–$1FEF are reserved ROM addresses that contain the instructions for a series of self-check tests. (Refer to **SECTION 9 SELF-CHECK MODE**.)

5.2 Data-Retention Mode

In data-retention mode, the MCU retains RAM contents and CPU register contents at V_{DD} voltages as low as 2.0 Vdc. Before the V_{DD} voltage is lowered, drive the $\overline{\text{RESET}}$ line to logical zero. During data-retention mode, $\overline{\text{RESET}}$ must remain low continuously . The data-retention mode allows the MCU to be left in a low power consumption mode during which data is held, but the CPU cannot execute instructions. To exit the data-retention mode, V_{DD} must be returned to its normal operating voltage before $\overline{\text{RESET}}$ is returned to logical one.

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SECTION 6
CAPTURE/COMPARE TIMER

This section describes the operation of the capture/compare timer. Figure 6-1 shows the structure of the capture/compare timer system.

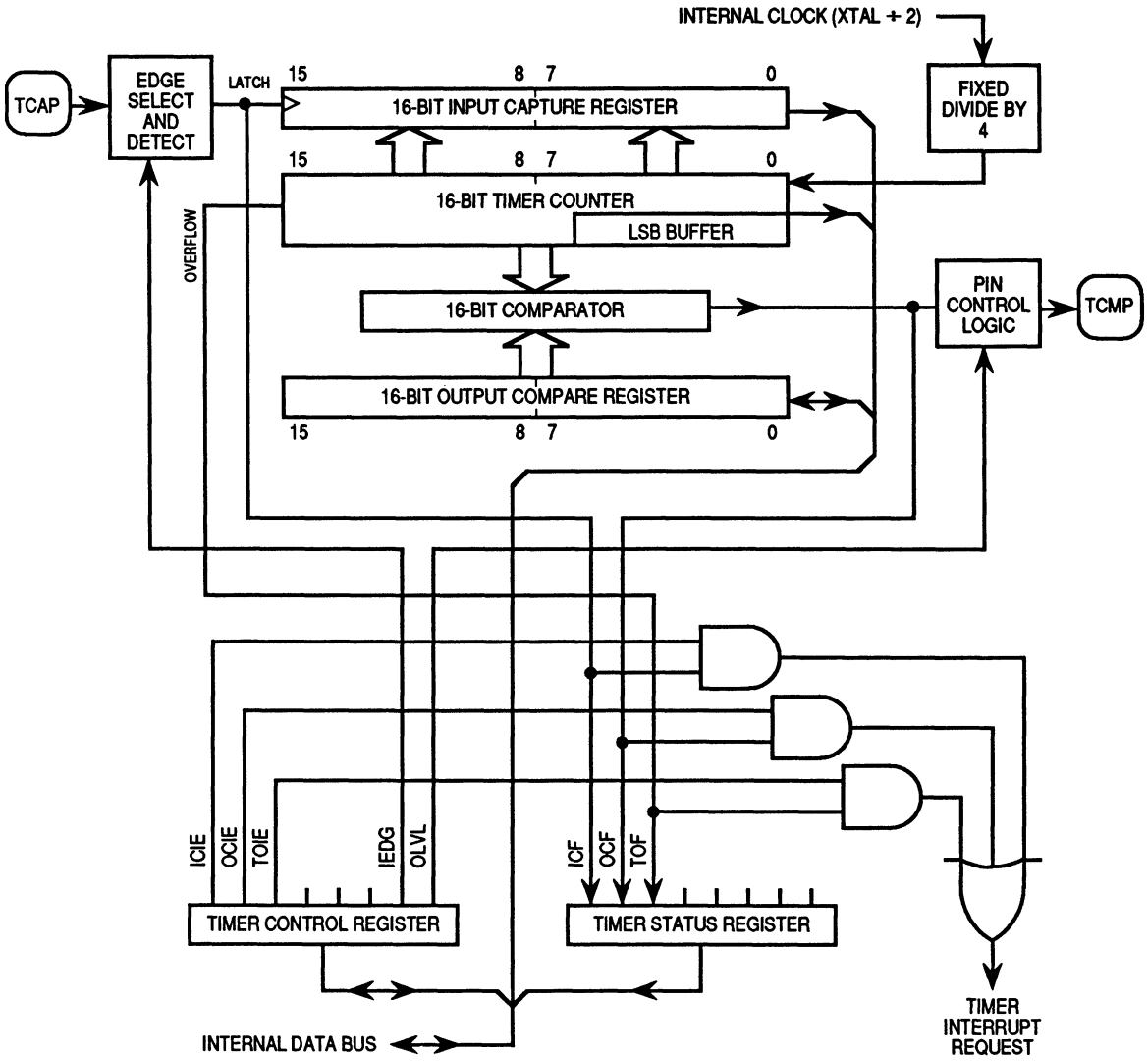

Figure 6-1. Capture/Compare Timer Block Diagram

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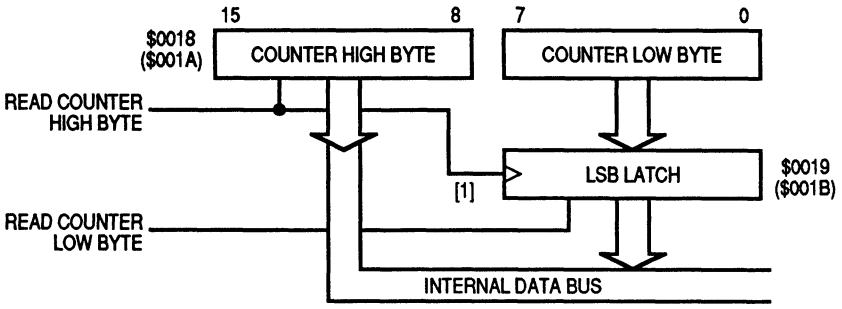
6.1 Timer Counter

The key element in the programmable capture/compare timer is a 16-bit, free-running counter, preceded by a prescaler that divides the internal clock by four. The counter provides the timing reference for the input capture and output compare functions. Software can read the counter value at any time from either of the following two registers with no affect on the counter sequence:

- Timer Counter Register (TCNT)
- Alternate Counter Register (ALTCNT)

Reading the high byte of the timer counter register or alternate counter register accesses the high byte value at the time of the read and causes the low byte to be latched into a buffer. (Refer to Figure 6-2.) This buffer value remains fixed after the first high byte read, even if the high byte is read more than once. The buffer is accessed when the read sequence is completed by reading the low byte of the timer counter register or the alternate counter register. If the high byte is read, the low byte must also be read to complete the read sequence.



[1] The LSB latch is normally transparent. It latches when the high byte of the counter is read and becomes transparent again when the low byte of the counter is read.

Figure 6-2. 16-Bit Counter Reads

The free-running counter is preset to $FFFC during reset. During a power-on reset, the counter is preset to $FFFC and begins running after the oscillator startup delay. Because the free-running counter is 16 bits long and preceded by a fixed divide-by-four prescaler, the value in the counter repeats every 262,144 internal clock cycles.

6.1.1 Timer Counter Register (TCNT)

The high and low bytes of the free-running counter can be read from the timer counter register at locations $0018 and $0019. (Refer to Figure 6-3.) Reading

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the low byte ($0018) of the timer counter register after reading the timer status register clears the timer overflow flag (TOF). On reset, the timer counter register resets to $FFFC.

TCNT — Timer Counter Register **$0018–$0019**

$0018	Bit 15	14	13	12	11	10	9	Bit 8	HIGH
$0019	Bit 7	6	5	4	3	2	1	Bit 0	LOW

Figure 6-3. Timer Counter Register (TCNT)

6.1.2 Alternate Counter Register (ALTCNT)

The high and low bytes of the free-running counter can be read from the alternate counter register at locations $001A and $001B. (Refer to Figure 6-4.) Reading the alternate counter register does not affect the timer overflow flag (TOF). The alternate counter register can be read at any time without risk of clearing TOF inadvertently. Normally, the timer value is read from the alternate counter register unless the read sequence is intended to clear TOF. On reset, the alternate counter register resets to $FFFC.

ALTCNT — Alternate Counter Register **$001A–$001B**

$001A	Bit 15	14	13	12	11	10	9	Bit 8	HIGH
$001B	Bit 7	6	5	4	3	2	1	Bit 0	LOW

Figure 6-4. Alternate Counter Register (ALTCNT)

NOTE

To prevent interrupts from occurring between readings of the high and low bytes of the timer counter register or the alternate counter register, the interrupt mask (I bit) in the condition code register can be set before reading the high byte and cleared after reading the low byte.

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6.2 Timer Functions

The input capture and output compare functions provide a means to latch the times at which external events occur, to measure input waveforms, and to generate output waveforms and timing delays.

6.2.1 Input Capture

The input capture feature provides a means to record the time at which an external event occurs. When the timer detects a selected (negative-going or positive-going) edge on the TCAP pin, it latches the contents of the timer counter register into the input capture register. The IEDG bit in the timer control register allows software to select the edge polarity that triggers the input capture function. The ICIE bit in the timer control register allows software to determine whether or not the input capture function generates a hardware interrupt request. (Refer to Figure 6-5.)

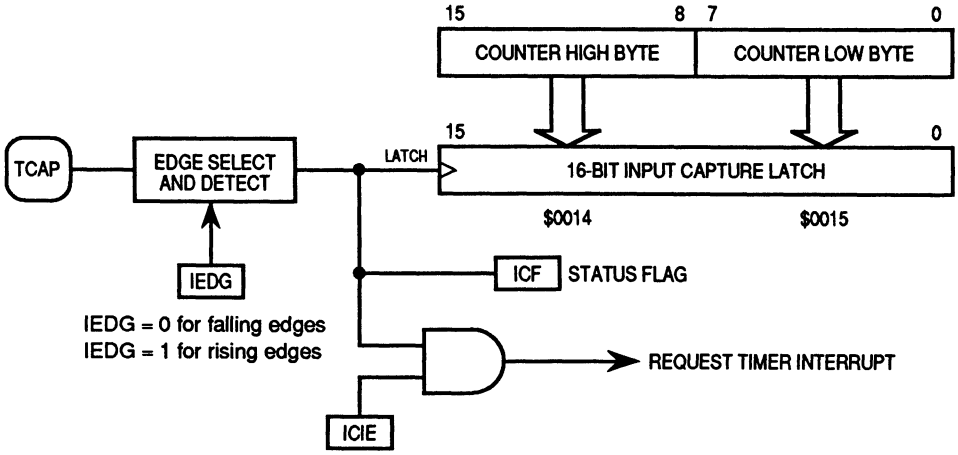

Figure 6-5. Input Capture Operation

Latching values into the timer counter register at successive edges of the same polarity measures the period of the input signal on the TCAP pin. Latching the counter values at successive edges of opposite polarity measures the pulse width of the signal.

6.2.2 Output Compare

The output compare feature provides a means of generating an output signal when the timer counter register reaches a selected value. The selected value is

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written into the output compare register. On every fourth internal clock cycle the capture/compare timer compares the value of the timer counter register to the contents of the output compare register. When a match occurs, the timer transfers the output level bit (OLVL) from the timer control register to the TCMP pin. (Refer to Figure 6-6.)

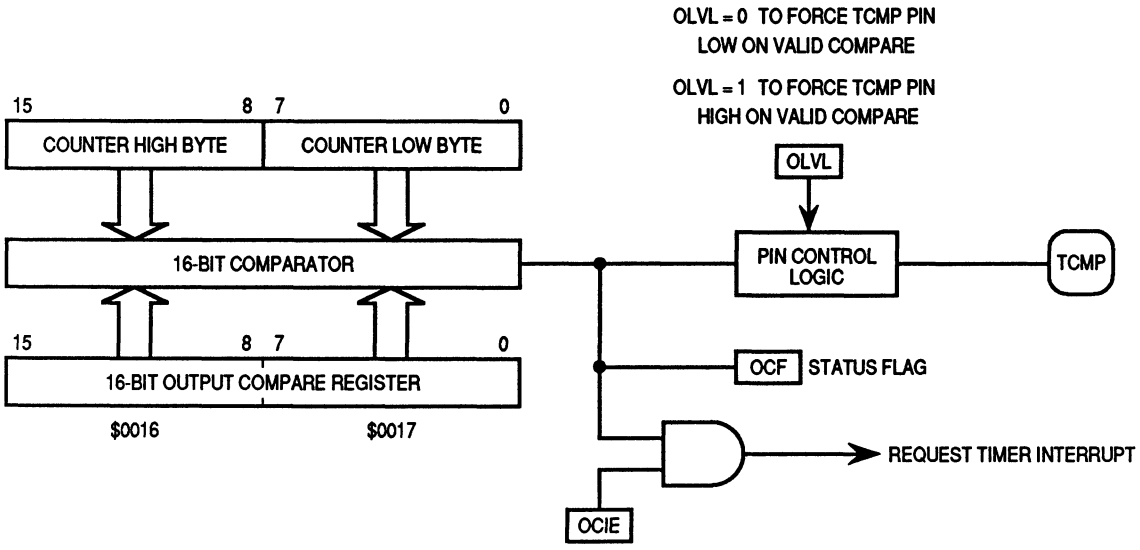

Figure 6-6. Output Compare Operation

The programmer can use the output compare register to measure time periods, to generate timing delays, or to generate a pulse of specific duration or a pulse train of specific frequency and duty cycle on the TCMP pin.

6.3 Input Capture Register (ICR)

The high and low bytes of the input capture register are at memory locations $0014 and $0015. (Refer to Figure 6-7.) The input capture register is a read-only register and is not affected by a reset.

ICR — Input Capture Register **$0014–$0015**

$0014	Bit 15	14	13	12	11	10	9	Bit 8	HIGH
$0015	Bit 7	6	5	4	3	2	1	Bit 0	LOW

Figure 6-7. Input Capture Register (ICR)

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When the input capture edge detector senses a defined transition on the TCAP pin, the input capture flag (ICF) is set, and the input capture register latches the value of the timer counter register. The contents of the timer counter register are transferred to the input capture register on every defined signal transition whether or not ICF was previously set. The input capture register always contains the value in the timer counter register at the time of the most recent input capture. The polarity of the level transition that triggers the counter capture is defined by the input edge bit (IEDG).

The timer counter register increments every fourth cycle of the internal clock. The counter value latched into the input capture register is one count more than the count at the time of the last rising edge of the clock before the defined transition on the TCAP pin occurred. This delay is required for internal synchronization.

Reading the high byte of the input capture register inhibits the input capture function until the low byte is also read. If the high byte is read first, both bytes must be read. Reading only the low byte does not inhibit the input capture function.

NOTE

To prevent interrupts from occurring between readings of the high and low bytes of the input capture register, set the interrupt flag before reading the high byte, and clear the flag after reading the low byte.

6.4 Output Compare Register (OCR)

The high and low bytes of the output compare register are at memory locations $0016 and $0017. (Refer to Figure 6-8.) All bits are readable and writable and are not altered by the capture/compare timer hardware or by a reset. If the compare function is not needed, the two bytes of the output compare register can be used as storage locations.

OCR — Output Compare Register **$0016–$0017**

$0016	Bit 15	14	13	12	11	10	9	Bit 8	HIGH
$0017	Bit 7	6	5	4	3	2	1	Bit 0	LOW

Figure 6-8. Output Compare Register (OCR)

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The output compare register contents are continually compared with the contents of the timer counter register. When a match occurs, the output compare flag (OCF) is set, and the OLVL bit is clocked to the TCMP pin. OLVL appears on TCMP whether or not OCF was previously set. An output compare interrupt is enabled if the output compare interrupt enable bit (OCIE) is set. The output compare register values and the output level bit are typically changed after each successful comparison to establish a new timeout period. Writing to either byte of the output compare register does not affect the other byte.

Writing the high byte of the output compare register inhibits the output compare function until the low byte is also written. If the high byte is written first, both bytes must be written. Writing only the low byte does not inhibit the output compare function.

6.5 Timer Status Register (TSR)

The read-only timer status register shown in Figure 6-9 has three status flags to indicate the following conditions:

- A selected transition occurred at the TCAP pin, and the contents of the timer counter register were transferred to the input capture register.
- A match occurred between the timer counter register and the output compare register, and the OLVL bit was transferred to the TCMP pin.
- A timer counter register transition from $FFFF to $0000 occurred.

TSR — Timer Status Register **$0013**

	Bit 7	6	5	4	3	2	1	Bit 0
	ICF	OCF	TOF	0	0	0	0	0
RESET:	U	U	U	0	0	0	0	0

(U = UNAFFECTED)

Figure 6-9. Timer Status Register (TSR)

ICF — Input Capture Flag

ICF is automatically set when an edge of the selected polarity occurs on TCAP. Clear the ICF bit by reading the timer status register with ICF set, and then reading the low byte ($0015) of the input capture register.

OCF — Output Compare Flag

OCF is automatically set when the value of the timer counter register matches the contents of the output compare register. Clear the OCF bit by

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reading the timer status register with OCF set, and then reading or writing the low byte ($0017) of the output compare register.

TOF — Timer Overflow Flag

TOF is automatically set when the timer counter register changes from $FFFF to $0000. Clear the TOF bit by reading the timer status register with TOF set, and then reading the low byte ($0019) of the timer counter register.

Bits 4–0 — Not used; always read zero

To clear a status bit, read the timer status register. Then access the low byte of the register associated with the status bit.

When using the timer overflow function and reading the timer counter register at random times to measure elapsed time, TOF could unintentionally be cleared. This problem can occur when reading the timer status register and the low byte of the timer counter register, but not for the purpose of servicing the TOF flag.

The alternate counter register at locations $001A and $001B contains the same value as the timer counter register at locations $0018 and $0019. Because reading the alternate counter register has no effect on the timer status register, the alternate counter register can be read at any time without clearing TOF.

6.6 Timer Control Register (TCR)

The read/write timer control register has five control bits. (Refer to Figure 6-10.) Three bits control interrupts associated with the timer status register flags ICF, OCF, and TOF. Another bit determines the edge polarity (positive-going or negative-going) that activates the input capture edge detector. Another bit determines the output level clocked onto TCMP when a successful output compare occurs.

TCR — Timer Control Register **$0012**

	Bit 7	6	5	4	3	2	1	Bit 0
	ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL
RESET:	0	0	0	0	0	0	U	0

(U = UNAFFECTED)

Figure 6-10. Timer Control Register (TCR)

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ICIE — Input Capture Interrupt Enable
1 = ICF interrupt enabled
0 = ICF interrupt disabled

OCIE — Output Compare Interrupt Enable
1 = OCF interrupt enabled
0 = OCF interrupt disabled

TOIE — Timer Overflow Interrupt Enable
1 = TOF interrupt enabled
0 = TOF interrupt disabled

IEDG — Input Edge
This bit determines which transition on the TCAP pin triggers a transfer of the contents of the timer counter register to the input capture register.
1 = Positive edge (low level to high level)
0 = Negative edge (high level to low level)

OLVL — Output Level
This bit determines the output level on the TCMP pin when a successful output compare occurs.
1 = High output
0 = Low output

Bits 4, 3, and 2 — Not used; always read zero

6.7 Timer During WAIT Mode

The internal clock halts during WAIT mode, but the capture/compare timer and COP counter remain active. An interrupt from the capture/compare timer causes the processor to exit WAIT mode.

6.8 Timer During STOP Mode

In STOP mode, the capture/compare timer stops counting and holds the last count value. If $\overline{IRQ}$ is used to exit STOP mode, the timer resumes counting from the count value that was present when STOP mode was entered. If $\overline{RESET}$ is used to exit STOP mode, the counter is forced to $FFFC.

If a defined transition occurs on the TCAP pin during STOP mode, ICF goes high as soon as an external interrupt brings the MCU out of STOP mode. If a power-on reset or a logical zero on the $\overline{RESET}$ pin brings the MCU out of STOP mode, all timer interrupt enable bits are cleared.

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SECTION 7
SERIAL I/O PORT

The serial I/O port (SIOP) enables simple high-speed synchronous serial data transfer between the MCU and peripheral devices. Figure 7-1 shows the structure of the SIOP system.

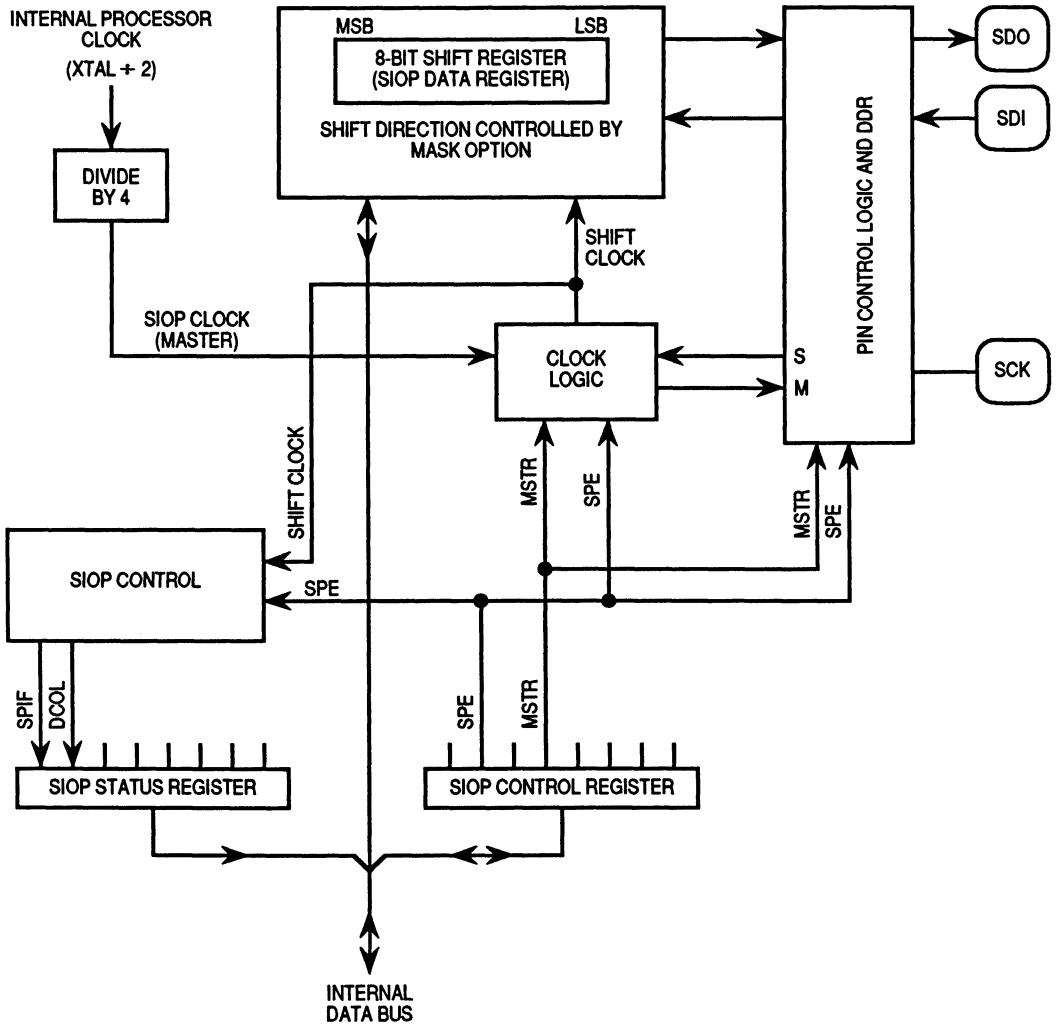

Figure 7-1. Serial I/O Port (SIOP) Block Diagram

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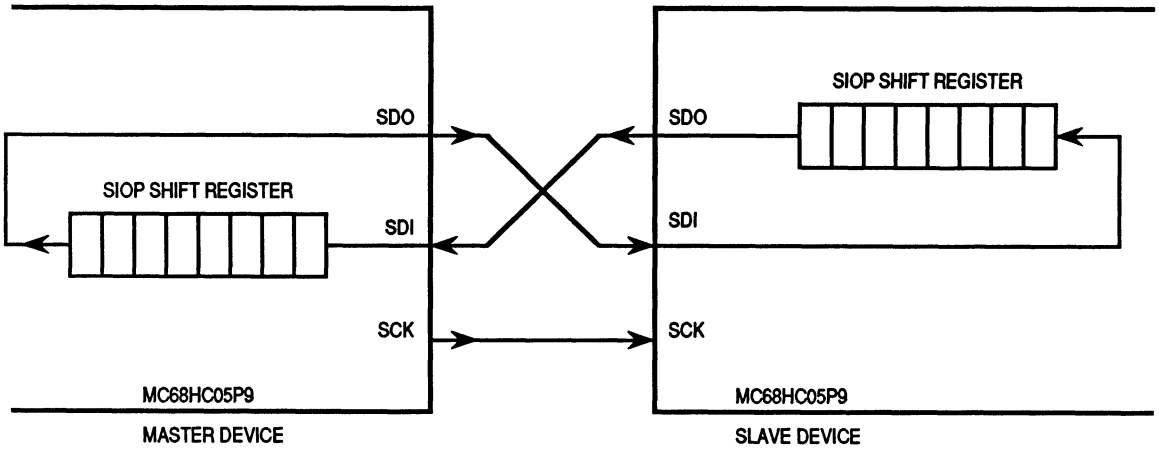
7.1. Data Movement

The SIOP can be used with simple shift registers to increase the number of parallel I/O pins controlled by the MCU. More powerful peripherals such as analog-to-digital (A/D) converters and real-time clocks are also compatible with this interface. A factory-set mask option allows the SIOP to transfer data MSB first or LSB first.

The SIOP data register in a master MCU and the SIOP data register in a slave MCU are connected to form a 16-bit circular shift register. During an SIOP transfer, the master shifts out the contents of its SIOP data register on its SDO pin. At the same time, the slave MCU shifts out the contents of its SIOP data register on its SDO pin, so that the master and slave exchange the contents of their data registers. (Refer to Figure 7-2.)



NOTE: Both MC68HC05P9 devices shown are programmed for MSB first data format.

Figure 7-2. SIOP Shift Register Operation

Many simple slave devices are designed either to receive data from a master or to supply data to a master. For example, when a serial-to-parallel shift register is used as an 8-bit output port, the master MCU initiates transfers of 8-bit data values to the shift register. Because the serial-to-parallel shift register does not send any data to the master, the MCU ignores whatever it receives as a result of the transmission.

The SIOP system is simpler than the SPI system on some other Motorola MCUs. The polarity of the serial clock (SCK) is fixed. There is no slave select pin on

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the SIOP system, and the direction of serial data does not automatically switch as on the SPI because the SIOP is not intended for use in multimaster systems.

Most applications use one MCU as the master to initiate and control data transfer between one or more slave peripheral devices.

7.2 SIOP Pin Descriptions

PB7/SCK, PB6/SDI, and PB5/SDO form the 3-bit shared-function I/O port B. Port B can be either the SIOP or a general-purpose I/O port.

When bit 6 (SPE) of the SIOP control register (SCR) is a logical one, port B is dedicated to SIOP functions. When SPE is cleared, port B reverts to standard parallel I/O without affecting the port B data register or data direction register.

After SPE is set, the SDO output driver can be disabled by writing a zero to DDRB5, configuring SDO as a high-impedance input.

NOTE

Do not use port B for general-purpose I/O while the SIOP system is enabled.

When the master mode select (MSTR) bit of the SIOP control register is set, the SIOP is configured for master mode. The SCK pin is an output whose signal is derived from the internal clock. SDI is the serial input, and SDO is the serial output. The master MCU initiates and controls the transfer of data to and from one or more slave peripheral devices. In master mode, a transmission is initiated by writing to the SIOP data register (SDR). Data written to SDR is parallel-loaded and shifted out serially to the slave device(s).

When MSTR is a logical zero, the SIOP is configured for slave mode. SDI and SDO have the same functions as they do in master mode, but SCK is configured as an input.

7.2.1 SIOP Clock

SCK synchronizes the movement of data into and out of the MCU through the SDI and SDO pins. In master mode, the SCK pin is an output. The transmission rate for master mode is one-fourth the internal clock rate. For example, if the OSC1 input frequency is 4 MHz, the internal clock frequency is 2 MHz, and the SCK frequency is 0.5 MHz.

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In slave mode, the SCK pin is an input. The maximum SCK input rate for slave mode is the internal clock divided by four. There is no minimum SCK frequency for slave mode.

Figure 7-3 shows the timing relationships between SCK, SDI, and SDO. The state of SCK between transmissions is logical one. The first falling edge of SCK signals the beginning of a transmission, and data is presented to the SDO pin. Data is captured at the SDI pin on the rising edge of SCK, and the transmission is ended on the eighth rising edge of SCK.

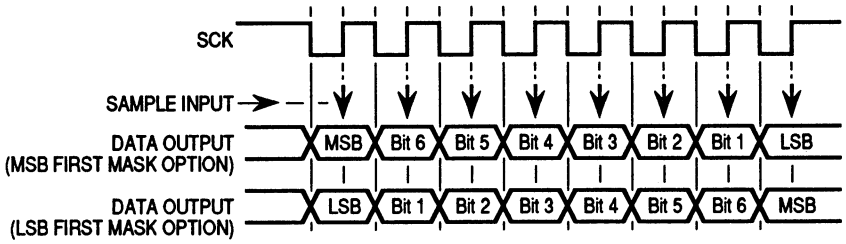

Figure 7-3. SIOP Data/Clock Timing

7.2.2 SIOP Data Input

The SDI pin becomes a serial input as soon as the SIOP is enabled. As shown in Figure 7-3, valid SDI data must be present for an SDI setup time before the rising edge of SCK and remain valid for an SDI hold time after the rising edge of SCK. (Refer to **10.9 SIOP Timing (V_{DD} = 5.0 Vdc)** and **10.10 SIOP Timing (V_{DD} = 3.3 Vdc)**.)

7.2.3 SIOP Data Output

The SDO pin becomes a serial output and goes to a logical one as soon as the SIOP is enabled. Between transfers, the state of the SDO pin reflects the value of the last bit received on the previous transmission. SDO cannot be used as a standard output while the SIOP is enabled, because it is coupled to the last stage of the serial shift register. On the first falling edge of SCK, the first data bit to be shifted out is presented to the SDO pin.

7.3 SIOP Control Register (SCR)

The SIOP control register is a read/write register containing only two bits. (Refer to Figure 7-4.) One bit enables the SIOP, and the other configures the SIOP for master or slave mode.

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SCR — SIOP Control Register **$000A**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	SPE	0	MSTR	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Figure 7-4. SIOP Control Register (SCR)

SPE — Serial Port Enable

SPE is readable and writable any time, but clearing SPE during a transmission aborts the transmission, resets the bit counter, and returns port B to its normal I/O function.

1 = Enables the SIOP and initializes the port B data direction register such that SCK is an input (in slave mode) or an output (in master mode), SDI is an input, and SDO is an output

0 = Disables the SIOP and returns port B to its normal I/O function

MSTR — Master Mode Select

Clearing MSTR aborts any transmission in progress.

1 = Configures SIOP as a master

0 = Configures SIOP as a slave

Bits 7, 5, and 3–0 — Not used; always read zero

7.4 SIOP Status Register (SSR)

The SIOP status register is a read-only register containing only two bits. (Refer to Figure 7-5.) One bit indicates that an SIOP transfer is complete, and the other indicates that an invalid access of the serial status register occurred while a transfer was in progress.

SSR — SIOP Status Register **$000B**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIF	DCOL	0	0	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Figure 7-5. SIOP Status Register (SSR)

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SPIF — SIOP Peripheral Interface Transfer Complete Flag

SPIF is automatically set on the eighth rising edge of SCK and indicates that a data transfer took place. SPIF does not inhibit further transmissions and can be ignored in master mode. Clear SPIF by reading the SIOP status register while SPIF is set, and then reading or writing the SIOP data register. SPIF is also cleared by a reset.

DCOL — Data Collision Flag

DCOL is automatically set if the SIOP data register is accessed while a data transfer is in progress. Reading or writing the SIOP data register while a data transfer is in progress results in invalid data being transmitted or read. Clear DCOL by reading the SIOP status register with SPIF set, and then accessing the SIOP data register. To clear DCOL when SPIF is not set, turn off the SIOP by writing a zero to SPE, and then turn it back on by writing a one to SPE. If the clearing sequence is not completed before another transmission starts, DCOL is set again. DCOL is also cleared by a reset.

Bits 5–0 — Not used; always read zero

7.5 SIOP Data Register (SDR)

The SIOP data register is both the transmit and receive data register. (Refer to Figure 7-6.)

SDR — SIOP Data Register **$000C**

	Bit 7	6	5	4	3	2	1	Bit 0
RESET:	SIOP DATA REGISTER NOT AFFECTED BY RESET							

Figure 7-6. SIOP Data Register (SDR)

This register is not double buffered, i.e., writing to the SIOP data register overwrites the previous contents. Reading or writing to the SIOP data register while a transmission is in progress can cause invalid data to be transmitted or received. The SIOP data register can be read and written only when the SIOP is enabled (SPE = 1).

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SECTION 8
ANALOG-TO-DIGITAL CONVERTER

Section 8 describes the four-channel, 8-bit, multiplexed input, successive-approximation A/D converter.

8.1 Conversion Process

The A/D conversion process is ratiometric, using two reference voltages, V_{RH} and V_{SS}. Conversion accuracy is guaranteed only if V_{RH} is equal to V_{DD}.

A multiplexer selects one of four analog input channels (AN3, AN2, AN1 or AN0) for sampling. A comparator successively compares the output of an internal D/A converter to the sampled analog input. Control logic changes the D/A converter input one bit at a time, starting with the MSB, until the D/A converter output matches the sampled analog input. The conversion is monotonic and has no missing codes.

An analog input voltage equal to V_{RH} converts to digital $FF; an input voltage greater than V_{RH} converts to $FF with no overflow. An analog input voltage equal to V_{SS} converts to digital $00. For ratiometric conversions, the source of each analog input should use V_{RH} as the supply voltage and be referenced to V_{SS}.

Pins PC6–PC3 are the four inputs to the multiplexer. Each channel of conversion takes 32 internal clock cycles, and the clock frequency must be equal to or greater than 1 MHz. If the internal clock frequency is less than 1 MHz, the A/D internal RC oscillator (nominally 1.5 MHz) must be used for the A/D conversion clock. Make this selection by setting the ADRC bit in the A/D status and control register to logical one.

8.2 A/D Status and Control Register (ADSCR)

The A/D status and control register contains a status flag and four writable control bits. (Refer to Figure 8-1.)

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ADSCR — A/D Status and Control Register **$001E**

	Bit 7	6	5	4	3	2	1	Bit 0
	CCF	ADRC	ADON	0	0	0	CH1	CH0
RESET:	0	0	0	0	0	0	0	0

Figure 8-1. A/D Status and Control Register (ADSCR)

CCF — Conversion Complete Flag

This read-only bit is automatically set when an analog-to-digital conversion is complete, and a new result can be read from the A/D data register . CCF is automatically cleared when a new conversion begins or when either the A/D status and control register or the A/D data register is accessed. Writing to or reading the A/D status and control register or the A/D data register starts a new conversion sequence. Data from the previous conversion is overwritten regardless of the state of the CCF bit. While CCF is a logical zero, the requested A/D result is not yet available in the A/D data register.

ADRC — A/D RC Oscillator Control

When the RC oscillator is turned on, it requires a time (t_{ADRC}) to stabilize, and results can be inaccurate during this time. If the internal clock rate is above 1 MHz, the ADRC bit should be cleared.

1 = Internal RC oscillator drives A/D converter

0 = Internal clock drives A/D converter

When the internal RC oscillator is being used as the A/D converter clock, two limitations apply:

- Because of the frequency tolerance of the RC oscillator and its asynchronism with the internal clock, the conversion complete flag (CCF) must be used to determine when a conversion sequence has been completed.
- The conversion process runs at the nominal 1.5 MHz rate, but the conversion results must be transferred to the A/D data register synchronously with the internal clock; therefore, the conversion process is limited to a maximum of one channel every internal clock cycle.

ADON — A/D On

When the A/D is turned on, it requires a time (t_{ADON}) for the current sources to stabilize. During this time, results can be inaccurate.

1 = A/D converter enabled

0 = A/D converter disabled

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Bits 4–2 — Not used; always read logical zero.

CH1–CH0 — Channel Select

These bits select one of the four A/D inputs (AN3, AN2, AN1, or AN0) for conversion. (Refer to Table 8-1).

Table 8-1. A/D Input Selection

CH1:CH0	Input Selected
00	AN0, Port C Bit 6
01	AN1, Port C Bit 5
10	AN2, Port C Bit 4
11	AN3, Port C Bit 3

To prevent excess power dissipation, do not use a port C pin as an analog input and a digital input at the same time.

Using one of the port C pins as the A/D converter input does not affect the ability to use the remaining port C pins as digital inputs.

Performing a digital read of A port C pin that is selected as an analog input returns a logical zero.

8.3 A/D Data Register (ADDR)

The A/D data register is a read-only register that contains the result of the most recent A/D conversion. This register is updated each time the conversion complete flag (CCF) is set in the A/D status and control register.

ADDR — A/D Data Register **$001D**

	Bit 7	6	5	4	3	2	1	Bit 0
RESET:	A/D DATA REGISTER NOT AFFECTED BY RESET							

Figure 8-2. A/D Data Register (ADDR)

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8.4 A/D Converter During WAIT Mode

The A/D converter continues to operate normally while the MCU is in WAIT mode. If the A/D converter is not being used, clear the ADON and ADRC bits in the A/D status and control register to decrease power consumption during WAIT mode.

8.5 A/D Converter During STOP Mode

STOP mode disables the comparator and charge pump and aborts any conversion in progress or pending. When the MCU leaves STOP mode, the built-in delay for oscillator start-up allows enough time for the A/D circuits to stabilize. Therefore, no software delays are needed after exiting from STOP mode.

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SECTION 9
SELF-CHECK MODE

This section describes how the self-check mode tests the operation of the MCU.

9.1 Self-Check Circuit

The self-check function determines if the MCU is operating properly. Figure 9-1 shows the self-check circuit. The MCU enters self-check mode on the rising edge of $\overline{\text{RESET}}$ if $\overline{\text{IRQ}}$ is at 9 V and PD7/TCAP is at logical one. Port C pins PC3–PC0 are monitored for the self-check results. The self-check ROM automatically performs the following tests:

- I/O — Functional test of ports A, B, and C
- RAM — Counter test for each RAM byte
- Timer — Test of timer counter register and OCF bit
- ROM — Checksum of entire ROM pattern
- SIOP — Test of data transmission from SDO to SDI in master mode
- Interrupts — Test of external and timer interrupts
- A/D converter — Conversion test of internal channels 4 and 6

9.2 Self-Check Results

Table 9-1 gives the codes displayed by the light-emitting diodes to indicate the self-check results.

Table 9-1. Self-Check Results

PC3	PC2	PC1	PC0	Remarks
1	0	0	1	Bad I/O
1	0	1	0	Bad RAM
1	0	1	1	Bad Timer
1	1	0	0	Bad ROM
1	1	0	1	Bad SIOP
1	1	1	0	Bad Interrupts or $\overline{\text{IRQ}}$ Request
1	1	1	1	Bad A/D Converter
Flashing				Good Device
All Others				Bad Device

NOTE: Zero indicates LED is on; 1 indicates LED is off.

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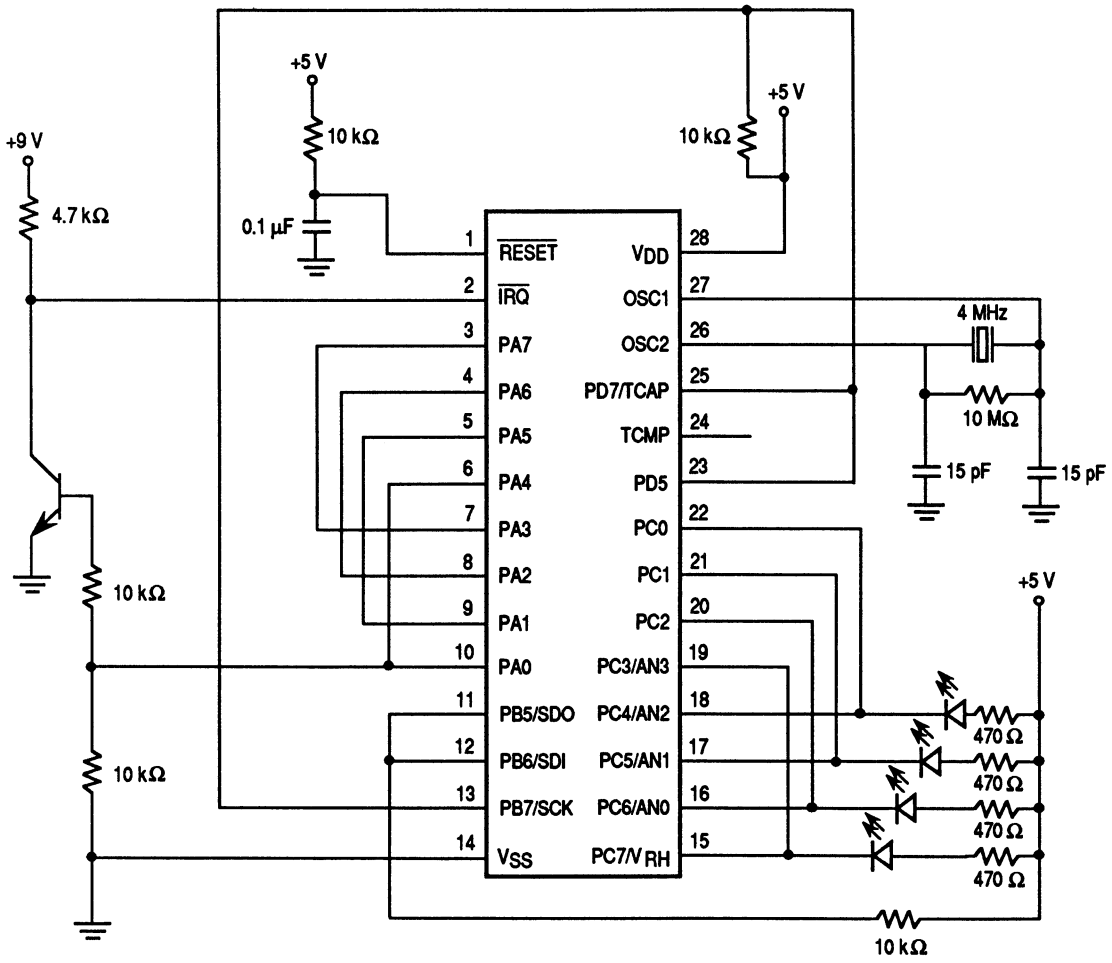

Figure 9-1. Self-Check Circuit

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SECTION 10
ELECTRICAL SPECIFICATIONS

This section contains MCU electrical specifications and timing information.

10.1 Maximum Ratings

The MCU contains circuitry that protects the inputs against damage from high static voltages; however, take precautions to avoid applying voltages higher than those shown in Table 10-1. V_{in} and V_{out} should be kept within the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Connect unused inputs to an appropriate logical voltage level (e.g., either V_{SS} or V_{DD}).

Table 10-1. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to +7.0	V
Input Voltage	V_{in}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Self-Check Mode ($\overline{IRQ}$ Pin Only)	V_{in}	V_{SS} – 0.3 to 2 × V_{DD} + 0.3	V
Current Drain per Pin (Excluding V_{DD} and V_{SS})	I	25	mA
Operating Temperature Range MC68HC05P9P (Standard) MC68HC05P9CP (Extended)	T_A	 0 to +70 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

10.2 Thermal Characteristics

Table 10-2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic SOIC	$R_{\theta JA}$	 60 60	°C/W

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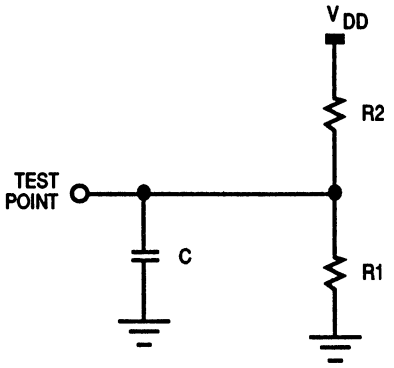

V_{DD} = 4.5 V

Pins	R1	R2	C
PA7–PA0 PB7–PB5 PC7–PC0 PD5	3.26 kΩ	2.38 kΩ	50 pF

Figure 10-1. Test Load

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10.3 Power Considerations

The average chip junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where:

T_A = Ambient temperature in °C
θ_{JA} = Package thermal resistance, junction to ambient in °C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{CC} \times V_{CC}$, watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user-determined

For most applications $P_{I/O} \ll P_{INT}$ and can be neglected.

The following is an approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected):

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273°C) + R_{\theta JA} \times P_D \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

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10.4 DC Electrical Characteristics (V_{DD} = 5.0 Vdc)

Table 10-3. DC Electrical Characteristics (V_{DD} = 5.0 Vdc)

(V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage					
I_{Load} = 10.0 µA	V_{OL}	–	–	0.1	V
I_{Load} = –10.0 µA	V_{OH}	V_{DD} – 0.1	–	–	V
Output High Voltage (I_{Load} = –0.8 mA) PA7–PA0, PB7–PB5, PC7–PC0, PD5, TCMP	V_{OH}	V_{DD} – 0.8	–	–	V
Output Low Voltage (I_{Load} = 1.6 mA) PA7–PA0, PB7–PB5, PC7–PC0, PD5, TCMP	V_{OL}	–	–	0.4	V
Input High Voltage PA7–PA0, PB7–PB5, PC7–PC0, PD5, PD7/TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	–	V_{DD}	V
Input Low Voltage PA7–PA0, PB7–PB5, PC7–PC0, PD5, PD7/TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	–	0.2 × V_{DD}	V
Supply Current (refer to NOTES)	I_{DD}				
RUN		–	TBD	TBD	mA
WAIT		–	TBD	TBD	mA
STOP					
25 °C		–	TBD	TBD	µA
0 to 70°C (Standard)			TBD	TBD	µA
I/O Ports Hi-Z Leakage Current PA7–PA0, PB7–PB5, PC7–PC0, PD5	I_{IL}	–	–	±10	µA
A/D Ports Hi-Z Leakage Current	I_{OZ}	–	–	±1	µA
Input Current $\overline{RESET}$, $\overline{IRQ}$, OSC1, PD7/TCAP	I_{in}	–	–	±1	µA
Capacitance					
Ports (As Input or Output)	C_{out}	–	–	12	pF
$\overline{RESET}$, $\overline{IRQ}$	C_{in}	–	–	8	pF

NOTES:

1. Typical values at midpoint of voltage range, 25°C only.
2. WAIT I_{DD}: Timer and A/D converter systems active.
3. RUN (operating) I_{DD} and WAIT I_{DD} measured using external square wave clock source (f_{osc} = 4.2 MHz), all inputs 0.2 V from rail; no dc loads, less than 50 pF on all outputs, C_L = 20 pF on OSC2.
4. WAIT I_{DD} and STOP I_{DD}: all ports configured as inputs, V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V.
5. STOP I_{DD} measured with OSC1 = V_{SS}.
6. WAIT I_{DD} is affected linearly by the OSC2 capacitance.

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10.5 DC Electrical Characteristics (V_{DD} = 3.3 Vdc)

Table 10-4. DC Electrical Characteristics (V_{DD} = 3.3 Vdc)

(V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($I_{Load} \leq 10.0\ \mu A$)	V_{OL} V_{OH}	– $V_{DD} - 0.1$	– –	0.1 –	V
Output High Voltage ($I_{Load} = -0.2$ mA) PA7–PA0, PB7–PB5, PC7–PC0, PD5, TCMP	V_{OH}	$V_{DD} - 0.3$	–	–	V
Output Low Voltage (I_{Load} = 0.4 mA) PA7–PA0, PB7–PB5, PC7–PC0, PD5, TCMP	V_{OL}	–	–	0.3	V
Input High Voltage PA7–PA0, PB7–PB5, PC7–PC0, PD5, PD7/TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	$0.7 \times V_{DD}$	–	V_{DD}	V
Input Low Voltage PA7–PA0, PB7–PB5, PC7–PC0, PD5, PD7/TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	–	$0.2 \times V_{DD}$	V
Data-Retention Mode Supply Voltage (0 to 70°C)	V_{RM}	2.0	–	–	V
Supply Current (refer to NOTES) RUN WAIT STOP 25°C 0 to 70°C (Standard)	I_{DD}	 – – – –	 TBD TBD TBD –	 TBD TBD TBD TBD	 mA mA µA µA
I/O Ports Hi-Z Leakage Current PA7–PA0, PB7–PB5, PC7–PC0, PD5	I_{IL}	–	–	±10	µA
Input Current $\overline{RESET}$, $\overline{IRQ}$, OSC1, PD5, PD7/TCAP	I_{in}	–	–	±1	µA
Capacitance Ports (As Input or Output) $\overline{RESET}$, $\overline{IRQ}$, PD5, PD7/TCAP	 C_{out} C_{in}	 – –	 – –	 12 8	 pF pF

NOTES:

1. Typical values at midpoint of voltage range, 25°C only.
2. WAIT I_{DD}: timer and A/D converter active
3. RUN (operating) I_{DD}, WAIT I_{DD} measured using external square wave clock source (f_{osc} = 4.2 MHz), all inputs 0.2 V from rail; no dc loads, less than 50 pF on all outputs, C_L = 20 pF on OSC2..
4. WAIT I_{DD} and STOP I_{DD}: all ports configured as inputs, V_{IL} = 0.2 V, $V_{IH} = V_{DD} - 0.2$ V.
5. STOP I_{DD} measured with OSC1 = V_{SS}.
6. WAIT I_{DD} is affected linearly by the OSC2 capacitance.

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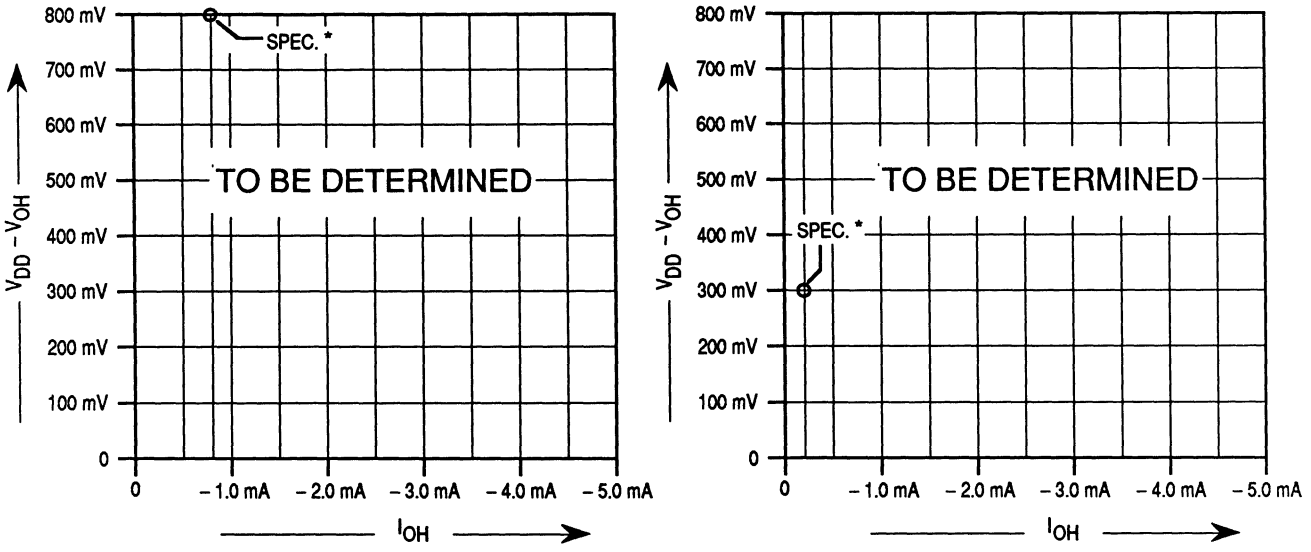

Figure 10-2. Typical High-Side Driver Characteristics

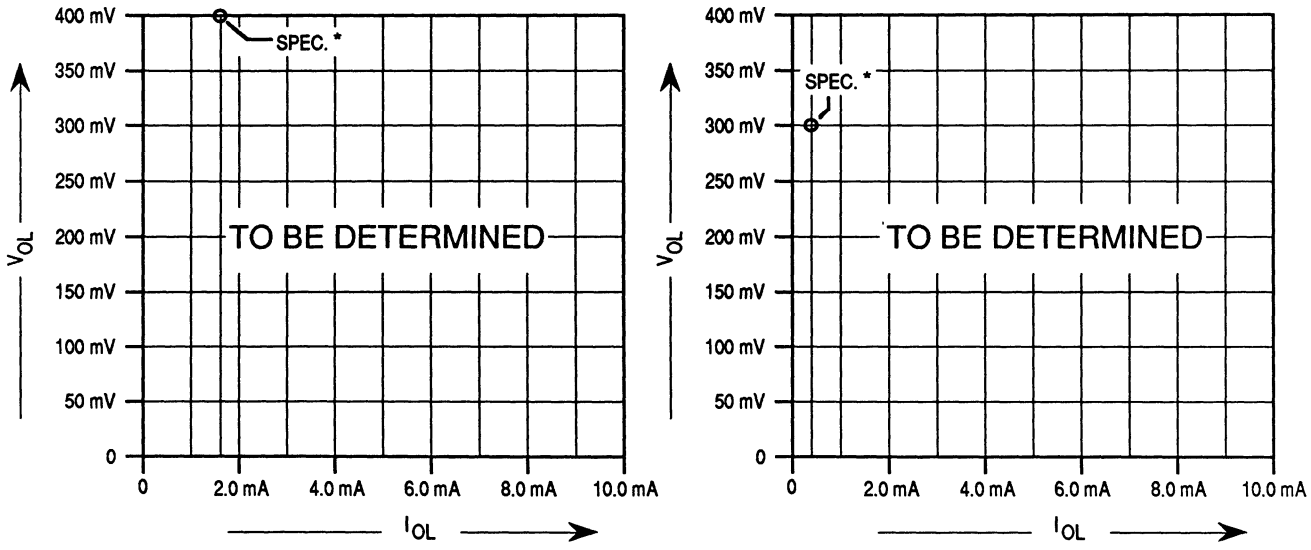

Figure 10-3. Typical Low-Side Driver Characteristics

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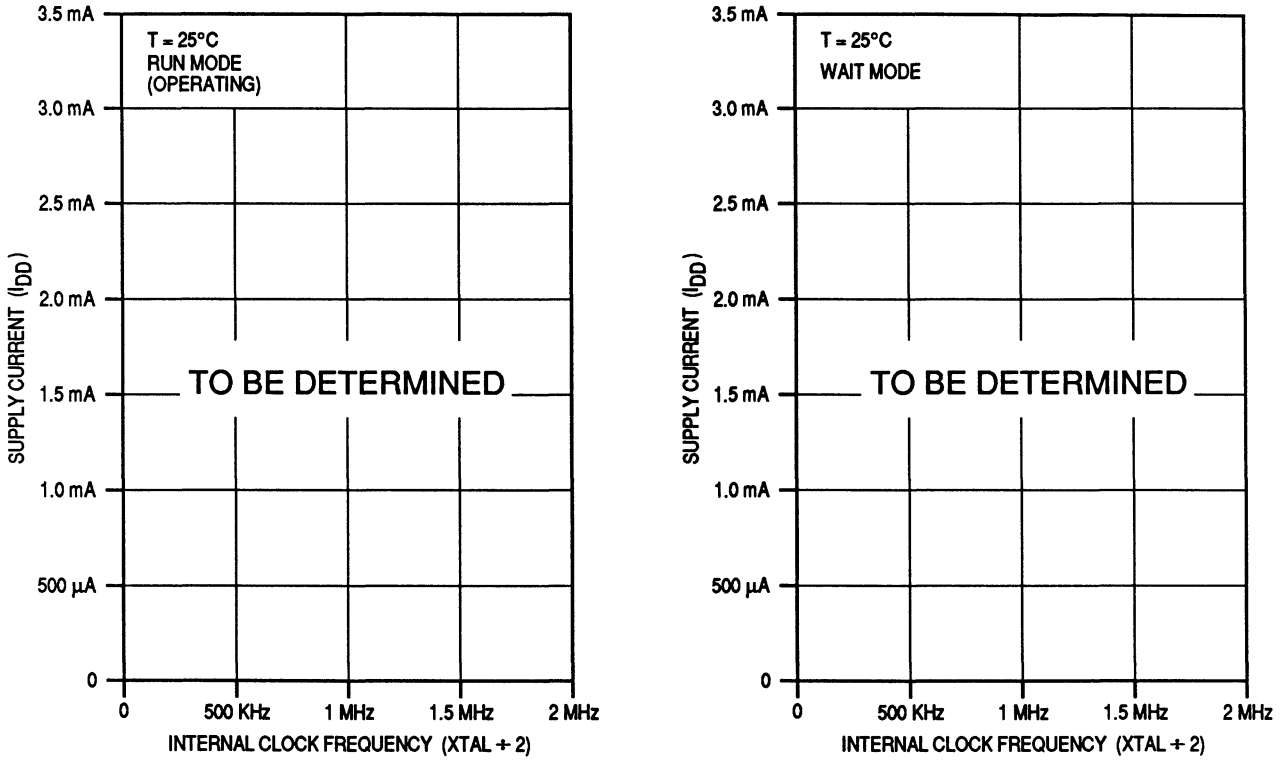

Figure 10-4. Typical Supply Current vs Internal Clock Frequency

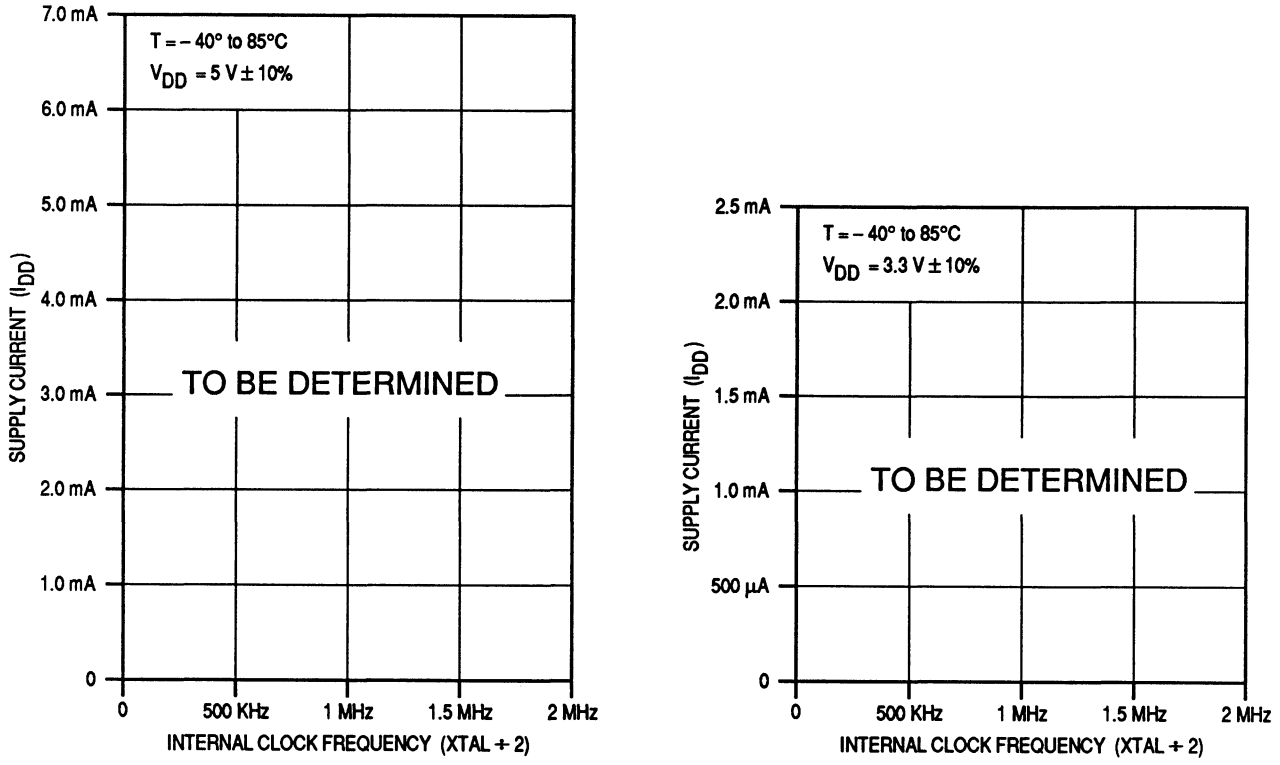

Figure 10-5. Maximum Supply Current vs Internal Clock Frequency

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10.6 A/D Converter Charactristics

Table 10-5. A/D Converter Characteristics

Characteristic	Min	Max	Unit
Resolution	8	8	Bit
Absolute Accuracy (4.0 V> V_{RH} > V_{DD}) (refer to NOTE 1)	–	±1-1/2	LSB
Conversion Range V_{RH}	V_{SS} V_{SS}	V_{RH} V_{DD}	V V
Conversion Time (Includes Sampling Time) External Clock (XTAL) Internal RC Oscillator (ADRC = 1)	 32 32	 32 32	 t_{AD} µs
Power-Up Time	–	100	µs
Monotonicity	Inherent (Within Total Error)		
Zero Input Reading (V_{in} = 0 V)	00	01	Hex
Full-Scale Reading (V_{in} = V_{RH})	FF	FF	Hex
Sample Acquisition Time (refer to NOTE 2) External Clock (XTAL) Internal RC Oscillator (ADRC) = 1	 12 –	 12 12	 t_{AD} µs
Input Capacitance PC3/AN3–PC6/AN0	–	12	pF
Analog Input Voltage	V_{SS}	V_{RH}	V
Input Leakage (refer to NOTE 4) AN0–AN3 V_{RH}	 – –	 ±1 ±1	 µA µA

NOTES:

1. A/D accuracy may decrease proportionately as V_{RH} is reduced below 4.0 V.
2. Source impedances greater than 10 kΩ adversely affect internal RC charging time during input sampling.
3. t_{AD} = t_{cyc} if clock source is MCU.
4. The external system error caused by input leakage current is approximately equal to the product of R source and input current.

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10.7 Control Timing (V_{DD} = 5.0 Vdc)

Table 10-6. Control Timing (V_{DD} = 5.0 Vdc)

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency Crystal Option External Clock Option	f_{osc}	 – dc	 4.2 4.2	 MHz MHz
Internal Operating Frequency Crystal (f_{osc} ÷ 2) External Clock (f_{osc} ÷ 2)	f_{op}	 – dc	 2.1 2.1	 MHz MHz
Cycle Time	t_{cyc}	480	–	ns
Crystal Oscillator Startup Time	t_{OXOV}	–	100	ms
STOP Recovery Startup Time (Crystal Oscillator)	t_{ILCH}	–	100	ms
$\overline{\text{RESET}}$ Pulse Width	t_{RL}	1.5	–	t_{cyc}
Timer Resolution (refer to NOTE 1)	t_{RESL}	4.0	–	t_{cyc}
Interrupt Pulse Width Low (Edge Triggered)	t_{ILIH}	125	–	ns
Interrupt Pulse Period	t_{ILIL}	(refer to NOTE 2)	–	t_{cyc}
OSC1 Pulse Width	t_{OH}, t_{OL}	90	–	ns
RC Oscillator Stabilization Time	t_{RCON}	–	5	µs
V_{DD} Slew Rate Rising Falling	 S_{VDDR} S_{VDDF}	 – –	 0.05 0.1	V/µs
A/D On Current Stabilization Time	t_{ADON}	–	100	µs

NOTES:

1. Because a 2-bit prescaler in the timer must count four internal cycles (t_{cyc}), this is the limiting minimum factor in determining the timer resolution.
2. The period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 19 t_{cyc}.

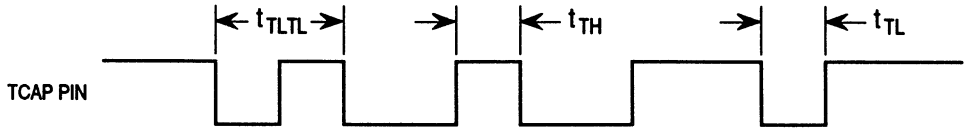

Figure 10-6. TCAP Timing

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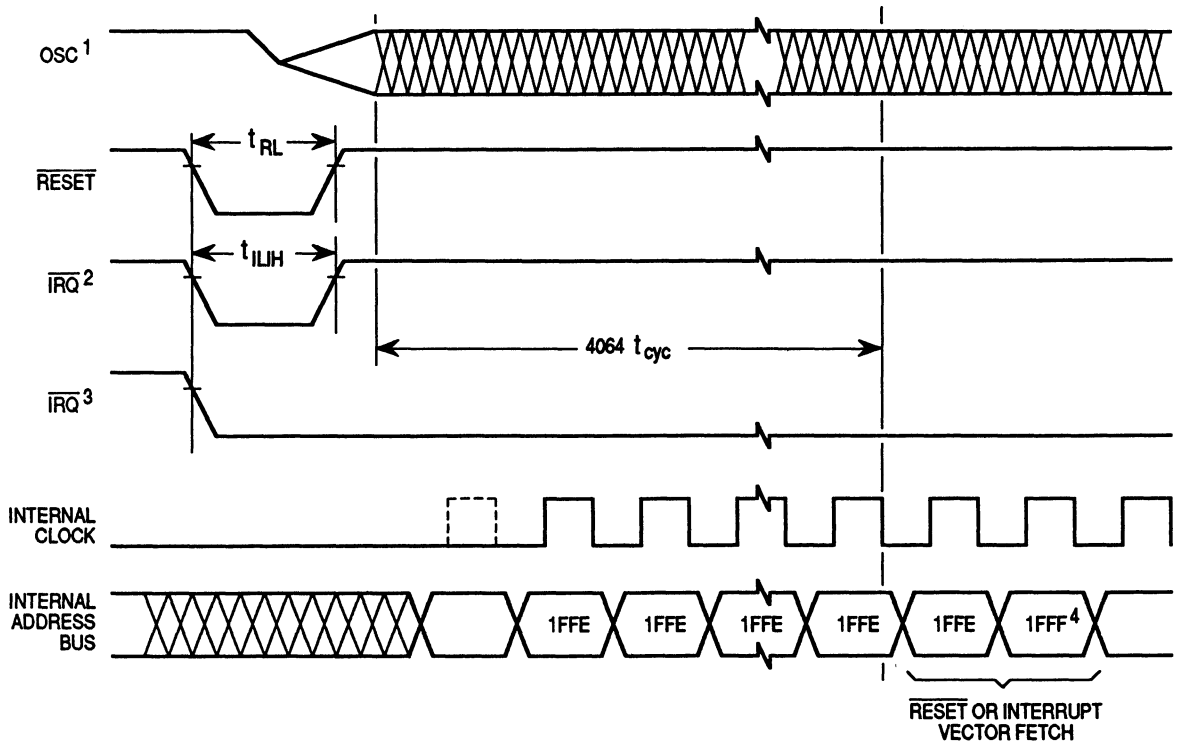

NOTES:

1. Represents the internal clocking of the OSC1 pin.
2. $\overline{IRQ}$ pin edge-sensitive mask option.
3. $\overline{IRQ}$ pin level- and edge-sensitive mask option.
4. $\overline{RESET}$ vector address shown for timing example.

Figure 10-7. STOP Recovery Timing

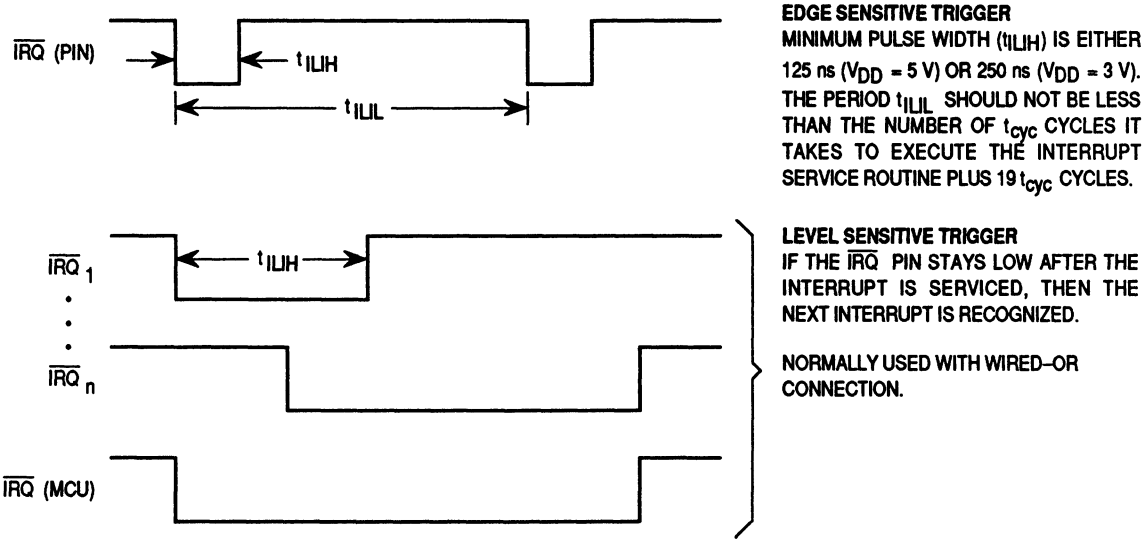

Figure 10-8. External Interrupt Timing

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10.8 Control Timing (V_{DD} = 3.3 Vdc)

Table 10-7. Control Timing (V_{DD} = 3.3 Vdc)

(V_{DD} = 3.3 Vdc ±10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency	f_{osc}			
Crystal Option		–	2.0	MHz
External Clock Option		dc	2.0	MHz
Internal Operating Frequency	f_{op}			
Crystal (f_{osc} ÷ 2)		–	1.0	MHz
External Clock (f_{osc} ÷ 2)		dc	1.0	MHz
Cycle Time	t_{cyc}	1	–	ms
Crystal Oscillator Startup Time	t_{OXOV}	–	100	ms
STOP Recovery Startup Time (Crystal Oscillator)	t_{ILCH}	–	100	ms
$\overline{\text{RESET}}$ Pulse Width	t_{RL}	1.5	–	t_{cyc}
Timer Resolution (refer to NOTE 1)	t_{RESL}	4.0	–	t_{cyc}
Interrupt Pulse Width Low (Edge Triggered)	t_{ILIH}	250	–	ns
Interrupt Pulse Period	t_{ILIL}	(refer to NOTE 2)	–	t_{cyc}
OSC1 Pulse Width	t_{OH}, t_{OL}	200	–	ns

NOTES:

1. Because a 2-bit prescaler in the timer must count four internal cycles (t_{cyc}), this is the limiting minimum factor in determining the timer resolution.
2. The period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 19 t_{cyc}.

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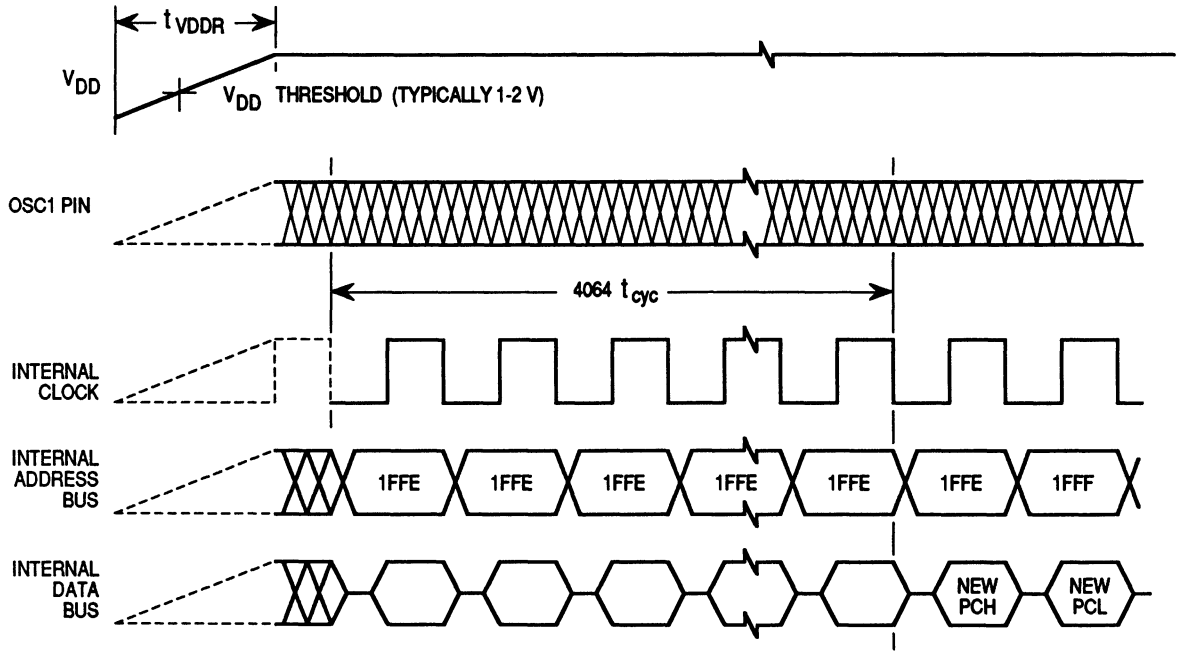
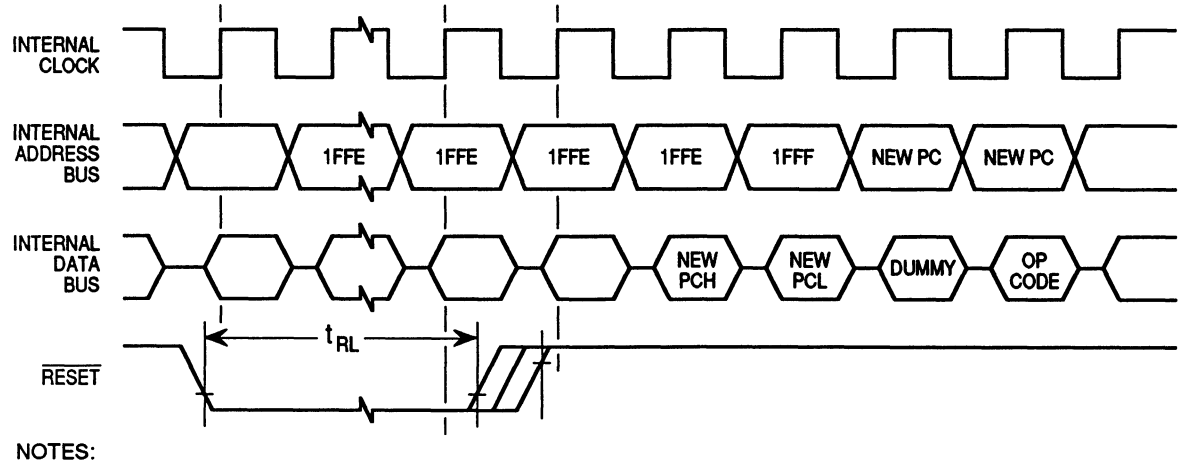


NOTES:

1. Internal clock, internal address bus, and internal data bus signals are not available externally.
2. An internal POR reset is triggered as V_{DD} rises through a threshold (typically 1-2 V).

Figure 10-9. Power-On Reset Timing



NOTES:

1. Internal clock, internal address bus, and internal data bus signals are not available externally.
2. The next rising edge of the internal processor clock after the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

Figure 10-10. External Reset Timing

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10.9 SIOP Timing (V_{DD} = 5.0 Vdc)

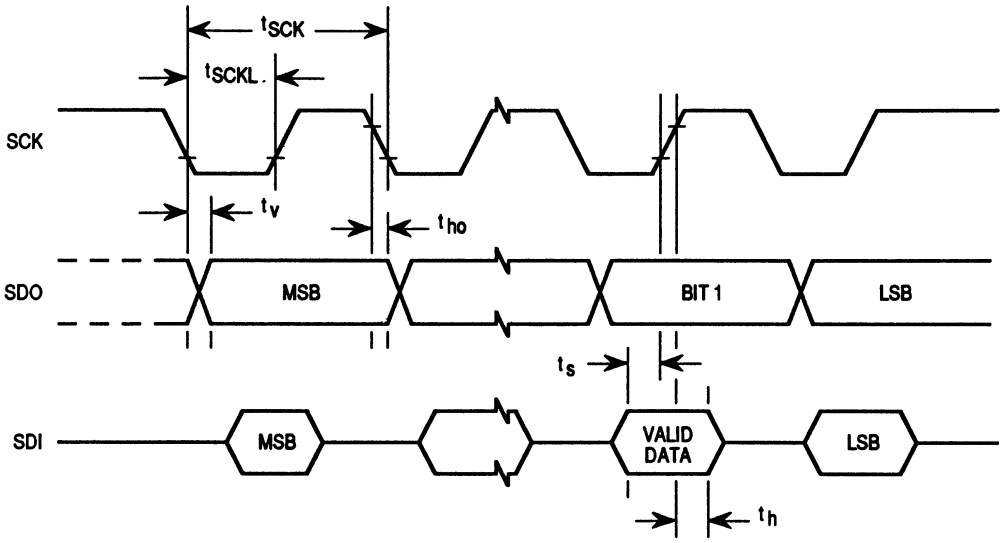
Table 10-8. SIOP Timing (V_{DD} = 5.0 Vdc)

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation (refer to NOTE 1) Master Slave	 $f_{SIOP(M)}$ $f_{SIOP(S)}$	 0.25 dc	 0.25 0.25	 f_{op} f_{op}
Cycle time (refer to NOTE 1) Master Slave	 $t_{SCK(M)}$ $t_{SCK(S)}$	 4.0 –	 4.0 4.0	 t_{cyc} t_{cyc}
Clock (SCK) Low Time (f_{op} = 2.1 MHz) (refer to NOTE 2)	t_{SCKL}	932	–	ns
SDO Data Valid Time	t_v	–	200	ns
SDO Hold Time	t_{ho}	0	–	ns
SDI Setup Time	t_s	100	–	ns
SDI Hold Time	t_h	100	–	ns

NOTES:

1. $f_{op} = f_{osc} \div 2$ = 2.1 MHz maximum; $t_{cyc} = 1 \div f_{op}$.
2. In master mode, SCK is generated by dividing the internal clock (f_{op}) by 4.



NOTES:

1. This diagram applies to both the master and slave modes of the SIOP.
2. Bit order is shown for MSB first option.

Figure 10-11. SIOP Timing

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10.10 SIOP Timing (V_{DD} = 3.3 Vdc)

Table 10-9. SIOP Timing (V_{DD} = 3.3 Vdc)

(V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation Master Slave	 $f_{SIOP(M)}$ $f_{SIOP(S)}$	 0.25 dc	 0.25 0.25	 f_{op} f_{op}
Cycle time Master Slave	 $t_{SCK(M)}$ $t_{SCK(S)}$	 4.0 –	 4.0 4.0	 t_{cyc} t_{cyc}
Clock (SCK) Low Time (f_{op} = 1.0 MHz)	t_{SCKL}	1980	–	ns
SDO Data Valid Time	t_v	–	400	ns
SDO Hold Time	t_{ho}	0	–	ns
SDI Setup Time	t_s	200	–	ns
SDI Hold Time	t_h	200	–	ns

NOTE: f_{op} = 1.0 MHz maximum

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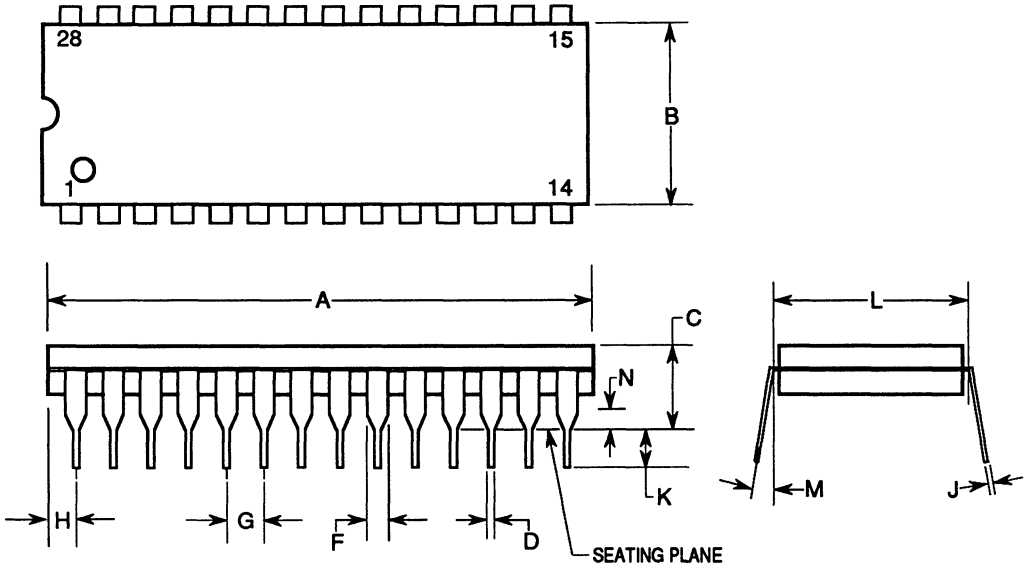
SECTION 11
MECHANICAL SPECIFICATIONS

This section describes the dimensions of the DIP (Dual-In-line Package) and SOIC (Small Outline Integrated Circuit) MCU packages.

11.1 Dual-In-Line Package (DIP)



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

Figure 11-1. DIP Dimensions

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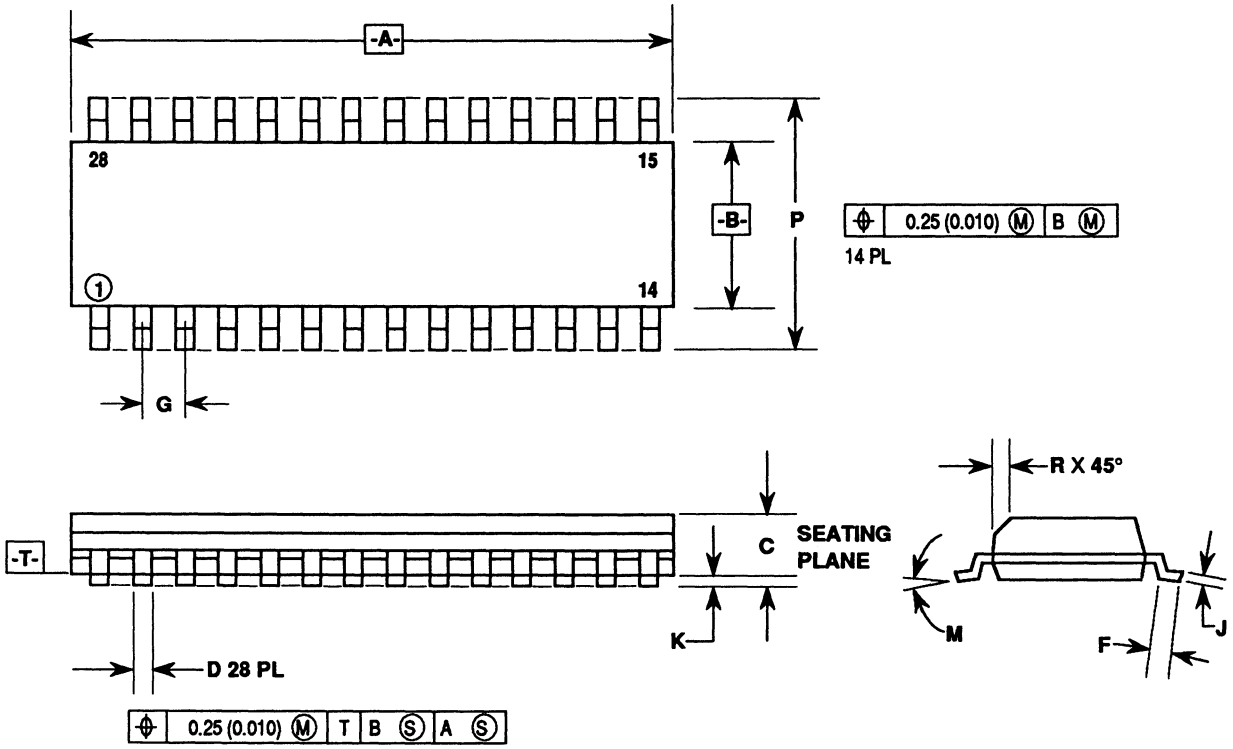
11.2 Small Outline Integrated Circuit (SOIC)



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.710
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Figure 11-2. SOIC Dimensions

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SECTION 12
ORDERING INFORMATION

Use the information in this section to order the MC68HC05P9 MCU.

12.1 ROM Pattern Media

Ordering information can be delivered to Motorola in the following media:

- MS™-DOS[1] or PC-DOS flexible disk (360K)
- EPROM(s) 2764, MCM68764, MCM68766

To initiate a ROM pattern for the MCU, first contact the local field service office, a sales person, or a Motorola representative.

12.1.1 Flexible Disks

A flexible disk containing the customer's program (using positive logic for address and data), can be submitted for pattern generation. Clearly label the disk with the customer's name, data, project or product name, and the name of the file containing the pattern.

In addition to the program pattern, a file containing the program source code list can be included. This data is kept confidential and used to expedite the process in case of any difficulty with the pattern file.

MS-DOS is the Microsoft Disk Operating System. PC-DOS is the IBM®[2] Personal Computer (PC) Disk Operating System. Disks submitted must be standard density (360K) double-sided 5-1/4 in. The disks must contain object file code in Motorola's S-record format, a character-based object file format generated by M6805 cross assemblers and linkers on IBM PC-style machines.

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[1]MS-DOS is a trademark of Microsoft, Inc.

[2]IBM is a registered trademark of International Business Machines Corporation.

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12.1.2 EPROMs

A type 2764, 68764, or 68766 EPROM containing the customer's program (using positive logic for address and data), may be submitted for pattern generation. User ROM is programmed at addresses $0020 through $004F (page zero) and $0100 through $08FF with vectors at addresses $1FF0 to $1FFF. Set at logical zero all unused bytes, including those in the user's space. For shipment to Motorola, pack EPROMs securely in a conductive IC carrier. Do not package the EPROMs in a Styrofoam container.

12.2 ROM Pattern Verification

12.2.1 Verification Media

All original pattern media are filed for contractual purposes and are not returned. A computer listing of the ROM code is generated and returned along with a listing verification form. The listing should be thoroughly checked, and the verification form should be completed, signed, and returned to Motorola. The signed verification form constitutes the contractual agreement for the creation of the customer mask. To aid in the verification process, Motorola programs the *customer-supplied* blank EPROMs or DOS disks from the data file used to create the custom mask.

12.2.2 ROM Verification Units (RVUs)

Ten RVUs containing the customer's ROM pattern are sent for program verification. These units are made using the custom mask, but are for the purpose of ROM verification only. For expediency, the RVUs are unmarked, packaged in ceramic, and tested with 5 V at room temperature. These RVUs are free of charge with the minimum order quantity, but are not production parts. RVUs are not backed or guaranteed by Motorola Quality Assurance.

12.3 MCU Order Numbers

Table 13-1 provides ordering information for available package types.

Table 12-1. MCU Order Numbers

Package Type	MCU Order Number
Plastic DIP	MC68HC05P9P
SOIC	MC68HC05P9DW

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