Freescale Semiconductor, Inc.

Addendum to
68HC08AZ32
Technical Data

This addendum provides changes to the 68HC08AZ32 Advance Information Technical Data Book (Motorola document order number MC68HC08AZ32/D).

CGM - Reaction Time Calculation

The following paragraphs should be added to the end of the Reaction Time Calculation section on page 118 of the data book:

When defining a limit in software for the maximum lock time, the value must allow for variation due to all of the factors mentioned in this section, especially due to the Cf capacitor and application specific influences.

The calculated lock time is only an indication and it is the customer's responsibility to allow enough of a guard band for their application. Prior to finalising any software and while determining the maximum lock time, take into account all device to device differences. Typically, applications set the maximum lock time as an order of magnitude higher than the measured value. This is considered sufficient for all such device to device variation.

Motorola recommends measuring the lock time of the application system by utilising dedicated software, running in Flash, EEPROM or RAM. This should toggle a port pin when the PLL is first configured and switched on, then again when it goes from acquisition to lock mode and finally again when the PLL lock bit is set. The resultant waveform can be captured on an oscilloscope and used to determine the typical lock time for the micro controller and the associated external application circuit.

e.g.
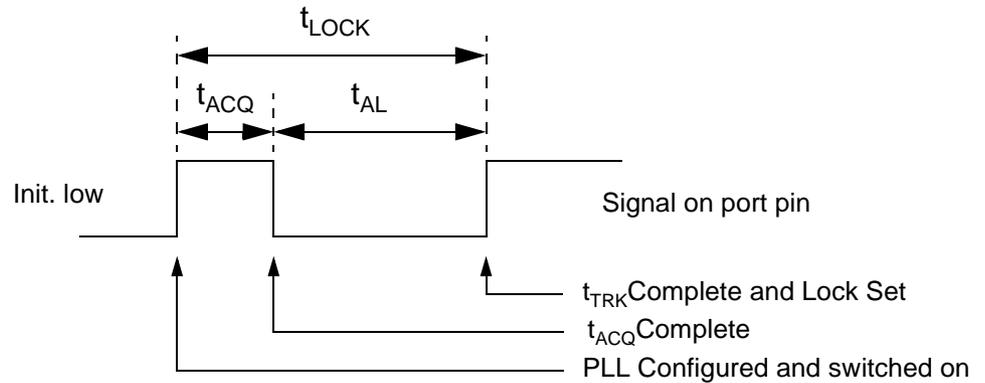
Electrical Specifications - CGM Acquisition/Lock Time information

The following additions have been made to the CGM Acquisition/Lock Time information on page 387 of the data book.

Description	Symbol	Min	Typ	Max	Unit
K value for automatic mode time to stable	K_{acq}	—	0.1	—	
K value for automatic mode stable to lock	K_{trk}	—	0.0015	—	
Automatic Lock Time	t_{LOCK}	—	1.7	25	ms

3. Conditions for typical and maximum values are for Run mode with f_{XCLK} = 8MHz, f_{BUSDES} = 8MHz, N = 4, L= 7, discharged C_F = 15nF, V_{DD} = 5V

4. Refer to Phase-Locked Loop (PLL) section for guidance on the use of the PLL.