MOTOROLA

Ayame

MC68HC705L26 (菖蒲) MCU

PRODUCT SPECIFICATION

Rev 0.3

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The MC68HC705L26 is an MCU device in a 48-pin QFP package with the HC05 CPU core, a 24x4/25x3 LCD Driver, an SPI, a Pulse Width Counter, IR Carrier output, 16-bit Event Counter, dual on-chip oscillators, a COP watchdog timer, a 2-channel A/D converter, and total of 20 general purpose I/O port lines. The I/O port includes software programmable pull-ups and open drain outputs, and high current, high voltage outputs. The 8 K byte memory map has 6160 bytes of user EPROM and 176 bytes of user RAM.

CHANGES MADE IN REVISION 0.3

- Fix various typo errors.
- Added missing STOP mode clock section.
- Changed RMO port output condition to include setting DDR.
- Removed references to AWOML bit and changed AWOMH name to AWOM
- Rewrote the LCD cycle frame equation.
- Changed the I_{DD} DC electrical spec.
- Buzzer clock is 2KHz and 4KHz at 2MHz bus clock
- (Eliminated Conditional Text; eps-> FM polygons)

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SECTION 1INTRODUCTION

The Motorola MC68HC705L26 is a member of M68HC05 family of low-cost microcontrollers (MCUs). A functional block diagram of the MC68HC705L26 is shown in **1.3**.

1.1 FEATURES

- Low cost, HC05 Core
- 48-pin QFP Package
- 6160 Bytes of User EPROM (including 16 Bytes of User Vectors)
- 176 Bytes of User RAM
- 24 x 4 or 25 x 3 Multiplexed LCD Driver
- 6-level Queued Pulse Width Counter
- Serial Peripheral Interface (SPI)
- 2 channel Analog to Digital Converter
- 16-bit Event Counter
- Time Base Timer
- COP Watchdog Timer
- IR Remote Carrier Output (software selectable 33-67% or 50-50% duty)
- Buzzer Output (software selectable frequencies)
- STOP Instruction Disable Option
- 20 Bidirectional I/O Lines including:
  4 Key Wake-up Input Lines
  Software Programmable Pull-ups
  Software Programmable Open Drain Lines
  High Voltage (9 V_{DC}), High Current (20 mA) Lines
- Software Selectable Sensitivity on IRQ Interrupt
  (Edge- and Level-Sensitive or Edge-Sensitive Only)
- On-Chip Dual 4MHz/32KHz (typ.) Oscillators
- Single-Chip, Self-Check, and Test Modes
- Power Saving STOP and WAIT Modes

1.2 MCU STRUCTURE

The overall block diagram of the MC68HC705L26 is shown in **1.3**.

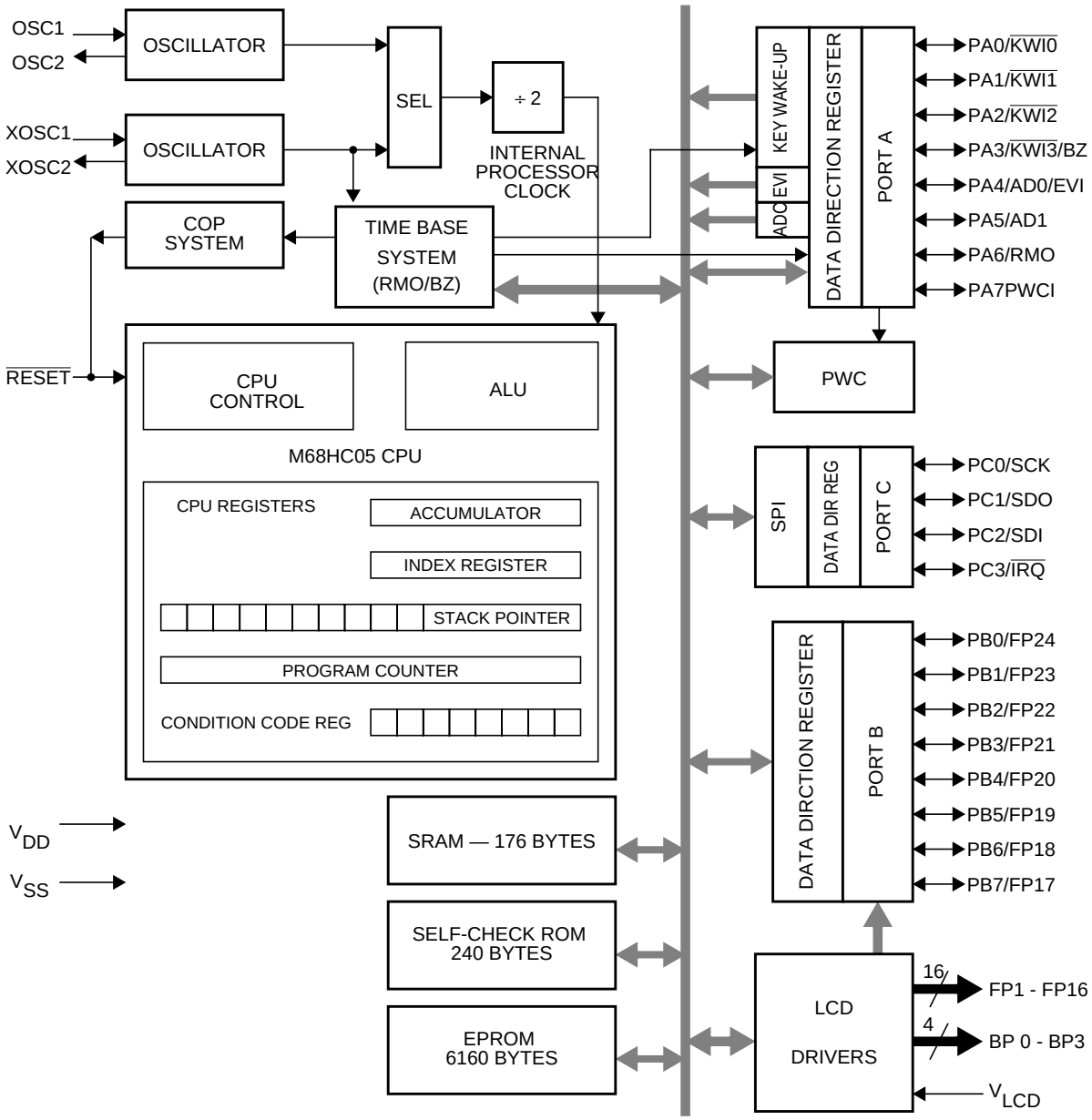

Figure 1-1: MC68HC705L26 Block Diagram

1.3 MASK OPTIONS

There are no Mask Options on the MC68HC705L26.

1.4 FUNCTIONAL PIN DESCRIPTION

NOTE: A line over a signal name indicates an active low signal. For example, RESET is active high and $\overline{\text{RESET}}$ is active low.
Any reference to voltage, current, resistance, capacitance, time, or frequency specified in the following sections will refer to the nominal values. The exact values and their tolerance or limits are specified in **SECTION 15.**

The MC68HC705L26 is available in the 48-pin QFP. The pin assignments for the package are shown in **Figure 1-2**.

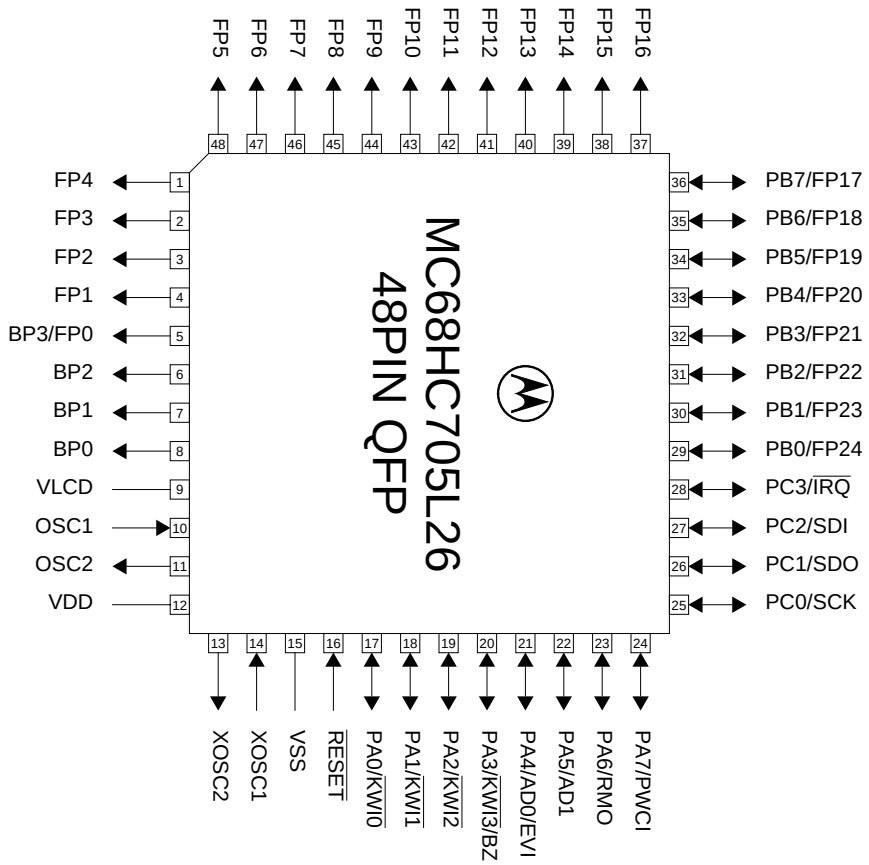

Figure 1-2: 48 QFP Single-Chip Mode Pinout

The following paragraphs describe the general function of each pin.

Table 1-1: Pin Configurations

Pin Nbr	Pin Name	I/O DIR
10	OSC1	I
11	OSC2	O
12	VDD	DC
13	XOSC2	O
14	XOSC1	I
15	VSS	DC
16	$\overline{\text{RESET}}$	I
17	PA0/$\overline{\text{KWI0}}$	IO
18	PA1/$\overline{\text{KWI1}}$	IO
19	PA2/$\overline{\text{KWI2}}$	IO
20	PA3/$\overline{\text{KWI3}}$/BZ	IO
21	PA4/AD0/EVI	IO
22	PA5/AD1	IO
23	PA6/RMO	IO
24	PA7/PWCI	IO
25	PC0/SCK	IO
26	PC1/SDO	IO
27	PC2/SDI	IO
28	PC3/$\overline{\text{IRQ}}$/VPP	IO

Pin Nbr	Pin Name	I/O DIR
29	PB0/FP24	IO
30	PB1/FP23	IO
31	PB2/FP22	IO
32	PB3/FP21	IO
33	PB4/FP20	IO
34	PB5/FP19	IO
35	PB6/FP18	IO
36	PB7/FP17	IO
37	FP16	O
38	FP15	O
39	FP14	O
40	FP13	O
41	FP12	O
42	FP11	O
43	FP10	O
44	FP9	O
45	FP8	O
46	FP7	O
47	FP6	O
48	FP5	O
1	FP4	O
2	FP3	O
3	FP2	O
4	FP1	O
5	BP3/FP0	O
6	BP2	O
7	BP1	O
8	BP0	O
9	VLCD	DC

1.4.1 VDD AND VSS

Power is supplied to the MCU through V_{DD} and V_{SS}. V_{DD} is the positive supply, and V_{SS} is ground. The MCU operates from a single power supply.

Very fast signal transitions occur on the MCU pins. The short rise and fall times place very high short-duration current demands on the power supply. To prevent noise problems, special care should be taken to provide good power supply bypassing at the MCU by using bypass capacitors with good high-frequency characteristics that are positioned as close to the MCU as possible. Bypassing requirements vary, depending on how heavily the MCU pins are loaded.

1.4.2 OSC1, OSC2

The OSC1 and OSC2 pins are the connections for the 2-pin on-chip oscillator. The OSC1 and OSC2 pins can accept the following sets of components:

1. A crystal as shown in **Figure 1-3(a)**
2. An external clock signal as shown in **Figure 1-3(b)**

The frequency, f_{OSC}, of the oscillator or external clock source is divided by two to produce the internal operating frequency, f_{OP}.

1.4.2.1 Crystal

The circuit in **Figure 1-3(a)** shows a typical 2-pin oscillator circuit for an AT-cut, parallel resonant crystal. The crystal manufacturer's recommendations should be followed, as the crystal parameters determine the external component values required to provide maximum stability and reliable start-up. The load capacitance values used in the oscillator circuit design should include all stray capacitances. The crystal and components should be mounted as close as possible to the pins for start-up stabilization and to minimize output distortion.

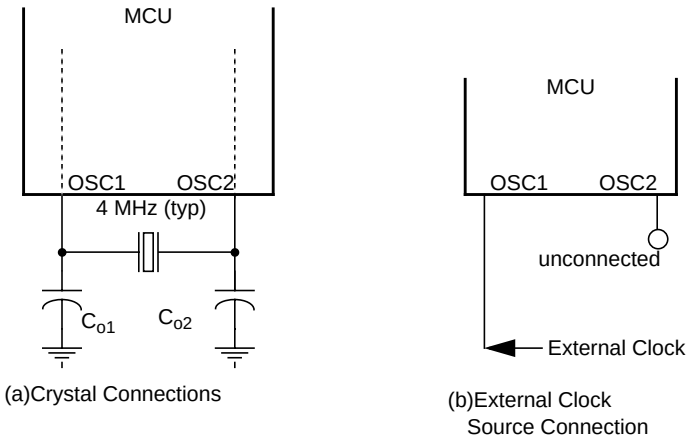

Figure 1-3: Oscillator Connections

1.4.2.2 External Clock

An external clock from another CMOS-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in **Figure 1-3(b)**. This configuration is possible regardless of the oscillator is setup.

1.4.3 XOSC1, XOSC2

The XOSC1 and XOSC2 pins are the connections for the 2-pin on-chip oscillator. The XOSC1 and XOSC2 pins can accept the following sets of components:

1. A crystal as shown in **Figure 1-4(a)**
2. An external clock signal as shown in **Figure 1-4(b)**

The frequency, f_{OSC}, of the oscillator or external clock source is divided by two to produce the internal operating frequency, f_{OP}.

1.4.3.1 Crystal

The circuit in **Figure 1-4(a)** shows a typical 2-pin oscillator circuit for an AT-cut, parallel resonant crystal. The crystal manufacturer's recommendations should be followed, as the crystal parameters determine the external component values required to provide maximum stability and reliable start-up. The load capacitance values used in the oscillator circuit design should include all stray capacitances. The crystal and components should be mounted as close as possible to the pins for start-up stabilization and to minimize output distortion.

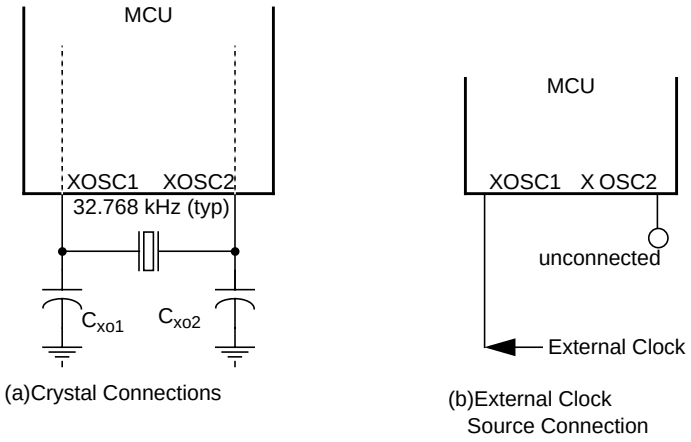

Figure 1-4: Oscillator Connections

1.4.3.2 External Clock

An external clock from another CMOS-compatible device can be connected to the XOSC1 input, with the XOSC2 input not connected, as shown in **Figure 1-4(b)**. This configuration is possible regardless of the oscillator is setup.

1.4.4 $\overline{\text{RESET}}$

This pin can be used as an input to reset the MCU to a known start-up state by pulling it to the low state. The $\overline{\text{RESET}}$ pin contains a steering diode to discharge any voltage on the pin

to V_{DD}, when the power is removed. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger to improve its noise immunity as an input. Refer to **SECTION 5**.

1.4.5 PA0:PA2/$\overline{\text{KWI0}}$:$\overline{\text{KWI2}}$, PA3/$\overline{\text{KWI3}}$/BZ, PA4/AD0/EVI, PA5/ADI, PA6/RMO, PA7/PWCI

Port A is a 8 bit I/O port. The state of any pin is software programmable and all Port A lines are configured as inputs during power-on or reset. Bits 0:3 is shared with the Key Wake-up Subsystem, and bit 3 is also shared with Buzzer Subsystem. Bit 4 is shared with A/D Converter and Event Counter. Bit 5 is shared with A/D Converter. Bit 6 is shared with IR Remote Output. Bit 7 is shared with the Pulse Counter Subsystem. See **SECTION 7** for more details on the I/O ports.

1.4.6 PC0/SCK, PC1/SDO, PC2/SDI, PC3/$\overline{\text{IRQ}}$

These four I/O lines comprise Port C. Bits 0 thru 2 are shared with the SPI subsystem. Bit 3 is shared with the $\overline{\text{IRQ}}$ input. The state of any pin is software programmable and all Port C lines are configured as port inputs during power-on or reset. Each Port C pins may be configured with a pull-up resistor by a software option. SPI output pins SCK and SDO may be configured as open drain output by a software option. See **SECTION 7** for more details on the I/O ports. The PC3/IRQ pin is used for special mode entry. Do not apply voltages above VDD for normal single chip mode operation. See **SECTION 15** for more details.

1.4.7 PB0:PB7/FP24:FP17

These eight I/O lines comprise Port B. The state of any pin is software programmable and all bits are configured as LCD output during power-on or reset. These bits are shared with LCD Front Plane drivers. See **SECTION 7** for more details on the I/O ports.

1.4.8 VLCD

This pin provides offset to LCD driver bias for adjusting the contrast of LCD. See **SECTION 11** for additional information.

1.4.9 BP3/FP0, FP1:FP18, PB0:PB7/FP24:FP17

There are 25 front plane drivers for the LCD display. Front Planes 17 thru 24 are shared with Port B bit 7 thru 0, respectively. Front Plane 0 is shared with Back Plane 3. See **SECTION 11** for additional information.

1.4.10 BP0:BP2, BP3/FP0

There are 4 back plane drivers for the LCD display. Back Plane 3 is multiplexed with Front Plane 0. See **SECTION 11** for additional information.

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SECTION 2MEMORY MAP

2.1 SINGLE-CHIP MODE MEMORY MAP

When the MC68HC705L26 is in the Single-Chip Mode 80 bytes of I/O registers, 176 bytes of user RAM (including a 64 byte stack), 6144 bytes of user ROM, and 16 bytes of user vectors are available in the 8K memory map as shown in **2.2**.

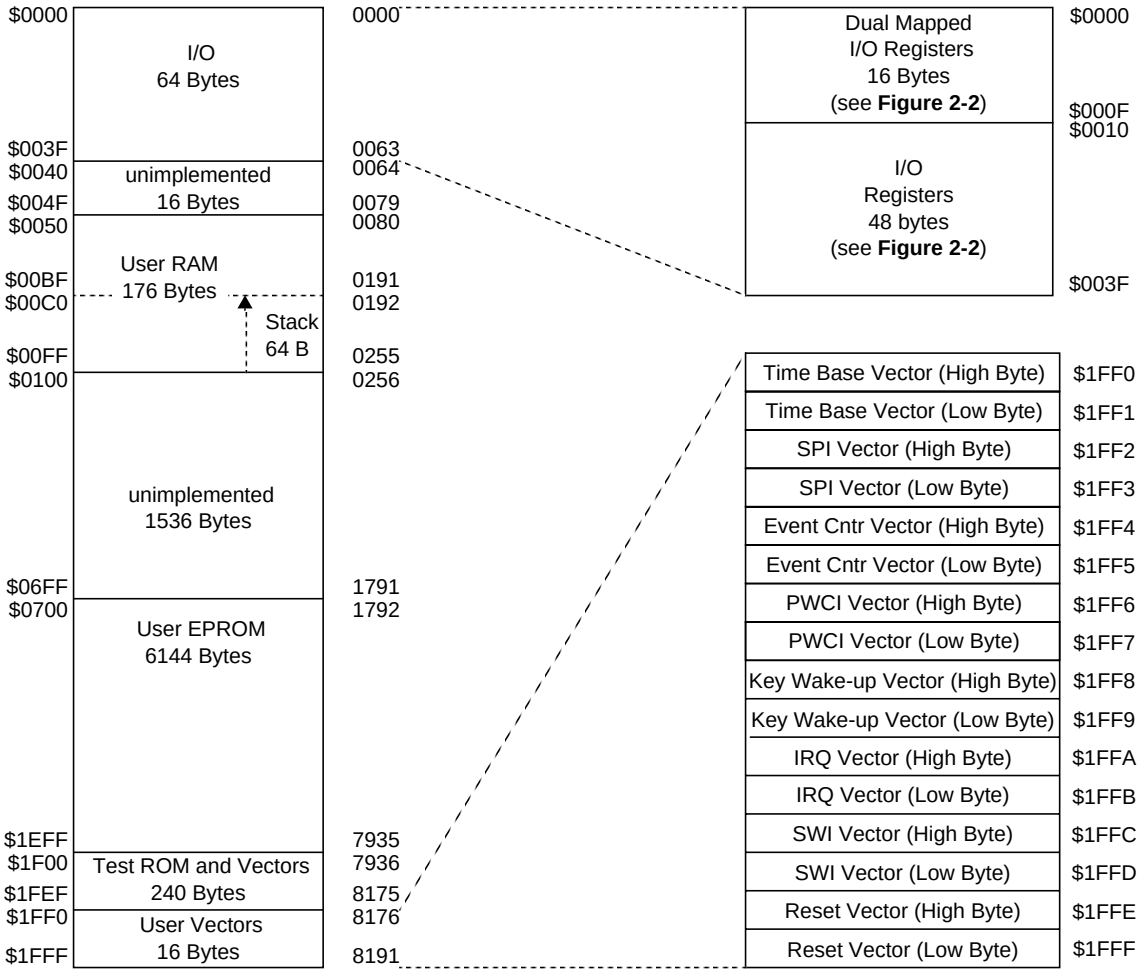

Figure 2-1: MC68HC705L26 Single-Chip Mode Memory Map

2.2 I/O AND CONTROL REGISTERS

The I/O and Control Registers reside in locations $0000-$003F. A summary of these registers is shown in **Figure 2-2**. The bit assignments for each register are shown in **Figure 2-3** thru **Figure 2-7**. Reading from unimplemented bits (denoted with '—') will return unknown states, and writing to unimplemented bits will be ignored.

Address locations $0000:$000F are dual mapped. When OPTM bit in the MISC register is cleared, main address map is accessed. When OPTM bit in the MISC register is set, option address map is accessed.

Addr	Name (Main Map Registers)
$0000	Port A Data Register
$0001	Port B Data Register
$0002	Port C Data Register
$0003	unimplemented
$0004	unimplemented
$0005	unimplemented
$0006	unimplemented
$0007	unimplemented
$0008	Interrupt Control Register
$0009	Interrupt Status Register
$000A	Serial Peripheral Control Register
$000B	Serial Peripheral Status Register
$000C	Serial Peripheral Data Register
$000D	Pulse Width Counter Control Register
$000E	Pulse Width Counter Status Register
$000F	Pulse Width Counter Data Register
$0010	TimeBase Control Register 1
$0011	TimeBase Control Register 2
$0012	unimplemented
$0013	unimplemented
$0014	unimplemented
$0015	unimplemented
$0016	unimplemented
$0017	unimplemented
$0018	unimplemented
$0019	unimplemented
$001A	unimplemented
$001B	unimplemented
$001C	unimplemented
$001D	A/D Data Register
$001E	A/D Control/Status Register
$001F	TimeBase Control Register 3
$0020	LCD Control Register
$0021	LCD Data Register 1
$0022	LCD Data Register 2
$0023	LCD Data Register 3
$0024	LCD Data Register 4
$0025	LCD Data Register 5
$0026	LCD Data Register 6
$0027	LCD Data Register 7

Addr	Name
$0028	LCD Data Register 8
$0029	LCD Data Register 9
$002A	LCD Data Register 10
$002B	LCD Data Register 11
$002C	LCD Data Register 12
$002D	LCD Data Register 13
$002E	Event Counter Control/Status Register
$002F	Event Counter Timing Register
$0030	Event Counter Data High Register
$0031	Event Counter Data Low Register
$0032	unimplemented
$0033	unimplemented
$0034	unimplemented
$0035	unimplemented
$0036	unimplemented
$0037	unimplemented
$0038	unimplemented
$0039	unimplemented
$003A	unimplemented
$003B	unimplemented
$003C	unimplemented
$003D	reserved
$003E	Miscellaneous Register
$003F	unimplemented

OPTN Addr	Name (Option Map Registers)
$0000	Port A Data Direction Register
$0001	Port B Data Direction Register
$0002	Port C Data Direction Register
$0003	unimplemented
$0004	unimplemented
$0005	unimplemented
$0006	unimplemented
$0007	unimplemented
$0008	Resistor Control Register
$0009	Resistor Control Register
$000A	Wired-OR Mode Register
$000B	unimplemented
$000C	unimplemented
$000D	unimplemented
$000E	Key Wake-up Input Enable Register
$000F	Mask Option Status Register

Figure 2-2: I/O Register Memory Map Summary

ADDR (hex)	REGISTER NAME ABBREV.	READ WRITE	Bit Number Significance							
			7	6	5	4	3	2	1	0
$0000	PORT A DATA PORTA	R	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		W								
$0001	PORT B DATA PORTB	R	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		W								
$0002	PORT C DATA PORTC	R	0	0	0	0	PC3	PC2	PC1	PC0
		W	—	—	—	—				
$0003	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0004	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0005	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0006	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0007	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0008	INTERRUPT CONTROL REG. INTCR	R	IRQE	0	0	KWIE	IRQS	0	0	0
		W		—	—			—	—	—
$0009	INTERRUPT STATUS REG. INTSR	R	IRQF	0	0	KWIF	0	0	0	0
		W	—	—	—	—	RIRQ	—	—	RKWIF
$000A	SERIAL PERI. CONTROL REG SPCR	R	SPIE	SPE	DORD	MSTR	0	0	0	SPR
		W					—	—	—	
$000B	SERIAL PERI. STATUS REG SPSR	R	SPIF	DCOL	0	0	0	0	0	0
		W	—	—	—	—	—	—	—	—
$000C	SERIAL PERI. DATA REG SPDR	R	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
		W								
$000D	PWC CONTROL REGISTER PWCCR	R	PWCE	EM	IS	POL	CCK1	CCK0	NCK1	NCK0
		W								
$000E	PWC STATUS REGISTER PWCSR	R	PL	SIG	PWCIE	COVF	PWCIF	QOR	QFUL	QEMP
		W	—	—		—	—	—	—	—
$000F	PWC DATA REGISTER PWCDR	R	PWC7	PWC6	PWC5	PWC4	PWC3	PWC2	PWC1	PWC0
		W	—	—	—	—	—	—	—	—

Figure 2-3: I/O Register $0000:$000F (Main Map)

ADDR (hex)	REGISTER NAME ABBREV.	READ WRITE	Bit Number Significance							
			7	6	5	4	3	2	1	0
OPTN $0000	PORT A DATA DIRECTION DDRA	R	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		W								
OPTN $0001	PORT B DATA DIRECTION DDRB	R	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		W								
OPTN $0002	PORT C DATA DIRECTION DDRC	R	0	0	0	0	DDRC3	DDRC2	DDRC1	DDRC0
		W	—	—	—	—				
OPTN $0003	unimplemented	R	—	—	—	—	—	—	—	—
		W								
OPTN $0004	unimplemented	R	—	—	—	—	—	—	—	—
		W								
OPTN $0005	unimplemented	R	—	—	—	—	—	—	—	—
		W								
OPTN $0006	unimplemented	R	—	—	—	—	—	—	—	—
		W								
OPTN $0007	unimplemented	R	—	—	—	—	—	—	—	—
		W								
OPTN $0008	RESISTOR CONTROL REG. RCR1	R	0	0	0	0	RBH	RBL	RAH	RAL
		W	—	—	—	—				
OPTN $0009	RESISTOR CONTROL REG. RCR2	R	0	0	0	0	0	0	0	RC
		W	—	—	—	—	—	—	—	
OPTN $000A	WIRED-OR MODE REG WOMR	R	BWOMH	BWOML	0	0	0	CWOM	AWOM	0
		W			—	—	—			—
OPTN $000B	unimplemented	R	—	—	—	—	—	—	—	—
		W								
OPTN $000C	unimplemented	R	—	—	—	—	—	—	—	—
		W								
OPTN $000D	unimplemented	R	—	—	—	—	—	—	—	—
		W								
OPTN $000E	KEY WAKE-UP INPUT ENABLE KWIEN	R	0	0	0	0	KWIE3	KWIE2	KWIE1	KWIE0
		W	—	—	—	—				
OPTN $000F	MASK OPTION STATUS REG MOSR (see notes)	R	RSTR	OSCR	XOSCR	STOPD	0	0	0	0
		W	—	—	—	—	—	—	—	—

Figure 2-4: I/O Register $0000:$000F (Option Map)

Note:
1. Mask Option Status Register is available for MC68HC05L25 only.

ADDR (hex)	REGISTER NAME ABBREV.	READ WRITE	Bit Number Significance							
			7	6	5	4	3	2	1	0
$0010	TIME BASE CONTROL REG 1 TBCR1	R	TBCLK	0	LCLK	RMC4	RMC3	RMC2	RMC1	RMC0
		W		—						
$0011	TIME BASE CONTROL REG 2 TBCR2	R	TBIF	TBIE	TBR1	TBR0	0	0	COPE	0
		W	—				RTBIF	—		COPC
$0012	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0013	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0014	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0015	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0016	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0017	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0018	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0019	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$001A	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$001B	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$001C	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$001D	A/D DATA REGISTER ADDR	R	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		W	—	—	—	—	—	—	—	—
$001E	A/D STATUS/CONTROL REG ADSCR	R	CC	ADRC	ADON	0	0	CH2	CH1	CH0
		W	—			—	—			
$001F	TIME BASE CONTROL REG 3 TBCR3	R	0	RMON	RPOL	RMPE	BCLK	BZON	BPOL	BZPE
		W	—							

Figure 2-5: I/O Register $0010:$001F

ADDR (hex)	REGISTER NAME ABBREV.	READ WRITE	Bit Number Significance							
			7	6	5	4	3	2	1	0
$0020	LCD CONTROL REG LCDCR	R	LCDE	PBEH	DUTY	PBEL	0	0	FC	LC
		W					—	—		
$0021	LCD DATA REGISTER LDAT1	R	F1B3	F1B2	F1B1	F1B0	F0B3	F0B2	F0B1	F0B0
		W								
$0022	LCD DATA REGISTER LDAT2	R	F3B3	F3B2	F3B1	F3B0	F2B3	F2B2	F2B1	F2B0
		W								
$0023	LCD DATA REGISTER LDAT3	R	F5B3	F5B2	F5B1	F5B0	F4B3	F4B2	F4B1	F4B0
		W								
$0024	LCD DATA REGISTER LDAT4	R	F7B3	F7B2	F7B1	F7B0	F6B3	F6B2	F6B1	F6B0
		W								
$0025	LCD DATA REGISTER LDAT5	R	F9B3	F9B2	F9B1	F9B0	F8B3	F8B2	F8B1	F8B0
		W								
$0026	LCD DATA REGISTER LDAT6	R	F11B3	F11B2	F11B1	F11B0	F10B3	F10B2	F10B1	F10B0
		W								
$0027	LCD DATA REGISTER LDAT7	R	F13B3	F13B2	F13B1	F13B0	F12B3	F12B2	F12B1	F12B0
		W								
$0028	LCD DATA REGISTER LDAT8	R	F15B3	F15B2	F15B1	F15B0	F14B3	F14B2	F14B1	F14B0
		W								
$0029	LCD DATA REGISTER LDAT9	R	F17B3	F17B2	F17B1	F17B0	F16B3	F16B2	F16B1	F16B0
		W								
$002A	LCD DATA REGISTER LDAT10	R	F19B3	F19B2	F19B1	F19B0	F18B3	F18B2	F18B1	F18B0
		W								
$002B	LCD DATA REGISTER LDAT11	R	F21B3	F21B2	F21B1	F21B0	F20B3	F20B2	F20B1	F20B0
		W								
$002C	LCD DATA REGISTER LDAT12	R	F23B3	F23B2	F23B1	F23B0	F22B3	F22B2	F22B1	F22B0
		W								
$002D	LCD DATA REGISTER LDAT13	R	0	0	0	0	F24B3	F24B2	F24B1	F24B0
		W	—	—	—	—				
$002E	EVENT CNTR STAT/CONT REG EVSCR	R	EVCE	EVIE	EVOE	EVIF	EVOF	0	0	0
		W				—	—	RCCF	ROFF	—
$002F	EVENT COUNTER TIMING REG EVTR	R	WT3	WT2	WT1	WT0	MT3	MT2	MT1	MT0
		W								

Figure 2-6: I/O Register $0020:$002F

ADDR (hex)	REGISTER NAME ABBREV.	READ WRITE	Bit Number Significance							
			7	6	5	4	3	2	1	0
$0030	EVENT CNTR DATA REG H EVDH	R	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
		W								
$0031	EVENT CNTR DATA REG L EVDL	R	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W								
$0032	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0033	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0034	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0035	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0036	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0037	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0038	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$0039	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$003A	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$003B	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$003C	unimplemented	R	—	—	—	—	—	—	—	—
		W								
$003D	reserved	R	—	—	—	—	—	—	—	—
		W								
$003E	MISCELLANEOUS REGISTER MISC	R	FTUP	STUP	0	0	SYS1	SYS0	FOSCE	OPTM
		W	—	—	—	—				
$003F	unimplemented	R	—	—	—	—	—	—	—	—
		W								

Figure 2-7: I/O Register $0030:$003F

2.3 RAM

The user RAM consists of 176 bytes (including the stack) at locations $0050 thru $00FF. The stack can access 64 locations begins at address $00FF and proceeds down to $00C0.

NOTE: Using the stack area for data storage or temporary work locations requires care to prevent it from being overwritten due to stacking from an interrupt or subroutine call.

2.4 ROM

There are a total of 6160 bytes of ROM on chip. These are implemented as 6144 bytes of user ROM at locations $0700 thru $1EFF and 16 bytes of user vectors at locations $1FF0 thru $1FFF. Total of 240 bytes of Test ROM and vectors are located from $1F00 thru $1FEF.

SECTION 3OPERATING MODES

The MC68HC705L26 has three modes of operation that affect the pin-out and architecture of the MCU: Single-Chip Mode, Internal Test Mode, and Expanded Test Mode. The Single-Chip Modes will normally be used, and the Test Modes are required for the special needs of production test and burn-in.

3.1 SINGLE-CHIP MODE

The Single-Chip Mode allows the MCU to function as a self-contained microcontroller, with maximum use of the pins for on-chip peripheral functions. The pinout for the Single-Chip Mode is shown in **Figure 1-2**.

In the Single-Chip Mode all address and data activity occurs within the MCU and is not available externally.

3.2 TEST MODES

The Internal Test Mode and Expanded Test Mode are reserved for factory test.

3.3 LOW-POWER MODES

In each of its configuration modes the MC68HC705L26 is capable of running in one of two low-power operational modes. The WAIT and STOP instructions provide two modes that reduce the power required for the MCU by stopping various internal clocks and/or the on-chip oscillator. The STOP and WAIT instructions are not normally used if the COP Watchdog Timer is enabled. The flow of the STOP and WAIT modes is shown in **Figure 3-1**.

3.3.1 STOP INSTRUCTION

Execution of the STOP instruction places the MCU in its lowest power consumption mode. In the STOP Mode the internal oscillator is turned off, halting *all* internal processing, except the Time Base/COP Watchdog Timer if it is enabled and clocked from XOSC.

Execution of the STOP instruction automatically clears the I-bit in the Condition Code Register. All other registers, and memory remain unaltered. All input/output lines remain unchanged. Therefore, unused ports must be programmed as output or tied to the power rails to prevent excessive current consumption.

The MCU can be brought out of the STOP Mode by an external IRQ interrupt, KWI interrupt, SPI (slave mode only) interrupt, PWC or TBI interrupt clocked by XOSC, or a RESET.

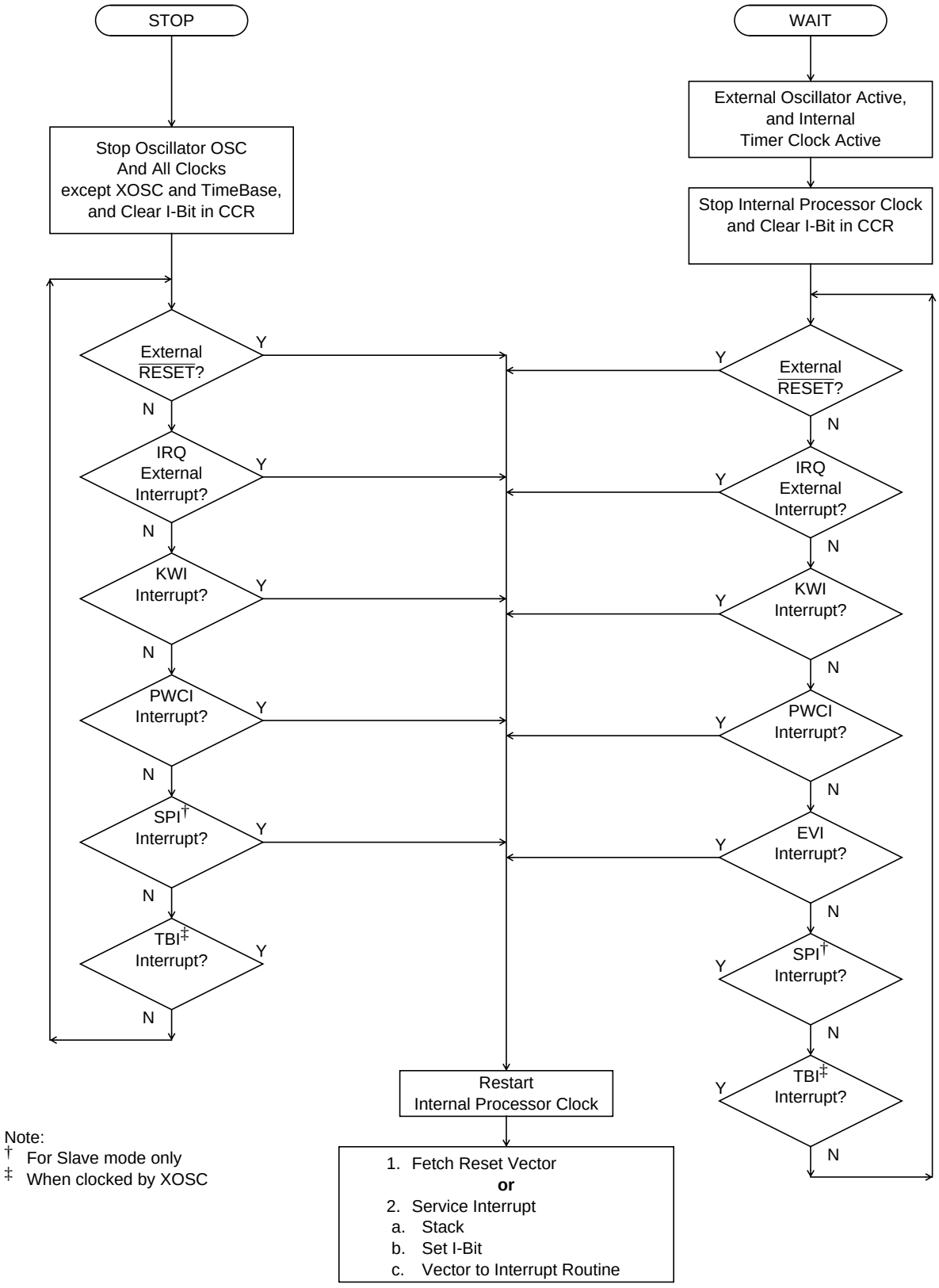

Figure 3-1: STOP/WAIT Flowcharts

3.3.2 WAIT INSTRUCTION

The WAIT instruction places the MCU in a low-power mode, which consumes more power than the STOP Mode. In the WAIT Mode the internal processor clock is halted, suspending all processor and internal bus activity. Internal timer clocks remain active, permitting interrupts to be generated from the timer or a reset to be generated from the COP Watchdog Timer. Execution of the WAIT instruction automatically clears the I-bit in the Condition Code Register and external interrupt is allowed. All other registers, memory, and input/output lines remain in their previous states.

If Time Base interrupts are enabled, a Time Base interrupt will cause the processor to exit the WAIT Mode and resume normal operation. The Time Base may be used to generate a periodic exit from the WAIT Mode. The WAIT Mode may also be exited when an external interrupt ($\overline{\text{IRQ}}$) or RESET occurs.

3.4 COP WATCHDOG TIMER CONSIDERATIONS

The COP Watchdog Timer is active in all modes of operation if enabled by an TBCR2 select bit. If the COP Watchdog Timer is selected by the TBCR2 bit, any execution of the STOP instruction (either intentional or inadvertent due to the CPU being disturbed) will cause the oscillator (OSC) to halt and thus the COP Watchdog Timer will not time out if driven from OSC. Thus for applications that require use of COP Watchdog from OSC, STOP instruction must be disabled, or COP must be driven from XOSC.

If the COP Watchdog Timer is selected by the TBCR2 select bit, the COP will reset the MCU when it times out. Therefore, it is recommended that the COP Watchdog should be **disabled** for a system that must have intentional uses of the WAIT or STOP Modes for periods longer than the COP timeout period.

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SECTION 4CPU CORE

The MC68HC705L26 has an 8 K memory map. Therefore it uses 13 bits of the address bus.

4.1 REGISTERS

The MCU contains five registers which are hard-wired within the CPU and are not part of the memory map. These five registers are shown in **Figure 4-1** and are described in the following paragraphs.

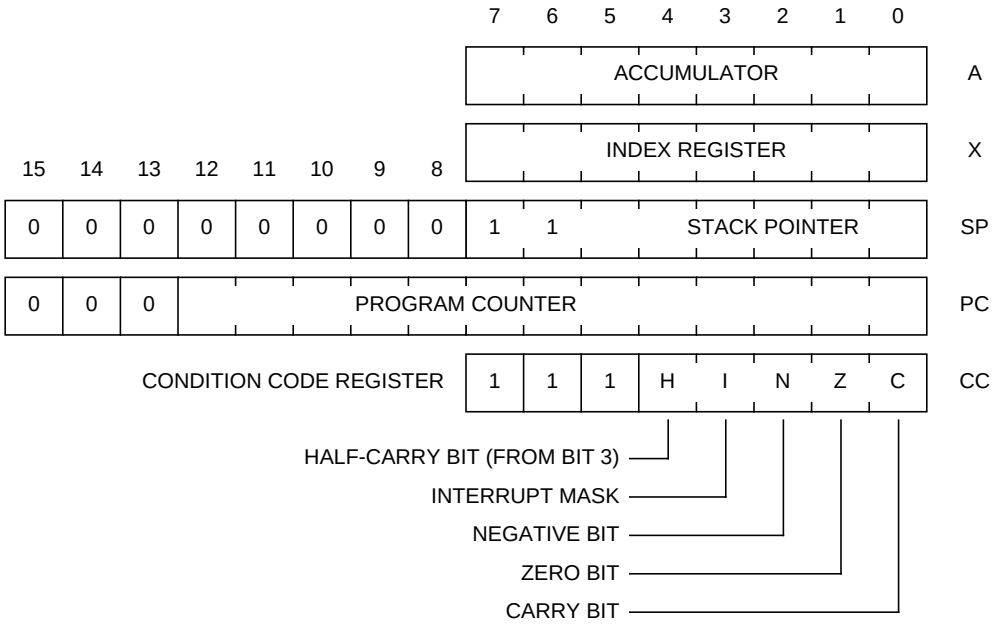

Figure 4-1: M68HC05 Programming Model

4.1.1 ACCUMULATOR (A)

The accumulator is a general purpose 8-bit register as shown in **Figure 4-1**. The CPU uses the accumulator to hold operands and results of arithmetic calculations or non-arithmetic operations. The accumulator is unaffected by a reset of the device.

4.1.2 INDEX REGISTER (X)

The index register shown in **Figure 4-1** is an 8-bit register that can perform two functions:

- Indexed addressing
- Temporary storage

In indexed addressing with no offset, the index register contains the low byte of the operand address, and the high byte is assumed to be $00. In indexed addressing with an 8-bit offset, the CPU finds the operand address by adding the index register contents to an 8-bit immediate value. In indexed addressing with a 16-bit offset, the CPU finds the operand address by adding the index register contents to a 16-bit immediate value

The index register can also serve as an auxiliary accumulator for temporary storage.The index register is unaffected by a reset of the device.

4.1.3 STACK POINTER (SP)

The stack pointer shown in **Figure 4-1** is a 16-bit register internally. In devices with memory maps less than 64 K bytes the unimplemented upper address lines are ignored. The stack pointer contains the address of the next free location on the stack. During a reset or the reset stack pointer (RSP) instruction, the stack pointer is set to $00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the ten most significant bits are permanently set to 0000000011. The five least significant register bits are appended to these eleven fixed bits to produce an address within the range of $00FF to $00C0. Subroutines and interrupts may use up to 64 ($40) locations. If 64 locations are exceeded, the stack pointer wraps around and writes over the previously stored information. A subroutine call occupies two locations on the stack; and an interrupt uses five locations.

4.1.4 PROGRAM COUNTER (PC)

The program counter shown in **Figure 4-1** is a 16-bit register internally. In devices with memory maps less than 64 K bytes the unimplemented upper address lines are ignored, and memory image is mirrored. The program counter contains the address of the next instruction or operand to be fetched.

Normally, the address in the program counter increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, and interrupt operations load the program counter with an address other than that of the next sequential location.

4.1.5 CONDITION CODE REGISTER (CCR)

The CCR shown in **Figure 4-1** is a 5-bit register in which four bits are used to indicate the results of the instruction just executed. The fifth bit is the interrupt mask. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. The condition code register should be thought of as having three additional upper bits that are always ones. Only the interrupt mask is affected by a reset of the device. The following paragraphs explain the functions of the lower five bits of the condition code register.

4.1.5.1 Half Carry Bit (H-Bit)

When the half-carry bit is set, it means that a carry occurred between bits 3 and 4 of the accumulator during the last ADD or ADC (add with carry) operation. The half-carry bit is required for binary-coded decimal (BCD) arithmetic operations.

4.1.5.2 Interrupt Mask (I-Bit)

When the interrupt mask is set, the internal and external interrupts are disabled. Interrupts are enabled when the interrupt mask is cleared. When an interrupt occurs, the interrupt mask is automatically set after the CPU registers are saved on the stack, but before the interrupt vector is fetched. If an interrupt request occurs while the interrupt mask is set, the

interrupt request is latched. Normally, the interrupt is processed as soon as the interrupt mask is cleared.

A return from interrupt (RTI) instruction pulls the CPU registers from the stack, restoring the interrupt mask to its state before the interrupt was encountered. After any reset, the interrupt mask is set and can only be cleared by the Clear I-Bit (CLI), STOP, or WAIT instructions.

4.1.5.3 Negative Bit (N-Bit)

The negative bit is set when the result of the last arithmetic operation, logical operation, or data manipulation was negative. (Bit 7 of the result was a logical one.)

The negative bit can also be used to check an often-tested flag by assigning the flag to bit 7 of a register or memory location. Loading the accumulator with the contents of that register or location then sets or clears the negative bit according to the state of the flag.

4.1.5.4 Zero Bit (Z-Bit)

The zero bit is set when the result of the last arithmetic operation, logical operation, data manipulation, or data load operation was zero.

4.1.5.5 Carry/Borrow Bit (C-Bit)

The carry/borrow bit is set when a carry out of bit 7 of the accumulator occurred during the last arithmetic operation, logical operation, or data manipulation. The carry/borrow bit is also set or cleared during bit test and branch instructions and during shifts and rotates. This bit is not set by an INC or DEC instruction.

4.2 INSTRUCTION SET

The MCU has a set of 62 basic instructions. They can be divided into five different types: register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. For more information on the instruction set, refer to the M6805 Family User's Manual (M6805UM/AD2) or the associated MC68HC05 Data Sheet.

4.2.1 REGISTER/MEMORY INSTRUCTIONS

Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing

modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to the following instruction list.

Function	Mnemonic
Load A from Memory	LDA
Load X from Memory	LDX
Store A in Memory	STA
Store X in Memory	STX
Add Memory to A	ADD
Add Memory and Carry to A	ADC
Subtract Memory	SUB
Subtract Memory from A with Borrow	SBC
AND Memory to A	AND
OR Memory with A	ORA
Exclusive OR Memory with A	EOR
Arithmetic Compare A with Memory	CMP
Arithmetic Compare X with Memory	CPX
Bit Test Memory with A (Logical Compare)	BIT
Jump Unconditional	JMP
Jump to Subroutine	JSR
Multiply	MUL

4.2.2 READ-MODIFY-WRITE INSTRUCTIONS

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read-modify-write sequence since it does not modify the value. Do not use these read-modify-write instructions on write-only locations. Refer to the following list of instructions.

Function	Mnemonic
Increment	INC
Decrement	DEC
Clear	CLR
Complement	COM
Negate (Two's Complement)	NEG
Rotate Left Thru Carry	ROL
Rotate Right Thru Carry	ROR
Logical Shift Left	LSL
Logical Shift Right	LSR
Arithmetic Shift Right	ASR
Test for Negative or Zero	TST

4.2.3 BRANCH INSTRUCTIONS

This set of instruction branches if a particular condition is met; otherwise, no operation is performed. Branch instructions are two-byte instructions. Refer to the following list for branch instructions.

Function	Mnemonic
Branch Always	BRA
Branch Never	BRN
Branch if Higher	BHI
Branch if Lower or Same	BLS
Branch if Carry Clear	BCC
Branch if Higher or Same	BHS
Branch if Carry Set	BCS
Branch if Lower	BLO
Branch if Not Equal	BNE
Branch if Equal	BEQ
Branch if Half Carry Clear	BHCC
Branch if Half Carry Set	BHCS
Branch if Plus	BPL
Branch if Minus	BMI
Branch if Interrupt Mask Bit is Clear	BMC
Branch if Interrupt Mask Bit is Set	BMS
Branch if Interrupt Line is Low	BIL
Branch if Interrupt Line is High	BIH
Branch to Subroutine	BSR

4.2.4 BIT MANIPULATION INSTRUCTIONS

The MCU is capable of setting or clearing any read/write bit which resides in the first 256 bytes of the memory space where all port registers, port DDRs, timer, timer control, and on-chip RAM reside. An additional feature allows the software to test and branch on the state of any bit within these 256 locations. The bit set, bit clear, and bit test and branch functions are each implemented with a single instruction. For test and branch instructions, the value of the bit tested is also placed in the carry bit of the condition code register. The bit set and bit clear instructions are also read-modify-write instructions and should not be used to manipulate write-only locations. Refer to the following list for bit manipulation instructions.

Function	Mnemonic
Set Bit n	BSET n (n = 0. . .7)
Clear Bit n	BCLR n (n = 0. . .7)
Branch if Bit n is Set	BRSET n (n = 0. . .7)
Branch if bit n is Clear	BRCLR n (n = 0. . .7)

4.2.5 CONTROL INSTRUCTIONS

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to the following list for control instructions.

Function	Mnemonic
Transfer A to X	TAX
Transfer X to A	TXA
Set Carry Bit	SEC
Clear Carry Bit	CLC
Set Interrupt Mask Bit	SEI
Clear Interrupt Mask Bit	CLI
Software Interrupt	SWI
Return from Subroutine	RTS
Return from Interrupt	RTI
Reset Stack Pointer	RSP
No-Operation	NOP
Stop	STOP
Wait	WAIT

4.3 ADDRESSING MODES

The MCU uses ten different addressing modes to provide the programmer with an opportunity to optimize the code for all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables, and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions; the longest instructions (three bytes) permit accessing tables throughout memory. Short and long absolute addressing is also included. One- or two-byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory.

The term "effective address" (EA) is used in describing the various addressing modes. Effective address is defined as the address from which the argument for an instruction is fetched or stored.

4.3.1 IMMEDIATE

In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants that do not change during program execution (e.g., a constant used to initialize a loop counter).

4.3.2 DIRECT

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with single two-byte instructions.

4.3.3 EXTENDED

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode byte. Instructions with extended addressing mode are

capable of referencing arguments anywhere in memory with a single three-byte instruction. When using the Motorola assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the shortest form of the instruction.

4.3.4 RELATIVE

The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed offset byte (which is the last byte of the instruction) is added to the PC if, and only if, the branch conditions are true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from -128 to +127 from the address of the next opcode. The programmer need not calculate the offset when using the Motorola assembler, since it calculates the proper offset and checks to see that it is within the span of the branch.

4.3.5 INDEXED, NO OFFSET

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. This addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

4.3.6 INDEXED, 8-BIT OFFSET

In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. The addressing mode is useful for selecting the Kth element in an element table. With this two-byte instruction, K would typically be in X with the address of the beginning of the table in the instruction. As such, tables may begin anywhere within the first 256 addressable locations and could extend as far as location 510. $1FE is the highest location which can be accessed in this way.

4.3.7 INDEXED, 16-BIT OFFSET

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This address mode can be used in a manner similar to indexed, 8-bit offset except that this three-byte instruction allows tables to be anywhere in memory. As with direct and extended addressing, the Motorola assembler determines the shortest form of indexed addressing.

4.3.8 BIT SET/CLEAR

In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode specifies the direct address of the byte in which the specified bit is to be set or cleared. Any read/write register bit in the first 256 locations of memory, including I/O, can by selectively set or cleared with a single two-byte instruction.

4.3.9 BIT TEST AND BRANCH

The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit that is to be tested and its condition (set or clear), is included in the opcode. The address of the byte to be tested is in the single byte immediately following the opcode byte. The signed relative 8-bit offset in the third byte is added to the PC if the specified bit is set or cleared in the specified memory location. This single three-byte instruction allows the program to branch based on the condition of any readable bit in the first 256 locations of memory. The span of branching is from -128 to +127 from the address of the next opcode. The state of the tested bit is also transferred to the carry bit of the condition code register.

4.3.10 INHERENT

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register and/or accumulator as well as the control instructions with no other arguments are included in this mode. These instructions are one byte long.

SECTION 5RESETS

The MCU can be reset from following sources: one external input and two internal restart conditions. The $\overline{\text{RESET}}$ pin is an input with a Schmitt trigger as shown in **Figure 5-1**. All the peripheral modules which drive external pins will be reset by the synchronous reset signal (RST) coming from a latch, which is synchronized to the PH2 bus clock and set by the any of the five reset sources.

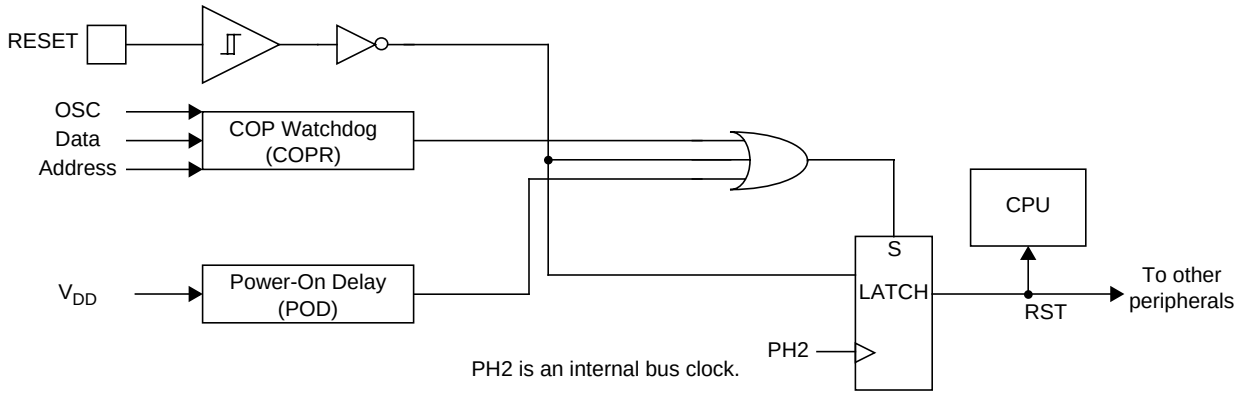

Figure 5-1: Reset Block Diagram

5.1 EXTERNAL RESET ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ pin is the only external source of a reset. This pin is connected to a Schmitt trigger input gate to provide an upper and lower threshold voltage separated by a minimum amount of hysteresis. This external reset occurs whenever the $\overline{\text{RESET}}$ pin is pulled below the lower threshold and remains in reset until the $\overline{\text{RESET}}$ pin rises above the upper threshold. This active low input will generate the RST signal and reset the CPU and peripherals. Termination of the external RESET input or the internal COP Watchdog reset are the only reset sources that can alter the operating mode of the MCU.

NOTE: Activation of the RST signal is generally referred to as reset of the device, unless otherwise specified.

5.2 INTERNAL RESETS

The two internally generated resets are the initial power-on delay function and the COP Watchdog Timer reset. Termination of the external RESET input or the internal COP Watchdog Timer are the only reset sources that can alter the operating mode of the MCU. The other internal resets will not have any effect on the mode of operation when their reset state ends.

5.2.1 POWER-ON DELAY (POD)

The internal POD is generated on power-up to allow the clock oscillator to stabilize. The POD is strictly for power turn-on conditions and is not able to detect a drop in the power supply voltage (brown-out). There is an oscillator stabilization delay of between 16128 to 16384 internal processor bus clock cycles (PH2) after the oscillator becomes active.

The POR will generate the RST signal which will reset the CPU. If any other reset function is active at the end of this 16128 to 16384 cycle delay, the RST signal will remain in the reset condition until the other reset condition(s) end.

5.2.2 COMPUTER OPERATING PROPERLY RESET (COPR)

The internal COPR reset is generated automatically (if enabled via a TBCR2 select bit) by a time-out of the COP Watchdog Timer. This time-out occurs if the counter in the COP Watchdog Timer is not reset (cleared) within a specific time by a program reset sequence. The COP Watchdog Timer can be disabled by a TBCR2 select bit. Refer to **Section 9.1.4** for more information on this timeout feature.

The COPR will generate the RST signal which will reset the CPU and other peripherals. If any other reset function is active at the end of the COPR reset signal, the RST signal will remain in the reset condition until the other reset condition(s) end.

SECTION 6INTERRUPTS

The MCU can be interrupted in the following ways:

1. Nonmaskable Software Interrupt Instruction (SWI)
2. External Interrupt via $\overline{\text{IRQ}}$ (IRQ)
3. Serial Peripheral Interface Interrupt (SPII)
4. Pulse Width Counter Interrupt (PWCI)
5. Internal Time Base Interrupt (TBI)
6. Key Wake-up Interrupt (KWI)
7. Event Counter Overflow Interrupt (EVOF)

6.1 CPU INTERRUPT PROCESSING

Interrupts cause the processor to save register contents on the stack and to set the interrupt mask (I-bit) to prevent additional interrupts. Unlike RESET, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction is complete.

If interrupts are not masked (I-bit in the CCR is clear) and the corresponding interrupt enable bit is set, the processor will proceed with interrupt processing. Otherwise, the next instruction is fetched and executed. If an interrupt occurs the processor completes the current instruction, then stacks the current CPU register states, sets the I-bit to inhibit further interrupts, and finally checks the pending hardware interrupts. If more than one interrupt is pending following the stacking operation, the interrupt with the highest vector location shown in **Table 6-1** will be serviced first. The SWI is executed the same as any other instruction, regardless of the I-bit state.

When an interrupt is to be processed the CPU fetches the address of the appropriate interrupt software service routine from the vector table at locations $1FF0 thru $1FFF as defined in **Table 6-1**.

Table 6-1: Vector Address for Interrupts and Reset

Register	Flag Name	Interrupts	CPU Interrupt	Vector Address
N/A	N/A	Reset	RESET	$1FFE:$1FFF
N/A	N/A	Software	SWI	$1FFC:$1FFD
INTCR	IRQF	External Interrupt	IRQ	$1FFA:$1FFB
KWIEN	KWIF	Key Wake-up	KWI	$1FF8:$1FF9
PWSR	PWCF	Pulse Width Counter	PWCI	$1FF6:$1FF7
EVSCR	ECOF	Event Counter	EVI	$1FF4:$1FF5
SPSR	SPIF	Serial Peripheral	SPII	$1FF2:$1FF3
TBCR2	TBIF	Time Base Periodical	TBI	$1FF0:$1FF1

An RTI instruction is used to signify when the interrupt software service routine is completed. The RTI instruction causes the register contents to be recovered from the stack and normal processing to resume at the next instruction that was to be executed when the interrupt took place. **Figure 6-1** shows the sequence of events that occur during interrupt processing.

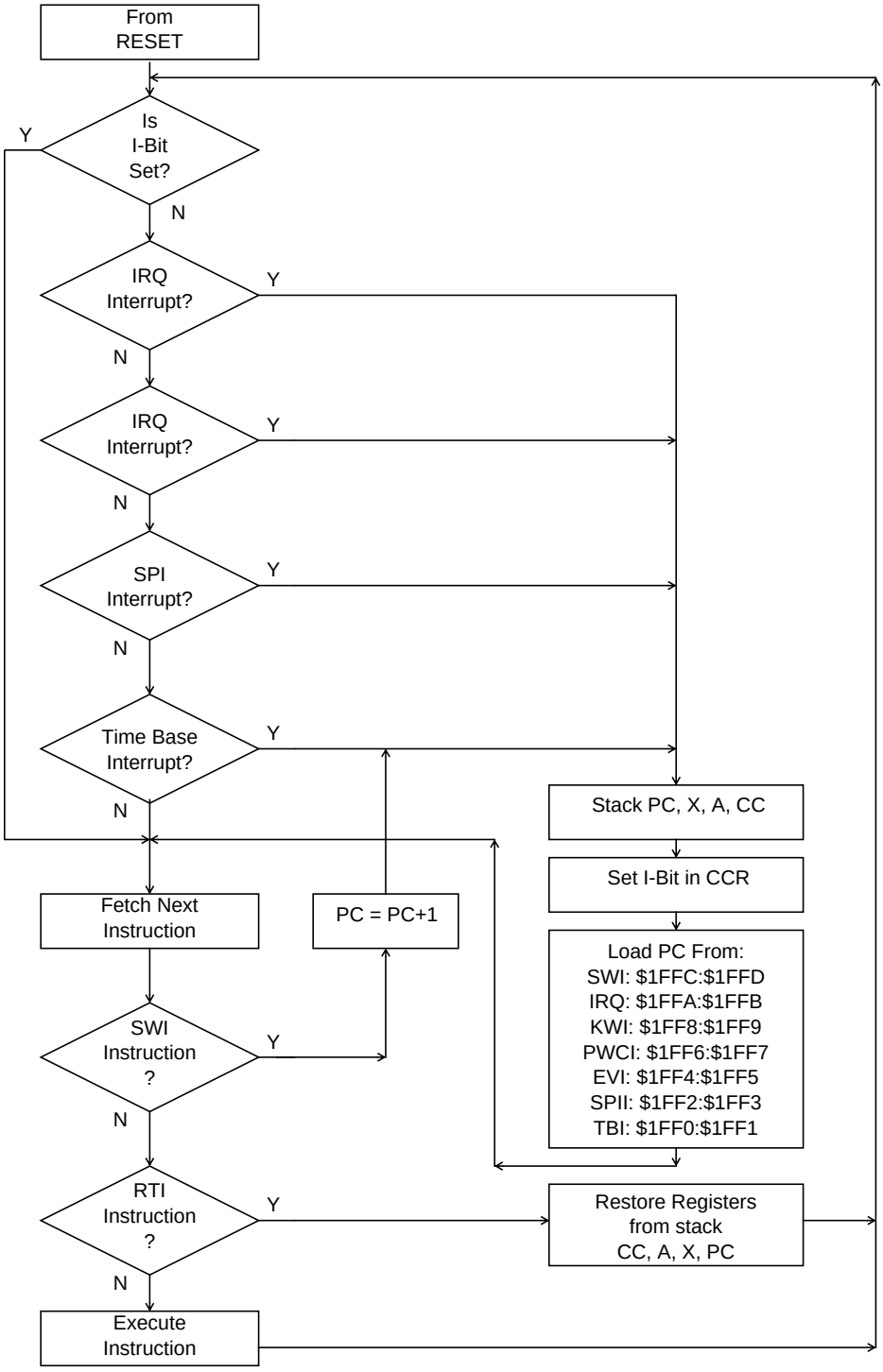

Figure 6-1: Interrupt Processing Flowchart

6.2 RESET INTERRUPT SEQUENCE

The RESET function is not in the strictest sense an interrupt; however, it is acted upon in a similar manner as shown in **Figure 6-1**. A low level input on the $\overline{\text{RESET}}$ pin or internally generated RST signal causes the program to vector to its starting address which is specified by the contents of memory locations $1FFE:$1FFF. The I-bit in the condition code register is also set. The MCU is configured to a known state during this type of reset as previously described in **SECTION 5**.

6.3 SOFTWARE INTERRUPT (SWI)

The SWI is an executable instruction and a non-maskable interrupt since it is executed regardless of the state of the I-bit in the CCR. If the I-bit is zero (interrupts enabled), the SWI instruction executes after interrupts which were pending before the SWI was fetched, or before interrupts generated after the SWI was fetched. The interrupt service routine address is specified by the contents of memory locations $1FFC:$1FFD.

6.4 HARDWARE INTERRUPTS

All hardware interrupts except RESET are maskable by the I-bit in the CCR. If the I-bit is set, all hardware interrupts (internal and external) are disabled. Clearing the I-bit enables the hardware interrupts. There are two types of hardware interrupts which are explained in the following sections.

6.5 EXTERNAL INTERRUPT ($\overline{\text{IRQ}}$)

The IRQ pin provides an asynchronous interrupt to the CPU. The IRQ is enabled by the IRQE bit in the INTCR. See also **Section 7.3**. The interrupt service routine address is specified by the contents of memory locations $1FFA:$1FFB.

CPU instructions BIH and BIL test the pin state of PC3/$\overline{\text{IRQ}}$ pin.

6.5.1 EXTERNAL INTERRUPT TRIGGER CONDITION

- External interrupt (IRQ) is activated by the negative edged signal.

The limit on the minimum pulse width (t_{ILIH}) is as specified. The pulse interval (t_{ILIL}) must be longer than the interrupt service routine's service time + 21 machine cycles.

6.5.2 INTERRUPT CONTROL REGISTER (INTCR)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$0008	INTERRUPT CONTROL REG. INTCR	R	IRQE	0	0	KWIE	IRQS	0	0	0
		W		—	—			—	—	—
		RESET:	0	0	0	0	0	0	0	0

Figure 6-2: Interrupt Control Register

IRQE External Interrupt (IRQ) Enable

IRQE bit enables external interrupt when interrupt mask is cleared and IRQF is set. This bit is cleared at reset.

1 = IRQ is enabled
0 = IRQ is disabled

BITS6:5 Reserved

These bits are not used and always return 0.

KWIE KWI Enable

KWIE bit enables Key Wake-up Interrupt when KWIF is set. The KWIEx bit in KWIEN bit must also be set for enabling KWI. This bit is cleared at reset.

1 = KWI is enabled
0 = KWI is disabled

IRQS External Interrupt (IRQ) Select edge sensitivity only

IRQS bit determines whether the LEVEL and EDGE or EDGE only will trigger the IRQ interrupt. This bit is cleared at reset.

1 = trigger only on negative EDGEs
0 = trigger on low LEVEL and negative EDGEs

BITS2:0 Reserved

These bits are not used and always return 0.

6.5.3 INTERRUPT STATUS REGISTER (INTSR)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$0009	INTERRUPT STATUS REG. INTSR	R	IRQF	0	0	KWIF	0	0	0	0
		W	—	—	—	—	RIRQF	—	—	RKWIF
RESET:			0	0	0	0	0	0	0	0

Figure 6-3: Interrupt Status Register

IRQF External Interrupt (IRQ) Flag

A falling edge at $\overline{IRQ}$ pin sets IRQF bit. If IRQE bit and this bit are set, and the interrupt mask is cleared, interrupt is generated. This bit is read only bit and clearing IRQF is accomplished by writing a 1 to the RIRQF bit. Reset clears this bit.

BITS6:5 Reserved

These bits are not used and always return 0.

KWIF Key Wake-up Interrupt Flag

When KWIEx bit in the KWIEN register is set, the falling edge at KWIx pin sets the KWIF bit. If KWIE bit and this bit are set, an interrupt is generated. This bit is a read only bit and clearing it is accomplished by writing a 1 to the RKWIF bit. Reset clears this bit.

RIRQF Reset IRQ Flag

The RIRQF bit is write only bit and always read as 0. Writing a 1 to this bit clears IRQF bit and writing 0 to this bit has no effect.

1 = clear IRQF
0 = no effect

BITS2:1 Reserved

These bits are not used and always return 0.

RKWIF Reset KWI Flag

The RKWIF bit is write only bit and always read as 0. Writing a 1 to this bit clears KWIF bit and writing 0 to this bit has no effect.

1 = clear KWIF
0 = no effect

6.6 PULSE WIDTH COUNTER INTERRUPT (PWCI)

The PWC interrupt is generated by the Pulse Width Counter System at the end of one pulse or every edge. The I-bit in the CCR must be clear and PWCIE bit in PWCR must be set in order for the PWC interrupt to be generated. This interrupt will vector to the interrupt service routine located at the address specified by the contents of memory locations The interrupt service routine address is specified by the contents of memory locations $1FF6:$1FF7. See **SECTION 12** for more information.

6.7 SERIAL PERIPHERAL INTERRUPT (SPII)

The SPI interrupt is generated by the Serial Peripheral Interface System at the end of one byte of data transmission or reception. The I-bit in the CCR must be clear and SPIE bit in SPCR must be set in order for the SPI interrupt to be generated. This interrupt will vector to the interrupt service routine located at the address specified by the contents of memory locations The interrupt service routine address is specified by the contents of memory locations $1FF2:$1FF3. See **SECTION 10** for more information.

6.8 EVENT COUNTER INTERRUPT (EVI)

The EVI interrupt is generated by the Event Counter System. The I-bit in the CCR must be clear in order for the EVI interrupt to be enabled. This interrupt will vector to the interrupt service routine located at the address specified by the contents of memory locations The interrupt service routine address is specified by the contents of memory locations $1FF4:$1FF5. See **SECTION 14** for more information.

6.9 TIME BASE INTERRUPT (TBI)

The TBI interrupt is generated periodically by the Time Base System. The I-bit in the CCR must be clear in order for the TBI interrupt to be enabled. This interrupt will vector to the interrupt service routine located at the address specified by the contents of memory locations The interrupt service routine address is specified by the contents of memory locations $1FF0:$1FF1. See **SECTION 9** for more information.

6.10 KEY WAKE-UP INTERRUPT (KWI)

The KWI interrupt is generated by the Key Wake-Up System. The I-bit in the CCR must be clear in order for the KWI interrupt to be enabled. This interrupt will vector to the interrupt service routine located at the address specified by the contents of memory locations The interrupt service routine address is specified by the contents of memory locations $1FF8:$1FF9. See **SECTION 7** for more information.

SECTION 7INPUT/OUTPUT PORTS

In the Single-Chip Mode there are 20 bidirectional I/O lines arranged as three ports (Ports A, B, and C). The individual bits in these ports are programmable as either inputs or outputs under software control by the data direction registers (DDR's). If enabled by select bits in RCR or WOMR, port pins may have software programmable pullup resistors, or open drain outputs, respectively.

7.1 PORT A

Port A is an 8-bit bidirectional port which shares bits 0:3 with Key Wake-up subsystem and bit 3 is also shared with Buzzer Subsystem as shown in **Figure 7-1** and **Figure 7-2**. Bit 4 shares with A/D Converter and Event Counter Subsystems as shown in **Figure 7-4**. Bit 5 shares with A/D Converter Subsystem as shown in **Figure 7-5**. Bit 6 shares with Time Base Subsystem as shown in **Figure 7-6**. Bit 7 shares with Pulse Width Counter Subsystem as shown in **Figure 7-7**. Each Port A pin is controlled by the corresponding bits in a data direction register and a data register enable bits of appropriate sub-systems. The Port A Data Register is located at address $0000. The Port A Data Direction Register (DDRA) is located at address $0000 of the option map. Reset clears the DDRA. The Port A Data Register is unaffected by reset.

Port A bits 0:3 when configured as output port is an open drain output. Maximum of 9V may be applied to these pins regardless of V_{DD}. Each pin may sink maximum of 20mA at V_{OL} (max) = 0.3V. See **Section 15.1**, **Section 15.3** and **Section 15.4**.

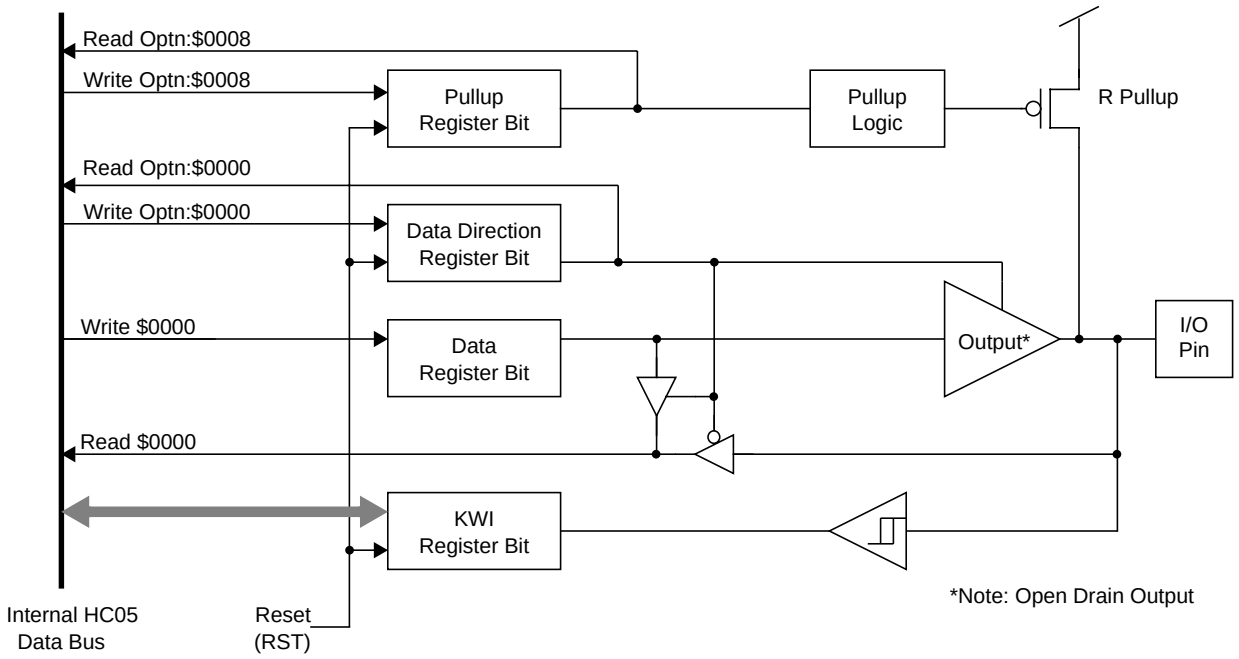

Figure 7-1: Port A0:3/KWI0:3 I/O Circuitry

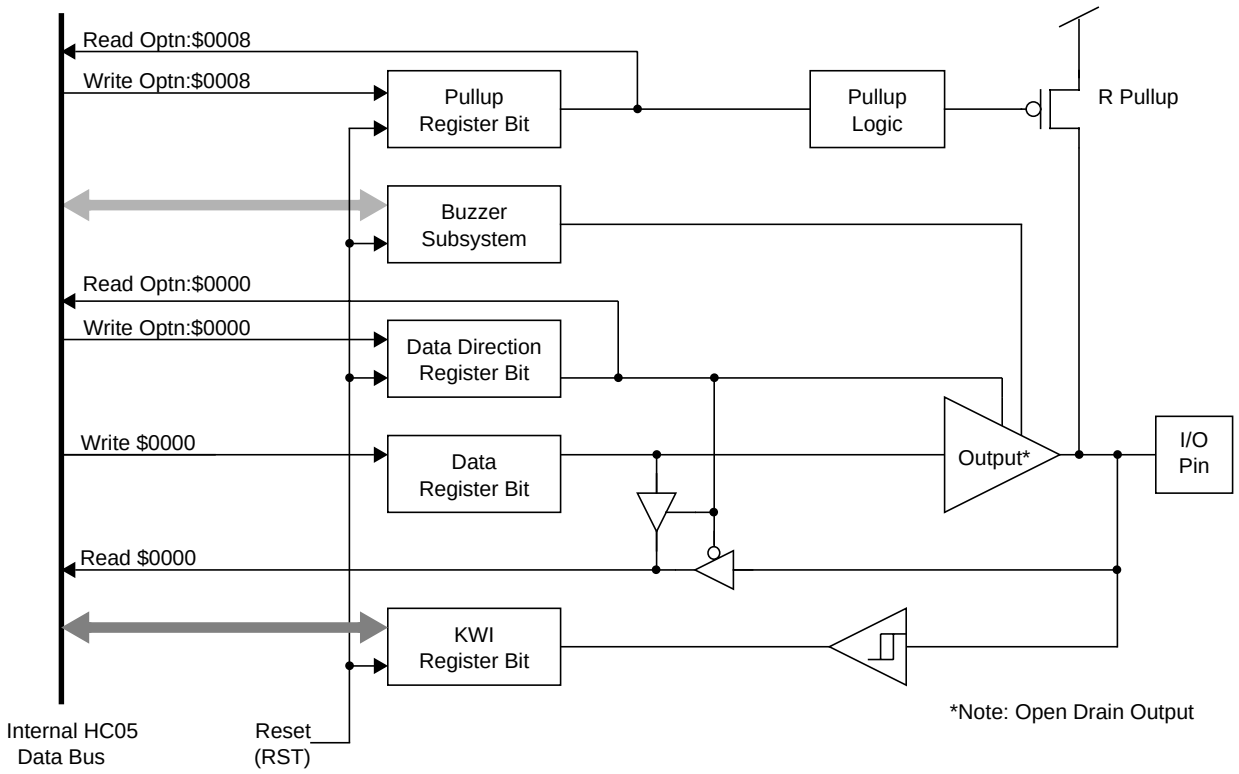

Figure 7-2: Port A3/KWI3/BZ I/O Circuitry

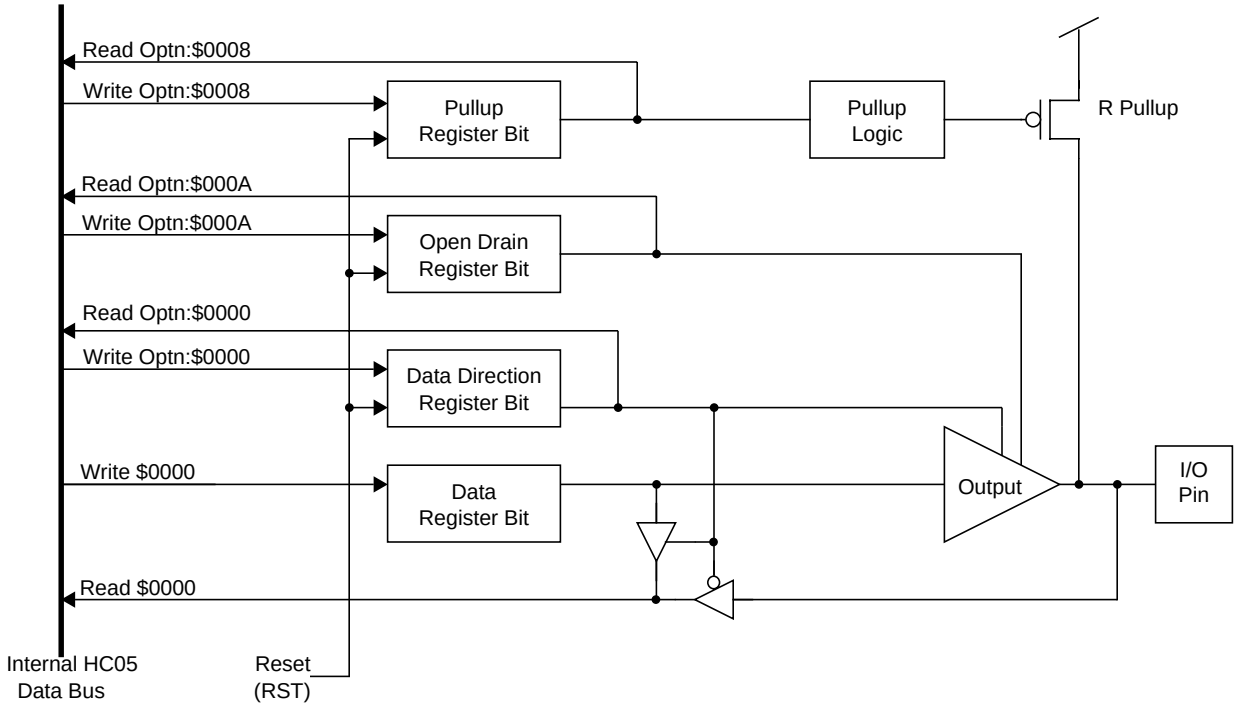

Figure 7-3: Port A4:6 I/O Circuitry

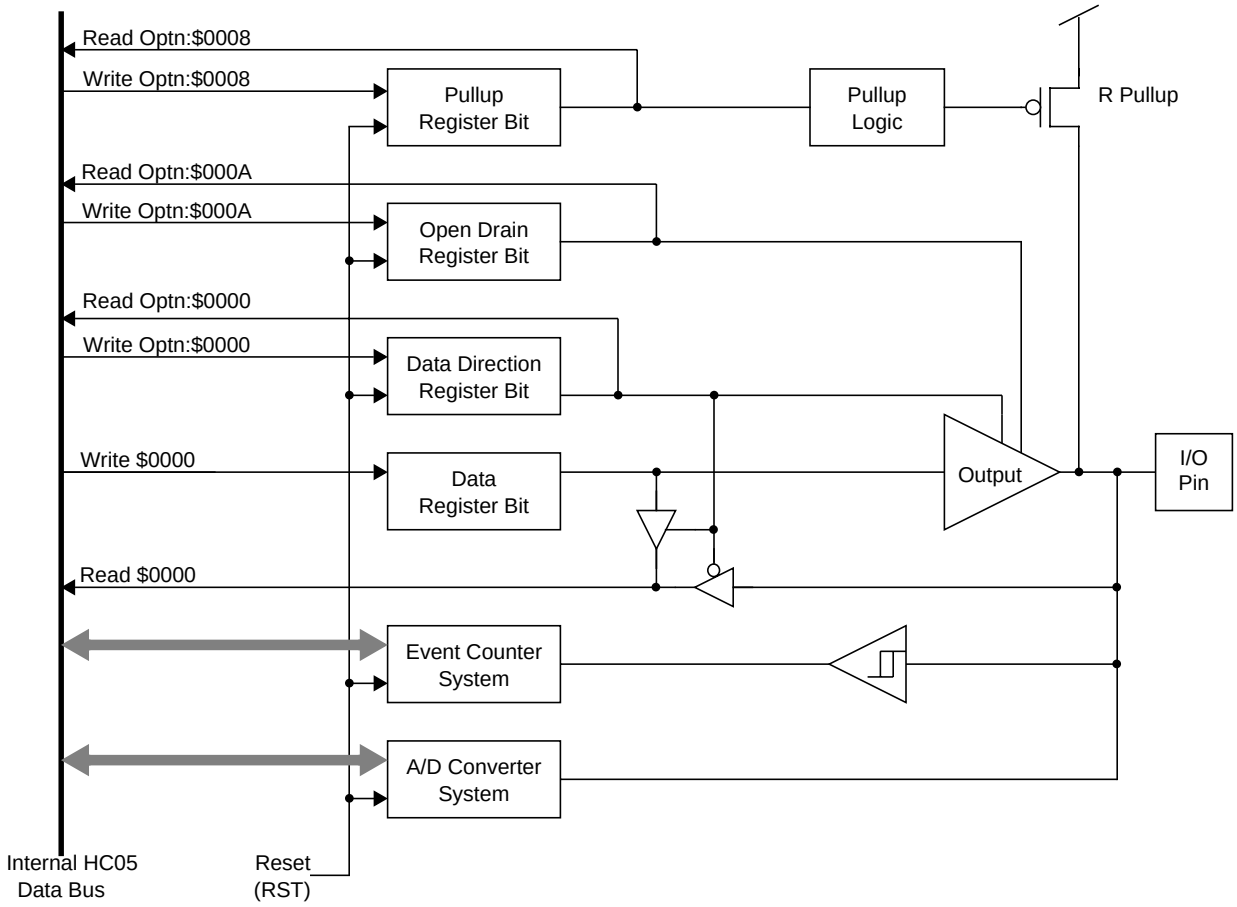

Figure 7-4: Port A4/AD0/EVI I/O Circuitry

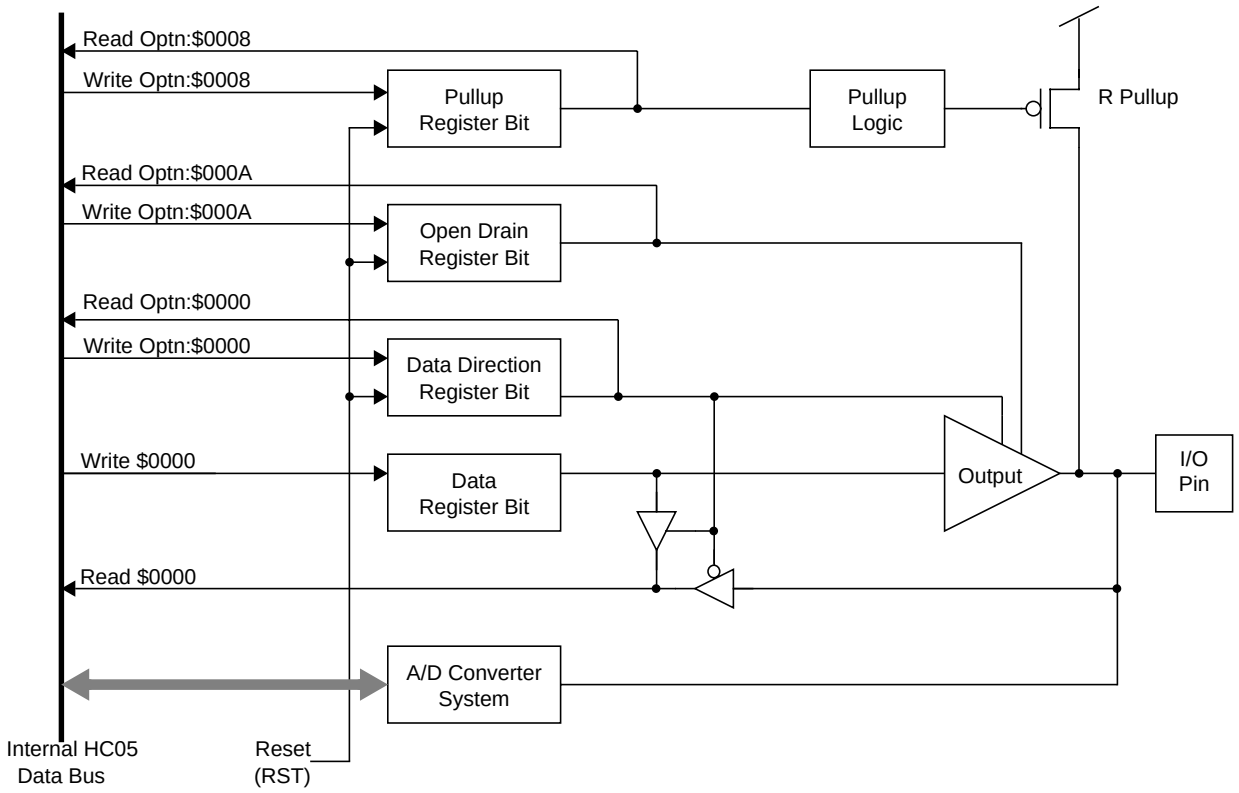

Figure 7-5: Port A5/AD1 I/O Circuitry

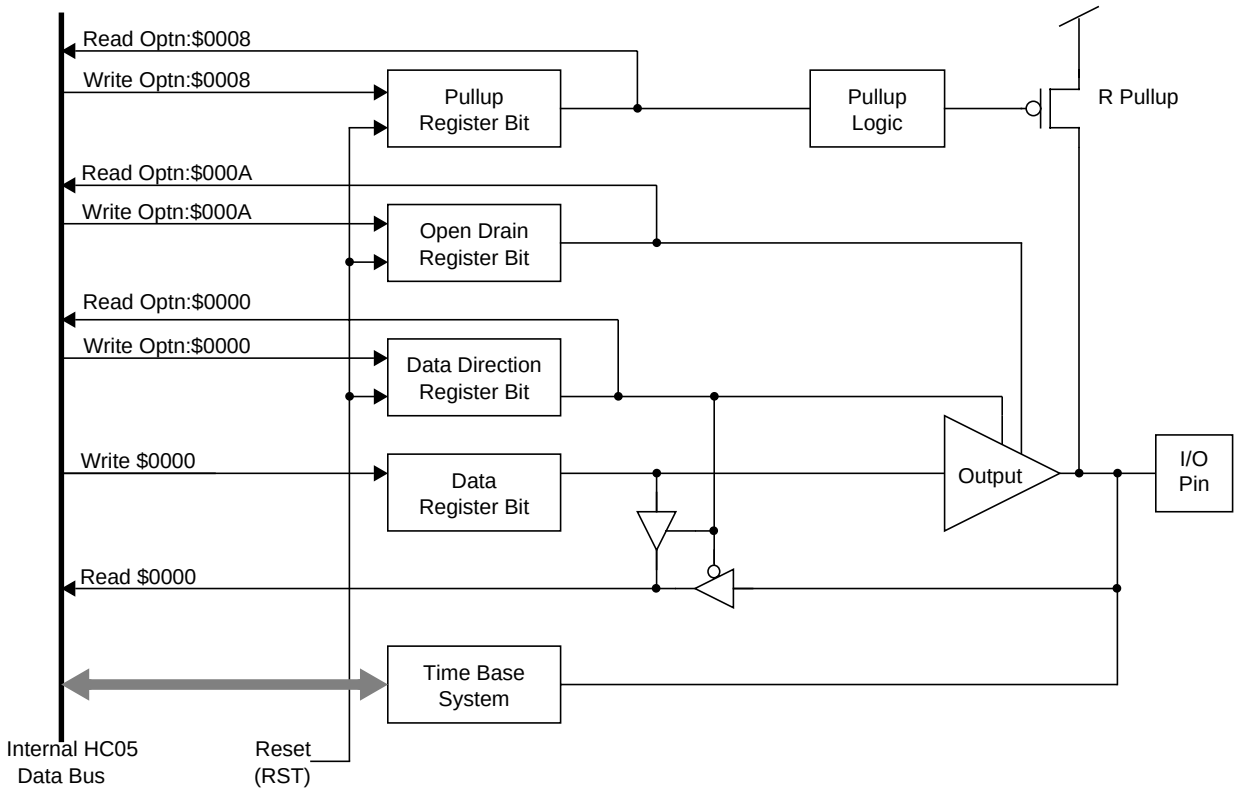

Figure 7-6: Port A6/RMO I/O Circuitry

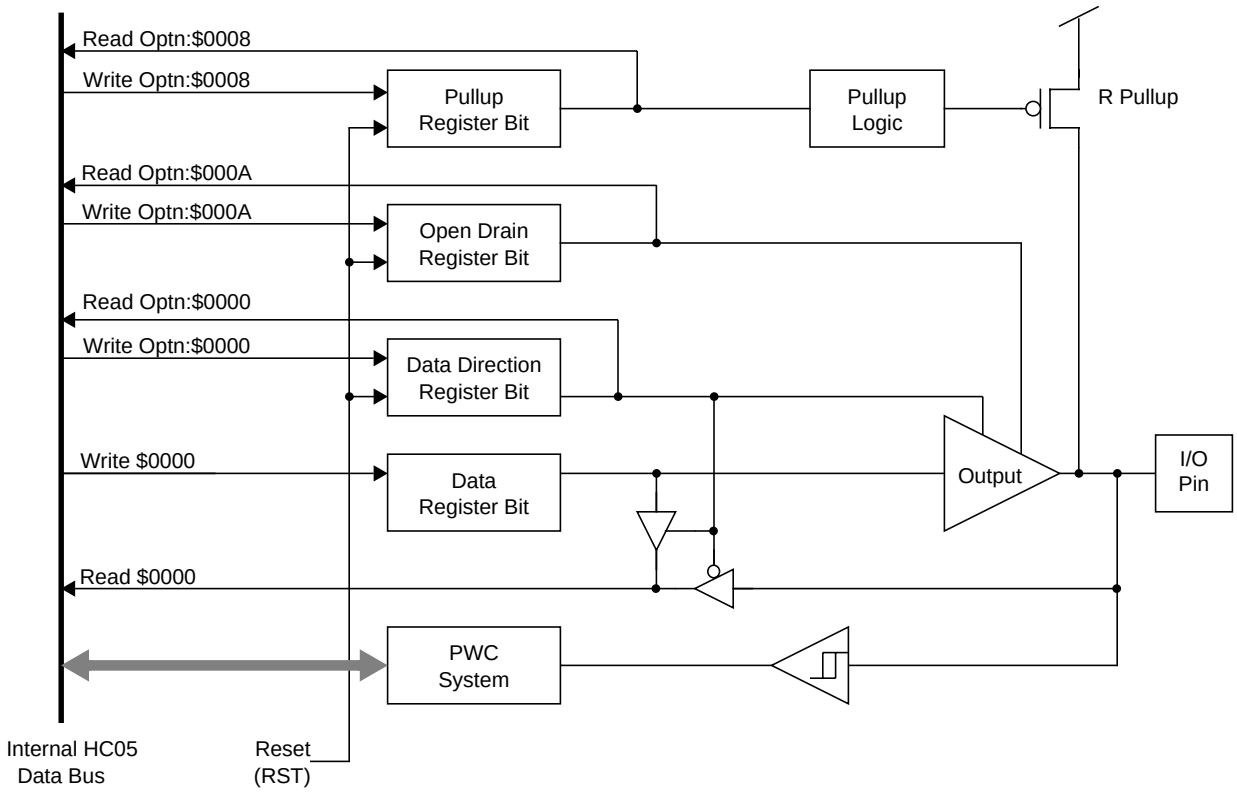

Figure 7-7: Port A7/PWCI I/O Circuitry

7.1.1 PORT A DATA REGISTER

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$0000	PORT A DATA PORTA	R	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		W								
		RESET:	U	U	U	U	U	U	U	U

Figure 7-8: Port A Data Register

Each Port A I/O pin has a corresponding bit in the Port A Data Register. When a Port A pin is programmed as an output the state of the corresponding data register bit determines the state of the output pin. When a Port A pin is programmed as an input, any read of the Port A Data Register will return the logic state of the corresponding I/O pin. The Port A data register is unaffected by reset.

7.1.2 PORT A DATA DIRECTION REGISTER

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
OPTN $0000	PORT A DATA DIRECTION DDRA	R	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		W								
		RESET:	0	0	0	0	0	0	0	0

Figure 7-9: Port A Data Direction Register

Each Port A I/O pin may be programmed as an input by clearing the corresponding bit in the DDRA, or programmed as an output by setting the corresponding bit in the DDRA. The DDRA can be accessed at address $0000 of the option map. The DDRA is cleared by reset.

7.1.3 PORT A PULLUP RESISTER

Each Port A pin may have software programmable pullup device enabled by the RCR select bits RAH and RAL. The pullup is activated whenever the corresponding bit in the RCR is set. The typical resistance at V_{DD}=3V is 50 KΩ. Since reset clears the RCR, all pins will initialize with the pullup devices disabled.

7.1.4 PORT A WIRED-OR MODE REGISTER

Port A bits 0:3 configured for output pins are wired-or mode (open drain) only. Port A bits 4:7 configured for output pins may have software programmable wired-or mode (open drain) output enabled by the AWOM bit in the WOMR. Since reset clears the WOMR, the wired-or mode disabled on reset.

7.1.5 KEY WAKE-UP INTERRUPT (KWI)

Four Key Wake-up inputs ($\overline{KWI0}$-$\overline{KWI3}$) share pins with Port A. Each key wake-up input is enabled by the corresponding bit in the KWIEN register which resides in the options map, and Key Wake-up Interrupt (KWI) is enabled by the KWIE bit in the INTCR.

When a falling edge is detected at one of the enabled key wake-up inputs, the KWIF bit in the INTSR is set and KWI is generated if KWIE = 1. Each input has a latch which responds only to the falling edge at the pin and all input latches are cleared at the same time by clearing KWIF bit. See **Figure 7-10**.

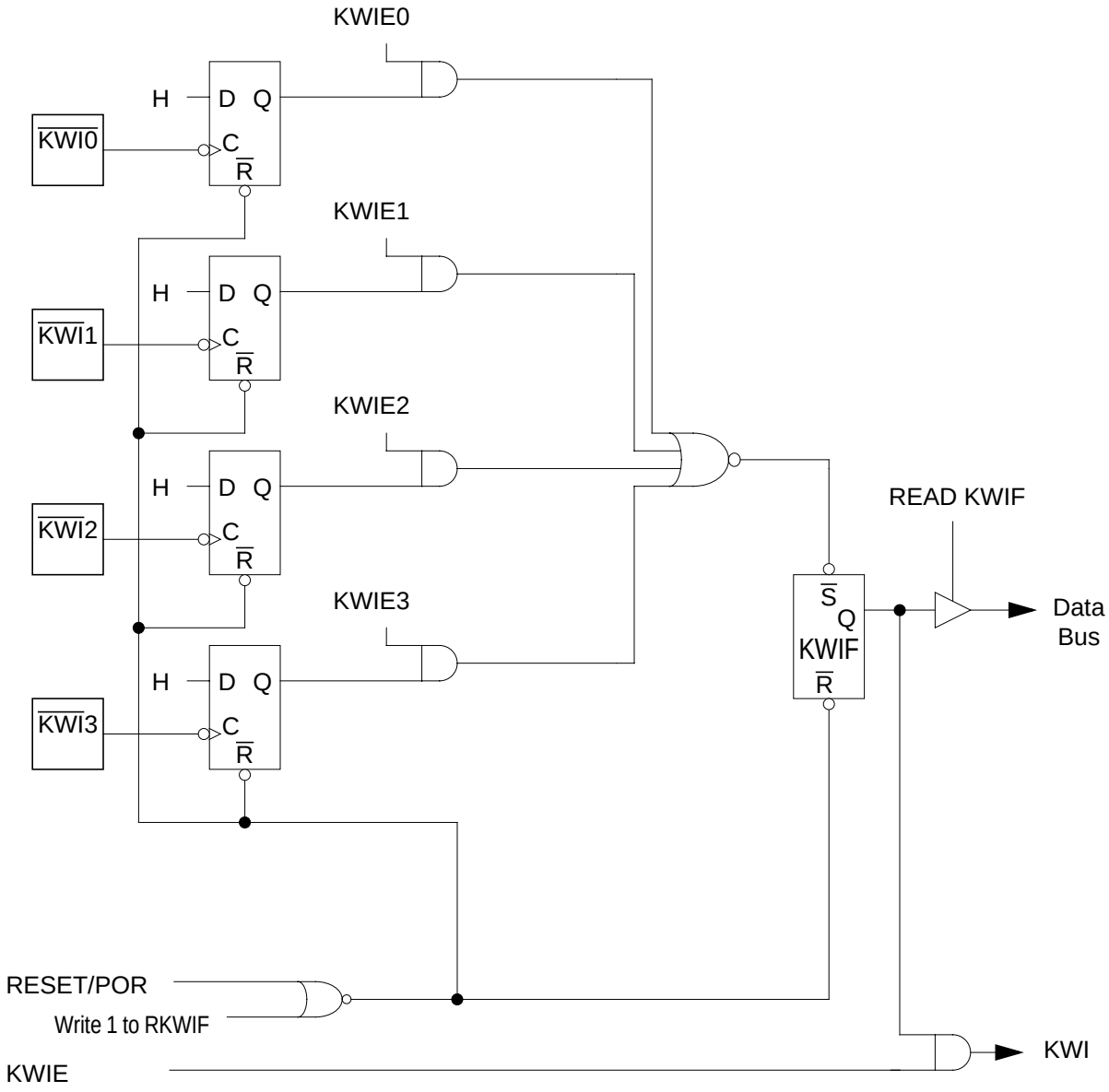

Figure 7-10: Key Wake-up Interrupt (KWI)

7.1.6 I/O PIN TRUTH TABLES

Table 7-1 thru **Table 7-1** summarizes the input or output mode programming for Port A.

Table 7-1: PA0:2/$\overline{\text{KWI0:2}}$ I/O Pin Functions

DDR	Output Latch	KWIE0:2	RAL	I/O Pin Modes	Access to DDRA0:2	Access to Data Register Latch PA0:2	
					Read/Write	Read	Write
0	X	0	0	IN, Hi-Z, KWI disable	DDRA0:2	Pin	Latch*
0	X	0	1	IN, KWI disable, Pullup	DDRA0:2	Pin	Latch*
0	X	1	0	IN, Hi-Z, KWI enable	DDRA0:2	Pin	Latch*
0	X	1	1	IN, KWI enable, Pullup	DDRA0:2	Pin	Latch*
1	0	0	X	OUT, OD	DDRA0:2	Latch	Latch, Pin
1	1	0	0	OUT, OD, Hi-Z	DDRA0:2	Latch	Latch, Pin
1	1	0	1	OUT, OD, Pullup	DDRA0:2	Latch	Latch, Pin
1	0	1	X	OUT, OD, KWI enable	DDRA0:2	Latch	Latch, Pin
1	1	1	0	OUT, OD, Hi-Z, KWI enable	DDRA0:2	Latch	Latch, Pin
1	1	1	1	OUT, OD, Pullup, KWI enable	DDRA0:2	Latch	Latch, Pin

Note:
1. X is don't care state.
2. * Does not affect input, but stored to Data Register Latch

Table 7-2: PA3/$\overline{\text{KWI3}}$/BZ I/O Pin Functions

DDR	Output Latch	KWIE3	BZPE	RAL	I/O Pin Modes	Access to DDRA3	Access to Data Register Latch PA3	
						Read/Write	Read	Write
0	X	0	0	0	IN, Hi-Z, KWI disable	DDRA3	Pin	Latch*
0	X	0	0	1	IN, Hi-Z, KWI disable, Pullup	DDRA3	Pin	Latch*
0	X	1	0	0	IN, Hi-Z, KWI enable	DDRA3	Pin	Latch*
0	X	1	0	1	IN, Hi-Z, KWI enable, Pullup	DDRA3	Pin	Latch*
1	0	0	0	X	Port OUT, OD, KWI disable	DDRA3	Latch	Latch, Pin
1	1	0	0	0	Port OUT, OD, Hi-Z, KWI disable	DDRA3	Latch	Latch, Pin
1	1	0	0	1	Port OUT, OD, KWI disable, Pullup	DDRA3	Latch	Latch, Pin
1	0	1	0	X	Port OUT, OD, KWI enable	DDRA3	Latch	Latch, Pin
1	1	1	0	0	Port OUT, OD, Hi-Z, KWI enable	DDRA3	Latch	Latch, Pin
1	1	1	0	1	Port OUT, OD, Pullup, KWI enable	DDRA3	Latch	Latch, Pin
0	X	0	1	0	BZ OUT, OD, KWI disable	DDRA3	Pin	Latch*
1							Latch	
0	X	0	1	1	BZ OUT, OD, KWI disable, Pullup	DDRA3	Pin	Latch*
1							Latch	
0	X	1	1	0	BZ OUT, OD, KWI enable	DDRA3	Pin	Latch*
1							Latch	
0	X	1	1	1	BZ OUT, OD, KWI enable, Pullup	DDRA3	Pin	Latch*
1							Latch	

Note:
1. X is don't care state.
2. * Does not affect input, but stored to Data Register Latch

Table 7-3: PA4/AD0/EVI I/O Pin Functions

DDR	Out-put Latch	EVCE	ADON	A/D CH	AWOM	RAH	I/O Pin Modes	Access to DDRA4	Access to Data Register Latch PA4	
								Read/Write	Read	Write
0	X	0	0	X	X	0	Port IN, Hi-Z	DDRA4	Pin	Latch*
0	X	0	0	X	X	1	Port IN, Pullup	DDRA4	Pin	Latch*
0	X	X	1	0	X	X	A/D IN	DDRA4	0	Latch*
0	X	X	1	1-7	X	0	Port IN, Hi-Z	DDRA4	Pin	Latch*
0	X	X	1	1-7	X	1	Port IN, Pullup	DDRA4	Pin	Latch*
0	X	1	X	X	X	0	Port IN, Hi-Z, Event In	DDRA4	Pin	Latch*
0	X	1	X	X	X	1	Port IN, Pullup, Event In	DDRA4	Pin	Latch*
1	X	0	0	X	0	X	OUT, CMOS	DDRA4	Latch	Latch, Pin
1	0	0	0	X	1	X	OUT, OD	DDRA4	Latch	Latch, Pin
1	1	0	0	X	1	0	OUT, OD, Hi-Z	DDRA4	Latch	Latch, Pin
1	1	0	0	X	1	1	OUT, OD, Pullup	DDRA4	Latch	Latch, Pin
1	X	0	1	X	0	X	OUT, CMOS	DDRA4	Latch	Latch, Pin
1	0	0	1	X	1	X	OUT, OD	DDRA4	Latch	Latch, Pin
1	1	X	1	0	1	0	OUT, OD	DDRA4	Latch	Latch, Pin
1	1	0	1	1-7	1	0	OUT, OD, Hi-Z	DDRA4	Latch	Latch, Pin
1	1	0	1	X	1	1	OUT, OD, Pullup	DDRA4	Latch	Latch, Pin
1	X	1	0	X	0	X	OUT, CMOS, Event In	DDRA4	Latch	Latch, Pin
1	0	1	0	X	1	X	OUT, OD, Event In	DDRA4	Latch	Latch, Pin
1	1	1	0	X	1	0	OUT, OD, Hi-Z, Event In	DDRA4	Latch	Latch, Pin
1	1	1	0	X	1	1	OUT, OD, Event In, Pullup	DDRA4	Latch	Latch, Pin
1	X	1	1	1-7	0	X	OUT, CMOS, Event In	DDRA4	Latch	Latch, Pin
1	0	1	1	1-7	1	X	OUT, OD, Event In	DDRA4	Latch	Latch, Pin
1	1	1	1	1-7	1	0	OUT, OD, Hi-Z, Event In	DDRA4	Latch	Latch, Pin
1	1	1	1	1-7	1	1	OUT, OD, Event In, Pullup	DDRA4	Latch	Latch, Pin

Note:
1. X is don't care state.
2. * Does not affect input, but stored to Data Register Latch
3. Do not apply analog voltage to this pin unless the I/O pin mode is set to A/D IN. Excessive current may be drawn if this pin is read as digital input port while analog voltage is applied.

Table 7-4: PA5/AD1 I/O Pin Functions

DDR	Output Latch	ADON	A/D CH	AWOM	RAH	I/O Pin Modes	Access to DDRA5	Access to Data Register Latch PA5	
							Read/Write	Read	Write
0	X	0	X	X	0	Port IN, Hi-Z	DDRA5	Pin	Latch*
0	X	0	X	X	1	Port IN, Pullup	DDRA5	Pin	Latch*
0	X	1	1	X	X	A/D IN	DDRA5	0	Latch*
0	X	1	0, 2-7	X	0	Port IN, Hi-Z	DDRA5	Pin	Latch*
0	X	1	0, 2-7	X	1	Port IN, Pullup	DDRA5	Pin	Latch*
1	X	0	X	0	X	OUT, CMOS	DDRA5	Latch	Latch, Pin
1	0	0	X	1	X	OUT, OD	DDRA5	Latch	Latch, Pin
1	1	0	X	1	0	OUT, OD, Hi-Z	DDRA5	Latch	Latch, Pin
1	1	0	X	1	1	OUT, OD, Pullup	DDRA5	Latch	Latch, Pin
1	X	1	X	0	X	OUT, CMOS	DDRA5	Latch	Latch, Pin
1	0	1	X	1	X	OUT, OD	DDRA5	Latch	Latch, Pin
1	1	1	X	1	0	OUT, OD, Hi-Z	DDRA5	Latch	Latch, Pin
1	1	1	X	1	1	OUT, OD, Pullup	DDRA5	Latch	Latch, Pin

Note:
1. X is don't care state.
2. * Does not affect input, but stored to Data Register Latch
3. Do not apply analog voltage to this pin unless the I/O pin mode is set to A/D IN. Excessive current may be drawn if this pin is read as digital input port while analog voltage is applied.

Table 7-5: PA6/RMO I/O Pin Functions

I/O Port		Remote Carrier Output			AWOM	RAH	I/O Pin Modes	Access to DDRA6	Access to Data Register Latch PA6	
DDR	OL	RMPE	RMON	RPOL				Read/Write	Read	Write
0	X	X	X	X	X	0	Port IN, Hi-Z	DDRA6	Pin	Latch*
0	X	X	X	X	X	1	Port IN, Pullup	DDRA6	Pin	Latch*
1	X	0	X	X	0	X	OUT, output latch, CMOS	DDRA6	Latch	Latch, Pin
1	0	0	X	X	1	X	OUT, output latch, OD	DDRA6	Latch	Latch, Pin
1	1	0	X	X	1	0	OUT, output latch, OD, Hi-Z	DDRA6	Latch	Latch, Pin
1	1	0	X	X	1	1	OUT, output latch, OD, Pullup	DDRA6	Latch	Latch, Pin
1	X	1	0	0	0	X	OUT, remote idle, CMOS = Vss	DDRA6	Latch	Latch*
1	X	1	0	1	0	X	OUT, remote idle, CMOS = Vdd	DDRA6	Latch	Latch*
1	X	1	1	X	0	X	OUT, remote carrier, CMOS	DDRA6	Latch	Latch*
1	X	1	1	X	1	0	OUT, remote carrier, OD/Hi-Z	DDRA6	Latch	Latch*
1	X	1	1	X	1	1	OUT, remote carrier, OD/Pullup	DDRA6	Latch	Latch*

Note:
1. OL = Output Latch
2. X is don't care state.
3. * Does not affect input, but stored to Data Register Latch
4. Vss/Hi-Z = output is either Vss (N-ch on) or Hi-Z (N- and P-ch off) depending on clock pulse
5. Vss/Pullup = output is either Vss (N-ch on) or Pullup (resistive) depending on clock pulse

Table 7-6: PA7/PWCI I/O Pin Functions

DDR	Out-put Latch	PWCE	AWOM	RAH	I/O Pin Modes	Access to DDRA7	Access to Data Register Latch PA7	
						Read/Write	Read	Write
0	X	0	X	0	Port IN, Hi-Z	DDRA7	Pin	Latch*
0	X	0	X	1	Port IN, Pullup	DDRA7	Pin	Latch*
0	X	1	X	0	Port IN, Hi-Z, PWCI	DDRA7	Pin	Latch*
0	X	1	X	1	Port IN, Pullup, PWCI	DDRA7	Pin	Latch*
1	X	0	0	X	OUT, CMOS	DDRA7	Latch	Latch, Pin
1	0	0	1	X	OUT, OD	DDRA7	Latch	Latch, Pin
1	1	0	1	0	OUT, OD, Hi-Z	DDRA7	Latch	Latch, Pin
1	1	0	1	1	OUT, OD, Pullup	DDRA7	Latch	Latch, Pin
1	X	1	0	X	OUT, CMOS, PWCI	DDRA7	Latch	Latch, Pin
1	0	1	1	X	OUT, OD, PWCI	DDRA7	Latch	Latch, Pin
1	1	1	1	0	OUT, OD, Hi-Z, PWCI	DDRA7	Latch	Latch, Pin
1	1	1	1	1	OUT, OD, Pullup, PWCI	DDRA7	Latch	Latch, Pin

Note:
1. X is don't care state.
2. * Does not affect input, but stored to Data Register Latch

7.2 PORT B

Port B is an 8-bit bidirectional port that are shared with LCD Front Plane Drivers as shown in **Figure 7-11**. Each Port B pin is controlled by the corresponding bits in a data direction register and a data register. The Port B Data Register is located at address $0001. The Port B Data Direction Register (DDRB) is located at address $0001 of the option map. Reset clears the DDRB. The Port B Data Register is unaffected by reset. The LCD Front Plane Drivers are enabled on reset.

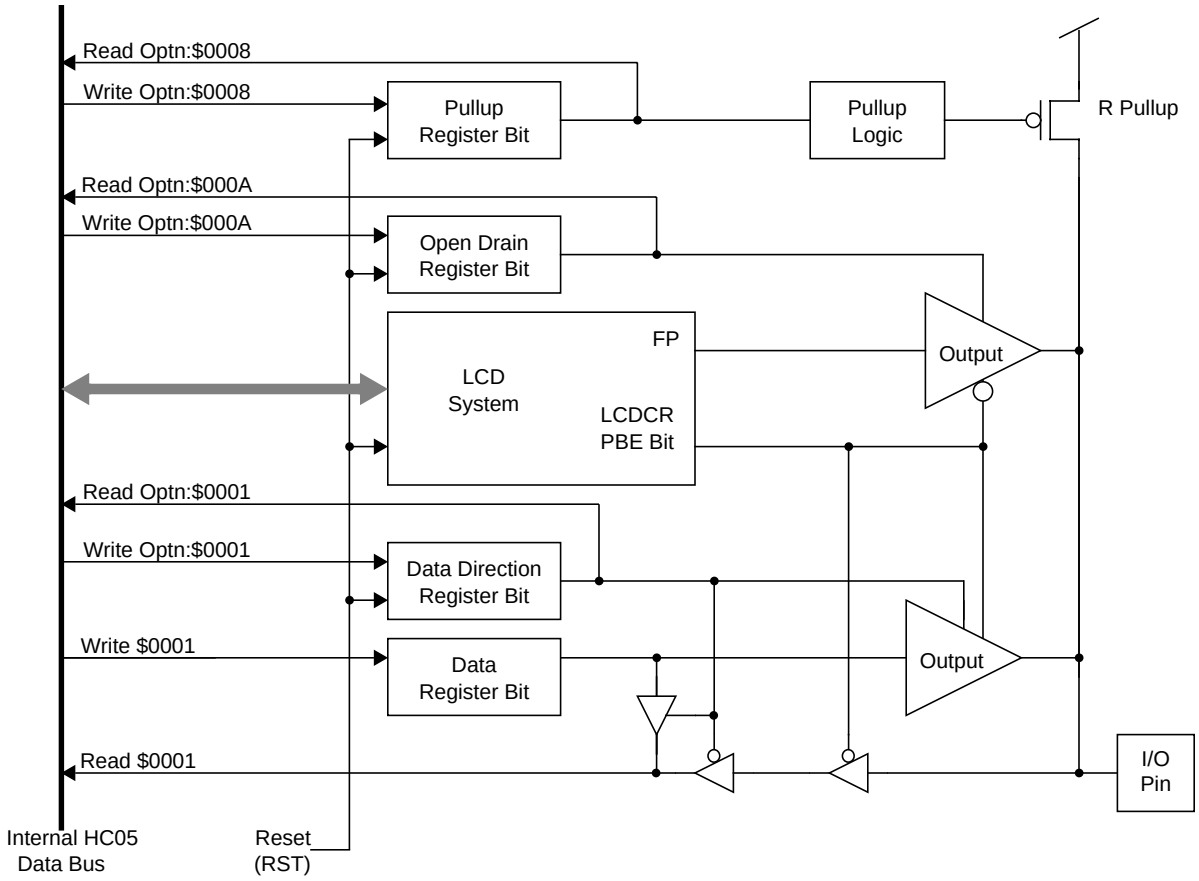

Figure 7-11: Port B0:B7/FP24:FP17 I/O Circuitry

7.2.1 PORT B DATA REGISTER

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$0001	PORT B DATA PORTB	R	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		W								
		RESET:	U	U	U	U	U	U	U	U

Figure 7-12: Port B Data Register

Each Port B I/O pin has a corresponding bit in the Port B Data Register. When a Port B pin is programmed as an output the state of the corresponding data register bit determines the state of the output pin. When a Port B pin is programmed as an input, any read of the Port B Data Register will return the logic state of the corresponding I/O pin. The Port B data register is unaffected by reset.

7.2.2 PORT B DATA DIRECTION REGISTER

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
OPTN $0001	PORT B DATA DIRECTION DDRB	R	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		W								
	RESET:		0	0	0	0	0	0	0	0

Figure 7-13: Port B Data Direction Register

Each Port B I/O pin may be programmed as an input by clearing the corresponding bit in the DDRB, or programmed as an output by setting the corresponding bit in the DDRB. The DDRB can be accessed at address $0001 of the option map. The DDRB is cleared by reset.

7.2.3 PORT B PULLUP RESISTER

Each Port B pin may have software programmable pullup device enabled by the RCR select bits RBH and RBL. The pullup is activated whenever the corresponding bit in the RCR is set. The typical resistance at V_{DD}=3V is 50 KΩ. Since reset clears the RCR, all pins will initialize with the pullup devices disabled. See **Section 7.4.6**.

7.2.4 PORT B WIRED-OR MODE REGISTER

Port B bits 0:7 configured for output pins may have software programmable wired-or mode (open drain) output enabled by the BWOMH and BWOML bits in the WOMR. Since reset clears the WOMR, the wired-or mode disabled on reset. See **Section 7.4.8**.

7.2.5 I/O PIN TRUTH TABLES

Table 7-1 and **Table 7-1** summarize the input or output and LCD mode programming for Port B.

Table 7-7: PB0:PB3/FP24:FP21 I/O Pin Functions

DDR	Output Latch	LCD-CR PBEL	BWOML	RBL	I/O Pin Modes	Access to DDRB0:3	Access to Data Register Latch PB0:3	
						Read/Write	Read	Write
X	X	0	X	0	LCD FP output	DDRB0:3	0	Latch*
X	X	0	X	1	LCD FP output, Pullup	DDRB0:3	0	Latch*
0	X	1	X	0	Port IN, Hi-Z	DDRB0:3	Pin	Latch*
0	X	1	X	1	Port IN, Pullup	DDRB0:3	Pin	Latch*
1	X	1	0	X	OUT, CMOS	DDRB0:3	Latch	Latch, Pin
1	0	1	1	X	OUT, OD	DDRB0:3	Latch	Latch, Pin
1	1	1	1	0	OUT, OD, Hi-Z	DDRB0:3	Latch	Latch, Pin
1	1	1	1	1	OUT, OD, Pullup	DDRB0:3	Latch	Latch, Pin

Note:
1. X is don't care state.
2. * Does not affect input, but stored to Data Register Latch
3. Do not turn on Pullup R (PBL=1) when using these pins as LCD port.

Table 7-8: PB4:PB7/FP20:FP17 I/O Pin Functions

DDR	Output Latch	LCDCR PBEH	BWOMH	RBH	I/O Pin Modes	Access to DDRB4:7	Access to Data Register Latch PB4:7	
						Read/Write	Read	Write
X	X	0	X	0	LCD FP output	DDRB4:7	0	Latch*
X	X	0	X	1	LCD FP output, Pullup	DDRB4:7	0	Latch*
0	X	1	X	0	Port IN, Hi-Z	DDRB4:7	Pin	Latch*
0	X	1	X	1	Port IN, Pullup	DDRB4:7	Pin	Latch*
1	X	1	0	X	OUT, CMOS	DDRB4:7	Latch	Latch, Pin
1	0	1	1	X	OUT, OD	DDRB4:7	Latch	Latch, Pin
1	1	1	1	0	OUT, OD, Hi-Z	DDRB4:7	Latch	Latch, Pin
1	1	1	1	1	OUT, OD, Pullup	DDRB4:7	Latch	Latch, Pin

Note:
1. X is don't care state.
2. * Does not affect input, but stored to Data Register Latch
3. Do not turn on Pullup R (PBH=1) when using these pins as LCD port.

7.3 PORT C

Port C is an 4-bit I/O port which shares its pins with external interrupt $\overline{IRQ}$ and Serial Peripheral Interface (SPI) System as shown in **Figure 7-17** thru **Figure 7-17**. Each Port C pin is controlled by the corresponding bits in a wired-or mode register and a pullup register. The Port C Data Register is located at address $0002. The Port C Pullup Register (RCR) is located at address $0009 of the option map. The Wired-Or Mode Register (WOMR) is located at address $000A of the option map. Reset clears the RCR and the WOMR.

The PC0 thru PC2 pins are shared with the Serial Peripheral Interface (SPI). When the SPI is enabled (SPE = 1), the pins PC0, PC1, and PC2 are configured as serial clock output or input (SCK), serial data output (SDO), and serial data input (SDI) pins, respectively. The direction of the SCK depends on the MSTR bit in the SPCR. When the PORTC is read, the pin state is read. See **Table 7-1** thru **Table 7-1**. The SCK pin should be at V_{DD} level before SPI is enabled.

The PC3 pin is shared with the external interrupt $\overline{IRQ}$ pin. The $\overline{IRQ}$ pin has a Schmitt Trigger to improve noise immunity. The PC3 pin state may be read anytime regardless of the IRQ configurations.

Port C bits 2:3 when configured as output port is an open drain output. Maximum of twice the V_{DD} voltage (V_{pin} = 2xVDD) may be applied to these pins. See **Section 15.1**.

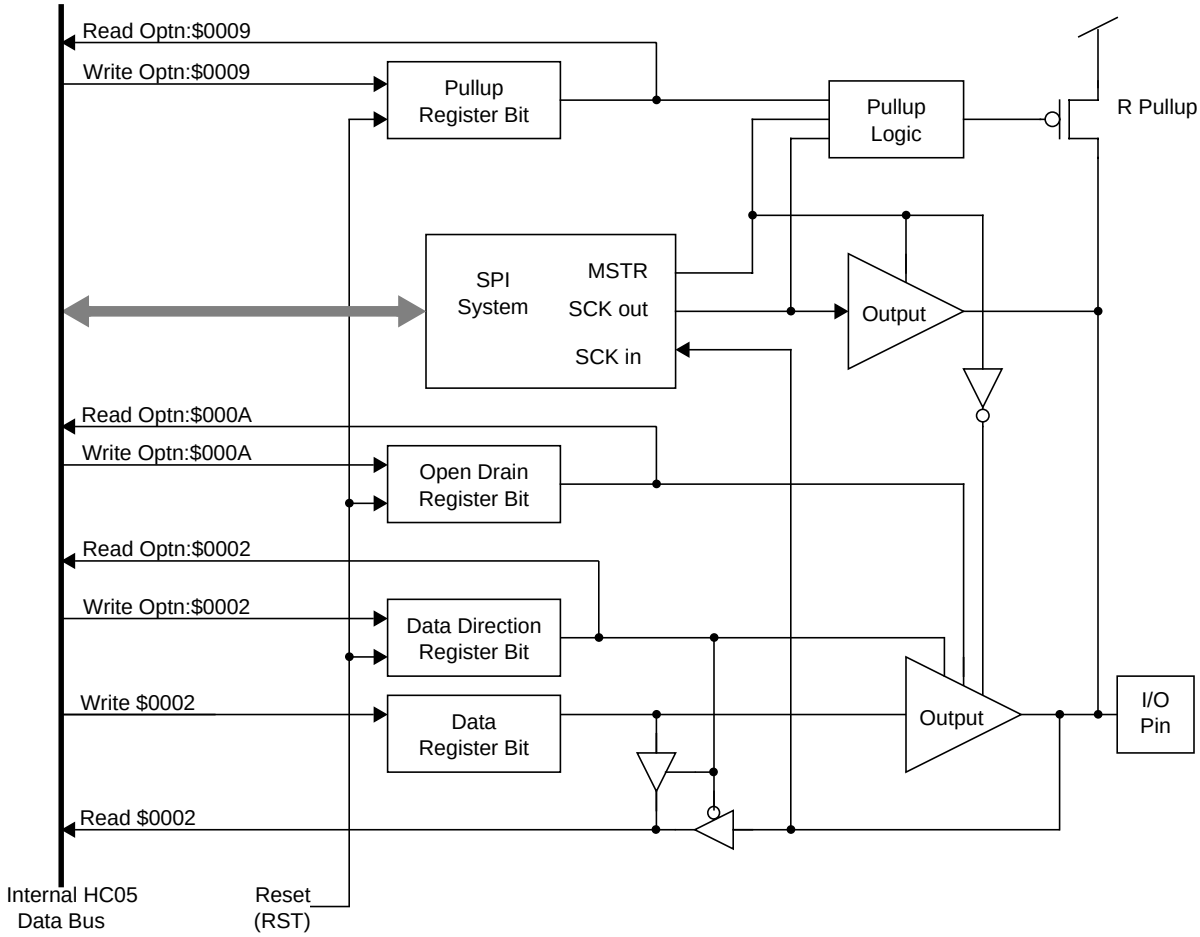

Figure 7-14: Port PC0/SCK Circuitry

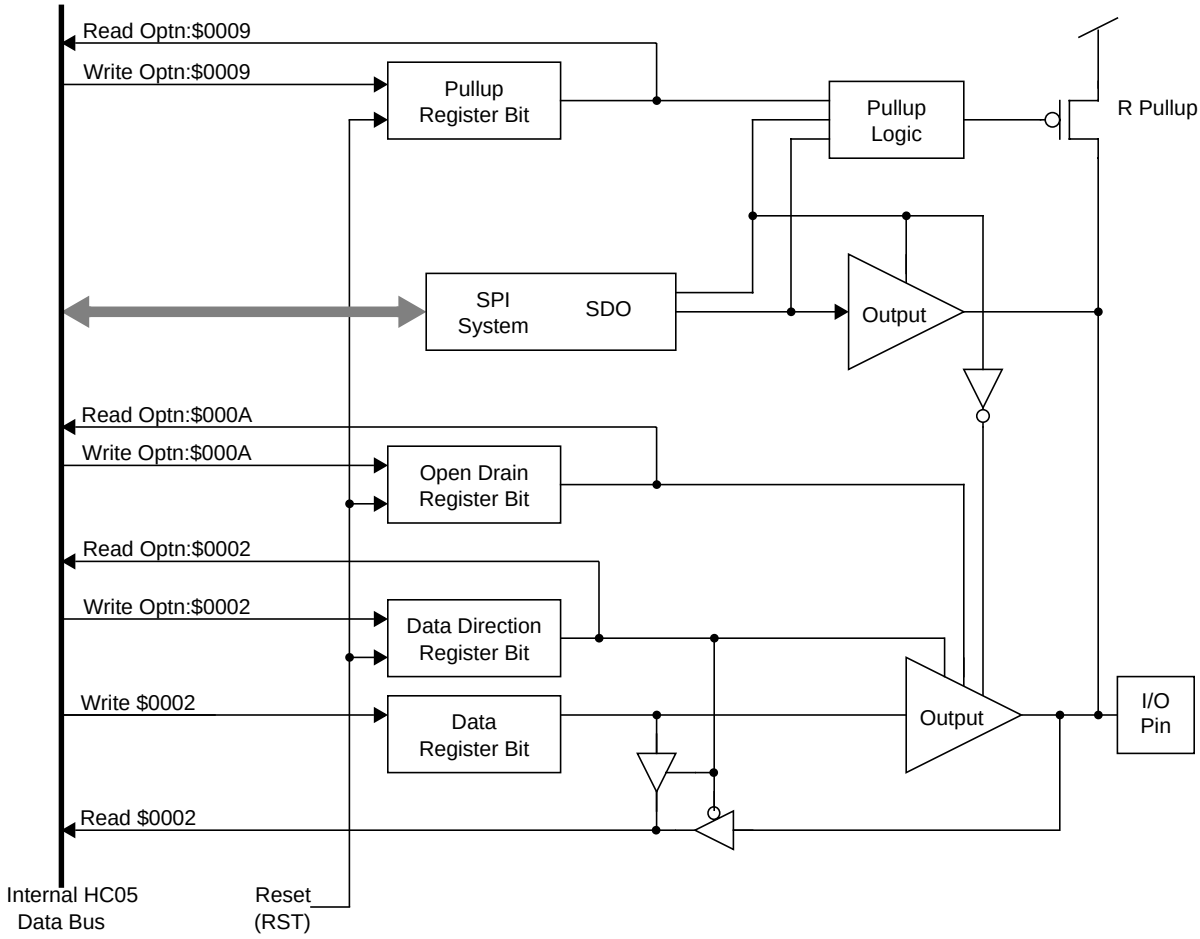

Figure 7-15: PC1/SDO Circuitry

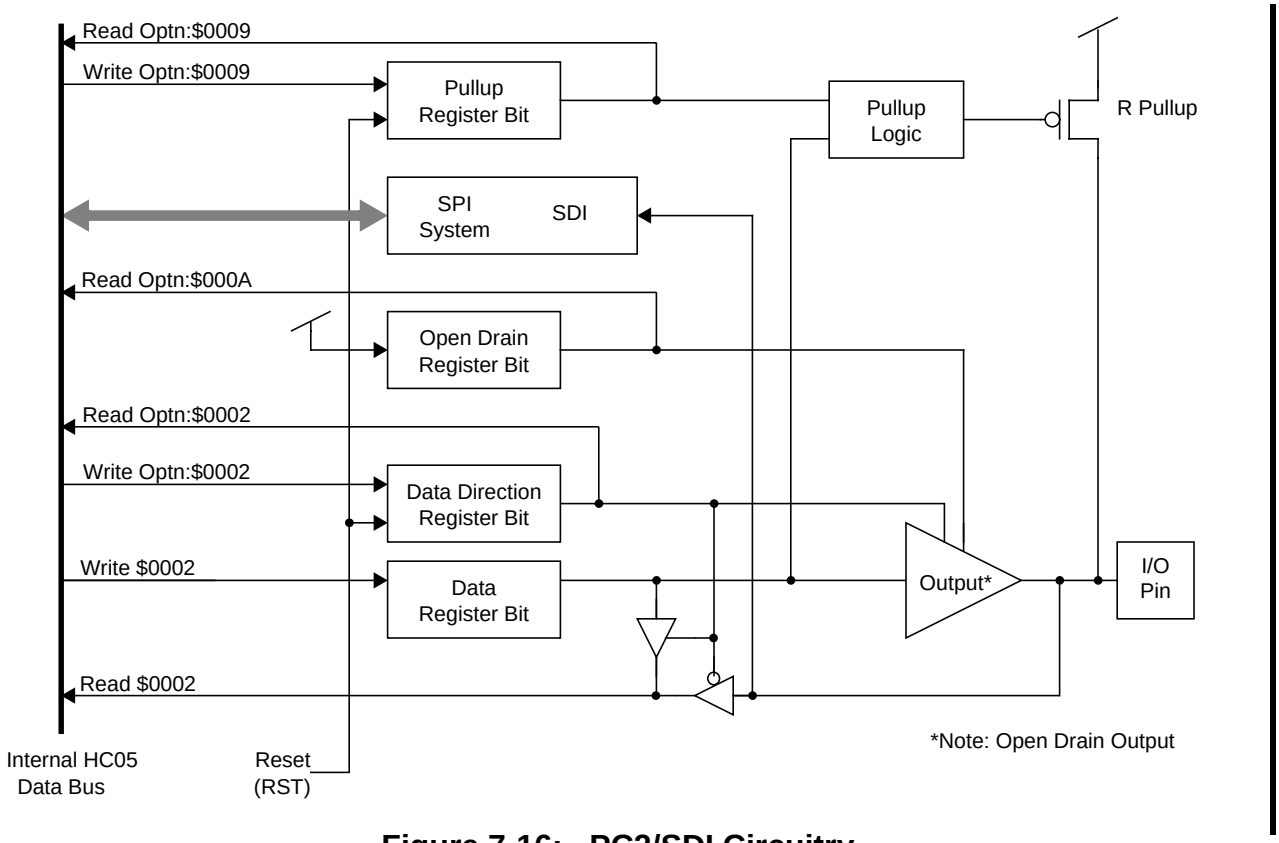

Figure 7-16: PC2/SDI Circuitry

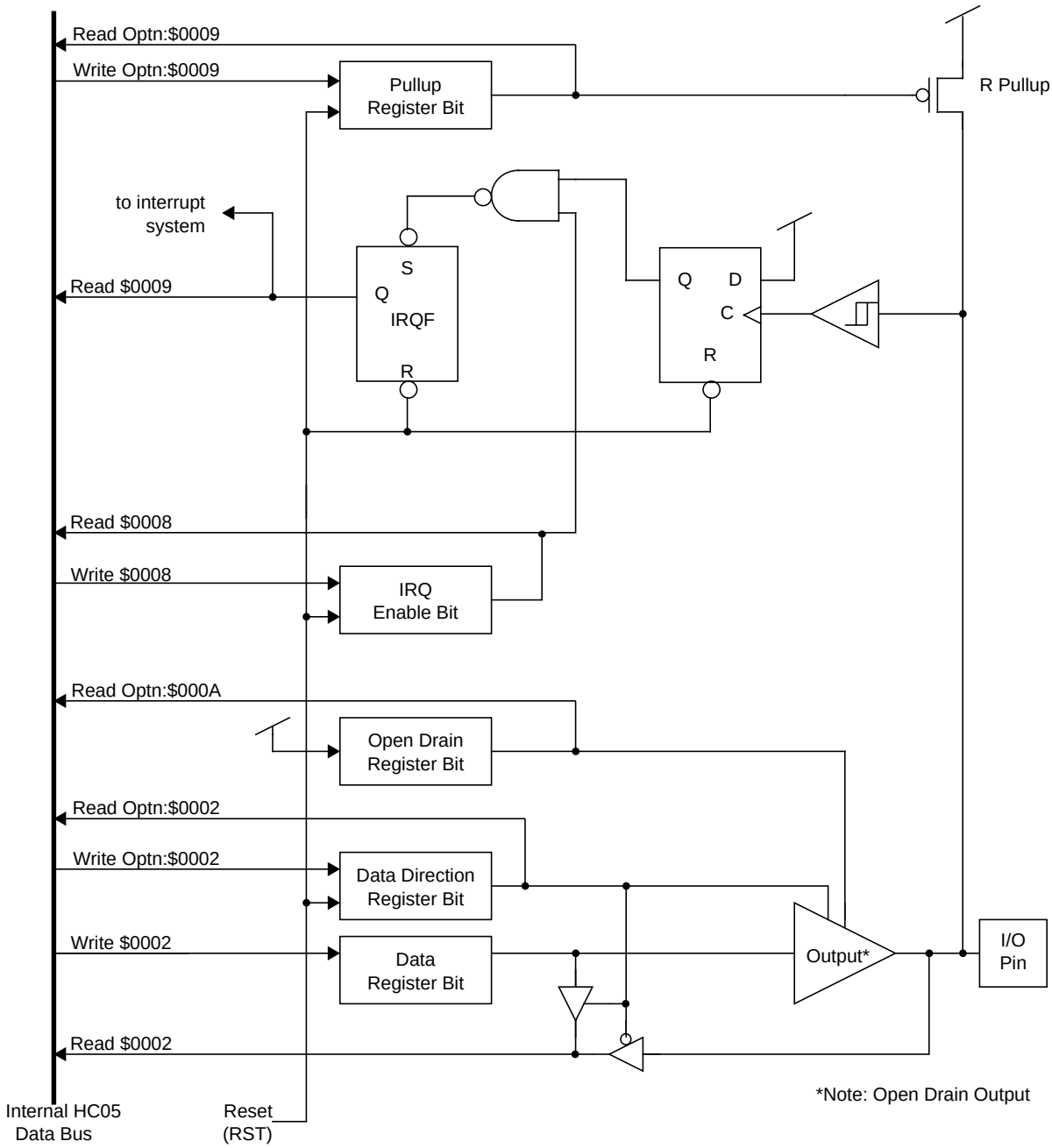

Figure 7-17: PC3/$\overline{\text{IRQ}}$ Circuitry

7.3.1 PORT C DATA REGISTER

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$0002	PORT C DATA PORTC	R	0	0	0	0	PC3	PC2	PC1	PC0
		W	—	—	—	—				
	RESET:		0	0	0	0	U	U	U	U

Figure 7-18: Port C Data Register

Each Port C input pin has a corresponding bit in the Port C Data Register. Regardless of peripheral configuration, any read of the Port C Data Register will return the logic state of the corresponding I/O pin. The Port C data register is unaffected by reset.

7.3.2 PORT C DATA DIRECTION REGISTER

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
OPTN $0002	PORT C DATA DIRECTION DDRC	R	0	0	0	0	DDRC3	DDRC2	DDRC1	DDRC0
		W	—	—	—	—				
	RESET:		0	0	0	0	0	0	0	0

Figure 7-19: Port C Data Direction Register

Each Port C I/O pin may be programmed as an input by clearing the corresponding bit in the DDRC, or programmed as an output by setting the corresponding bit in the DDRC. The DDRC can be accessed at address $0002 of the option map. The DDRC is cleared by reset.

7.3.3 PORT C PULLUP REGISTER

Each Port C pin may have software programmable pullup device enabled by the RCR2 select bit RC. The pullup is activated whenever the RC bit in the RCR2 is set. The typical resistance at V_{DD}=3V is 10KΩ. Since reset clears the RCR2, all pins will initialize with the pullup devices disabled. See **Section 7.4.7**.

7.3.4 PORT C WIRED-OR MODE REGISTER

Port C bits 0:2 configured for output pins may have software programmable wired-or mode (open drain) output enabled by the CWOM bit in the WOMR. Since reset clears the WOMR, the wired-or mode disabled on reset. Port C bit 3, when configured as output port, has wired-or mode output only. See **Section 7.4.8**.

7.3.5 I/O PIN TRUTH TABLES

Table 7-1 thru **Table 7-1** summarizes the input, pullup, wired-or mode, and SPI pin programming.

Table 7-9: PC0/SCK I/O Pin Functions

DDR	Output Latch	SPCR SPE	SPCR MSTR	WOMR CWOM	RCR2 RC bit	I/O Pin Modes	Access to DDRC0	Access to Data Register Latch PC0	
							Read/Write	Read	Write
0	X	0	X	X	0	Port IN, Hi-Z	DDRC0	Pin	Latch*
0	X	0	X	X	1	Port IN, Pullup	DDRC0	Pin	Latch*
1	X	0	X	0	X	OUT, CMOS	DDRC0	Latch	Latch, Pin
1	0	0	X	1	X	OUT, OD	DDRC0	Latch	Latch, Pin
1	1	0	X	1	0	OUT, OD, Hi-Z	DDRC0	Latch	Latch, Pin
1	1	0	X	1	1	OUT, OD, Pullup	DDRC0	Latch	Latch, Pin
0	X	1	0	X	0	SCK IN, Hi-Z	DDRC0	Pin	Latch*
1	X	1	0	X	0	SCK IN, Hi-Z	DDRC0	Latch	Latch*
0	X	1	1	0	0	SCK OUT, CMOS, Hi-Z	DDRC0	Pin	Latch*
0	X	1	1	0	1	SCK OUT, CMOS, Pullup	DDRC0	Pin	Latch*
1	X	1	1	0	0	SCK OUT, CMOS, Hi-Z	DDRC0	Latch	Latch*
1	X	1	1	0	1	SCK OUT, CMOS, Pullup	DDRC0	Latch	Latch*
0	X	1	1	1	0	SCK OUT, OD, Hi-Z	DDRC0	Pin	Latch*
0	X	1	1	1	1	SCK OUT, OD, Pullup	DDRC0	Pin	Latch*
1	X	1	1	1	0	SCK OUT, OD, Hi-Z	DDRC0	Latch	Latch*
1	X	1	1	1	1	SCK OUT, OD, Pullup	DDRC0	Latch	Latch*

Note:
1. X is don't care state.
2. * Does not affect input, but stored to Data Register Latch

Table 7-10: PC1/SDO I/O Pin Functions

DDR	Output Latch	SPCR SPE	WOMR CWOM	RCR2 RC bit	I/O Pin Modes	Access to DDRC1	Access to Data Register Latch PC1	
						Read/Write	Read	Write
0	X	0	X	0	Port IN, Hi-Z	DDRC1	Pin	Latch*
0	X	0	X	1	Port IN, Pullup	DDRC1	Pin	Latch*
1	X	0	0	X	Port OUT, CMOS	DDRC1	Latch	Latch, Pin
1	0	0	1	X	Port OUT, OD	DDRC1	Latch	Latch, Pin
1	1	0	1	0	Port OUT, OD, Hi-Z	DDRC1	Latch	Latch, Pin
1	1	0	1	1	Port OUT, OD, Pullup	DDRC1	Latch	Latch, Pin
0	X	1	0	0	SDO OUT, CMOS, Hi-Z	DDRC1	Pin	Latch*
0	X	1	0	1	SDO OUT, CMOS, Pullup	DDRC1	Pin	Latch*
1	X	1	0	0	SDO OUT, CMOS, Hi-Z	DDRC1	Latch	Latch*
1	X	1	0	1	SDO OUT, CMOS, Pullup	DDRC1	Latch	Latch*
0	X	1	1	0	SDO OUT, OD, Hi-Z	DDRC1	Pin	Latch*
0	X	1	1	1	SDO OUT, OD, Pullup	DDRC1	Pin	Latch*
1	X	1	1	0	SDO OUT, OD, Hi-Z	DDRC1	Latch	Latch*
1	X	1	1	1	SDO OUT, OD, Pullup	DDRC1	Latch	Latch*

Note:
1. X is don't care state.
2. * Does not affect input, but stored to Data Register Latch

Table 7-11: PC2/SDI I/O Pin Functions

DDR	Out-put Latch	SPCR SPE	WOMR CWOM	RCR2 RC	I/O Pin Modes	Access to DDRC2	Access to Data Register Latch PC2	
						Read/Write	Read	Write
0	X	0	X	0	Port IN, Hi-Z	DDRC2	Pin	Latch*
0	X	0	X	1	Port IN, Pullup	DDRC2	Pin	Latch*
1	0	0	X	X	Port OUT, OD	DDRC2	Latch	Latch, Pin
1	1	0	X	0	Port OUT, OD, Hi-Z	DDRC2	Latch	Latch, Pin
1	1	0	X	1	Port OUT, OD, Pullup	DDRC2	Latch	Latch, Pin
0	X	1	X	0	SDI IN, Hi-Z	DDRC2	Pin	Latch*
0	X	1	X	1	SDI IN, Pullup	DDRC2	Pin	Latch*
1	X	1	X	0	SDI IN, Hi-Z	DDRC2	Latch	Latch*
1	X	1	X	1	SDI IN, Pullup	DDRC2	Latch	Latch*

Note:
1. X is don't care state.
2. * Does not affect input, but stored to Data Register Latch

Table 7-12: PC3/$\overline{IRQ}$ I/O Pin Functions

DDR	Output Latch	INTCR IRQE	WOMR CWOM	RCR2 RC bit	I/O Pin Modes	Access to DDRC3	Access to Data Register Latch PC3	
						Read/Write	Read	Write
0	X	0	X	0	Port IN, Hi-Z	DDRC3	Pin	Latch*
0	X	0	X	1	Port IN, Pullup	DDRC3	Pin	Latch*
0	X	1	X	0	Port IN, Hi-Z, IRQ	DDRC3	Pin	Latch*
0	X	1	X	1	Port IN, Pullup, IRQ	DDRC3	Pin	Latch*
1	0	0	X	X	Port OUT, OD	DDRC3	Latch	Latch, Pin
1	1	0	X	0	Port OUT, OD, Hi-Z	DDRC3	Latch	Latch, Pin
1	1	0	X	1	Port OUT, OD, Pullup	DDRC3	Latch	Latch, Pin
1	0	1	X	X	Port OUT, OD, IRQ	DDRC3	Latch	Latch, Pin
1	1	1	X	0	Port OUT, OD, Hi-Z, IRQ	DDRC3	Latch	Latch, Pin
1	1	1	X	1	Port OUT, OD, Pullup, IRQ	DDRC3	Latch	Latch, Pin

Note:
1. X is don't care state.
2. * Does not affect input, but stored to Data Register Latch

7.4 I/O PORT PROGRAMMING

All bidirectional I/O pins can be programmed as inputs or outputs.

7.4.1 PIN DATA DIRECTION

The direction of a pin is determined by the state of its corresponding bit in the associated port Data Direction Register (DDR). A pin is configured as an output if its corresponding DDR bit is set to a logic one. A pin is configured as an input if its corresponding DDR bit is cleared to a logic zero.

The data direction bits DDRA0 thru DDRA7, DDRB0 thru DDRB7, and DDRC0 thru DDRC3 are read/write bits which can be manipulated with read-modify-write instructions. At power-on or reset, all DDRs are cleared, which configures all I/O port pins as input (except Port B is configured as an LCD port).

7.4.2 OUTPUT PIN

When an I/O pin is programmed as an output pin, the state of the corresponding data register bit will determine the state of the pin. The state of the data register bits can be altered by writing to address $0000 for Port A, address $0001 for Port B, and address $0002 for Port C. Reads of the corresponding data register bit at address $0000 or $0003 will return the state of the data register bit (not the state of the I/O pin itself). Therefore bit manipulation is possible on all pins programmed as outputs.

7.4.3 INPUT PIN

When an I/O pin is programmed as an input pin, or for an input only pin, the state of the pin can be determined by reading the corresponding data register bit. Any writes to the corresponding data register bit for an input only pin will be ignored.

If the corresponding bit in the pullup register is set the input pin will have an activated pullup device. Since the pullup register bits are read-write, bit manipulation may be used on these register bits.

7.4.4 I/O PIN TRANSITIONS

A "glitch" can be generated on an I/O pin when changing it from an input to an output unless the data register is first pre-conditioned to the desired before changing the corresponding DDR bit from a zero to a one.

7.4.5 I/O PINS WITH SUB-SYSTEMS

An I/O pin that is shared with another sub-system is in general configured as an input pin during reset, except for LCD driver pins. The LCD driver output pins BP0:BP3 and FP0:FP24 are configured to output V_{DD} level during and after reset. See truth tables of each I/O ports for more details.

Table 7-13: Port Control Register Bits Summary

Port	bit	DDR	WOM	Pull-up R		Module Control		Module
A	0	DDRA0	1	RAL	50 KΩ	KWIE	KWIE0	KWI0
	1	DDRA1	1				KWIE1	KWI1
	2	DDRA2	1				KWIE2	KWI2
	3	DDRA3	1			BZPE, KWIE	BZxx, KWIE3	KWI3/BZ
	4	DDRA4	AWOM	RAH		ADON, EVCE	CH2:0/EVxx	AD0/EVI
	5	DDRA5				ADON	CH2:0	AD1
	6	DDRA6				RME	TBCLK, RMC4:0	RMO
	7	DDRA7				PWCE	PWxx	PWCI
B	0	DDRB0	BWOML	RBL	50 KΩ	LCDE, PBEL	F24B3:0	FP24
	1	DDRB1					F23B3:0	FP23
	2	DDRB2					F22B3:0	FP22
	3	DDRB3					F21B3:0	FP21
	4	DDRB4	BWOMH	RBH		LCDE, PBEH	F20B3:0	FP20
	5	DDRB5					F19B3:0	FP19
	6	DDRB6					F18B3:0	FP18
	7	DDRB7					F17B3:0	FP17
C	0	DDRC0	CWOM	RC	10 KΩ	SPE	MSTR, SPR	SCK
	1	DDRC1					DORD, SPR	SDO
	2	DDRC2	1					SDI
	3	DDRC3	1			IRQE	IRQS	IRQ

Note:

1. Pull-up Resistor resistances are typical values with V_{DD}=3V.
2. Port C bits 2:3 are open drain outputs and do not have CMOS drive capability.

7.4.6 RESISTOR CONTROL REGISTER1 (RCR1)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
OPTN $0008	RESISTOR CONTROL REG. RCR1	R	0	0	0	0	RBH	RBL	RAH	RAL
		W	—	—	—	—				
RESET:			0	0	0	0	0	0	0	0

Figure 7-20: Resistor Control Register 1

BITS7:4 Reserved

These bits are not used and always read as 0.

RBH Port B pull up Resistor (H)

When this bit is set, pull up resistor is connected to upper 4 bits of Port B pins. However for those pins configured as CMOS output, or open drain output with output of logic low the pull up resistors are disabled. This bit is cleared on reset.

RBL Port B pull up Resistor (L)

When this bit is set, pull up resistor is connected to lower 4 bits of Port B pins. However for those pins configured as CMOS output, or open drain output with output of logic low the pull up resistors are disabled. This bit is cleared on reset.

RAH Port A pull up Resistor (H)

When this bit is set, pull up resistor is connected to upper 4 bits of Port A pins. However for those pins configured as CMOS output, or open drain output with output of logic low the pull up resistors are disabled. This bit is cleared on reset.

RAL Port A pull up Resistor (L)

When this bit is set, pull up resistor is connected to lower 4 bits of Port A pins. However for those pins configured as CMOS output, or open drain output with output of logic low the pull up resistors are disabled. This bit is cleared on reset.

7.4.7 RESISTOR CONTROL REGISTER2 (RCR2)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
OPTN $0009	RESISTOR CONTROL REG. RCR2	R	0	0	0	0	0	0	0	RC
		W	—	—	—	—	—	—	—	
		RESET:	0	0	0	0	0	0	0	0

Figure 7-21: Resistor Control Register 2

BITS7:1 Reserved

These bits are not used and always read as 0.

RC Port C pull up Resistor

When RC bit is set, pull up resistor is connected to all 4 bits of Port C pins. However for those pins configured as CMOS output, or open drain output with output of logic low the pull up resistors are disabled. This bit is cleared on reset.

7.4.8 OPEN DRAIN OUTPUT CONTROL REGISTER (WOM)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
OPTN $000A	WIRED-OR MODE REG WOMR	R	BWOMH	BWOML	0	0	0	CWOM	AWOM	0
		W			—	—	—			—
RESET:			0	0	0	0	0	0	0	0

Figure 7-22: Wired-OR Mode Register

BITS5:3 Reserved

These bits are not used and always return 0.

CWOM Port C Open Drain Mode

When this bit is set, Port C pins that are configured as output becomes open drain outputs. This bit is cleared on reset.

AWOM Port A Open Drain Mode (high nibble)

When this bit is set, upper 4 bits of Port A pins that are configured as output becomes open drain outputs. This bit is cleared on reset.

BIT0 Reserved

This bit is not used and always return 0.

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SECTION 8OSCILLATORS AND CLOCK

The MC68HC705L26 has dual on-chip oscillators for typ. 4.0 MHz and 32.768 KHz crystals. Refer to **Figure 8-1**. The clock generated is used by the CPU and by the subsystem modules such as Time Base and LCD. Refer to **Figure 8-2**.

8.1 OSC CLOCK DIVIDER AND POR COUNTER

The OSC clock is divided by a 7 bit counter which is used for the system clock, Time Base and POR Counter. Clocks divided by 2, 4, and 64 are available for the system clock selections and clock divided by 128 is provided for the Time Base and POR Counter.

The POR counter is a 6 bit clock counter that is driven by the OSC divided by128. The overflow of this counter is used for setting FTUP bit, release of power on reset (POR), and resuming operation from STOP mode.

The 7 bit divider and POR counter are initialized to $0078 by the following conditions.

- Power on detection
- When FOSCE bit is cleared

8.2 SYSTEM CLOCK CONTROL

The system clock is provided for all internal modules except Time Base.

Both OSC and XOSC are available as the system clock source. The divide ratio is selected by the SYS1 and SYS0 bits in the MISC register.

By default OSC divided by 2 is selected on reset.

Table 8-1: System Bus Frequency Selection

SYS1	SYS0	Divide Ratio	CPU Bus Frequency (Hz)		
			OSC = 4.0 M	OSC = 4.1943 M	XOSC = 32.768 K
0	**0**	**OSC Divided by 2**	**2.0 M**	**2.0972 M**	**—**
0	1	OSC Divided by 4	1.0 M	1.0486 M	—
1	0	OSC Divided by 64	62.5 K	65.536 K	—
1	1	XOSC Divided by 2	—	—	16.384 K

8.3 OSC AND XOSC

The secondary oscillator (XOSC) runs continuously after Power-Up. The main oscillator (OSC) can be stopped to conserve power via the STOP instruction or the FOSCE bit in the MISC register. The effects of restarting the OSC will vary depending on current state of the MCU, including SYS0:1 and FOSCE bits.

8.3.1 OSC ON LINE

If the system clock is OSC, FOSCE should remain set. Executing the STOP instruction in this condition will halt OSC, put the MCU into a low power mode and clear the 6-bit POR counter. The 7-bit divider is not initialized. Exiting STOP with external IRQ or Reset re-starts the oscillator. When the POR counter overflows, internal Reset is released and execution can begin. The stabilization time will vary between 8064 and 8192 counts.

NOTE: Exiting STOP with external Reset will always return the MCU to the state as defined by the register definitions prior to executing the STOP instruction. i.e. SYS0:1=1:0, FOSCE=1.

8.3.2 XOSC ON LINE

If XOSC is the System Clock (SYS0:1=1:1), OSC can be stopped either by the STOP instruction or by clearing the FOSCE bit.

The sub oscillator (XOSC) never stops except during power down. This clock may also be used as the clock source of the system clock and Time Base.

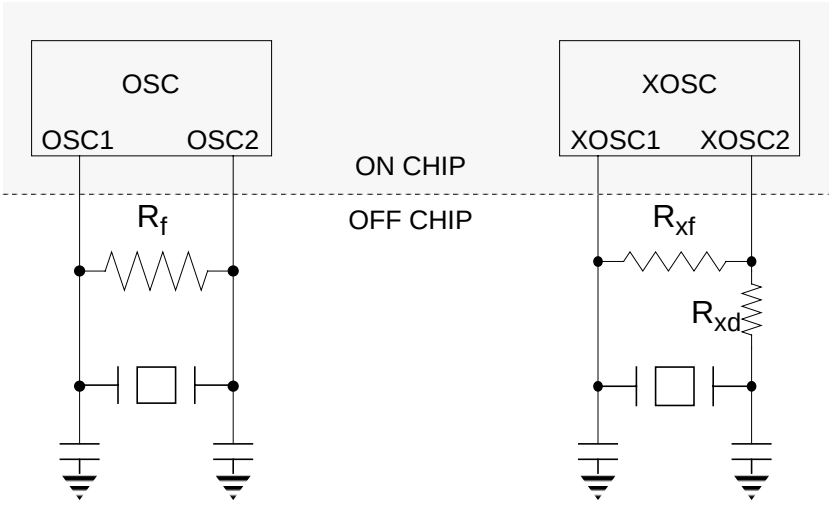


Figure 8-1: OSC1, OSC2, XOSC1, and XOSC2

8.3.2.1 XOSC WITH FOSCE=1

If the System Clock is XOSC and FOSCE=1, executing the STOP instruction will halt OSC, put the MCU into a low power mode and clear the 6-bit POR counter. The 7-bit divider is not initialized. Exiting STOP with external IRQ re-starts the oscillator, however execution begins immediately using XOSC. When the POR counter overflows, FTUP is set signaling that OSC is stable and OSC can be used as the System Clock. The stabilization time will vary between 8064 and 8192 counts.

8.3.2.2 XOSC WITH FOSCE=0

If XOSC is the System Clock, clearing FOSCE will stop OSC, and preset the 7-bit divider and 6-bit POR counter to $0078. Execution will continue with XOSC and when FOSCE is set again, OSC will re-start. When the POR counter overflows, FTUP is set signaling that OSC is stable and OSC can be used as the System Clock. The stabilization time will be 8072 counts.

8.3.2.3 XOSC WITH FOSCE=0 AND STOP

If XOSC is the System Clock and FOSCE is cleared, further power reduction can be achieved by executing the STOP instruction. In this case OSC is stopped, the7-bit divider and 6-bit POR counter is preset to $0078 (since FOSCE=0) and execution is halted. Exiting STOP with external IRQ does not re-start the OSC, however execution begins immediately using XOSC. OSC may be re-started by setting FOSCE, and when the POR counter overflows, FTUP be will set signaling that OSC is stable and can be used as the System Clock. The stabilization time will be 8072 counts.

8.4 STOP AND WAIT MODES

During STOP mode the main oscillator (OSC) is shut down and the clock path from the second oscillator (XOSC) is disconnected, such that all modules except Time Base are halted. Entering STOP mode clears FTUP flag in the MISC register, and initializes POR counter. The STOP mode is exited by RESET, IRQ, KWI, SPI (slave mode), or TBI Interrupt.

If OSC is selected as system clock source during STOP mode, CPU resumes after the overflow of POR counter and this overflow also sets FTUP status flag.

If XOSC is selected as system clock source during STOP mode, no stop recovery time is required for exiting STOP mode because XOSC never stops and re-start of main oscillator depends on FOSCE bit.

During WAIT mode, only the CPU clocks are halted and the peripheral modules are not affected. The WAIT mode is exited by the RESET and any interrupts.

Table 8-2: CPU Start-up Time Requirements

Before RESET or Interrupt			Power ON RESET	External RESET	Exit STOP Mode by an Interrupt
CPU Clock Source	CPU	FOSCE			
—	—	—	Delay	—	—
OSC (OSC ON)	RUN	1	—	No Delay	—
OSC (OSC OFF)	RUN	0[1]	—	Delay	—
	STOP	1	—	Delay	Delay
	STOP	0[2]	—	Delay	Delay
XOSC (OSC ON)	RUN	1	—	No Delay	—
XOSC (OSC OFF)	RUN	0	—	Delay	—
	STOP	1	—	Delay	No Delay
	STOP	0	—	Delay	No Delay

Note:
1. Do not enter this state
2. This state does not exist

NOTE: Power ON RESET is strictly for power on conditions and does not function as detecting drop in power.

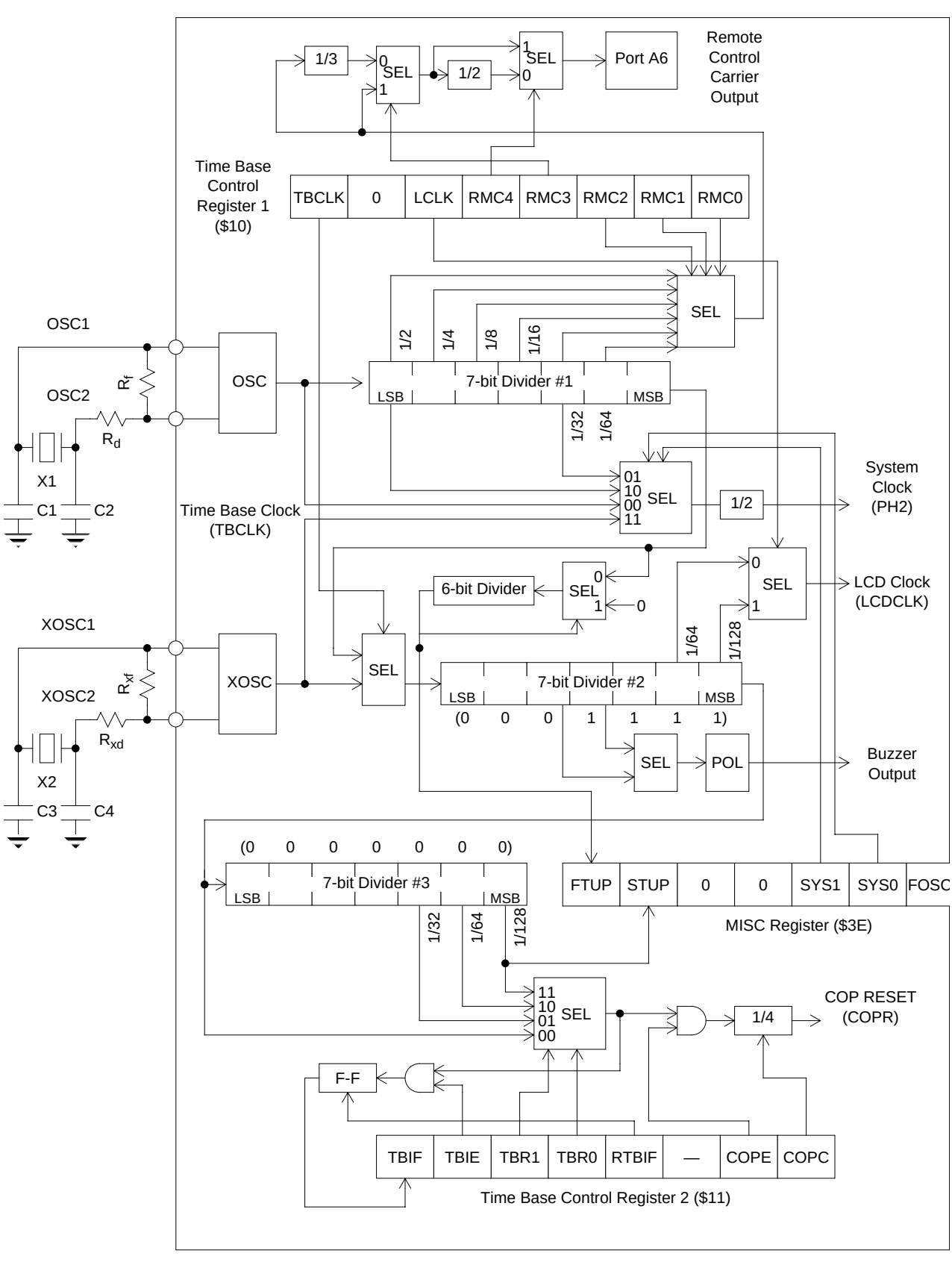


Figure 8-2: Clock Signal Distribution

8.5 XOSC CLOCK DIVIDER AND POD COUNTER

The XOSC clock divided by a 14 bit counter, also called Power on Divider (POD), is used for the system clock. Oscillator clock divided by 2 is used by the system clock and oscillator clock divided by 64 or 128 is provided for the LCD module.

The overflow of POD counter is used for setting STUP bit and release of power on reset (POR). The 14 bit divider/ POD counter is initialized to $0078 by Power on detection.

8.6 SYSTEM CLOCK CONTROL

The system clock (PH2) is provided for CPU and all internal modules.

8.7 XOSC

The oscillator (XOSC) runs continuously after Power-Up. The XOSC never stops while power is applied.

8.8 STOP AND WAIT MODES

Power reduction can be achieved by executing the STOP instruction and halting the CPU. During STOP mode CPU and all modules except Time Base are halted. The STOP mode is exited by external $\overline{\text{RESET}}$, COP reset, $\overline{\text{IRQ}}$, SPI (slave mode), or TB Interrupt. The CPU resumes immediately from STOP mode since XOSC never stops oscillating during STOP mode.

The CPU clock is halted and the peripheral modules are not affected during WAIT mode. The WAIT mode is exited by the RESET or any interrupts.

Mode Before RESET or Interrupt	Delay Time After RESET or Interrupt		
	Power ON RESET	COP and External RESET	Exit STOP Mode by Interrupt
POWER OFF	Delay	—	—
RUN	†	No Delay	—
STOP/WAIT	†	No Delay	No Delay

NOTE: † Power ON RESET is strictly for power on conditions and does not function as detecting drop in power.

Table 8-3: Recovery Time Requirements

8.9 MISCELLANEOUS REGISTER (MISC)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$003E	MISCELLANEOUS REGISTER MISC	R	FTUP	STUP	0	0	SYS1	SYS0	FOSCE	OPTM
		W	—	—	—	—				
	RESET:		U	U	0	0	0	0	0	0

Figure 8-3: Miscellaneous Register

FTUP OSC Time Up Flag

Power on detection and clearing FOSCE bit clears this bit. This bit is set by the overflow of the POR counter. An reset does not affect this bit.

read:
1 = OSC clock is available for the system clock
0 = during POR or OSC shut down

STUP XOSC Time Up Flag

The power on detection clears this bit. This bit is set after the Time Base has counted 16264 clocks. An reset does not affect this bit.

read:

1 = XOSC clock is available for the system clock
0 = XOSC is not stabilized or no signal on XOSC1 : XOSC2 pins

BITS5:4 Reserved

These bits are not used and always read as 0.

SYS1:0 System Clock Select

These two bits select the system clock source. On reset the SYS1 and SYS0 bits are initialized to 0 and 0, respectively.

Table 8-4: System Bus Frequency Selection

SYS1	SYS0	Divide Ratio	Φ2 CPU Bus Frequency (Hz)		
			OSC = 4.0 M	OSC = 4.1943 M	XOSC = 32.768 K
0	**0**	**OSC Divided by 2**	**2.0 M**	**2.0972 M**	—
0	1	OSC Divided by 4	1.0 M	1.0486 M	—
1	0	OSC Divided by 64	62.5 K	65.536 K	—
1	1	XOSC Divided by 2	—	—	16.384 K

OPTM Option Map Select

The OPTM bit selects one of two register maps at $0000:$000F. This bit is cleared on reset.

1 = Option map is selected
0 = Main register map is selected

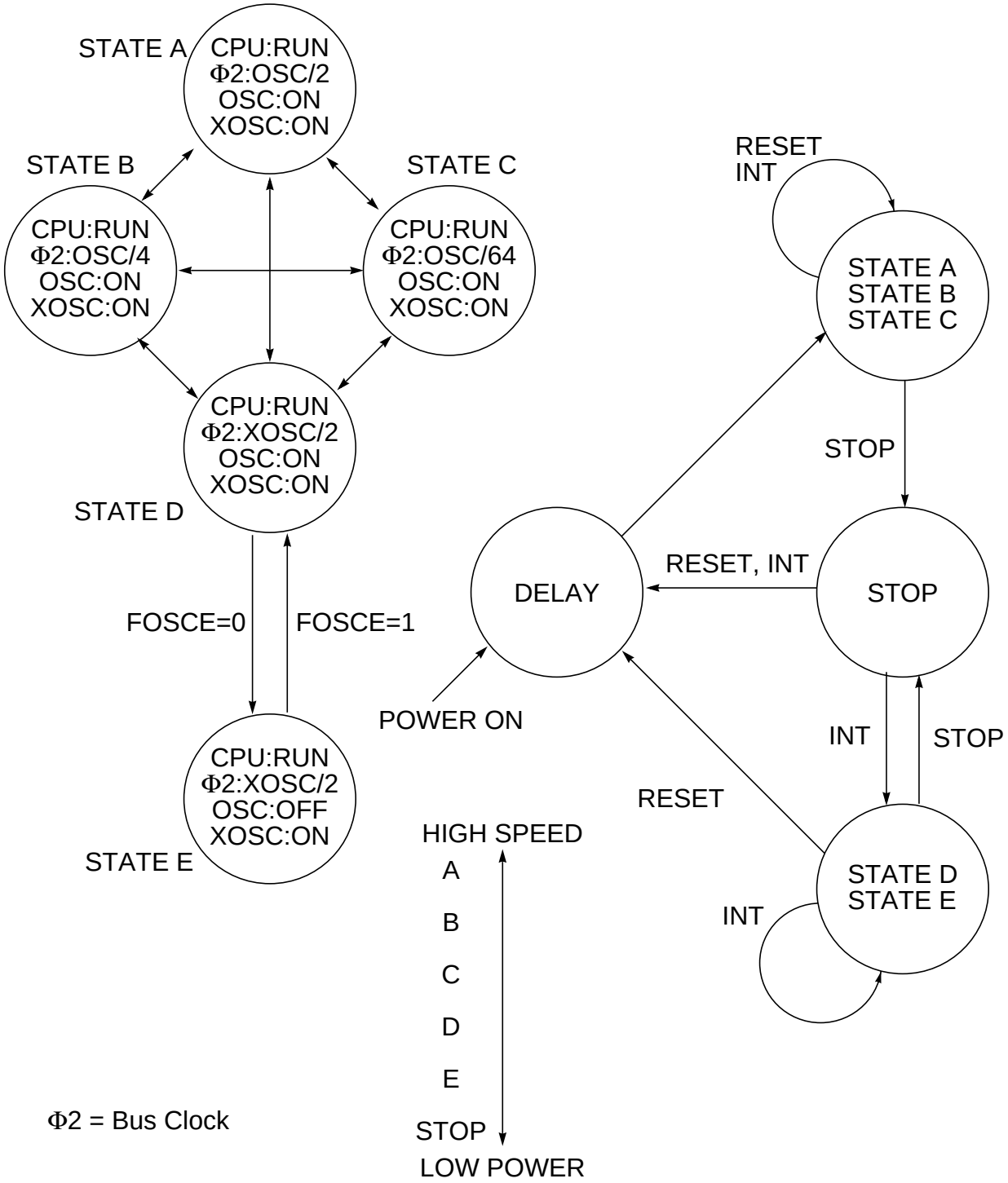


Figure 8-4: Clock State and STOP/POD Delay Diagram

SECTION 9TIME BASE

Time Base is a 14 bit up-counter which is clocked by XOSC.

This 14 bit divider is initialized to $0078 only upon power on reset (POD). After counting 16264 clocks, the STUP bit in the MISC register is set. See **Figure 8-2** for more information.

9.1 TIME BASE SUB-MODULES

The clock divided by the Time Base are used for LCDCLK, STUP, TBI, and COP. The Time Base clock can be provided either from OSC or XOSC.

9.1.1 LCDCLK

One of four clock frequency combinations may be selected for the LCD clock.

Table 9-1: LCD Clock Frequency

TBCR1		Divide Ratio	LCD Clock Frequency (Hz) (F_{XOSC} = 32.768 KHz)		
.TB-CLK	.LCLK		OSC = 2.0 MHz	OSC = 4.0 MHz	OSC = 4.1943 MHz
0	0	XOSC / 64	512	512	512
0	1	XOSC / 128	256	256	256
1	0	OSC / 8192	244	488	512
1	1	OSC / 16384	122	244	256

9.1.2 STUP

Time Base divider is initialized to $0078 at power on and when the count reaches 16264, STUP flag in the MISC register is set. Once STUP flag is set, it is never cleared while power is applied.

9.1.3 TBI

Time Base interrupt may be generated every 0.5, 0.25, 0.125, or 0.0039 seconds with 32.768 kHz crystal at XOSC pins. See **Table 9-2**.

Time Base Interrupt Flag (TBIF) is set every period and interrupt is requested if the enable bit (TBIE) is set. The clock divided by 128, 4096, 8192, or 16384 is used to set TBIF, and this clock is selected by the TBR1 and TBR0 bits in the TBCR2 register.

Table 9-2: Time Base Interrupt Frequency

TBCR2		Divide Ratio	Frequency (Hz)		
TBR1	TBR0		OSC = 4.0 MHz	OSC = 4.1943 MHz	XOSC = 32.768 KHz
0	0	TBCLK / 128	244	256	256
0	1	TBCLK / 4096	7.63	8.00	8.00
1	0	TBCLK / 8192	3.81	4.00	4.00
1	1	TBCLK / 16384	1.91	2.00	2.00

9.1.4 COP

The Computer Operating Properly Watchdog Timer (COP) on the MC68HC705L26 is controlled by the COPE and COPC bits in the TBCR2 register.

The COP uses the same clock as TBI that is selected by the TBR1 and TBR0 bits. The TBI clock is divided by 4 and overflow of this divider generates COP time-out reset if the COP enable (COPE) bit is set. The COP time-out reset has the same vector address as Power On and external RESET. To prevent the COP time-out the COP divider is cleared by writing a 1 to the COP Clear (COPC) bit.

When the Time Base divider is driven by the OSC clock, the clock for the divider is suspended during STOP mode or when FOSCE is equal to 0. This may cause stretching of the COP period or no COP timeout reset occurring when there is a processing error. Thus it is recommended that XOSC clock be used as the clock source for Time Base to avoid these problems.

When the COP is enabled during STOP mode and the Time Base is driven by the XOSC clock, the divider does not stop counting and the COPC bit must be triggered to prevent the COP time-out. Therefore it is recommended that the COP Watchdog should be disabled for a system that must have intentional use of the STOP mode period longer than the COP time-out period.

Table 9-3: COP Time-Out Period

TBCR2		COP Period (m Sec)					
TBR1	TBR0	OSC = 4.0 MHz		OSC = 4.1943 MHz		XOSC = 32.768 KHz	
		min	max	min	max	min	max
0	0	12.3	16.4	11.7	15.6	11.7	15.6
0	1	393	524	375	500	375	500
1	0	786	1048	750	1000	750	1000
1	1	1573	2097	1500	2000	1500	2000

9.1.5 REMOTE CONTROL CARRIER GENERATOR

The PA6/RMO pin functions as general purpose I/O port after RESET. The RMPE bit must be set in order to use this port as Remote control carrier output. The RMO outputs idle state is set by RPOL bit when RMON is cleared. The RMCLK signal selected by RMC4:0 bits is output on the pin when RMON is set.

Table 9-4: Remote Carrier Frequency Selection

RMC4	RMC3	RMC2:0	RMO Duty	Divider	Remote Carrier Frequency on RMO pin (RMCLK)		
					OSC = 440 KHz	OSC = 3.6 MHz	OSC = 4.0 MHz
0	1	0	50%	1/4	110 KHz	900 KHz	1000 KHz
		1		1/8	55.0 KHz	450 KHz	500 KHz
		2		1/16	27.5 KHz	225 KHz	250 KHz
		3		1/32	13.8 KHz	113 KHz	125 KHz
		4		1/64	6.88 KHz	56.3 KHz	62.5 KHz
		5		1/128	3.44 KHz	28.1 KHz	31.3 KHz
	0	0	50%	1/12	36.7 KHz	300 KHz	333 KHz
		1		1/24	18.3 KHz	150 KHz	167 KHz
		2		1/48	9.17 KHz	75.0 KHz	83.3 KHz
		3		1/96	4.58 KHz	37.5 KHz	41.7 KHz
		4		1/192	2.29 KHz	18.8 KHz	20.8 KHz
		5		1/384	1.15 KHz	9.38 KHz	10.4 KHz
1	1	0	50%	1/2	220 KHz	1800 KHz	2000 KHz
		1		1/4	110 KHz	900 KHz	1000 KHz
		2		1/8	55.0 KHz	450 KHz	500 KHz
		3		1/16	27.5 KHz	225 KHz	250 KHz
		4		1/32	13.8 KHz	113 KHz	125 KHz
		5		1/64	6.88 KHz	56.3 KHz	62.5 KHz
	0	0	33%	1/6	73.3 KHz	600 KHz	667 KHz
		1		1/12	36.7 KHz	300 KHz	333 KHz
		2		1/24	18.3 KHz	150 KHz	167 KHz
		3		1/48	9.17 KHz	75.0 KHz	83.3 KHz
		4		1/96	4.58 KHz	37.5 KHz	41.7 KHz
		5		1/192	2.29 KHz	18.8 KHz	20.8 KHz

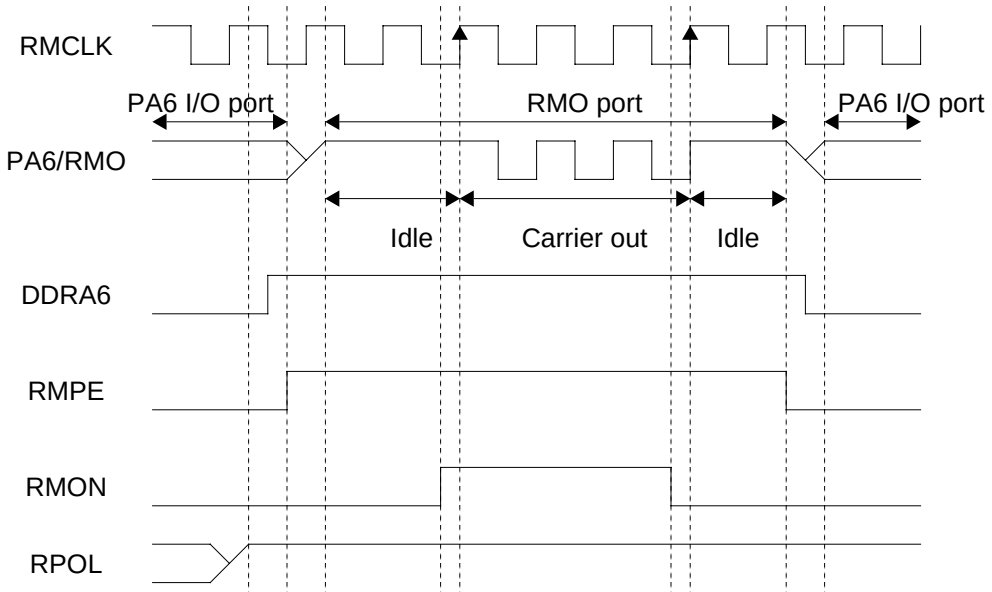


Figure 9-1: Remote Control Carrier Output Port Control (RPOL=1)

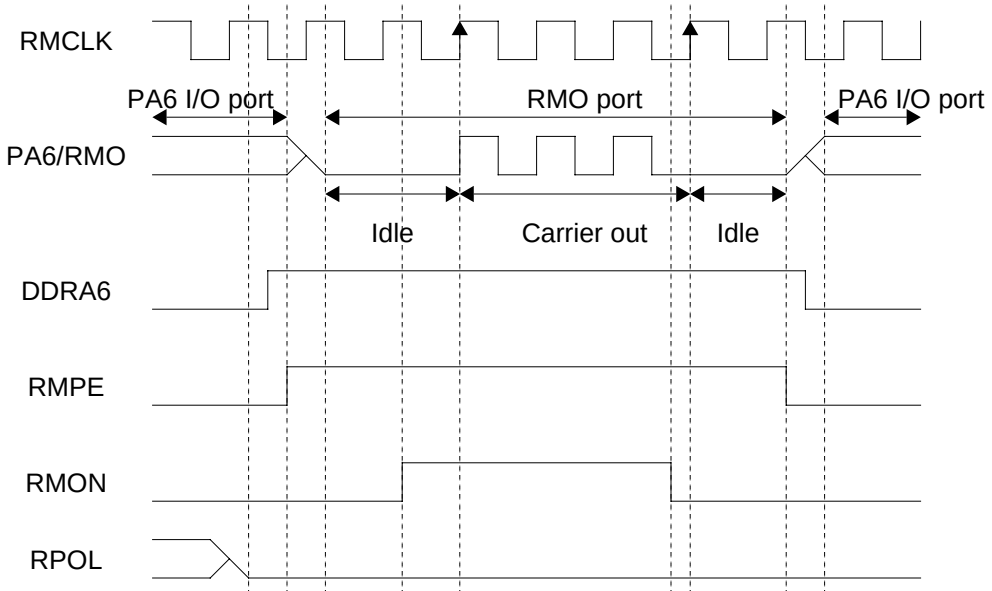


Figure 9-2: Remote Control Carrier Output Port Control (RPOL=0)

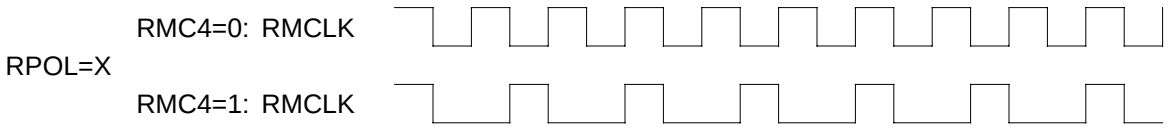


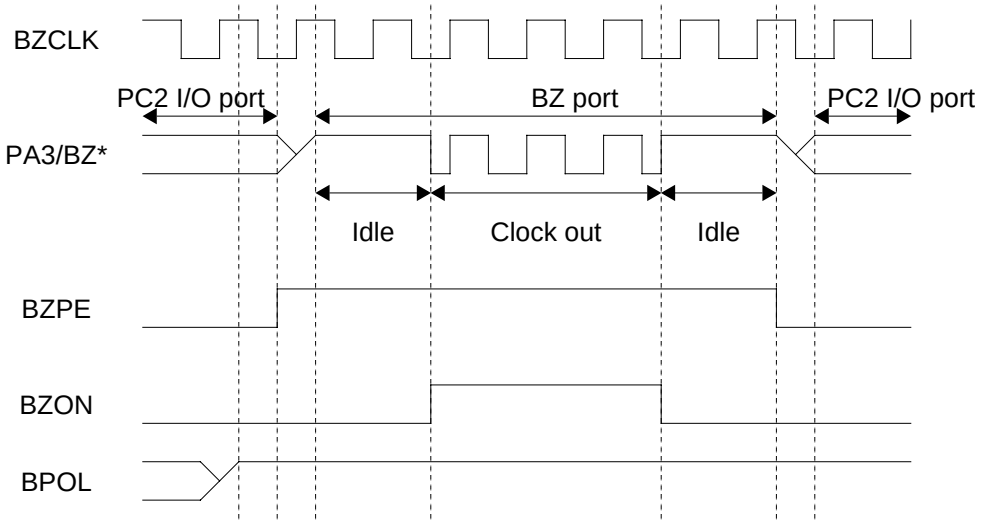
Figure 9-3: Remote Control Carrier Duty Control

9.1.6 BUZZER TONE GENERATOR

The PA3/$\overline{KWI3}$/BZ pin functions as general purpose I/O port after RESET. The BZPE bit must be set in order to use this port as Buzzer tone output. The BZ outputs idle state is set by BPOL bit when BZON is cleared. The BZCLK signal selected by BCLK bit is output on the pin when BZON is set. The BZ output pin is open drain.

Table 9-5: Buzzer Frequency

TBCR0 .BCLK	TBCR1 .TBCLK	Buzzer Frequency on BZ pin (BZCLK)			
		(Fosc = 2 MHz Fxosc = 32.768 KHz)	(Fosc = 3.6 MHz Fxosc = 32.768 KHz)	(Fosc = 4 MHz Fxosc = 32.768 KHz)	(Fosc = 4.194304 MHz Fxosc = 32.768 KHz)
0	0	approx. 977 Hz	approx. 1758 Hz	approx. 1953 Hz	2048 Hz
0	1	2048 Hz	2048 Hz	2048 Hz	2048 Hz
1	0	approx. 1953 Hz	approx. 3516 Hz	approx. 3906 Hz	4096 Hz
1	1	4096 Hz	4096 Hz	4096 Hz	4096 Hz



* The BZ output pin is open drain. The logic "1" shown for BZ pin is actually a Hi-Z state unless pullup.

Figure 9-4: Buzzer Tone Output Control

9.2 TIME BASE CONTROL REGISTER 1 (TBCR1)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$0010	TIME BASE CONTROL REG 1 TBCR1	R	TBCLK	0	LCLK	RMC4	RMC3	RMC2	RMC1	RMC0
		W		—						
	RESET:		0	0	0	0	0	0	0	0

Figure 9-5: Time Base Control Register 1

TBCLK Clock Source

This bit selects the Time Base clock source. This bit is cleared on reset.

1 = OSC is selected for Time Base clock source
0 = XOSC is selected for the Time Base clock source

BIT6 Reserved

This bit is not used and always read as 0.

LCLK LCD Clock

The LCLK bit selects clock for the LCD driver. This bit is cleared on reset.

When TBCLK=0:

1 = XOSC Divide by 128 is selected for the LCD clock
0 = XOSC Divide by 64 is selected for the LCD clock

When TBCLK=1:

1 = OSC Divide by 16384 is selected for the LCD clock
0 = OSC Divide by 8192 is selected for the LCD clock

RMC4 Remote Control Generator Divider

This bit selects the remote control carrier duty cycle. This bit is cleared on reset.

1 = 33-67% duty is selected if RMC3=0.
0 = 50-50% duty is selected.

RMC3:0 Remote Control Generator Divider

These bits select the remote control carrier frequency. See **Table 9-4**.These bits are cleared on reset.

9.3 TIME BASE CONTROL REGISTER 2 (TBCR2)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$0011	TIME BASE CONTROL REG 2 TBCR2	R	TBIF	TBIE	TBR1	TBR0	0	0	COPE	0
		W	—				RTBIF	—		COPC
RESET:			0	0	1	1	0	0	0	0

Figure 9-6: Time Base Control Register 2

TBIF Time Base Interrupt Flag

The TBIF bit is set every time-out interval of the Time Base Interrupt. This bit is read only bit and is cleared by writing a 1 to the TBIF bit. Reset clears TBIF bit. Time Base interrupt period between reset and first TBIF depends on the time elapsed during reset, since time base divider is not initialized on reset.

TBIE Time Base Interrupt Enable

The TBIE bit enables the Time Base Interrupt capability. If TBIF = 1 and TBIE = 1, the Time Base Interrupt is generated.

1 = TB Interrupt requested when TBIF = 1
0 = TB interrupt is disabled

TBR1:0 Time Base Interrupt Rate Select

The TBR1 and TBR0 bits select one of four rates for the Time Base Interrupt period. The TBI rate is also related to the COP time-out reset period. See **Table 9-1** and **Table 9-3**. These bits are set to 1 on reset.

RTBIF Reset TB Interrupt Flag

The RTBIF bit is a write only bit and always read as 0. Writing 1 to this bit clears the TBIF bit and writing 0 to this bit has no effect.

1 = reset TBIF
0 = no effect

COPE COP Enable

When the COPE bit is 1, COP reset function is enabled. This bit is cleared on reset (including COP time-out reset) and write to this bit is allowed only once after reset.

1 = COP is enabled
0 = COP is disabled

COPC COP Clear

Writing 1 to COPC bit clears the 2 bit divider to prevent COP time out. (The COP time-out period depends on the TBI rate.) This bit is write only bit and returns 0 when read.

1 = Clear COP time-out divider
0 = no effect

9.4 TIME BASE CONTROL REGISTER 3 (TBCR3)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$001F	TIME BASE CONTROL REG 3 TBCR3	R	0	RMON	RPOL	RMPE	BCLK	BZON	BPOL	BZPE
		W	—							
	RESET:		0	0	0	0	0	0	0	0

Figure 9-7: Time Base Control Register 3

BIT7 Reserved

This bit is not used and always reads as 0.

RMON ReMote control generator signal ON

When the port is used as Remote control output (RMPE=1) this bit turns on or off the remote control signal. The idle state is output when cleared. This bit is cleared on reset.

1 = Carrier is on
0 = Carrier is off; idle state defined by RPOL is output

RPOL Remote control idle POLarity

This bit controls the idle state of the remote control generator output on the port. This bit is cleared on reset.

1 = Remote idle state outputs logic "1".
0 = Remote idle state outputs logic "0".

RMPE ReMote control generator Port output Enable

This bit enables the remote control generator output on the port. The actual remote signal on/off is controlled by RMON bit. This bit is cleared on reset.

1 = Port pin functions as remote control output
0 = Port pin functions as general I/O port

BCLK Buzzer CLocK select

This bit selects the Buzzer tone output frequency. This bit is cleared on reset.

1 = OSC/2^{11} or XOSC/2^{4} is selected for Buzzer clock
0 = OSC/2^{10} or XOSC/2^{3} is selected for Buzzer clock

BZON Buzzer signal ON

When the port is used as Buzzer output (BZPE=1) this bit turns on or off the buzzer signal. This bit is cleared on reset.

This bit turns on the Buzzer output. This bit is cleared on reset.

1 = Buzzer is on
0 = Buzzer is off; idle state defined by BPOL is output

BPOL Buzzer output POLarity

This bit selects the buzzer output pin's polarity during buzzer idle (standby) period (BZON=0). When BZE=0, this bit has no effect. This bit is cleared on reset.

1 = Buzzer idle state outputs logic "1".
0 = Buzzer idle state outputs logic "0".

BZPE Buzzer output Port Enable

This bit controls whether the port functions as buzzer output or a general I/O port. The actual buzzer signal on/off is controlled by BZON bit. See **Table 7-1**. This bit is cleared on reset.

1 = Port pin functions as buzzer output
0 = Port pin functions as general I/O port

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SECTION 10SPI

10.1 INTRODUCTION

SPI is an interface built into the MC68HC705L26 to transmit or receive synchronous serial data. In this format, the serial clock is not included in the data stream and must be provided as a separate signal.

When the SPI is enabled reading Port C will return the actual pin level.

The MSTR bit selects the source of the serial clock from internal or the external clock. The internal clock speed is selectable as 1/2 or 1/16 of the system clock.

10.1.1 FEATURES

- Full Duplex 3 wire synchronous transfers
- Master or Slave operation
- Bit rate selection
- End of transmission interrupt
- Data collision flag
- Master mode maximum serial clock speed at 1/2 the CPU system clock
- Slave mode maximum serial clock speed up until the CPU system clock

10.2 BLOCK DIAGRAM

The following figure describes the block diagram of SPI module.

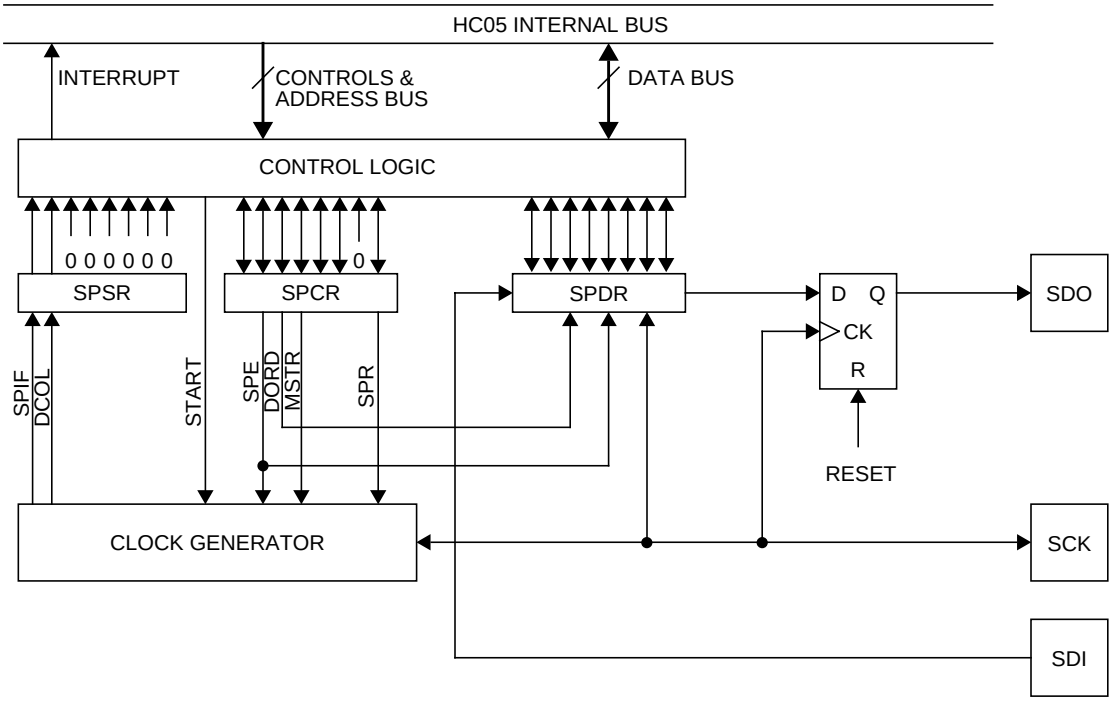


Figure 10-1: SPI Block Diagram

10.2.1 CONTROL

The control logic is an interface to the HC05 internal bus. It generates the clock start signal, when writing to SPDR is detected in the Master mode. It also generates flag clear signal and interrupt request to the CPU.

10.2.2 SPDR

The Serial Peripheral Data Register (SPDR) is an 8-bit shift register. This register can be read or written by the CPU. It can also change parallel data to serial or vice versa.

10.2.3 SPCR

The Serial Peripheral Control Register (SPCR) contains bit SPIE, SPE, DORD, SPR, and MSTR. The description on each bit can be found in the section on register description.

10.2.4 CLOCK GENERATOR

The clock generator includes a 3 bit serial clock counter. The counter starts after detecting the serial clock, and halts after setting SPIF when the counter overflows.

In Master mode, this block generates Serial Clock (SCK) when CPU writes to the data register (SPDR) and the clock rate is selected by SPR bit in the control register (SPCR).

In Slave Mode, external clock from the SCK pin is used instead of master mode clock and SPR has no effect.

10.2.5 OTHERS

The SPI does not use the data register of Port C. Therefore, regardless of whether the SPI is used, the data register can be read from Port C.

10.3 SIGNAL DESCRIPTION

The basic signals, SDO, SDI, and SCK of SPI are described in the following paragraphs. SCK, SDO, and SDI pins are shared with Port C pins PC0, PC1, and PC2, respectively.

10.3.1 SERIAL DATA OUT (SDO)

SDO is an output pin. This pin is shared with Port C pin PC1. When the SPI is enabled by SPE bit in the SPCR, this pin becomes an output pin. When the SPE is cleared, the pin becomes PC1 and thus becomes an input pin. The state of PC1/SDO may be read thru PC1 data register anytime.

When the SPI is enabled and PC1/SDO is an output, data output becomes valid at the falling edge of the serial clock.

10.3.2 SERIAL DATA IN (SDI)

The SDI pin is multiplexed with an general purpose I/O pin. This becomes an input only pin and accepts serial input data when the SPI is enabled.

10.3.3 SERIAL CLOCK (SCK)

The SCK pin is used for synchronization of both input and output data stream through SDI and SDO pins. The SCK pin should be at VDD level before SPI is enabled.

The Master and Slave devices are capable of exchanging a data byte during a sequence of eight clock pulses. Since SCK is generated by the Master, Slave data transfer is accomplished by synchronization of SCK.

When the MSTR bit in the SPCR is set, SCK becomes an output and the serial clock is supplied to the internal and external systems. When the serial clock is idling, high level is being output. When MSTR bit is "1", the CPU writes data to SPCR and outputs 8 clock pulses. After the end of the eighth clock, high level is being output while idling. The clock speed in Master mode is 1/2 the system clock.

When the MSTR bit in the SPCR is cleared, SCK becomes an input and the external system supplies the serial clock while the internal system operates by synchronizing to this clock. After eight serial clocks are input to the SCK pin, the SPIF bit in the SPSR is set and will not receive the next serial clock input until the SPIF bit is cleared. The clock speed in Slave mode is dependent upon the speed of the external system and has a maximum speed up till the internal system clock.

10.4 FUNCTIONAL DESCRIPTION

A block diagram of the SPI module is shown in **Figure 10-1**. In the SPI, if the SPE bit (SPI enable) of SPCR is set, bits 0, 1, and 2 of Port C will be connected. During this time, bit 0

is used as the SCK (serial clock), bit 1 as the SDO (serial data out), and bit 2 will become SDI. When SPE is “0”, SPI system is disabled.

In Master mode (MSTR=1), SCK becomes an output. When the CPU writes data to SPDR, start trigger will be applied from the control logic to the clock generator. The clock generator divides the system clock of the CPU (by 2 or 16) to generate the serial clock which is then output to the SCK pin. This clock is also used in the 3-bit clock counter and 8-bit shift register (SPDR). Data is output

In Slave mode (MSTR=0), SCK becomes an input, and the external serial clock is used. Therefore, the internal clock generator will not generate the serial clock. After detecting the external clock, the clock will be used by the 3-bit clock counter and the 8-bit shift register (SPDR) located in the clock generator. The SCK is used to latch incoming data.

Either in Master/Slave mode, the SPIF flag is set after the end of the transmission and if the SPIE bit in the SPCR is set, interrupt request is send to the CPU. This interrupt request is accepted when the I mask bit of Condition Code Register (CCR) is “0”, and is inhibited when the bit is “1” or until the mask is released. Also, if the SPIE bit is cleared, the interrupt request will not be accepted by the CPU.

To clear the SPIF while it is still set, the SPDR must be read or written after accessing SPSR.

Regardless of the Master/Slave I/O conditions, the DCOL bit of SPSR will be set when SPDR is accessed while the shift register is operating and while SPSR is not being accessed with SPIF set. DCOL is used to indicate that the data is not being properly read or written into SPDR.

To clear DCOL flag while it is still set, the SPDR must be read or written after accessing SPSR.

10.5 REGISTER DESCRIPTION

There are three registers in the SPI. They are Control register (SPCR), Status register (SPSR), and Data register (SPDR). SPCR and SPDR can be read or written by the CPU but SPSR can only be read.

10.5.1 SERIAL PERIPHERAL CONTROL REGISTER (SPCR)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$000A	SERIAL PERI. CONTROL REG SPCR	R	SPIE	SPE	DORD	MSTR	0	0	0	SPR
		W					—	—	—	
RESET:			0	0	0	0	0	0	0	0

Figure 10-2: SPI Control Register

SPIE **SPI Interrupt Enable**

When SPIE (SPI Interrupt Enable) is set, it allows the occurrence of processor interrupt when SPIF in the SPSR is set. This interrupt request is accepted when the I-bit in the CCR is cleared but inhibited when I-bit is set. If the interrupt request is send repeatedly while the I-bit and only when SPIE and SPIF are set, the interrupt will occur immediately after I-bit is cleared. Reset clears this bit.

1 = SPI interrupt is enabled
0 = SPI interrupt is disabled

SPE **SPI Enable**

When SPE (SPI Enable) is set, it enables the SPI system and connects bit 0 and bit 1 of Port C to SCK and SDIO. Clearing SPE initializes SPI system and disconnects SPI from Port C. Reset clears this bit.

1 = SPI is enabled
0 = SPI is disabled

DORD **Data transmission ORDer**

When DORD is set, the data in the 8-bit shift register (SPDR) is shifted in/out from LSB first. When clear, the data is shifted MSB first. Reset clears this bit.

1 = LSB first
0 = MSB first

MSTR **MaSTeR mode select**

This bit MSTR (Master mode select) determines whether to output the serial clock internally or input the clock externally. When set, SPI is in Master mode and SCK is configured as an output pin. SCK outputs the serial clock when CPU writes data to SPDR. When cleared, SPI is in Slave mode and SCK is configured as an input pin. SCK receives the serial clock externally. Reset clears this bit.

1 = Master mode
0 = Slave mode

BIT3:1 **Reserved**

These bits are reserved and always read as 0.

SPR **SPI clock rate select**

This is the clock rate selection bit. When set, the Master mode SCK rate is the system clock divided by 16. When clear, the rate system clock divided by 2. Reset clears this bit.

1 = system clock divided by 16
0 = system clock divided by 2

10.5.2 SERIAL PERIPHERAL STATUS REGISTER (SPSR)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$000B	SERIAL PERI. STATUS REG SPSR	R	SPIF	DCOL	0	0	0	0	0	0
		W	—	—	—	—	—	—	—	—
		RESET:	0	0	0	0	0	0	0	0

Figure 10-3: SPI Status Register

SPIF Serial transfer complete flag

SPIF (Serial Peripheral Interface Flag) notifies the user that the data transfer between MC68HC705L26 and the external device have completed. Upon completion of the data transfer, the rising edge of the eighth serial clock pulse sets SPIF. If SPIE in the SPCR is set, the SPI interrupt (SPII) will be generated.

While SPIF is set, all access to the SPDR is inhibited until SPSR is read by CPU. Also, even if the ninth serial clock is detected, the shift register (SPDR) will not operate.

Clearing the SPIF is accomplished by a software sequence of accessing the SPSR while SPIF is set, and followed by the SPDR access. (SPIF and DCOL can be cleared simultaneously.)

Reset clears this bit.

1 = serial data transfer complete
0 = serial data transfer in progress

DCOL Data COLlision

DCOL (Data Collision) notifies the user that an invalid access to the SPDR has been made. This bit is set when an attempt was made to read or write to SPDR while a data transfer was taking place with an external device. When DCOL is set, access to the SPDR becomes invalid. The transfer continues uninterrupted without any affect from the SPDR access. This flag does not generate SPI interrupt. It is read-only.

DCOL is cleared by reading the SPSR with SPIF set followed by a read or write to the SPDR. If the last part of the clearing sequence is done after another transmission has started, DCOL will be set again. (DCOL and SPIF can be cleared simultaneously.)

Reset clears this bit.

1 = data collision occurred
0 = data collision did not occur

BITS 5:0 Reserved

These bits are unused and always read as 0.

10.5.3 SPI DATA REGISTER (SPDR)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$000C	SERIAL PERI. DATA REG SPDR	R	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
		W								
	RESET:		U	U	U	U	U	U	U	U

Figure 10-4: SPI Data Register

The SPDR is used to transmit and receive data on the serial bus.

In Master mode, a write to SPDR initiates the transmission/reception of data byte. At the completion of transfer, SPIF status bit set.

In Slave mode, a write to SPDR will not initiate the serial clock. The serial clock is input to the SCK pin by the external device.

In either Master or Slave mode, a write to the SPDR is inhibited while this register is shifting (this condition cause DCOL to set) or when SPIF is set without reading SPSR. In this case, even if an access has occurred, the access becomes invalid. Refer to SPIF and DCOL description for more information.

When SPI is not being used, SPDR can be used as a data storage. This byte is not affected by reset.

10.6 TIMING DIAGRAM

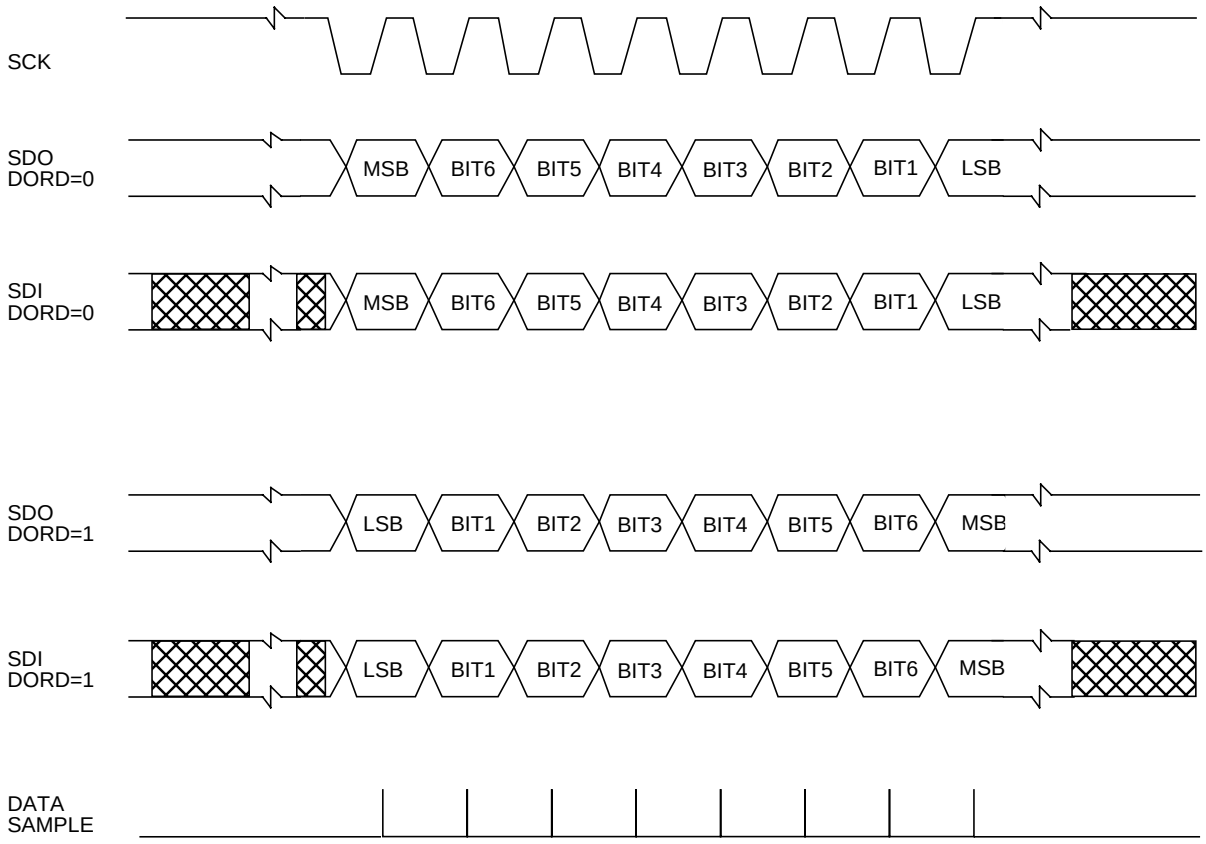


Figure 10-5: Clock/Data timing

10.7 STOP/WAIT CONDITION

10.7.1 STOP

The SPI configured as Master Mode is not operational during STOP mode since the system clock and SPI clock generator is halted. If STOP mode occurs while SPI is in progress (transmitting/ receiving) and in Master mode, the access will halt and remains halted until STOP is released.

Due to the static architecture, the previous conditions of SCK and SDIO are preserved during STOP mode.

In Slave mode, all access are possible during STOP mode. However, at the end of transmission, interrupt occurs but SPIF will not be set immediately until after the system clock starts operating. (This operation is transparent to the programmer.)

10.7.2 WAIT

In WAIT mode, the CPU halts but will not affect the SPI operation. Therefore, SPI interrupt in Master and Slave modes can be executed to wake-up the CPU.

SECTION 11LCD DRIVER

11.1 INTRODUCTION

The MC68HC705L26 has 25 or 24 Front Plane (FP) and 3 or 4 Back Plane drivers. The number of drivers for the FP and BP can be selected by software option. The maximum number of segments configurable are either 24 x 4 = 96 or 25 x 3 = 75 segments.

The MC68HC705L26 uses 1/3 biasing method. The bias voltages are supplied from an external source using VLCD pin. Voltages VLCD1, VLCD2, and VLCD3 are generated internally with resistor divider.

There are 11 bytes of data latch for selection (turned on) or non-selection (turned off) of segments. Each byte consists of 2 FP drivers and either 3 or 4 BP drivers depending on the duty configured. The data latch is available in memory locations $21-$2D and can be accessed by the CPU using the conventional memory access method (LOAD, STORE, BIT operations, etc.).

The clock which forms the LCD FP and BP waveforms is supplied by the Time Base module.

11.2 BLOCK DIAGRAM

The following figure describes the block diagram of the LCD module.

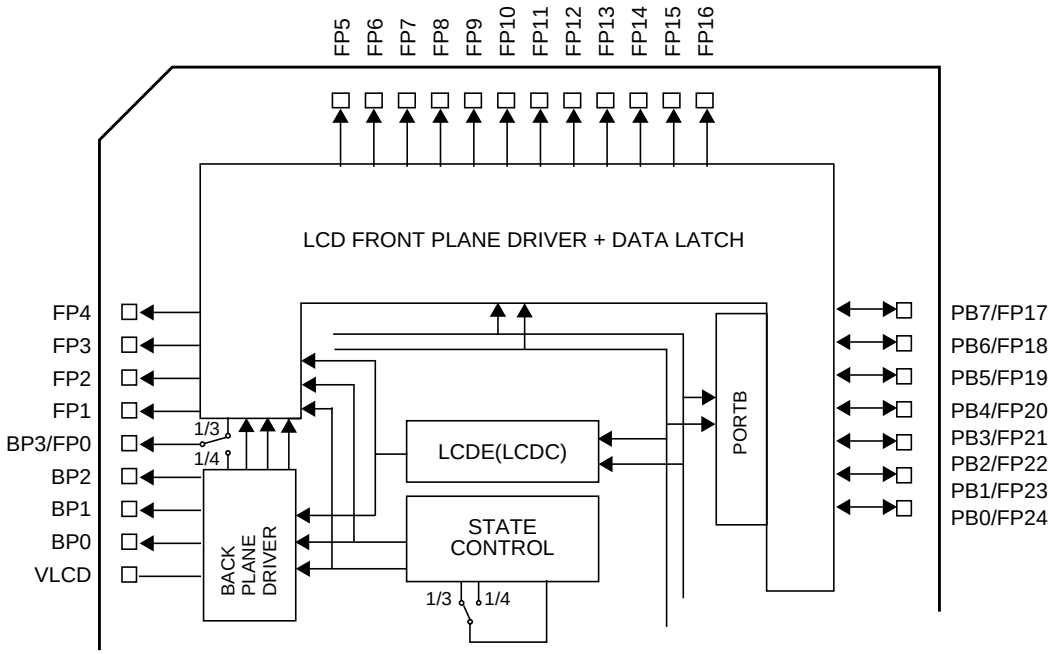


Figure 11-1: LCD Block Diagram

11.3 FUNCTIONAL DESCRIPTION

11.3.1 LCD CONTROL REGISTERS

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$0020	LCD CONTROL REG LCDCR	R	LCDE	PBEH	DUTY	PBEL	0	0	FC	LC
		W					—	—		
	RESET:		0	0	0	0	0	0	0	0

Figure 11-2: LCD Control Register

LCDE LCD Enable

Setting this bit enables the LCD waveforms to appear on the pins. Reset clears this bit.

1 = LCD drivers are operational. Each FP and BP driver outputs the driver waveform specified by the data latch.
0 = LCD drivers are halted. All FP, BP drivers have the same electric potential as V_{DD}. R_{LCD}'s are disconnected to reduce DC current.

PBEH Port B Enable High nibble

This bit enables the Port B I/O bits 4:7 that are multiplexed with Front Plane Drivers 20:17. Reset clears this bit.

1 = PB4:7/FP20:17 pins function as Port B bits 4:7.
0 = PB4:7/FP20:17 pins function as LCD Front Plane Drivers 20:17.

DUTY DUTY cycle select

This bit selects the duty cycle of the LCD waveforms between 1/3 duty and 1/4 duty and selects either BP3 or FP0 for the muxed pin. Reset clears this bit.

1 = 1/3 duty cycle is selected and BP3/FP0 pin functions as FP0.
0 = 1/4 duty cycle is selected and BP3/FP0 pin functions as BP3.

PBEL Port B Enable Low nibble

This bit enables the Port B I/O bits 0:3 that are multiplexed with Front Plane Drivers 24:21. Reset clears this bit.

1 = PB0:3/FP24:21 pins function as Port B bits 0:3.
0 = PB0:3/FP24:21 pins function as LCD Front Plane Drivers 24:21.

BIT3:2 Reserved

These bits are unused and always read as 0.

FC,LC Fast Charge, Low Current

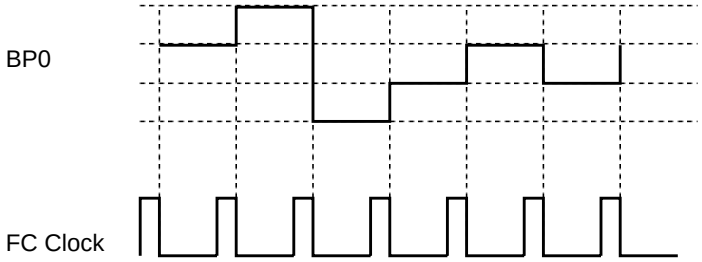
These bits are used to select various values of resistors in the voltage generator resistor chain. Reset clears these bits.

Table 11-1: RLCD Configuration

LC	FC	Action
0	X	Default value of approx. 30KΩ per resistor
1	0	Resistor value of approx. 170KΩ per resistor
1	1	Fast-Charge: For a period of LCDCLK/128 in each frame the resistor values are reduced to default (value for LC=0).

11.3.2 FAST CHAGE OPTION

The R_{LCD} as shown in **Figure 11-9** is approximately 30KΩ at VDD=3V by default. This value may be inappropriate for some applications. For those applications that require less DC current drain through the R_{LCD} chain, it may be increased to approximately 168KΩ at VDD=3V by setting the LC bit in LCDCR. Some application may require the default resistance (30KΩ) to drive the capacitive load of the LCD panel, yet do not wish to have the DC current drain of it while the LCD segments are not switching. For a compromise a Fast-Charge option is available. The R_{LCD} values are reduced to the default resistance for a fraction of the LCD segment cycle before the LCD segments change, and then are set to low current mode for the remainder of the LCD cycle frame. The DC current increase for is very negligible and will be within few percent increase of the low current mode.



11.3.3 LCD DATA REGISTER

The LCD data latches LDAT1:LDAT11 maintain the ON/OFF data for the FP and BP segments of the LCD.

Four bits of data latch are assigned to each front plane driver, from address space $21:$2D as in the following figure.

When "1" is written to the bits in the data latch the applicable FP-BP segment turns ON. When "0" is written to the bits, the segment is turned OFF.

The values in the data latches are not initialized and are unknown on reset.

If 1/3 duty is selected, each BP3 bit in the data latches are ignored.

ADDR (hex)	REGISTER NAME ABBREV.	READ WRITE	Bit Number Significance							
			7	6	5	4	3	2	1	0
$0020	LCD CONTROL REG LCDCR	R	LCDE	PBEH	DUTY	PBEL	0	0	FC	LC
		W					—	—		
$0021	LCD DATA REGISTER LDAT1	R	F1B3	F1B2	F1B1	F1B0	F0B3	F0B2	F0B1	F0B0
		W								
$0022	LCD DATA REGISTER LDAT2	R	F3B3	F3B2	F3B1	F3B0	F2B3	F2B2	F2B1	F2B0
		W								
$0023	LCD DATA REGISTER LDAT3	R	F5B3	F5B2	F5B1	F5B0	F4B3	F4B2	F4B1	F4B0
		W								
$0024	LCD DATA REGISTER LDAT4	R	F7B3	F7B2	F7B1	F7B0	F6B3	F6B2	F6B1	F6B0
		W								
$0025	LCD DATA REGISTER LDAT5	R	F9B3	F9B2	F9B1	F9B0	F8B3	F8B2	F8B1	F8B0
		W								
$0026	LCD DATA REGISTER LDAT6	R	F11B3	F11B2	F11B1	F11B0	F10B3	F10B2	F10B1	F10B0
		W								
$0027	LCD DATA REGISTER LDAT7	R	F13B3	F13B2	F13B1	F13B0	F12B3	F12B2	F12B1	F12B0
		W								
$0028	LCD DATA REGISTER LDAT8	R	F15B3	F15B2	F15B1	F15B0	F14B3	F14B2	F14B1	F14B0
		W								
$0029	LCD DATA REGISTER LDAT9	R	F17B3	F17B2	F17B1	F17B0	F16B3	F16B2	F16B1	F16B0
		W								
$002A	LCD DATA REGISTER LDAT10	R	F19B3	F19B2	F19B1	F19B0	F18B3	F18B2	F18B1	F18B0
		W								
$002B	LCD DATA REGISTER LDAT11	R	F21B3	F21B2	F21B1	F21B0	F20B3	F20B2	F20B1	F20B0
		W								
$002C	LCD DATA REGISTER LDAT12	R	F23B3	F23B2	F23B1	F23B0	F22B3	F22B2	F22B1	F22B0
		W								
$002D	LCD DATA REGISTER LDAT13	R	0	0	0	0	F24B3	F24B2	F24B1	F24B0
		W	—	—	—	—				

Figure 11-3: LCD Data Registers (LDAT1:LDAT13)

11.4 TERMINAL DESCRIPTION

There are total of 27 pins dedicated to the LCD driver.

11.4.1 VLCD BIAS INPUTS

VLCD1:VLCD3 are internal bias voltages for the LCD driver waveforms. VLCD3 potential is available externally as VLCD pin, and a variable resistor for contrast may be placed between VLCD and VSS. See **Figure 11-9**.

The LCD uses the 3 bias voltages typically as follows:

VLCD1 = VDD - 1/3VLCDA (VLCDA is the ON voltage for the LCD modules)
VLCD2 = VDD - 2/3VLCDA (Usually, VLCDA <= VDD is used)
VLCD3 = VDD - VLCDA = VLCD (VLCD is the external pin)

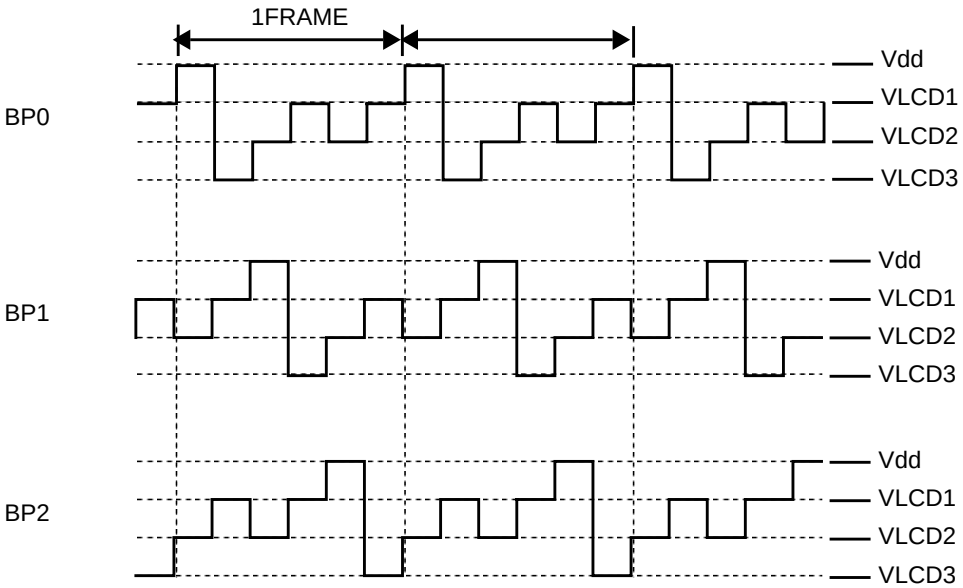
The 3 voltages shown above are arranged so that the external voltages will have VLCD1 > VLCD2 > VLCD3 relationship in a voltage divider configuration.

11.4.2 BACK PLANE DRIVERS (BP0:BP3)

Pins BP0:BP3 are the output terminals for the back plane drivers.

These are connected to the back plane of the LCD panel. Depending on the duty, the following waveforms appear on the back plane pins.

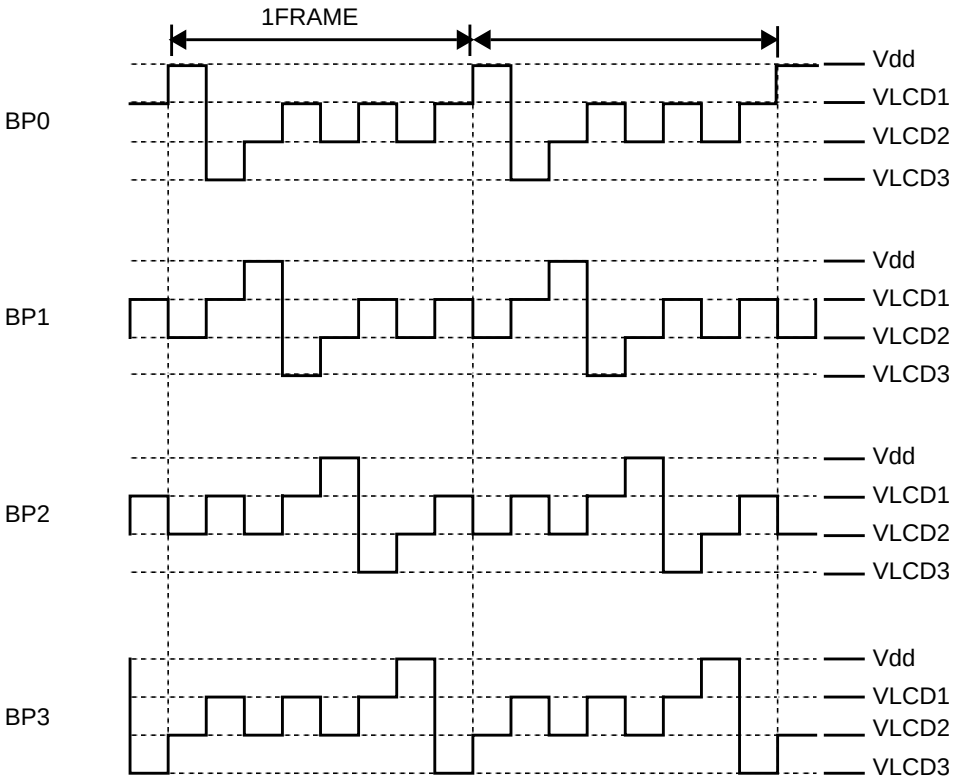
DUTY=1/3



* BP3 is not used.
* At 1/3 duty, 1FRAME has 3 times the cycle of LCD waveform base clock.

Figure 11-4: 1/3 Duty LCD Backplane Driver Waveforms

DUTY=1/4



* The element which selects or does not select the BP waveforms are as follow.

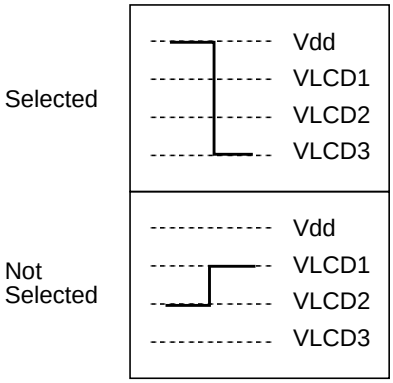


Figure 11-5: 1/4 Duty LCD Backplane Driver Waveforms

11.4.3 FRONT PLANE DRIVERS

Pins FP0:FP24 are the output terminals for the front plane drivers. These are connected to the front plane of the LCD panel. Depending on the content of the data latch, the following waveforms appear on the Front Plane drivers.

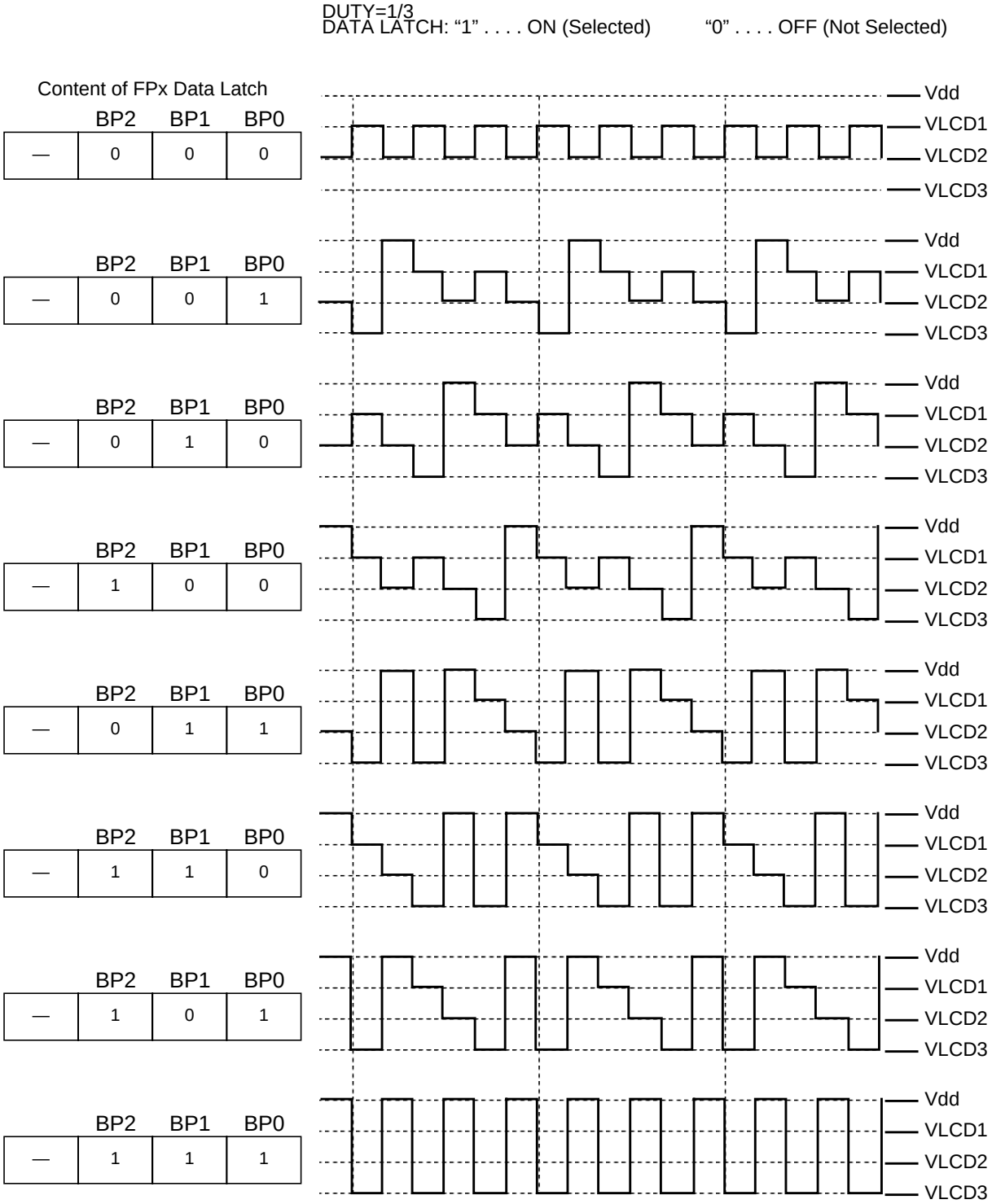
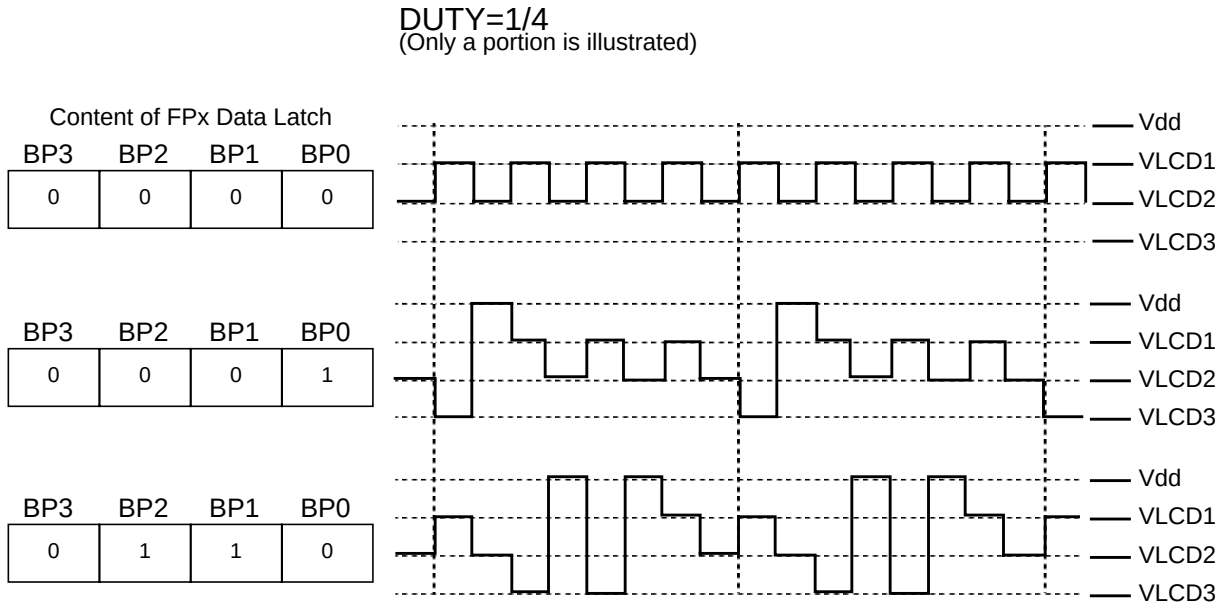


Figure 11-6: 1/3 Duty LCD Front Plane Driver Waveforms



* The fundamental elements which select or does not select the front plane waveforms are as follow.

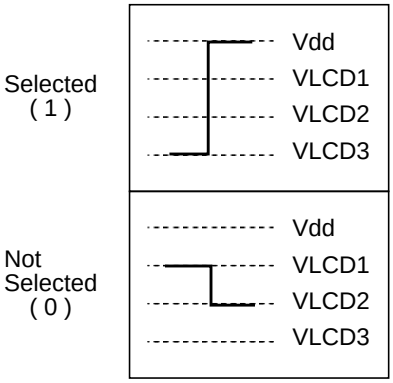


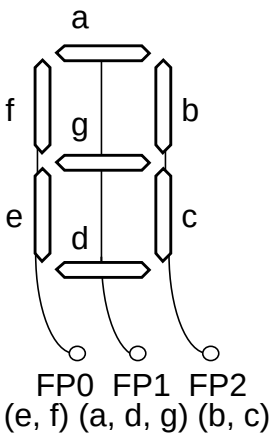
Figure 11-7: 1/4 Duty LCD Front Plane Driver Waveforms

11.5 LCD PANEL CONNECTION& LCD DRIVER OPERATION

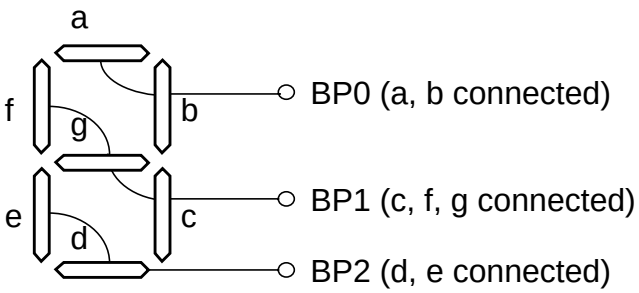
This section will discuss the connection between the MC68HC705L26 and the 7 segments of the LCD panel.

- A 1/3 duty example is illustrated below:

FP Connection



BP Connection



* The segment assignments for each bit in the data latch are as follow.

—	D	G	A	—	E	F	—

FP1 FP0

—	—	—	—	—	—	C	B

(Unrelated FP) FP2

(- . . . means not assigned in this case)

* To display a “4” using the assignments above will have the following data written to LDAT1 and LDAT2.

—	0	1	0	—	0	1	X

FP1 FP0

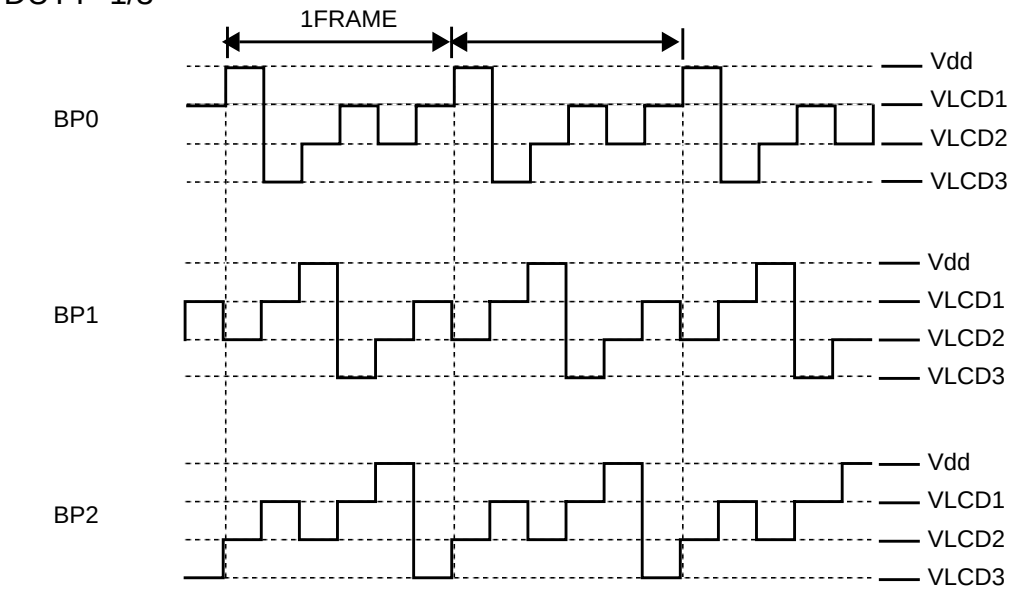
—	—	—	—	—	X	1	1

(Unrelated FP) FP2

(X . . . don’t care)
(“-”, “X” . . . are zero in this case)

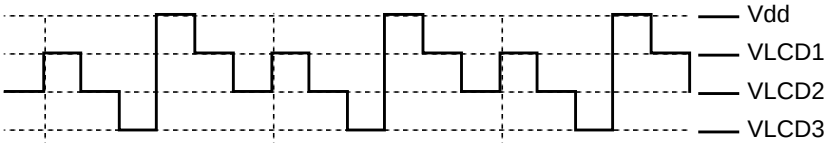
- Pins BP0, BP1, BP2, FP0, FP1, FP2 output the following waveforms.

DUTY=1/3



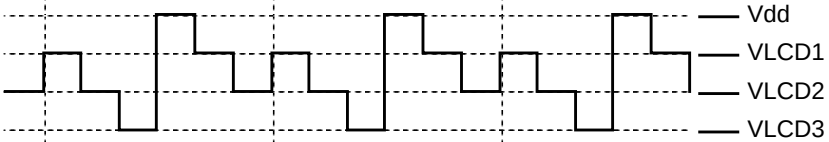
FP0 Waveform

	BP2	BP1	BP0
—	0	1	0



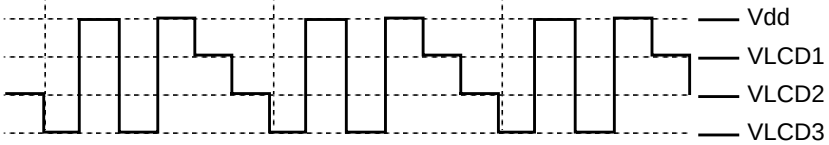
FP1 Waveform

	BP2	BP1	BP0
—	0	1	0

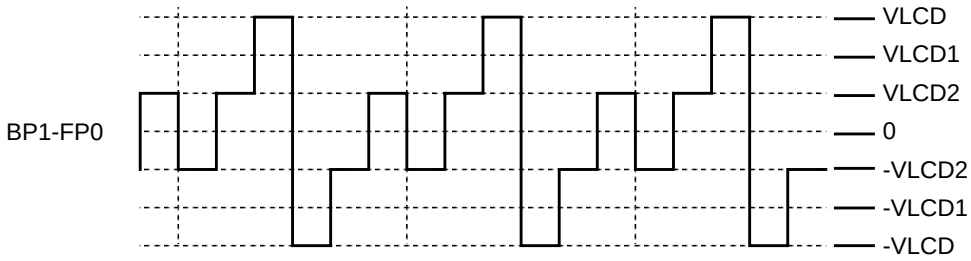


FP2 Waveform

	BP2	BP1	BP0
—	0	1	1

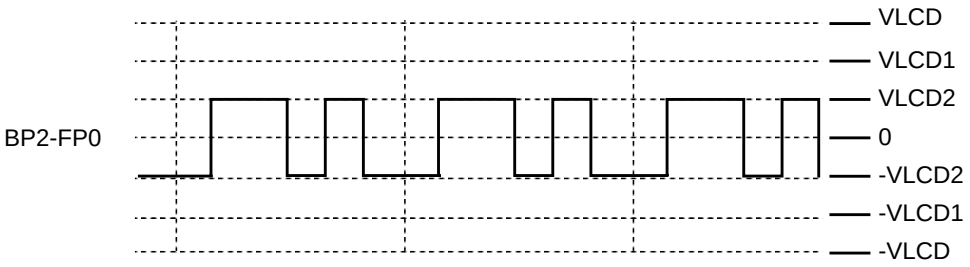


- The electric potential waveform for the F segment (between FP0 and BP1) will be as follows.



- As shown above, the LCD ON voltage (VLCD) of the AC waveform is attained, so the F segment will turn ON.

- The electric potential waveform for the E segment (between FP0 and BP2) will be as follows. This segment is not turned ON.



- The methods described will determine whether to turn ON or turn OFF the LCD segment. The waveform elements which select or not select the BP and FP waveforms are as follow.

FP Data Latch ->	1	0
FP BP	Selected Vdd VLCD1 VLCD2 VLCD3	Not Selected Vdd VLCD1 VLCD2 VLCD3
Selected Vdd VLCD1 VLCD2 VLCD3	ON +VLCD +2VLCD/3 +VLCD/3 0 -VLCD/3 -2VLCD/3 -VLCD	OFF +VLCD +2VLCD/3 +VLCD/3 0 -VLCD/3 -2VLCD/3 -VLCD
Not Selected Vdd VLCD1 VLCD2 VLCD3	OFF +VLCD +2VLCD/3 +VLCD/3 0 -VLCD/3 -2VLCD/3 -VLCD	ON +VLCD +2VLCD/3 +VLCD/3 0 -VLCD/3 -2VLCD/3 -VLCD

11.6 LCD WAVEFORM BASE CLOCK & LCD CYCLE FRAME

The clock which produce the LCD FP and BP output waveforms, the LCD Waveform Back clock, is generated from the Time Base module.

The frequency for the LCD waveform base clock can be changed by the time base control register.

11.6.1 TIME BASE CONTROL REGISTER 1 (TBCR1)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$0010	TIME BASE CONTROL REG. 1 TBCR1	R	TBCLK	0	LCLK	RMC4	RMC3	RMC2	RMC1	RMC0
		W		—						
	RESET:		0	0	0	0	0	0	0	0

Figure 11-8: Time Base Control Register 1

LCLK LCD Clock

The LCLK bit selects clock for the LCD driver. This bit is cleared on reset.

When TBCLK=0:

1 = XOSC Divide by 128 is selected for the LCD clock
0 = XOSC Divide by 64 is selected for the LCD clock

When TBCLK=1:

1 = OSC Divide by 16384 is selected for the LCD clock
0 = OSC Divide by 8192 is selected for the LCD clock

Table 11-2: LCD Waveform Base Clock Frequency

TBCR1		Divide Ratio	LCD Waveform Base Clock Frequency (Hz) (F_{XOSC} = 32.768 KHz)		
.TB-CLK	.LCLK		OSC = 2.0 MHz	OSC = 4.0 MHz	OSC = 4.1943 MHz
0	0	XOSC / 64	512	512	512
0	1	XOSC / 128	256	256	256
1	0	OSC / 8192	244	488	512
1	1	OSC / 16384	122	244	256

11.6.2 LCD CYCLE FRAME

The LCD Cycle Frame with respect to LCD Waveform Base Clock and Duty is

$$(\text{LCD Cycle Frame}) = \frac{1}{(\text{LCD Waveform Base Clock}) \cdot (\text{Duty})}$$

For Example, given 1/3 duty and 256 Hz waveform base clock,

$$(\text{LCD Cycle Frame}) = \frac{1}{256 \cdot \frac{1}{3}}$$

$$= 11.72 \text{ mS}$$

11.7 SIMPLIFIED LCD SCHEMATIC

The following figure is a simplified schematic of the LCD driver.

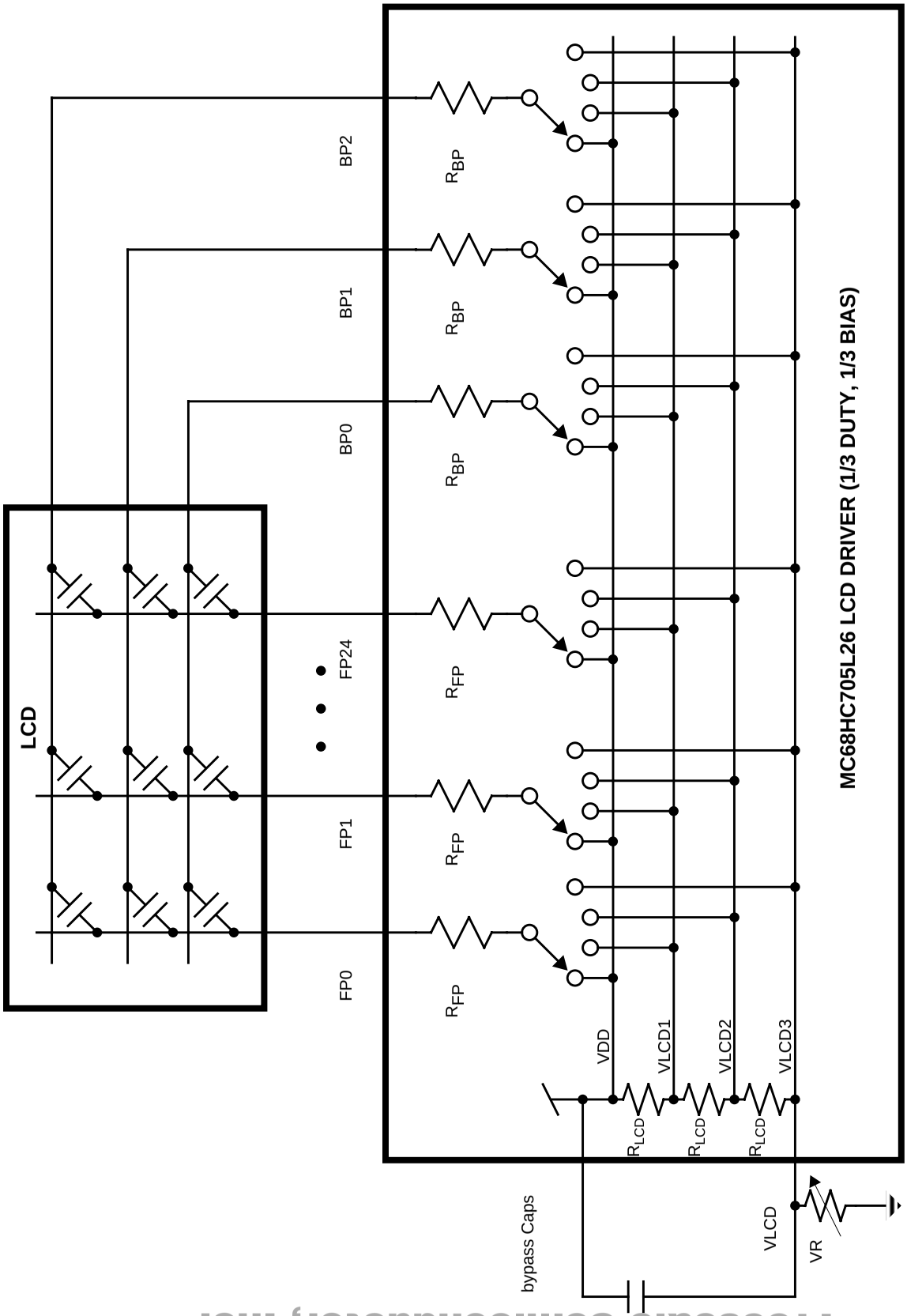


Figure 11-9: Simplified LCD Schematic

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SECTION 12PULSE WIDTH COUNTER

The Pulse Width Counter (PWC) measures length of input pulses. Input pulse is sampled every T_{NOI} to reduce noise. Lengths of either full period or high- and low-level of input pulses may be measured. The PWC can measure pulse length of T_{CLK} to 255 x T_{CLK} at T_{CLK} resolution. The lengths measured are stored in to a 6-level queue. See **1.3**.

- Noise cancel sampling rate of T_{NOI} = 30.5 µS, 3.81 µS, 7.63 µS, or 15.3µS
- Counter clock rate of T_{SAM} = 61.0 µS, 7.63 µS, 15.3 µS, 30.5 µS, or 122 µS
- Measures pulse width of (with XOSC=32.768KHz; OSC=4.19 MHz),
  using XOSC: 61.0 µS to 15.5 mS at 61.0 µS resolution,
  using OSC: 7.63 µS to 1.95 mS at 7.63 µS resolution,
  using OSC: 15.3 µS to 3.89 mS at 15.3 µS resolution,
  using OSC: 30.5 µS to 7.78 mS at 30.5 µS resolution, or
  using OSC: 122 µS to 31.1 mS at 122 µS resolution
- 8 bit counter with 9 bit x 6 queue
- Interrupts generated at every edge, after 4 bytes in queue, or counter overflow

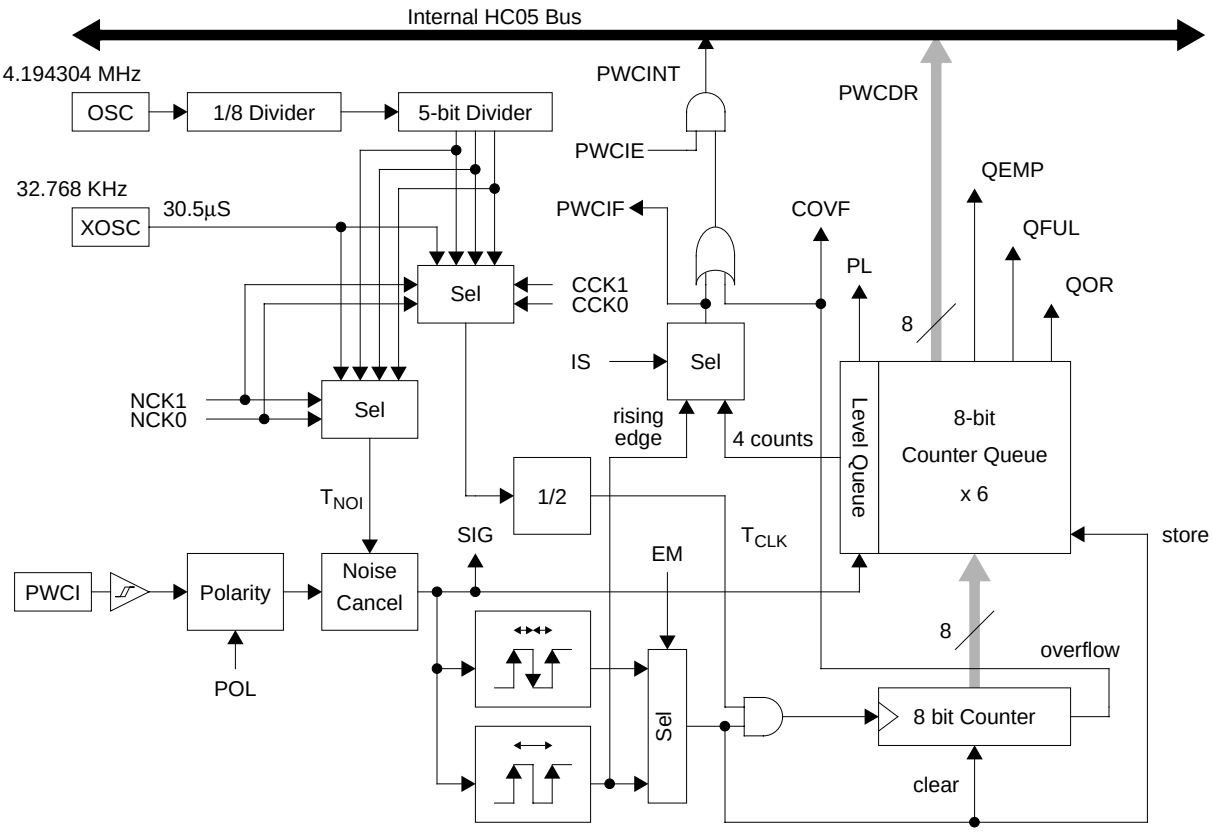

Figure 12-1: Queued Pulse Width Counter Block Diagram

12.1 NOISE CANCEL

The PWCI pin is sampled to reduce noise. One of four sampling rate may be selected using NCK1:0 bits. The following table assumes 32.768 KHz for XOSC and 4.19 MHz for OSC.

Table 12-1: PWC Counter Clock Rate

NCK1	NCK0	Clock Source	Noise Cancel Clock Rate	Maximum Noise Width
0	0	OSC / 16	3.82 µS	11.44 µS
0	1	OSC / 32	7.63 µS	22.89 µS
1	0	OSC / 64	15.3 µS	45.78 µS
1	1	XOSC	30.5 µS	91.55 µS

12.2 COUNTER

The 8-bit counter starts counting when an edge is detected in the sampled input signal. The edge may either be a rising edge or rising and falling edges, depending on the PWCCR.EM bit. The counter value when the next edge is detected is stored in the queue and the counter is cleared to $00. However, if an edge was detected while PWCSR.COVF flag is set, the overflow count of $FF is not stored in the queue.

When the 8-bit counter overflows the counter stops at $FF, PWCSR.COVF flag is set, and an interrupt request is generated. However, if a falling edge is detected while COVF flag is set, the counter is cleared to $00 and the counter resumes counting the width of the low pulse.

One of five counter clock rate may be selected using NCK1:0 and CCK1:0. The following table assumes 32.768 KHz for XOSC and 4.19 MHz for OSC. If NCK1:0 = 1:1 then CCK1:0 are ignored and XOSC/2 is used for the counter clock source.

The counter rate selected by CCK1:0 must not be faster than the noise cancel rate selected by NCK1:0.

Table 12-2: PWC Counter Clock Rate

NCK1	NCK0	CCK1	CCK0	Clock Source	Counter Clock Rate	Maximum Pulse Width
0 0, 0 1, or 1 0		0	0	OSC / 32	7.63 µS	1.945 mS
		0	1	OSC / 64	15.3 µS	3.890 mS
		1	0	OSC / 128	30.5 µS	7.782 mS
		1	1	OSC / 512	122 µS	31.12 mS
1	1	X	X	XOSC / 2	61.0 µS*	15.55 mS

Note:
1. * This rate is selected when NCK1:0 = 1:1 regardless of CCK.

12.3 PWC QUEUE

The PWC Queue is a 6 byte FIFO that stores the width measured using the 8-bit counter. Data is stored in the queue after the width of the input pulse (either full period or each pulse) is measured. If the queue is empty (PWCSR.QEMP = 1), data is stored in the first byte. If the queue already contains data, data is stored in the next open byte. When all 6 bytes are stored in the queue, PWCSR.QFUL bit is turned on. Subsequent data are stored in the last byte, overwriting latest byte stored.

The counter data stored in the queue may be read at location $000F. The 9th bit (PWCSR.PL) is updated only after the counter data is read. When a byte is read, the oldest byte in the queue is discarded and a new byte may be stored from the counter. When all bytes are read, the queue becomes empty (PWCSR.QEMP = 1). If the queue is read when empty, undefined data is returned.

Data in the queue may be initialized by disabling and enabling PWC by first clearing and then setting PWCCR.PWCE bit.

12.4 SOFTWARE CONSIDERATIONS

The data in Queue is undefined after reset or when it is cleared. Data read when the Queue is empty is undefined.

If the Queue is overrun, last data written is destroyed. Thus first clear the Queue by disabling and enabling PWC and re-measure the data. Care should be taken not to overrun the queue.

Do not change the selections of noise cancel clock rate, counter clock rate, input polarity, interrupt mode, or pulse measurement mode after enabling the PWCE.

Since interrupt may be requested due to one of three sources, when servicing interrupt, first check COVF flag. If this flag is set, the interrupt was due to counter overflow. Otherwise, if this flag is clear, interrupt was due to 4 counts are stored in buffer (IS=0) or an edge was detected (IS=1).

12.5 PWC DURING WAIT MODE

During WAIT Mode the PWC continues to operate normally. Pulse width may be measured during WAIT and WAIT Mode may be exited when the appropriate interrupt condition is met. To decrease power consumption during WAIT, the PWCE should be disabled if PWC subsystem is not being used.

12.6 PWC DURING STOP MODE

During STOP Mode the PWC continues to operate normally if XOSC is used for noise cancel clock source. Pulse width may be measured during STOP using XOSC and STOP Mode may be exited when the appropriate interrupt condition is met. If OSC is selected as clock source, PWC will not function during STOP. To decrease power consumption during STOP, the PWCE should be disabled if PWC subsystem is not being used.

12.7 PULSE WIDTH COUNTER CONTROL REGISTER (PWCCR)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$000D	PWC CONTROL REG PWCCR	R	PWCE	EM	IS	POL	CCK1	CCK0	NCK1	NCK0
		W								
	RESET:		0	0	0	0	1	1	1	1

Figure 12-2: PWC Control Register

PWCE PWC Enable

This bit enables the PWC sub-system. When the PWC is disabled, clocks to the PWC module are disabled, queue is initialized, and all flags bits are cleared to the reset state.

Read/Write:

1 = PWC is enabled; PA7/PWCI functions as PWCI input pin.
0 = PWC is disabled; PA7/PWCI functions as Port A I/O pin.

EM Edge Mode

This bit selects the measurement mode. Pulse width of either both high- and low-level or full period is measured.

Read/Write:

1 = Measures pulse width of both high- and low-level
0 = Measures pulse width of full period

IS Interrupt Select

This bit selects the PWC interrupt sources. An interrupt will be generated after every rising edge on the input pin or after 4 counts are stored in the queue, if enabled by PWCIE=1.

Read/Write:

1 = PWCIF is set at rising edge of SIG
0 = PWCIF is set after 4 counts are stored in the queue

POL PWC POLarity

This bit selects the polarity of input pulses.

Read/Write:

1 = Invert input pulses
0 = Do not invert input pulses

CCK1:0 Counter ClocK 1:0

These bits select the counter clock. See **Section 12.2** for more information.

NCK1:0 Noise cancel ClocK 1:0

These bits select the noise cancel clock. See **Section 12.1** for more information.

12.8 PULSE WIDTH COUNTER STATUS REGISTER (PWCSR)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$000E	PWC STATUS REG PWCSR	R	PL	SIG	PWCIE	COVF	PWCIF	QOR	QFUL	QEMP
		W	—	—		—	—	—	—	—
RESET:			0	U	0	0	0	0	0	1

Figure 12-3: PWC Status Register

PL **Pulse Level**

This bit is the pulse level stored in the PWC queue. This bit is updated AFTER reading the PWCDR.

This bit is cleared while PWCE is cleared.

Read:

1 = Pulse Level in the buffer (9th bit) is 1
0 = Pulse Level in the buffer (9th bit) is 0

Write:

No action. This bit is read only.

SIG **SIGnal**

This bit is the output of noise cancel circuit. This bit may be read any time.

Read:

1 = noise cancelled signal level is 1
0 = noise cancelled signal level is 0

Write:

No action. This bit is read only.

PWCIE **PWC Interrupt Enable**

This bit enables the PWC interrupts.

Read/Write:

1 = Interrupts are enabled
0 = Interrupts are disabled

COVF **Counter OVerFlow**

This bit indicates that the 8-bit counter has overflowed. An interrupt request is generated if PWC Interrupt is enabled. This flag is cleared by disabling the PWC.

Read:

1 = Counter has overflowed.
0 = Counter has not overflowed.

PWCIF PWC interrupt Flag

This bit is the status of PWC interrupt. There are three sources of interrupts: counter overflow (COVF=1), 4 bytes in queue (IS=1), or edge detect (IS=0). Clearing this flag is done by reading the PWCSR while this bit is set and then accessing the PWCDR. This flag must be serviced before the next time it is set.

Read:

1 = interrupt requested
0 = no interrupt requested

Table 12-3: PWC Interrupt Sources

PWCIF	COVF	IS	Source
0	0	X	No Interrupt
1	X	0	4 bytes in queue
1	X	1	rising edge detected
X	1	X	counter overflowed

Write:

No action. This bit is read only.

QOR Queue OverRUN

This bit is the status of the queue. This bit is cleared by disabling the PWC.

Read:

1 = queue overrun; data was written to the queue when full
0 = no queue overrun; data in queue is valid

Write:

No action. This bit is read only.

QFUL Queue FULl

This bit is the status of the queue. This bit is cleared by reading a byte from the queue, or disabling the PWC.

Read:

1 = Queue is full
0 = Queue is not full

Write:

No action. This bit is read only.

QEMP Queue EMPty

This bit is the status of the queue. This bit is cleared when a counter byte is stored.

Read:

1 = Queue is empty
0 = Queue has data

Write:

No action. This bit is read only.

12.9 PULSE WIDTH COUNTER DATA REGISTER (PWCDR)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$000F	PWC DATA REG PWCDR	R	PWC7	PWC6	PWC5	PWC4	PWC3	PWC2	PWC1	PWC0
		W	—	—	—	—	—	—	—	—
RESET:			0	0	0	0	0	0	0	0

Figure 12-4: PWC Data Register

This register contains the data stored in the queue. Undefined data is returned if the queue is read when it is empty.

This register is a read-only register.

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SECTION 13ANALOG SUBSYSTEM

The MC68HC05P6 includes a 2-channel, multiplexed input, 8-bit, successive approximation A/D converter. The A/D subsystem shares its inputs with Port A pins PA4:PA5.

13.1 ANALOG SECTION

The following paragraphs describe the operation and performance of analog modules within the analog subsystem.

13.1.1 RATIOMETRIC CONVERSION

The A/D converter is ratiometric, with pin V_{REFH} = V_{DD} supplying the high reference voltage. Applying an input voltage equal to V_{REFH} produces a conversion result of $FF (full scale). Applying an input voltage equal to V_{SS} produces a conversion result of $00. An input voltage greater than V_{REFH} will convert to $FF with no overflow indication. For ratiometric conversions, V_{REFH} should be at the same potential as the supply voltage being used by the analog signal being measured and be referenced to V_{SS}.

13.1.2 V_{REFH}

The reference supply for the A/D converter is tied to V_{DD} internally. The low reference is tied to the V_{SS} pin internally.

13.1.3 ACCURACY AND PRECISION

The 8-bit conversion result is accurate to within ±1 1/2 LSB, including quantization; however, the accuracy of conversions is tested and guaranteed only with external oscillator operation at VDD=5V. The error will increase at VDD less than 3V.

13.2 CONVERSION PROCESS

The A/D reference inputs are applied to a precision digital-to-analog converter. Control logic drives the D/A and the analog output is successively compared to the selected analog input which was sampled at the beginning of the conversion cycle. The conversion process is monotonic and has no missing codes.

13.3 DIGITAL SECTION

The following paragraphs describe the operation and performance of digital modules within the analog subsystem.

13.3.1 CONVERSION TIMES

Each input conversion requires 32 PH2 (bus) clock cycles, which must be at a frequency equal to or greater than 1 MHz.

13.3.2 INTERNAL VS. EXTERNAL OSCILLATOR

If the MCU PH2 clock frequency is less than 1 MHz (2 MHz external oscillator), the internal RC oscillator (approximately 1.5 MHz) must be used for the A/D converter clock. The internal RC clock is selected by setting the ADRC bit in the ADSC register.

When the internal RC oscillator is being used these limitations apply:

Since the internal RC oscillator is running asynchronously with respect to the PH2 clock, the Conversion Complete bit (CC) in register ADSC must be used to determine when a conversion sequence has been completed.

1. Electrical noise will slightly degrade the accuracy of the A/D converter. The A/D converter is synchronized to read voltages during the quiet period of the clock driving it. Since the internal and external clocks are not synchronized the A/D converter will occasionally measure an input when the external clock is making a transition.
2. If the PH2 clock is 1 MHz or greater (i.e. external oscillator 2 MHz or greater and SYS1:0 = 0:0), the internal RC oscillator must be turned off and the external oscillator used as the conversion clock.

13.3.3 MULTI-CHANNEL OPERATION

An input multiplexer allows the A/D converter to select from one of two external analog signals. Port A pins PA4 thru PA5 are shared with the inputs to the multiplexer.

NOTE: Applying analog voltage to A/D input pin that is not selected (used as an I/O port may result in excessive I_{DD}.

13.4 A/D SUBSYSTEM OPERATION DURING WAIT MODES

The A/D subsystem continues normal operation during WAIT modes. To decrease power consumption during WAIT, the ADON and ADRC bits in the A/D Status and Control Register should be cleared if the A/D subsystem is not being used.

13.5 A/D SUBSYSTEM OPERATION DURING STOP MODE

Execution of the STOP instruction will terminate all A/D subsystem functions. Any pending conversion is aborted. When the oscillator resumes operation upon leaving the Stop Mode, a finite amount of time passes before the A/D subsystem stabilizes sufficiently to provide conversions at its rated accuracy. The delays built into the MC68HC(7)05L26 when coming out of Stop Mode are sufficient for this purpose. No explicit delays need to be added to the application software.

13.6 A/D STATUS AND CONTROL REGISTER (ADSC)

The ADSC register reports the completion of A/D conversion and provides control over oscillator selection, analog subsystem power, and input channel selection.

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$001E	A/D STATUS/CONTROL REG ADSCR	R	CC	ADRC	ADON	0	0	CH2	CH1	CH0
		W	—			—	—			
RESET:			0	0	0	0	0	0	0	0

Figure 13-1: A/D Status and Control Register

13.6.1 CC - CONVERSION COMPLETE

This read-only status bit is set when a conversion sequence has completed and data is ready to be read from the ADC register. CC is cleared when a channel is selected for conversion, when data is read from the ADC register, or when the A/D subsystem is turned off. Once a conversion has been started, conversions of the selected channel will continue every 32 PH2 clock cycles until the ADSC register is written to again. During continuous conversion operation the ADC register will be updated with new data, and the CC bit set, every 32 PH2 clock cycles. Also, data from the previous conversion will be overwritten regardless of the state of the CC bit.

13.6.2 ADRC - RC OSCILLATOR CONTROL

When ADRC is set, the A/D subsystem operates from the internal RC oscillator instead of the PH2 clock. The RC oscillator requires a time t_{RCON} to stabilize before accurate conversion results can be obtained. See **Section 13.3.2** for more information.

13.6.3 ADON - A/D SUBSYSTEM ON

When the A/D subsystem is turned on (ADON = 1), it requires a time t_{ADON} to stabilize before accurate conversion results can be attained.

13.6.4 CH2-CH0 - CHANNEL SELECT BITS

CH2, CH1, and CH0 form a 3-bit field which is used to select an input to the A/D converter. Channels 0-1 correspond to Port A input pins PA4:PA5. Channels 4-6 are used for reference measurements. In Single-Chip Mode channels 2, 3, and 7 are reserved. If a conversion is attempted with channel 2, 3, or 7 selected the result will be undefined. **Table 13-1** lists the inputs selected by bits CH0:CH2 bits.

If the ADON bit is set, and an input from channels 0 or 1 is selected, the corresponding Port A pin will not function as a digital port. If the Port A data register is read when DDR=0 while the A/D is on, and one of the shared input channels is selected using bit CH0-CH2, the corresponding Port A pin will read as a logic zero. If the DDR=1, the Port A data register will read the output latch value; The remaining Port A pins will read normally. To digitally read a multiplexed Port A pin as an input port, the A/D subsystem must be disabled (ADON = 0), or input channel 2-7 must be selected. See **Table 7-1** and **Table 7-1**.

Table 13-1: A/D Multiplexer Input Channel Assignments

CHANNEL	SIGNAL
0	AD0 PORT A BIT 4
1	AD1 PORT A BIT 5
2	reserved
3	reserved
4	$V_{REFH} = V_{DD}$
5	$(V_{REFH} + V_{REFL})/2$
6	$V_{REFL} = V_{SS}$
7	FACTORY TEST

13.7 A/D CONVERSION DATA REGISTER (ADC)

This register contains the output of the A/D converter.

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$001D	A/D DATA REGISTER ADC	R	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		W	—	—	—	—	—	—	—	—
RESET:			U	U	U	U	U	U	U	U

Figure 13-2: A/D Conversion Value Data Register

SECTION 14EVENT COUNTER

The Event Counter consists of a 16-bit counter externally driven from the event counter pin, with input gate generation and filtering circuitry. Average frequency measurements can be made over user specified intervals ranging from 4 to 60 msec (with 2MHz bus clock). Measurements are continuously repeated at a user specified rate. A maskable and reset-able Event Count Complete Interrupt and Event Counter Overflow Interrupt are available. Using the Overflow interrupt, an effective 18-bit count can be achieved. See **Figure 7-11**.

- Asynchronous input up to 6Mhz
- Overflow Interrupt
- Event Count Complete Interrupt
- Variable Gate Generation
- “Spike” filter
- Effective 18-bit resolution

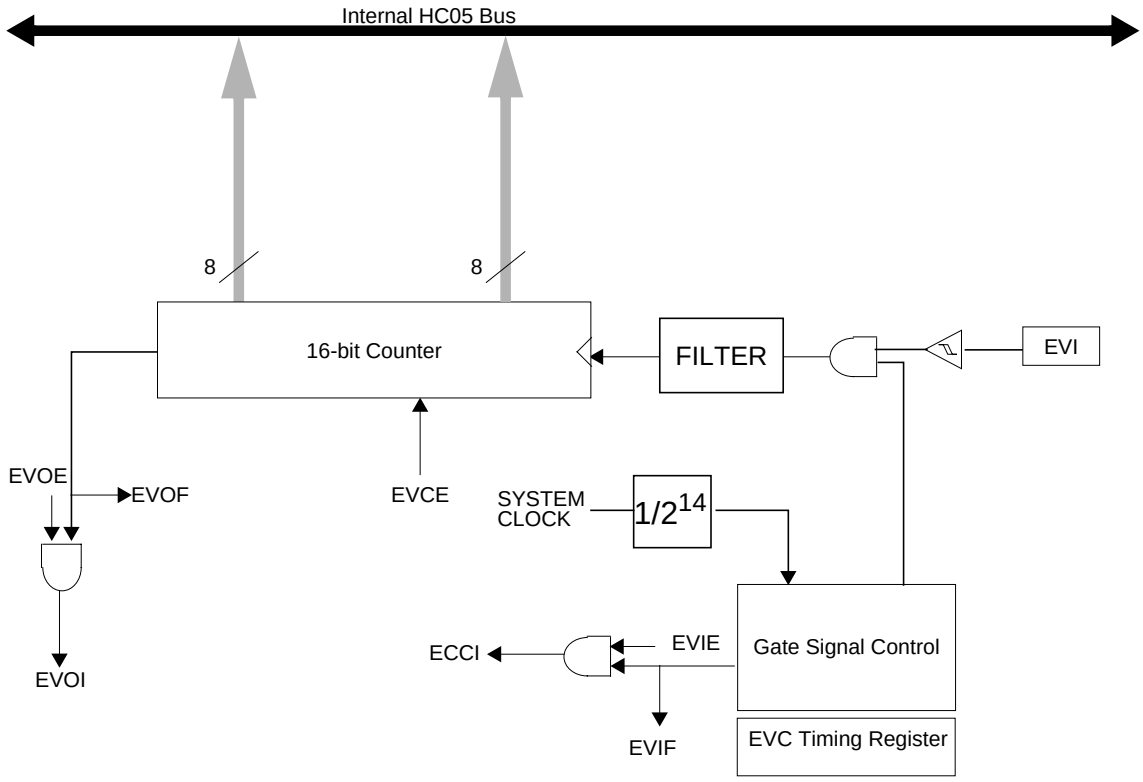


Figure 14-1: Event Counter Block Diagram

14.1 EVENT COUNTER STATUS/CONTROL REGISTER (EVSC)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$002E	EVENT CNTR STAT/CONT REG EVSCR	R	EVCE	EVIE	EVOE	EVIF	EVOF	0	0	0
		W				—	—	RCCF	ROFF	—
		RESET:	0	0	0	0	0	0	0	0

Figure 14-2: Event Counter Status/Control Register

EVCE - EVent Counter Enable
1 = Event Counter enabled
0 = Event Counter disabled

EVIE - EVent count complete Interrupt Enable
1 = Event Count Complete Interrupt enabled
0 = Event Count Complete Interrupt disabled

EVOE - EVent counter Overflow Enable
1 = Event Counter Overflow interrupt enabled
0 = Event Counter Overflow interrupt disabled

EVIF - EVent count complete Interrupt Flag (read only)
1 = Flag set when Gate Delay time expires
0 = Flag cleared when “1” is written to ROFF

EVOF - EVent counter Overflow Flag (read only)
1 = Flag set when Gate Delay time expires
0 = Flag cleared when “1” is written to ROFF

ROIF - Reset Overflow Interrupt Flag (write only)

When a “1” is written to this bit, EVOF is cleared. Always reads as “0”.

RCCF - Reset Count Complete interrupt Flag (write only)

When a “1” is written to this bit, EVIF is cleared. Always reads as “0”.

14.2 EVENT COUNTER TIMING REGISTER (EVTR)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$002F	EVENT COUNTER TIMING REG EVTR	R	WT3	WT2	WT1	WT0	MT3	MT2	MT1	MT0
		W								
	RESET:		1	1	1	1	1	1	1	1

Figure 14-3: Event Counter Timing Register

This register controls generation of the gate signal which is used to control the input to the Event Counter. See **Figure 14-4**.

The value in the Event Counter Timing register determines the length of the measurement and the length of the wait time between measurements. See **Table 14-1** and **Table 14-2**. The measurement time bits, MT3:0, determine the length of time that the input gate on the EVI pin is open. During this time the gate signal is a logic '1'. The wait time bits, WT3:0, determine the length of time that the gate signal is a logic '0'. T_{gc} is the length of a unit count. The specification for T_{gc} may be found in **Section 15.8** and **Section 15.9**.

After being enabled, EVCE = 1, the Event Counter will continuously make measurements. If the Event Counter Timing register is written, the current measurement will be aborted, and a new measurement will be initiated.

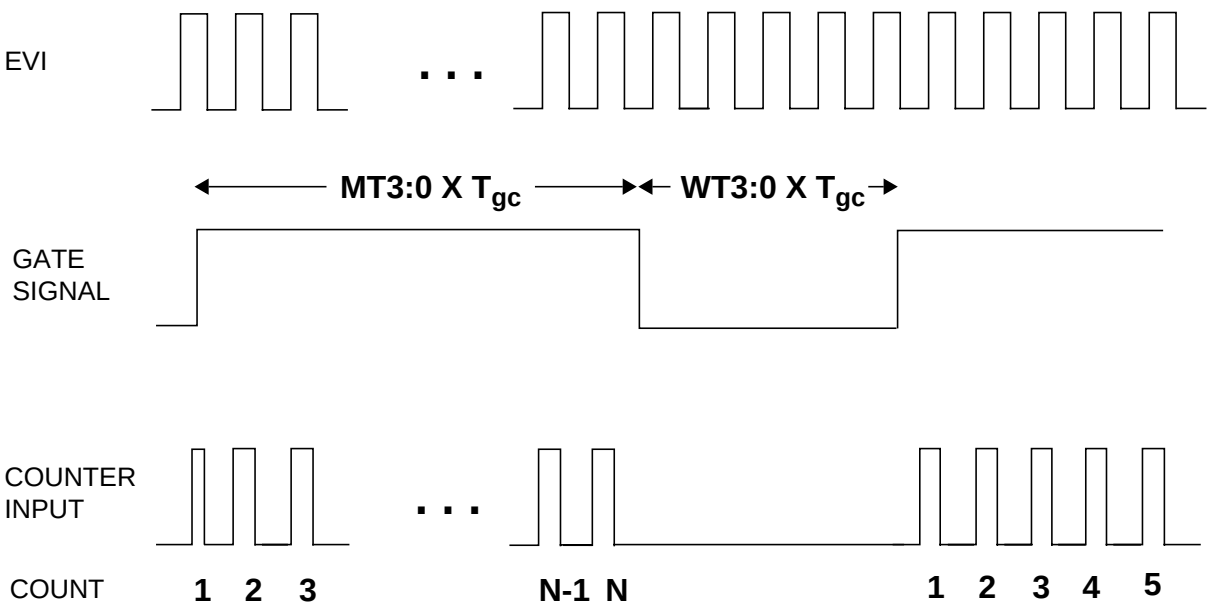


Figure 14-4 Event Counter Input Timing Example

The input to the Event Counter is the logical AND of the signal on the EVI pin and the internally generated gate signal. The rising edges of counter input signal are used to generate the events that increment the counter. If the pulse width of the AND'ed signal is less than that which the circuitry is capable of detecting, the narrow pulse will not be allowed to pass through the filter.

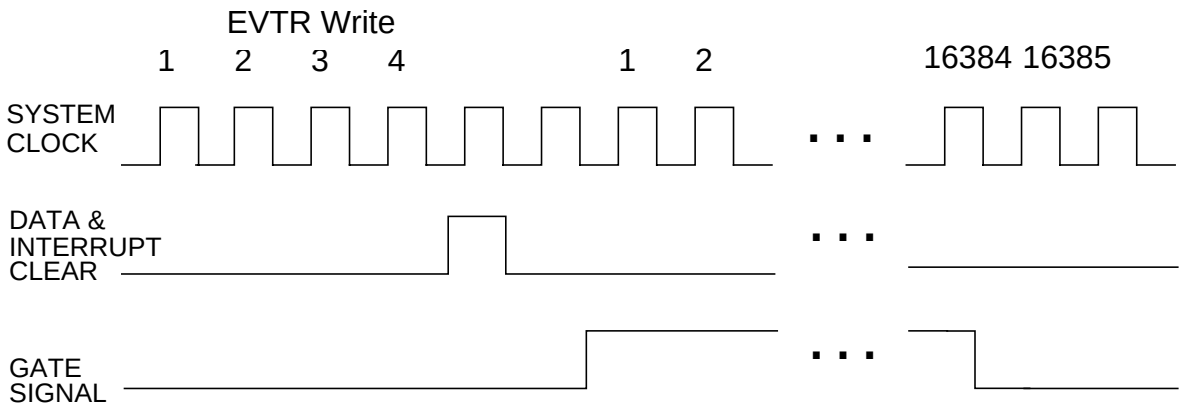
Table 14-1: Measurement Time Nibble

MT3:0	Measurement Time	MT3:0	Measurement Time
$X0	0 msec	$X8	31.250 msec
$X1	3.9063	$X9	35.156
$X2	7.8125	$XA	39.063
$X3	11.719	$XB	42.969
$X4	15.625	$XC	46.875
$X5	19.531	$XD	50.781
$X6	23.438	$XE	54.688
$X7	27.344	$XF	58.593

Table 14-2: Wait Time Nibble

WT3:0	Wait Time	WT3:0	Wait Time
$0X	0 msec	$8x	31.250 msec
$1X	3.9063	$9x	35.156
$2X	7.8125	$Ax	39.063
$3X	11.719	$BX	42.969
$4X	15.625	$CX	46.875
$5X	19.531	$DX	50.781
$6X	23.438	$EX	54.688
$7X	27.344	$FX	58.593

Note: SYS0:1 = 00, Fosc = 4.1943 MHz



Note: MT3:0 = $X1

Figure 14-5 Event Counter Gate Signal Timing Example

The above example illustrates the relation of the Gate Signal to external oscillator clocks for the case of MT3:0 = $1.

The beginning of the gate signal can be caused by a write to the Event Counter Timing Register or expiration of the Wait Time. If the Event Counter Timing Register is written, the rising edge of the gate signal will occur on the fourth internal processor clock cycle of the write to the Event Counter Timing register.The Event Counter Data Registers are cleared on the rising edge of the internal Gate Signal. The external Gate signal rises two clock cycles later.

After MT3:0 X T_{gt}, the Gate Signal will rise, terminating the measurement time. The Gate Signal will be the same length for all successive measurements.

Unless the start of the gate delay signal and the Event Counter Input signal are externally synchronized, the value of the least significant bit of the Event Counter Data Low Register may arbitrarily change.

If the fast oscillator, OSC, is disabled, the Event Counter will not function properly.

14.3 EVENT COUNTER INTERRUPTS

The Event Count Complete Interrupt, ECCI is generated at the falling edge of the gate signal. This interrupt indicates the presence of valid data in the Event Counter Data Registers. Since reading the data registers during the measurement time may give invalid results, the CPU must read the data registers before the rising edge of the gate signal. The Event Count Complete Interrupt may be cleared by writing a ’1’ to RCCF. The Event Count Complete Interrupt is automatically cleared at the beginning of each measurement.

The Event Counter Overflow Interrupt, EVOF is generated if the count exceeds 65,535, the maximum value of the 16-bit Event Counter. This interrupt may be used to indicate an invalid measurement or to increase the resolution of the Event Counter, as will be described later. The Event Counter Overflow Interrupt may be cleared by writing a ’1’ to ROIF. The Event Counter Overflow Interrupt is automatically cleared at the beginning of each measurement.

If an overflow occurs (the counter increments beyond $FFFF), the Event Counter Overflow Flag (EVOF) will be set. If EVOE is set, an interrupt will be generated. Following an overflow, the Event Counter will increment from zero.

The resolution of the Event Counter can be increased by using the Event Counter Overflow Interrupt. If a count of more than 65,535, the maximum value of the 16-bit Event Counter, is encountered, the Event Counter overflow interrupt service routine should note the number of “roll-overs” that occur. The Overflow Interrupt service routine should not clear the Event Counter Interrupt. In this way, the user can be assured that the correct count has been recorded.

14.4 EVENT COUNTER DATA REGISTERS (EVDH) & (EVDL)

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$0030	EVENT CNTR DATA REG H EVDH	R	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
		W								
		RESET:	0	0	0	0	0	0	0	0

Figure 14-6: Event Counter Data High Register

ADDR	REGISTER	RW	7	6	5	4	3	2	1	0
$0031	EVENT CNTR DATA REG L EVDL	R	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W								
		RESET:	0	0	0	0	0	0	0	0

Figure 14-7: Event Counter Data Low Register

These read only registers are the basis of all Event Counter operations. While the gate signal is low, the value of the most recent event count will remain in the Event Counter Data Registers. Following the Event Counter Interrupt, the result of the event count can be read. If the Event Counter Data Registers are read while the gate signal is high, an incorrect value may result.

14.5 EVENT COUNTER DURING WAIT MODE

The Event Counter continues to operate in WAIT mode. If EVOE is set and an event counter overflow interrupt occurs, the processor will exit WAIT mode. If EVIE is set and an event counter interrupt occurs, the processor will exit WAIT mode.

14.6 EVENT COUNTER DURING STOP MODE

In the STOP mode, the event counter is disabled.

SECTION 15ELECTRICAL SPECIFICATIONS

NOTE: Values specified as TBD are to be determined after a full characterization. These figures are design target values and do not reflect actual measurements.

15.1 MAXIMUM RATINGS

(Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage (normal digital level)	V_{IN}	V_{SS} -0.3 to V_{DD} +0.3	V
High Voltage (PA0:3, PC3, and PC2 only)	V_{IN}	V_{SS} -0.3 to 9.3	V
Current Drain Per Pin Excluding V_{DD} and V_{SS}	I	25	mA
Operating Temperature Range MC68HC705L26 (Standard)	T_A	T_L to T_H 0 to +70	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage (normal digital level)	V_{IN}	V_{SS} -0.3 to V_{DD} +0.3	V
High Voltage (PA0:3, PC3, and PC2 only)	V_{IN}	V_{SS} -0.3 to 9.3	V
Current Drain Per Pin Excluding V_{DD} and V_{SS}	I	25	mA
Operating Temperature Range MC68HC05L25 (Standard)	T_A	T_L to T_H 0 to +70	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

15.2 DC OPERATING CHARACTERISTICS

(V_{SS} = 0 VDC, T_A = +25°C)

Characteristic	Symbol	Min	Max	Unit
Operating Voltage				
MC68HC05L26 external clock source f_{osc} = 1.0 MHz	V_{DD}	2.2	5.5	V
MC68HC705L26 external clock source f_{osc} = 2.0 MHz	V_{DD}	2.8	5.5	V
MC68HC(7)05L26 external clock source f_{osc} = 4.0 MHz	V_{DD}	3.0	5.5	V
MC68HC(7)05L26 external clock source f_{osc} = 5.0 MHz	V_{DD}	3.7	5.5	V

Characteristic	Symbol	Min	Max	Unit
Operating Voltage				
MC68HC05L25 external clock source f_{osc} = 1.0 MHz	V_{DD}	2.2	5.5	V
MC68HC05L25 external clock source f_{osc} = 4.0 MHz	V_{DD}	3.0	5.5	V

15.3 DC ELECTRICAL CHARACTERISTICS (VDD = 3.3V)

(VDD = 3.3 VDC 10%, VSS = 0 VDC, TA = -40°C to +85°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage					
I_{Load} = 10.0 µA	V_{OL}	—	—	0.1	V
	V_{OH}	V_{DD} - 0.1	—	—	
Output High Voltage					
(I_{Load} = -0.8 mA) PA0:7, PB0:7, PC0:PC1	V_{OH}	V_{DD} - 0.8	—	—	V
Output Low Voltage					
(I_{Load} = 1.6 mA) PA0:7, PD0:7, PC0:3	V_{OL}	—	—	0.3	V
(I_{Load} = 20 mA) PA0:3		—	—	0.8	V
Input High Voltage					
(I_{Load} = -0.8 mA) PA0:7, PB0:7, PC0:3 $\overline{IRQ}$, $\overline{RESET}$, XOSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input Low Voltage					
(I_{Load} = 1.6 mA) PA0:7, PB0:7, PC0:3 $\overline{IRQ}$, $\overline{RESET}$, XOSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply Current (see Notes)					
Run (f_{op} = 1.0 MHz)	I_{DD}	—	1.0	5.0	mA
Wait (f_{op} = 1.0 MHz)	I_{DD}	—	0.5	3.0	mA
Stop (with Time Base running; LCD off)					
25 °C	I_{DD}	—	5.0	10	µA
0 °C to +70 °C (Standard)	I_{DD}	—	—	30	µA
I/O Ports Hi-Z Leakage Current					
(without individual pullup activated) PA0:7, PB0:7, PC0:3	I_{IL}	—	—	±10	µA
Pullup Resistor (with individual pullup activated)					
PA0:7, PB0:7	R_p	25	50	200	KΩ
PC0:3	R_p	5	10	40	KΩ
Input Current					
$\overline{RESET}$, $\overline{IRQ}$, XOSC1	I_{in}	—	—	±1	µA
Capacitance					
Ports (as Input or Output)	C_{out}	—	—	12	pF
$\overline{RESET}$, $\overline{IRQ}$, XOSC1, XOSC2	C_{in}	—	—	8	pF
Crystal Oscillator Mode Feedback Resistor					
OSC1 to OSC2	R_{OF}	1.0	2.0	4.0	MΩ
XOSC1 to XOSC2	R_{XOF}	1.0	2.0	4.0	MΩ
Crystal Oscillator Mode Damping Resistor					
on XOSC2	R_{XOD}	1.0	2.0	4.0	MΩ

NOTES:

1. All values shown reflect average measurements. (These values are design targets and not characterization results.)
2. Typical values at midpoint of voltage range, 25°C only.
3. Wait I_{DD}: Only time Base active.
4. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square wave clock source to OSC1 (f_{OP} = 1.0 MHz), all inputs 0.2 VDC from rail; no DC loads, less than 50pF on all outputs, C_L = 20 pF on OSC2.
5. Wait, Stop I_{DD}: All ports configured as inputs, V_{IL} = 0.2 VDC, V_{IH} = V_{DD}-0.2 VDC.
6. Wait, Stop I_{DD} is affected linearly by the OSC2, XOSC2 capacitance.

15.4 DC ELECTRICAL CHARACTERISTICS (VDD = 5.0V)

(VDD = 5.0 VDC ± 10%, VSS = 0 VDC, TA = -40°C to +85°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage					
I_{Load} = 10.0 µA	V_{OL}	—	—	0.1	V
	V_{OH}	V_{DD} - 0.1	—	—	
Output High Voltage					
(I_{Load} = -0.8 mA) PA0:7, PB0:7, PC0:PC1	V_{OH}	V_{DD} - 0.8	—	—	V
Output Low Voltage					
(I_{Load} = 1.6 mA) PA0:7, PD0:7, PC0:3	V_{OL}	—	—	0.3	V
(I_{Load} = 20 mA) PA0:3		—	—	0.8	V
Input High Voltage					
(I_{Load} = -0.8 mA) PA0:7, PB0:7, PC0:3 $\overline{IRQ}$, $\overline{RESET}$, XOSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input Low Voltage					
(I_{Load} = 1.6 mA) PA0:7, PB0:7, PC0:3 $\overline{IRQ}$, $\overline{RESET}$, XOSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply Current (see Notes)					
Run (f_{op} = 2.1 MHz)	I_{DD}	—	10	15	mA
Wait (f_{op} = 2.1 MHz)	I_{DD}	—	4.0	7	mA
Stop (with Time Base running)					
25 °C	I_{DD}	—	10	20	µA
0 °C to +70 °C (Standard)	I_{DD}	—	—	60	µA
I/O Ports Hi-Z Leakage Current					
(without individual pullup activated) PA0:7, PB0:7, PC0:3	I_{IL}	—	—	±10	µA
Pullup Resistor (with individual pullup activated)					
PA0:7, PB0:7	R_p	TBD	TBD	TBD	KΩ
PC0:3	R_p	TBD	TBD	TBD	KΩ
Input Current					
$\overline{RESET}$, $\overline{IRQ}$, XOSC1	I_{in}	—	—	±1	µA
Capacitance					
Ports (as Input or Output)	C_{out}	—	—	12	pF
$\overline{RESET}$, $\overline{IRQ}$, XOSC1, XOSC2	C_{in}	—	—	8	pF
Crystal Oscillator Mode Feedback Resistor					
OSC1 to OSC2	R_{OF}	TBD	TBD	TBD	MΩ
XOSC1 to XOSC2	R_{XOF}	TBD	TBD	TBD	MΩ
Crystal Oscillator Mode Damping Resistor					
on XOSC2	R_{XOD}	TBD	TBD	TBD	MΩ

NOTES:

1. All values shown reflect average measurements. (These values are design targets and not characterization results.)
2. Typical values at midpoint of voltage range, 25°C only.
3. Wait I_{DD}: Only time Base active.
4. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square wave clock source to OSC1 (f_{OP} = 32.768 KHz), all inputs 0.2 VDC from rail; no DC loads, less than 50pF on all outputs, C_L = 20 pF on OSC2.
5. Wait, Stop I_{DD}: All ports configured as inputs, V_{IL} = 0.2 VDC, V_{IH} = V_{DD}-0.2 VDC.
6. Wait, Stop I_{DD} is affected linearly by the OSC2, XOSC2 capacitance.

15.5 LCD DC ELECTRICAL CHARACTERISTICS (VDD = 3.3V)

(VDD = 3.3 VDC ± 10%, VSS = 0 VDC, VLCD=0 VDC, TA = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
LCD bias resistance Default Low current mode	R_{LCD}	 15 100	 30 200	 120 800	 KΩ KΩ
Output Current, Backplanes and Frontplanes High-Current State (Default)V_O = 2.85V V_O = 1.85V V_O = 1.15V V_O = 0.15V	I_{BH}	TBD	 - 235 -10.9 10.9 235	 — — — —	µA
Low-Current StateV_O = 2.85V V_O = 1.85V V_O = 1.15V V_O = 0.15V	I_{BL}	TBD	- 235 - 0.94 0.94 235	— — — —	

NOTES:
1. All values shown reflect average measurements. (These values are design targets and not characterization results.)
2. If the FC option is selected, for time 1/(32 x fLCD) after the backplane or frontplane waveform changes to a new voltage level, the circuit is maintained in the high current state to allow the load capacitors to charge quickly. Then the circuit is returned to the low-current state until the next voltage level change occurs.

15.6 LCD DC ELECTRICAL CHARACTERISTICS (VDD = 5.0V)

(VDD =5.0 VDC ± 10%, VSS = 0 VDC, VLCD=0 VDC, TA = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
LCD bias resistance Default Low current mode	R_{LCD}	 15 100	 30 200	 120 800	 KΩ KΩ
Output Current, Backplanes and Frontplanes High-Current State (Default)V_O = 4.85V V_O = 3.18V V_O = 1.82V V_O = 0.15V	I_{BH}	TBD	 - 395 - 13.6 13.6 395	 — — — —	µA
Low-Current StateV_O = 4.85V V_O = 3.18V V_O = 1.82V V_O = 0.15V	I_{BL}	TBD	- 395 - 0.96 0.96 395	— — — —	

NOTES:
1. All values shown reflect average measurements. (These values are design targets and not characterization results.)
2. If the FC option is selected, for time 1/(32 x fLCD) after the backplane or frontplane waveform changes to a new voltage level, the circuit is maintained in the high current state to allow the load capacitors to charge quickly. Then the circuit is returned to the low-current state until the next voltage level change occurs.

15.7 A/D CONVERTER CHARACTERISTICS

(V_{DD} = 5.0 V_{dc} ±10%, V_{SS} = 0 V_{dc}, T_A = -40°C to +85°C, unless otherwise noted)

Characteristic	Min	Max	Units	Comments
Resolution	TBD	8	Bit	
Absolute Accuracy (V_{DD} = 5.0V) (V_{DD} = 3.0V)	 — —	 ±1 1/2 ±2	 LSB LSB	 Refer to Note 1. Refer to Note 1.
Conversion Range	V_{SS}	V_{DD}	V	
Power-up Time	—	100	µs	
Conversion Time (Includes Sampling Time) External Clock (MCU System Clock) Internal RC Oscillator (ADRC=1)	 32 32	 32 32	 T_{AD} µs	 Refer to Note 3.
Monotonicity	Inherent (Within Total Error)			
Zero Input Reading	00	01	Hex	V_{in} = 0V
Ratiometric Reading	FF	FF	Hex	V_{in} = V_{DD}
Sample Acquisition Time External Clock (MCU System Clock) Internal RC Oscillator (ADRC=1)	 12 —	 12 12	 T_{AD} µs	Refer to Note 2. Refer to Note 3.
Input Capacitance	—	8	pF	
Analog Input Voltage	V_{SS}	V_{DD}	V	
Input Leakage AD0, AD1	 —	 ±400	 nA	Refer to Note 4.

Note:

1. Error includes quantization. A/D accuracy may decrease proportionately as V_{DD} is reduced below 3.0 V.
2. Souce impedances greater than 10kΩ adversely affect internal RC charging time during input sampling.
3. T_{AD} = t_{cyc} if clock source equals MCU.
4. The external system error caused by input leakage current is approximately equal to the product of R source and input current.

15.8 CONTROL TIMING (VDD = 3.3V)

(V_{DD} = 3.3 VDC ±10%, V_{SS} = 0 VDC, T_A = -40°C to +85°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of Operation					
OSC Crystal Oscillator Option	f_{OSC}	TBD	2.097152	4.0	MHz
XOSC Crystal Oscillator Option	f_{XOSC}	TBD	32.768	TBD	kHz
External Clock Source	f_{OSC}	DC	—	4.0	MHz
Internal Operating Frequency					
Crystal Oscillator (f_{OSC} ÷ 2)	f_{OP}	—	1.048576	2.0	MHz
External Clock (f_{OSC} ÷ 2)	f_{OP}	DC	1.048576	2.0	MHz
Cycle Time (1/f_{OP})	t_{CYC}	500	—	—	nS
Crystal Oscillator Start-up Time (Crystal Oscillator option)	t_{OXON}	—	—	100	mS
$\overline{\text{RESET}}$ Pulse Width Low	t_{RL}	1.5	—	—	t_{CYC}
$\overline{\text{IRQ}}$ Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	125	—	—	nS
$\overline{\text{IRQ}}$ Interrupt Pulse Period	t_{ILIL}	note 1	—	—	t_{CYC}
OSC1 Pulse Width	t	100	—	—	nS
Event Counter Gate Count	T_{GC}	16384	16384	16384	f_{osc}

NOTES:
1. The minimum period t_{ILIL} or t_{IHIH} should not be less than the number of cycles it takes to execute the interrupt service routine plus 21 t_{CYC}.
2. Effects of processing, temperature, and supply voltage (excluding tolerances of external R and C).

15.9 CONTROL TIMING (VDD = 5.0V)

(V_{DD} = 5.0 VDC ±10%, V_{SS} = 0 VDC, T_A = -40°C to +85°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of Operation					
OSC Crystal Oscillator Option	f_{OSC}	TBD	4.194304	8.0	MHz
XOSC Crystal Oscillator Option	f_{XOSC}	TBD	32.768	TBD	kHz
External Clock Source	f_{OSC}	DC	—	8.0	MHz
Internal Operating Frequency					
Crystal Oscillator (f_{OSC} ÷ 2)	f_{OP}	—	2.097152	4.0	MHz
External Clock (f_{OSC} ÷ 2)	f_{OP}	DC	2.097152	4.0	MHz
Cycle Time (1/f_{OP})	t_{CYC}	250	—	—	nS
Crystal Oscillator Start-up Time (Crystal Oscillator option)	t_{OXON}	—	—	100	mS
$\overline{\text{RESET}}$ Pulse Width Low	t_{RL}	1.5	—	—	t_{CYC}
$\overline{\text{IRQ}}$ Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	62.5	—	—	nS
$\overline{\text{IRQ}}$ Interrupt Pulse Period	t_{ILIL}	note 1	—	—	t_{CYC}
OSC1 Pulse Width	t	50	—	—	nS
Event Counter Gate Count	T_{GC}	16384	16384	16384	f_{osc}

NOTES:
1. The minimum period t_{ILIL} or t_{IHIH} should not be less than the number of cycles it takes to execute the interrupt service routine plus 21 t_{CYC}.
2. Effects of processing, temperature, and supply voltage (excluding tolerances of external R and C).