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MC68HC805C4/D
Rev. 0.1

MC68HC805C4

MC68HC805C4 Microcontroller Unit (MCU)

MC68HC805C4 microcontroller unit (MCU) is similar to the MC68HC05C4 MCU device with the exception of the electrically erasable programmable read-only memory (EEPROM) feature. This feature of the MC68HC805C4 MCU enables the user to emulate the MC68HC05C4 MCU device. The entire data sheet of the MC68HC05C4 MCU (Motorola document number MC68HC05/C4/D) applies to the MC68HC805C4 MCU with the exceptions provided in this document.

INTRODUCTION

Information contained in *MC68HC05C4 Technical Data* (general information, features, and block diagram) applies to the MC68HC805C4 MCU device except for the areas described in the following paragraphs.

Features

The features of the MC68HC805C4 MCU are as follows:

- Emulation of MC68HC05C4
- 4160 Bytes of EEPROM (Replaces 4160 Bytes of ROM on MC68HC05C4)
- On-Chip Bootstrap Firmware for Programming Use
- User Callable Subroutines to Simplify Programming[1]
- Breakpoint Register for Software Debugging
- Self-Check Mode Replaced by Bootstrap Capability
- Software Programmable External Interrupt Sensitivity (Default is Edge- and Level-Sensitive)

[1]Contact local Motorola representative.

Block Diagram

Figure 1 illustrates the MC68HC805C4 MCU device block diagram.

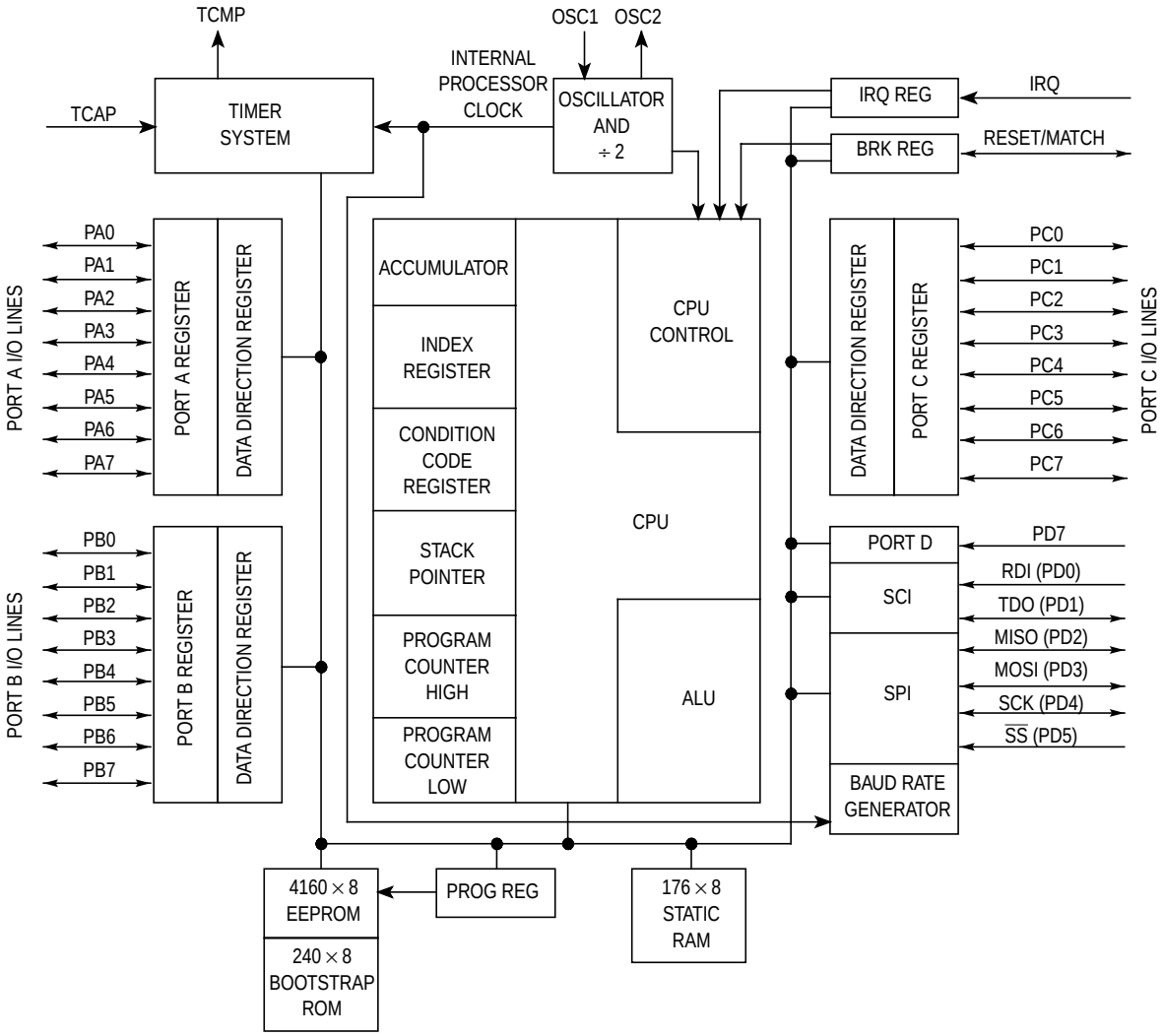


Figure 1. MC68HC805C4 Microcomputer Block Diagram

FUNCTIONAL PIN DESCRIPTION, INPUT/OUTPUT PROGRAMMING, MEMORY, CPU REGISTERS, AND SELF-CHECK

Information contained in *MC68HC05C4 Technical Data* applies to the MC68HC805C4 MCU device except for the areas described in the following paragraphs.

Reset/Match ($\overline{\text{RESET}}$/$\overline{\text{MATCH}}$)

The $\overline{\text{RESET}}$/$\overline{\text{MATCH}}$ pin (pin 1) provides two functions. These functions are used to master reset the MCU or generate an address match breakpoint pulse. When master resetting, pin 1 is an input to the MCU device. When generating the breakpoint pulse, pin 1 is an output from the MCU. Refer to **HARDWARE BREAKPOINT REGISTERS** for additional information pertaining to the $\overline{\text{RESET}}$/$\overline{\text{MATCH}}$ pin.

V_{PP}

External V_{PP} (19.75 Vdc ± 0.25 Vdc) must be supplied to the V_{PP} pin (pin 3) for programming and erasing the EEPROM arrays.

Memory

Figure 2 illustrates the MC68HC805C4 MCU device address map. As shown, page zero resides from $0000 through $00FF, and is accessed with short instructions.

All user defined reset and interrupt vectors are implemented in EEPROM.

Self-Check

The self-check ROM is replaced with the bootstrap ROM, therefore the self-check capability is not applicable for the MC68HC805C4 device. Timer test and ROM checksum subroutines are part of the self-check routine. Therefore, both subroutines are also not applicable.

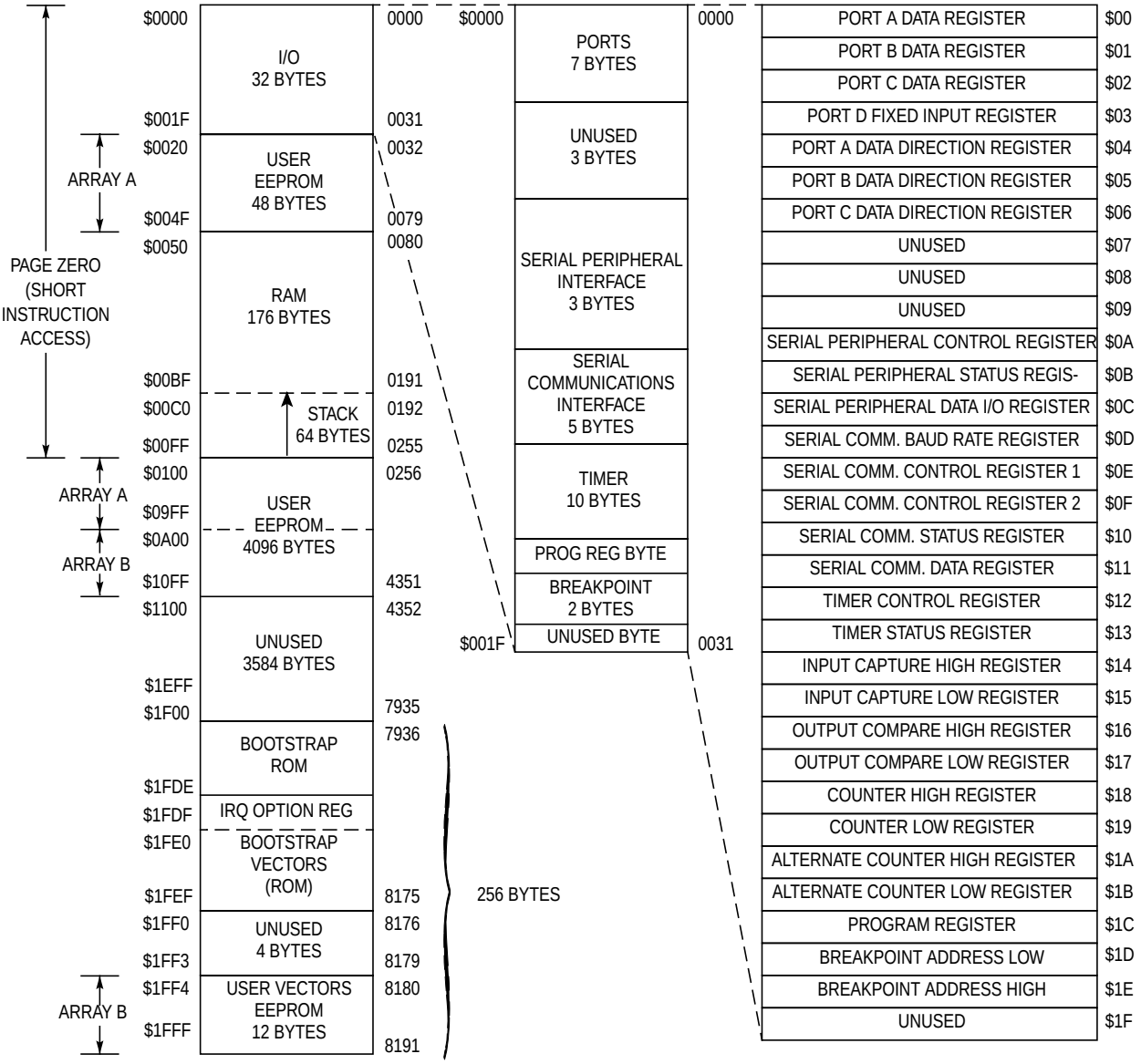


Figure 2. MC68HC805C4 Memory Map

RESETS, INTERRUPTS, AND LOW POWER MODES

Information contained in *MC68HC05C4 Technical Data* applies to the MC68HC805C4 MCU device except for the areas described in the following paragraphs.

External Interrupt

The MC68HC05C4 MCU $\overline{\text{IRQ}}$ pin sensitivity is mask programmable. Either negative edge- and level-sensitive triggering, or negative edge-sensitive triggering are available as a mask option. The MC68HC805C4 MCU uses the IRQ option register residing at location $1FDF to control the $\overline{\text{IRQ}}$ pin sensitivity.

IRQ Option Register

Bit 7	6	5	4	3	2	1	Bit 0	
0	0	0	0	0	0	IRQ	0	$1FDF

B7–B2 Logic zero

B1 When the interrupt request (IRQ) bit is set (logic one), the $\overline{\text{IRQ}}$ pin is negative edge- and level-sensitive. When the IRQ bit is cleared (logic zero), the $\overline{\text{IRQ}}$ pin is negative edge sensitive. The IRQ bit is set by system reset. This control bit can only be cleared once following a reset.

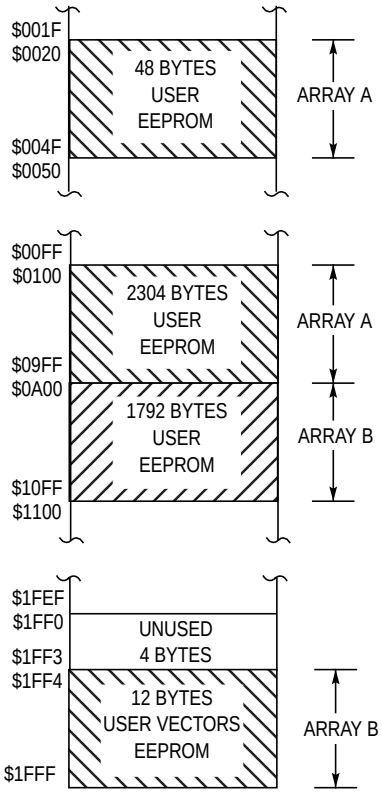
B0 Logic zero

Low Power Modes

Low power mode information for the MC68HC05C4 device is applicable for the MC68HC805C4 MCU device.

EEPROM

Information in this section pertains to the MC68HC805C4 MCU EEPROM. The MCU EEPROM consists of 4144 bytes of user EEPROM (which includes 48-bytes in page zero), and 16 bytes of user vector EEPROM. As shown in Figure 2, the user EEPROM resides at locations $0020–$004F, and $0100–$10FF. User vector EEPROM resides at locations $1FF0–$1FFF. The MCU EEPROM is implemented as two separate EEPROM arrays. These arrays (shown below) are designated as A and B. Array A consists of page zero EEPROM ($0020–$004F) and locations $0100–$09FF; and array B consists of locations $0A00–$10FF, and locations $1FF0–$1FFF. Each array has assigned programming address and data buses which are latched while a programming function is being performed. Separate arrays allow program execution in one array, while writing/erasing in the other array.



Two types of EEPROM programming (single-byte or multi-byte) can be performed. Single-byte EEPROM programming is accomplished via the program register residing at location $001C. Multi-byte EEPROM programming is used to load a user program into the MC68HC805C4 MCU EEPROM in order to emulate the MC68HC05C4 device. This type of programming is accomplished via the bootstrap mode operation. (See **MC68HC05C4 EMULATION**.)

Program Register

The program register (shown below) is used to perform single-byte EEPROM programming.

Program Register

Bit 7	6	5	4	3	2	1	Bit	
0	EEEN	0	0	ERASE	LATA	LATB	EEPGM	$1C

B7 Logic zero.

B6 The EEEN bit must be enabled for any EEPROM write/erase operation. Reset clears the EEEN bit. The EEEN bit should be cleared upon completion of any EEPROM write/erase operation, or before entering the low power modes (via the STOP or WAIT instructions) to reduce power usage. This bit is both readable and writable.

B5/B4 Logic zero.

B3 When the erase (ERASE) bit is set, the erase mode of the EEPROM programming operation is enabled. Reset clears the ERASE bit. When the ERASE bit is cleared, normal read or program modes can be specified. This bit is both readable and writable.

B2 Prior to an array A write or erase operation, the latch A (LATA) bit must be set. This enables the EEPROM array A data and address buses to be latched for programming/erasing on the next byte write cycle. Reset clears the LATA bit. When the LATA bit is cleared, array A data and address buses are unlatched for normal CPU operations. This bit is both readable and writable.

B1 Prior to an array B write or erase operation, the latch B (LATB) bit must be set. This enables the EEPROM array B data and address buses to be latched for programming/erasing on the next byte write cycle. Reset clears the LATB bit. When the LATB bit is cleared, array B data and address buses are unlatched for normal CPU operations. This bit is both readable and writable.

B0 When the electrically erase/program (EEPGM) bit is set, V_{PP} power is applied to the EEPROM array for programming or erasing modes of operation. Reset clears the EEPGM bit. This bit is readable, but only writable when LATA or LATB bits are set and a write operation to the corresponding array has occurred. If LATA and LATB bits are cleared, EEPGM bit cannot be set.

Single-Byte Programming

Figure 3 illustrates the MC68HC805C4 EEPROM single-byte programming operation. The write cycle timing listed in the flowchart is preliminary and subject to change.

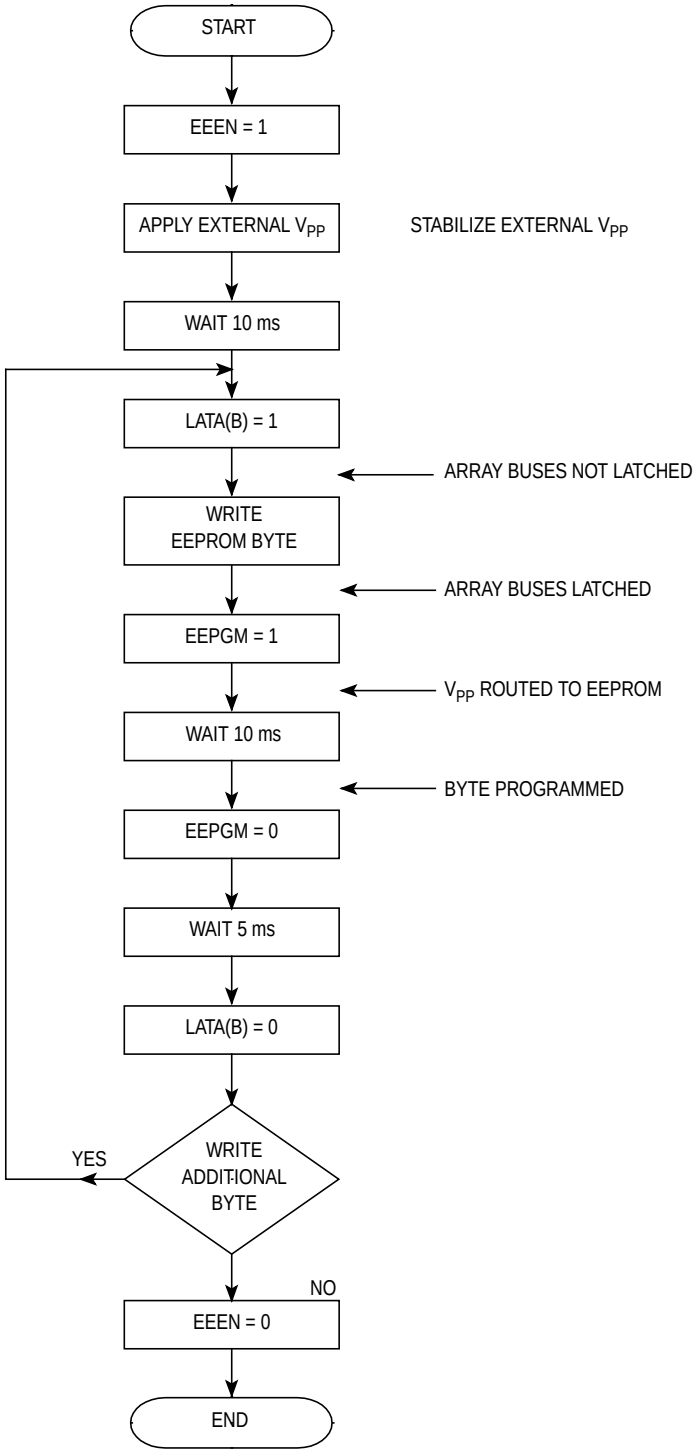


Figure 3. Single-Byte EEPROM Programming

Erasing

Each array can be erased independently or simultaneously. Figure 4 illustrates the MC68HC805C4 EEPROM erasing operation. EEPROM erasing operation takes up to 100 milliseconds. If both arrays A and B are erased simultaneously, the operation takes up to 200 milliseconds. Both arrays may be erased by setting both LATA and LATB bits, and writing (any kind of data) to a byte in both arrays before setting the EEPGM bit.

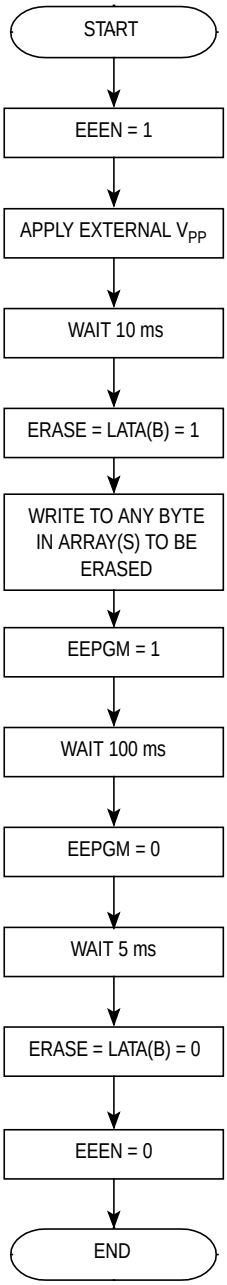


Figure 4. EEPROM Erasing

HARDWARE BREAKPOINT REGISTERS

The hardware breakpoint registers (shown below) are used as a program debugging aid.

Breakpoint Address Register Low (ARL)

Bit 7	6	5	4	3	2	1	Bit 0	
A7	A6	A5	A4	A3	A2	A1	A0	$1D

B7–B0 Breakpoint address bits A7 through A0. Reset clears address bits A7 through A0.

Breakpoint Address Register High (ARH)

Bit 7	6	5	4	3	2	1	Bit	
0	0	MATCH	A12	A11	A10	A9	A8	$1E

B7/B6 Logic zero.

B5 When the match (MATCH) enable bit is set, the address match comparator is enabled. Reset clears the MATCH bit.

B4–B0 Breakpoint address bits A12 through A8. Reset clears address bits A12 through A8.

A breakpoint address is written into address registers ARL and ARH by the user. The lower eight bits (A0–A7) of the breakpoint address are written into the ARL. The upper five bits (A8–A12) of the breakpoint address are written into the ARH. ARL and ARH are then concatenated to form the breakpoint address. When the processor fetches an instruction with the same address as the breakpoint address, $\overline{\text{RESET}}$/$\overline{\text{MATCH}}$ pin goes low for one-half machine cycle. The pin is then driven high (completing the breakpoint pulse) for one-half cycle to ensure that no false resets are generated on successive cycles. This operation will not alter program flow.

The $\overline{\text{RESET}}$/$\overline{\text{MATCH}}$ pin will require that the user provide an open-drain device during debugging operations to avoid any conflicts. A maximum of 100 picofarads load is allowed on the $\overline{\text{RESET}}$/$\overline{\text{MATCH}}$ pin when in the debug mode.

ELECTRICAL SPECIFICATIONS

Information contained in *MC68HC05C4 Technical Data* applies to the MC68HC805C4 MCU device except for the areas described in the following paragraphs.

Estimated operating (run) current at 5.0 Vdc ± 10% is typically 2 milliamperes greater than MC68HC05C4. The wait mode increase (from MC68HC05C4 to MC68HC805C4) is typically 200–300 microamperes. Maximum supply current specifications for the MC68HC805C4 are to be determined.

$\overline{\text{RESET}}$/$\overline{\text{MATCH}}$ pin output levels are equivalent to the output levels of ports A, B, and C.

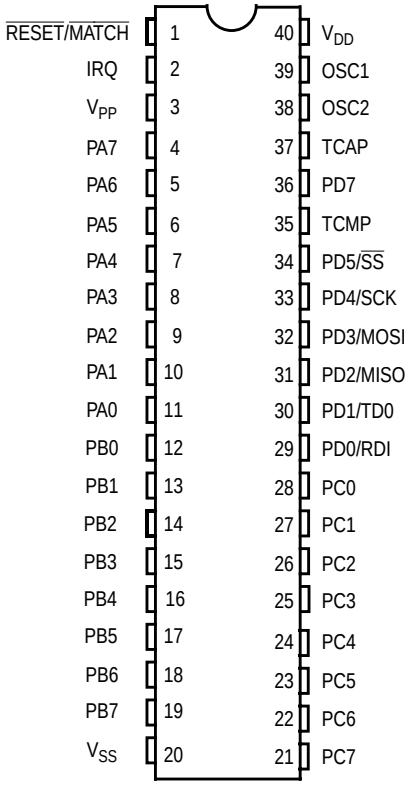
ORDERING INFORMATION

Refer to *MC68HC05C4 Technical Data* for MCU ordering form information.

MECHANICAL DATA

Information contained in *MC68HC05C4 Technical Data* applies to the MC68HC805C4 MCU device except for the pin assignments which are identified in Figure 5.

40-PIN DUAL IN-LINE PACKAGE



NOTE: BULK SUBSTRATE TIED TO V_{SS}.

44-LEAD PLCC PACKAGE

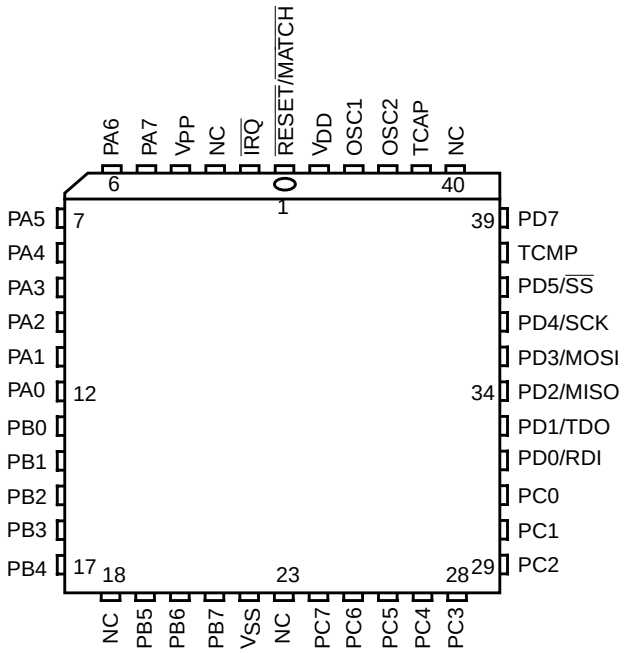


Figure 5. Pin Assignments

MC68HC05C4 EMULATION

The EEPROM feature of the MC68HC805C4 MCU enables the user to emulate the MC68HC05C4 MCU device. The following paragraphs describe the multi-byte EEPROM programming technique used to program the MC68HC805C4 MCU internal EEPROM to

emulate the MC68HC05C4 MCU device. The multi-byte EEPROM programming technique uses a bootstrap program contained in ROM to program the MC68HC805C4 MCU internal EEPROM. Figure 6 illustrates typical MC68HC805C4 MCU EEPROM programming board/circuitry used in conjunction with the multi-byte EEPROM programming technique.

MULTI-BYTE PROGRAMMING

The multi-byte EEPROM programming technique is used to load a user program into the MC68HC805C4 MCU EEPROM in order to emulate the MC68HC05C4 device. This type of multi-byte programming is accomplished via a bootstrap mode of operation. The user program contained in EPROM is copied into the internal EEPROM of the MC68HC805C4 device.

The MC68HC805C4 device is inserted into the programming board/circuitry as illustrated in Figure 6. Programming routine is selected via mode switches S1 through S4, and +5 volt power is applied to the programming circuitry. The MCU is removed from the reset state and placed in the run mode of operation via switch S5, and MCU control is transferred to the bootstrap ROM. The selected programming routine is then executed.

EEPROM programming sequence of events are as follows:

1. Place switch S5 to RESET position.
2. Select programming routine via switches S1–S4.
3. Apply +5 volt power to programming circuitry.
4. Apply external V_{PP} to programming circuitry.
5. Place switch S5 in RUN position.
6. Programming routine is executed.
7. Place switch S5 to RESET position.
8. Remove external V_{PP} from programming circuitry.
9. Remove +5 volt power, or select and run new routine.

Once the bootstrap mode is entered, mode switch settings are scanned to establish the routine to be executed. The routines are as follows:

- Program and Verify EEPROM
- Bulk Erase and Verify EEPROM
- Load Program in RAM and Execute
- Verify EEPROM Contents
- Dump EEPROM Contents
- Execute Program in RAM

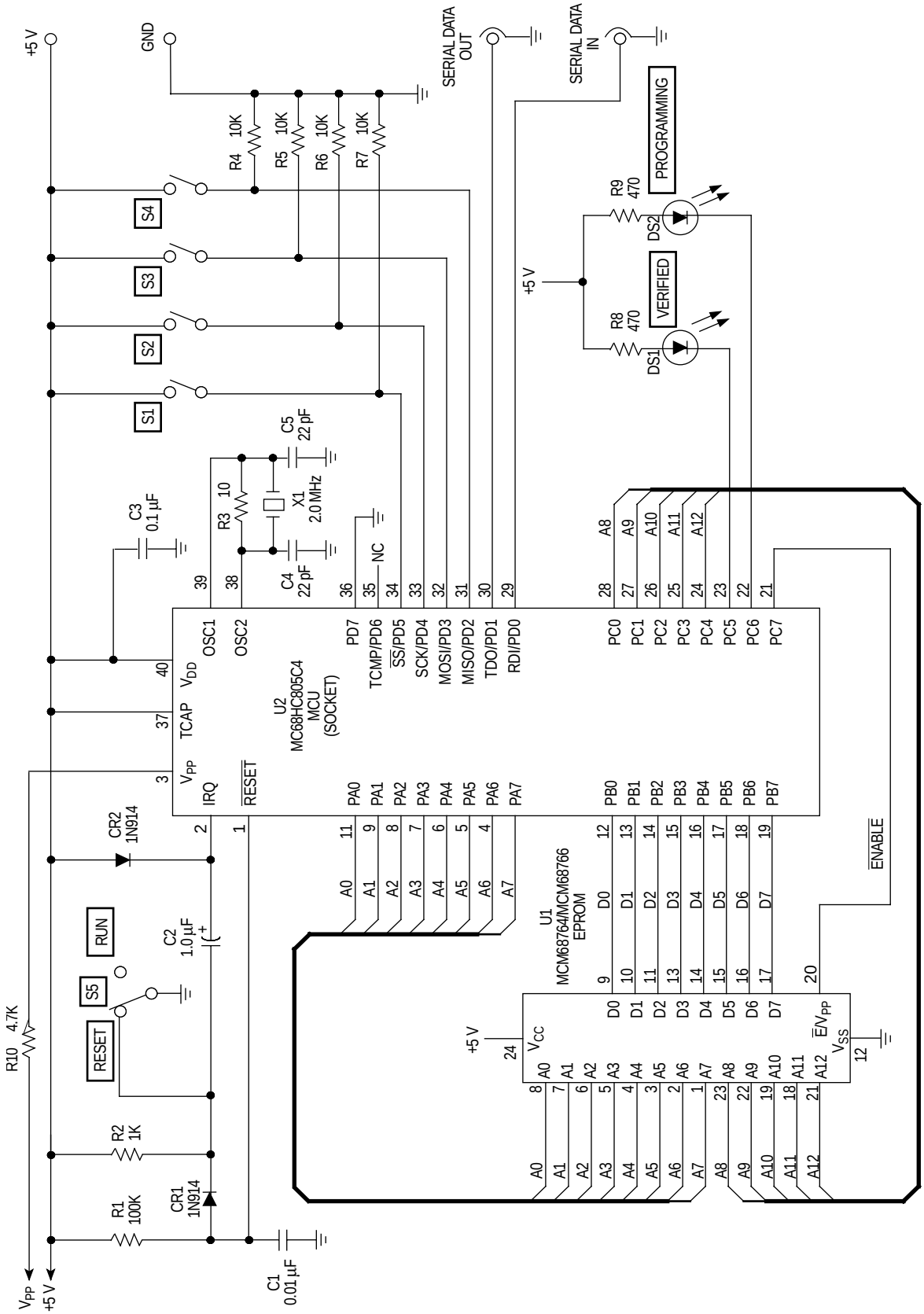


Figure 6. MC68HC805C4 MCU EEPROM Programming Board/Circuitry

Program and Verify EEPROM

In the program and verify EEPROM routine, the contents of an external 8K EPROM are copied into the EEPROM areas of the MC68HC805C4 device. There is a direct correspondence of addresses between the two devices. Non-EEPROM addresses are ignored so data contained in those areas are not accessed. Unprogrammed EPROM address locations should contain $FF to speed up the programming operation. During the programming routine the PROGRAMMING LED DS2 is illuminated. At the end of the programming routine, DS2 is turned off, and the verification routine is entered. If the contents of the EEPROM and external ROM exactly match, then the VERIFIED LED DS1 is illuminated. The verification routine stops if a discrepancy has been detected and the error address location will be placed on the external memory address bus.

Devices from the A65G mask set do not automatically verify at the end of the programming routine. When the programming LED DS2 turns off, reset the MC68HC805C4 and follow the procedure described in **Verify EEPROM Contents**.

Bulk Erase and Verify EEPROM

In the bulk erase and verify EEPROM routine, all EEPROM locations are returned to the unprogrammed ($FF) state. Upon completion of this erasing operation, every EEPROM location is verified for $FF. When every location is erased and verified, the VERIFIED LED DS1 is illuminated. If a location did not erase, the error address location will be placed on the external memory address bus. If required, this routine can be reexecuted until all EEPROM locations are erased and verified.

During the erase verification routine external memory is disabled, the data port is switched to output data, and $FF data value is written into the output register. All locations are compared to the erased byte state ($FF). The verification routine stops if a discrepancy has been detected and the error address location will be placed on the external memory address bus.

Load Program in RAM and Execute

In the load program in RAM and execute routine, user programs are loaded into MCU RAM via the serial communications interface (SCI) port, and then executed. Data is loaded sequentially, starting at RAM location $0050, until the last byte is loaded. Program control is then transferred to the RAM program starting at location $0051. The first byte loaded is the count of the total number of bytes in the program plus the count byte. The program starts at the second byte in RAM. During the firmware initialization stage the SCI is configured for the NRZ data format (idle line, start bit, eight data bits, and stop bit). The baud rate is 4800 with a 2 MHz crystal.

If immediate execution is not desired after loading the RAM program, it is possible to hold off execution. This is accomplished by the setting of the byte count to a value that is greater than the overall length of the loaded data. When the last byte is loaded, the

firmware will halt operations expecting additional data to arrive. At this point, switch S5 is placed in the RESET position which will reset the MCU but keep the RAM program intact. All other routines (modes) can now be entered from this state, including the one which will execute the program in RAM, once switch S5 is placed in the RUN position. At the end of the RAM load routine, ports A and C are configured as outputs.

Verify EEPROM Contents

The verify EEPROM contents routine is normally entered automatically after the EEPROM is programmed or erased. Direct entry of this mode will cause the EEPROM contents to be compared to external memory contents residing at the same address locations. Both DS1 and DS2 LEDs are turned off at this time until verification is completed. Upon completion of the verification routine (every location verified) the VERIFIED LED DS1 is illuminated. If DS1 does not illuminate, a discrepancy has been detected and the error address location will be placed on the external memory address bus.

Dump EEPROM Contents

In the dump EEPROM contents routine, entire EEPROM contents are dumped sequentially to the SCI output. The first location transmitted will be $0020 and the last one will be $1FFF. Unused locations will be bypassed so that no gaps will appear in the data stream. The external memory address lines will always indicate the current location being transmitted. The data is sent out in exactly the same NRZ format described in the load program in RAM routine.

Execute Program in RAM

Using this routine, the MCU will transfer control to a program that has been previously loaded into RAM. This program will be executed once the bootstrap mode has been entered, if mode switch S4 is activated. No firmware initializations will take place. The program must start at RAM location $0051 to be compatible with the load program in RAM routine.

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