MC68QH302/D
(Motorola Order Number)

11/97
REV 0

# MC68QH302

*Advance Information*

## MC68QH302 Quad HDLC Integrated Multiprotocol Processor Technical Summary

The MC68QH302, quad HDLC integrated multiprotocol processor, is based on the three-SCC MC68302 family of chips with the addition of the QH protocol and two extra serial DMA channels. The QH302 supports a total of four independent communications channels, handling two HDLC or transparent channels on SCC1; see Figure 1 for a block diagram.

In non-QH mode, the QH302 can be used in standard 302 applications as well.

To locate any published errata or updates for this document, refer to the website at http://www.mot.com/netcomm.

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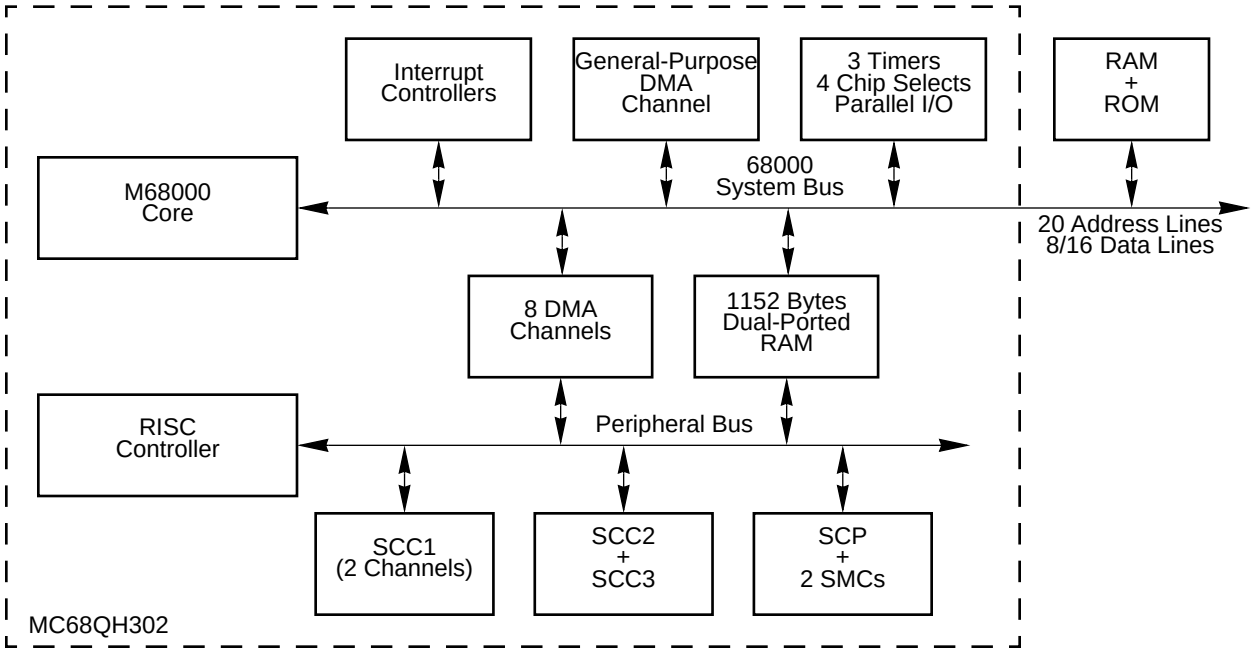
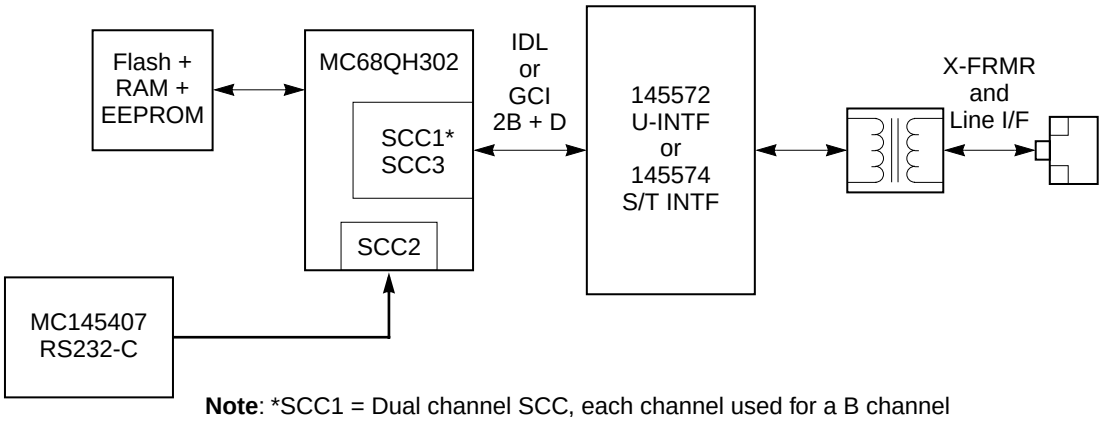



**Figure 1. MC68QH302 Block Diagram**

The MC68QH302 supports a full ISDN basic rate interface with one serial channel left over to communicate with the DTE as shown in Figure 2. The dual-channel SCC1 is used to support the two B channels.




**Note**: *SCC1 = Dual channel SCC, each channel used for a B channel

**Figure 2. MC68QH302 Supporting a Full ISDN Basic Rate Interface**

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## 1.1 FEATURES

The main features of the MC68QH302 are as follows (**new features indicated in bold**):

- MC68000/MC68008 microprocessor core (may be disabled to use the IMP as a peripheral)
- Serial interface block including:
  - Independent direct memory access (IDMA) controller
  - Interrupt controller with two modes of operation
  - Parallel I/O ports, some with interrupt capability
  - On-chip 1152 bytes of dual-ported RAM
  - Three timers, including a software watchdog timer
  - Four programmable chip-select lines with wait-state logic
  - Programmable address mapping of dual-ported RAM and IMP registers
  - On-chip clock generator with an output clock signal
  - System control
    - System control register
    - Bus arbitration logic with low-interrupt latency support
    - Hardware watchdog for monitoring bus activity
    - Low power (standby) modes
    - Disable CPU logic (M68000)
    - Freeze control for debugging selected on-chip peripherals
    - DRAM refresh controller
- CP including:
  - Main controller (RISC processor)
  - Three physical full-duplex serial communication controllers (SCCs) with the following protocols:
    - HDLC/SDLC
    - UART
    - Totally transparent
    - V.110
  - **SCC1 can support two logical HDLC or transparent channels running QH protocol**
  - **Eight serial DMA channels dedicated to the four serial channels**
  - Capability to send /receive up to eight buffers/frames without M68000 core intervention
  - Flexible physical interface accessible by SCCs for interchip digital link (IDL), general circuit interface (GCI, also called IOM2), pulse code modulation (PCM), and nonmultiplexed serial interface (NMSI) operation
  - Serial communication port (SCP) for synchronous communication
  - Serial management controllers (SMCs) for IDL and GCI channels
- Application development system available with M68302FADS.

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## 1.2 MC68QH302 Ordering Information

Table 1 identifies operating frequencies available for the MC68QH302.

**Table 1. MC68QH302 Package/Frequency Availability**

| Package Type | Operating Voltage | Frequency (MHz) | Temperature | Order Number |
|---|---|---|---|---|
| 144-pin thin quad flat pack (PV suffix) | 5 V | 16.67 | 0° C to 70° C | MC68QH302PV16 |
| | | 20 | | MC68QH302PV20 |
| | | 25 | | MC68QH302PV25 |

The documents listed in Table 2 contain detailed information on the MC68QH302. These documents can be obtained from the Literature Distribution Centers at the addresses listed on the back page. Visit the website at http://www.mot.com/netcomm/ for more information.

**Table 2. Documentation**

| Document Title | Order Number | Contents |
|---|---|---|
| MC68302 User's Manual | MC68302UM/AD | Detailed information for design |
| M68000 Family Programmer's Reference Manual | M68000PM/AD | M68000 family instruction set |
| The 68K Source | BR729/D | Independent vendor listing supporting software and development tools |
| The MC68QH302 Supplement to MC68302 User's Manual | MC68QH302SUPL/AD | Highlights implementation-specific features of the MC68QH302, and discusses how they differ from the MC68302. |

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