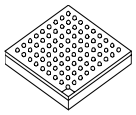
Advance Information

MC71000TB/D
Rev. 2, 8/2002

MC71000 Bluetooth Baseband Controller

MC71000



Package Information
Plastic Package
Case 1347
(MAPBGA–100)

Ordering Information

Device	Operating Temperature Range	Package
MC71000	TA = – 40° to 85° C	MAPBGA – 100

Contents

The MC71000 Bluetooth Baseband Controller is a part of the Bluetooth™ chipset from Motorola that provides a complete, low-power Bluetooth radio system. The design is based on Motorola's third-generation Bluetooth architecture that has set the industry standard for interoperability, complete functionality, and compliance with the Bluetooth specification.

The MC71000 Bluetooth Baseband Controller from Motorola implements the baseband and host controller interface (HCI) of the Bluetooth protocol. It operates with a core voltage of 1.8 V and I/Os between 1.8 V and 3.3 V. The MC71000 is the ideal solution for low-power, short-range Bluetooth applications and includes superior performance features like the dedicated Bluetooth audio processor module and on-chip memory. Debug and production test are fully supported through the joint test action group (JTAG) interface. The MC71000 provides a zero-glue logic interface for the companion MC13180 Bluetooth RF Integrated Circuit (IC), allowing the implementation of a two-chip Bluetooth Class 2 radio. The addition of the MRFIC2408 External Power Amplifier provides a Class 1 solution.

Preliminary

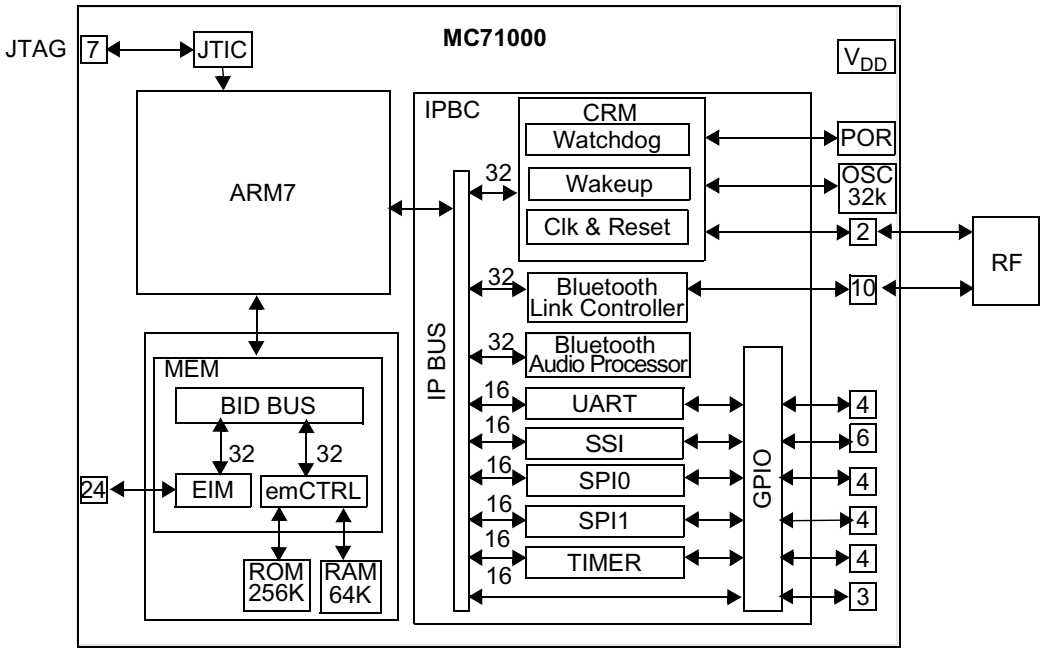


Figure 1. MC71000 Block Diagram

1 Applications

- Mobile phone connectivity
- Personal digital assistant (PDA) connectivity
- Internet appliance connectivity
- Mobile phone headsets

2 Typical Bluetooth Solution Using the MC71000

The following figure shows a sample two-chip Bluetooth solution.

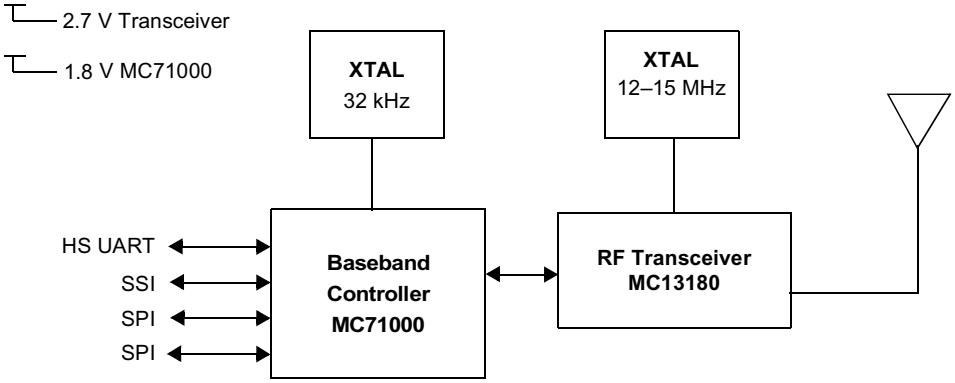


Figure 2. Sample Two-Chip Bluetooth Solution

3 Overview

This section describes the overall system architecture of the MC71000 Bluetooth Baseband Controller. It highlights the main features and requirements, as well as provides an overview of the operational blocks of MC71000 Bluetooth Baseband Controller at a system level. The subsequent sections describe the detailed design requirements by major blocks and functions.

The MC71000 Bluetooth Baseband Controller implements the baseband and host controller interface (HCI) of the Bluetooth protocol and is specifically designed to meet the immediate market needs for low-power Bluetooth applications. To improve the total system throughput and reduce component cost and board size, the MC71000 Bluetooth Baseband Controller integrates a Motorola-unique ARM7TDMI platform with intelligent peripheral modules focused on communications and system integration. The MC71000 Bluetooth Baseband Controller includes superior performance features for audio and power conservation, as well as debug and production test support.

The MC71000 Bluetooth Baseband Controller provides a zero glue logic interface to the MC13180 Bluetooth RF Integrated CircuitC, a 2.4GHz Bluetooth radio for implementing a Bluetooth Class 2 solution. The addition of the MRFIC2408 External Power Amplifier IC provides a Class 1 solution. A power management chip, MC13181, is also available for headset and mobile phone accessory applications. The MC13181 integrates power management functions common to these applications. The architecture of the MC7100 is shown in Figure 1 on page 2.

3.1 MC71000 Bluetooth Features

- Bluetooth Specification 1.1 Compliant
  - Point-to-multipoint (piconet) with 7 slaves
  - All connection types
  - All packet types
  - All power saving modes
  - Master/slave switch
  - Encryption
  - HCI UART transport layer
- Superior Audio Performance
  - Sample rate synchronization between CODEC and Bluetooth clock domains to avoid “clicking” effects
  - 3 simultaneous SCO channels supported
  - All Bluetooth encoding/decoding schemes supported (CVSD, A-Law, μ-Law)
  - Very low audio delay to avoid the need for echo cancellation
- Support for 8, 16, 32, and 64 kHz Sample Rate CODECs

3.2 MC71000 Hardware Features

The MC71000 is specifically designed to work with the Bluetooth protocol and supports a wide range of Bluetooth user profiles and applications. The MC71000 offers the following features:

- Bluetooth Link Controller
- Bluetooth Audio Processor
- ARM7 Processor Complex
- Peripherals

- High-speed UART (up to 2 Mbps)
- High-speed SSI (up to 2 Mbps)
- Dual high-speed SPI (up to 2 Mbps)

- Embedded Memory
  - SRAM (64K)
  - ROM (256K)
- External Interface Module (EIM)
- JTAG Test Interface Controller (JTIC)
- 32 kHz Oscillator (OSC32k) for Low Power Operation
- Operating Voltage: 1.65 V to 1.95 V
- Package: 100-pin MAPBGA, 7 mm x 7 mm, 0.65 mm ball pitch

4 Architectural Overview

The following sections describe the functionality and performance of the MC71000 Bluetooth Baseband Controller.

4.1 ARM7 Platform (A7P)

4.1.1 ARM7TDMI

The MC71000 Bluetooth Baseband Controller architecture is based around the 32-bit ARM7TDMI microprocessor. It is an industry-standard processor recognized for its efficient MIPS/WATT benchmark, along with excellent code efficiency when working in the 16-bit THUMB mode. The architecture is based on RISC principles and supports two instruction sets:

- The 32-bit ARM instruction set
- The 16-bit THUMB instruction set

4.2 Memory Sub-System

Program execution in the MC71000 Bluetooth Baseband Controller is predominantly ROM-based, with internal SRAM being used for code patching. An image can be uploaded from a host system, or a low-cost serial E2PROM (four-wire connection).

4.2.1 External Interface Module (EIM)

The external interface module (EIM) handles the interface to external devices, as well as generation of chip selects for external peripherals and memory. It contains a zero-glue interface to external memories (SRAM, E2PROM, and FLASH chips).

4.3 Peripherals Sub-System

4.3.1 Clock and Reset Module (CRM)

The clock and reset module (CRM) is dedicated to handling all clock, reset, and power management features in the MC71000 Bluetooth Baseband Controller. It assures that the different clock and reset signals are stable before they are fed to the internal logic in the MC71000 Bluetooth Baseband Controller.

The CRM is designed to make full use of the facilities supplied by the Bluetooth standard to conserve power, while still maintaining a Bluetooth link. For this purpose, the CRM is connected to an on-chip low-power oscillator, which generates a frequency using an external low cost 32.768 kHz crystal. The CRM module also includes a watchdog to safeguard against any potential software failures.

4.3.2 Bluetooth Link Controller (BTLC)

The Bluetooth link controller module (BTLC) handles all link controller specific functions. Raw data can be read from/written to the module, and the BTLC takes care of transmission related timing, as well as data signal processing functions like encryption and cyclic redundancy check (CRC)/header error correction (HEC) generation. Embedded in the BTLC are also the dedicated Bluetooth timers, which maintain an accurate estimate of time in both the native and the remote module. A small and dedicated Bluetooth serial peripheral interface controller handles all serial communication with the MC13180 Bluetooth RF Integrated Circuit.

4.3.3 Bluetooth Audio Signal Processor (BTASP)

Special attention has been put on audio quality for the end user. For this purpose, a dedicated Bluetooth audio signal processing module (BTASP) has been designed to give users excellent and superior audio performance. With a minimum of processor intervention, this module handles all filtering, interpolation, as well as encoding/decoding (aLaw, uLaw, and CVSD).

4.3.4 High-Speed UART (up to 2 Mb/sec @ 24 MHz)

The Universal Asynchronous Receiver/Transmitter (UART) module provides one of the main interfaces to the MC71000 Bluetooth Baseband Controller. The generated baud rate is based upon a configurable divisor and input clock. It can be configured to send one or two stop bits as well as odd, even, or no parity. The UART transmit and receive buffer sizes are 32 bytes each.

4.3.5 Dual High-speed CSPI (up to 2 Mb/sec @ 24 MHz)

The MC71000 Bluetooth Baseband Controller contains two configurable serial peripheral interface (CSPI) modules, CSPI0 and CSPI1. CSPI0 can connect to a variety of SEEPROM and serial flash devices.

Both CSPI modules are master/slave configurable, equipped with 16 byte data out buffers (transmit and receive FIFOs), and allow the MC71000 Bluetooth Baseband Controller to interface with external CSPI master or slave devices. Incorporating the $\overline{\text{SPIRDY}}$ and $\overline{\text{SS}}$ control signals, it enables fast data communication with a fewer number of software interrupts.

4.3.6 High-Speed SSI (up to 2 Mb/sec @ 24 MHz)

The synchronous serial interface module (SSI) is a full-duplex serial port allowing digital signal processors (DSPs) to communicate with a variety of serial devices, including industry-standard CODECs, other DSPs, microprocessors, and peripherals. The SSI is typically used to transfer samples in a periodic manner and consists of a variety of registers that handle port, status, control, transmit and receive, serial clock generation, and frame synchronization.

4.3.7 Timer (TMR)

The dual timer module (TMR) is a general purpose module, used for timing control and application-specific tasks. The TMR can also be configured to perform pulse width modulation (PWM) or put into a quadrature-count mode if needed. The TMR contains two identical 16-bit counter/timer groups, each supports counting, prescaling, comparing, loading, capturing, and holding options.

4.3.8 General Purpose (GPIO)

The MC71000 Bluetooth Baseband Controller supports a maximum of 27 GPIO lines grouped together in two ports. Port B contains 14 lines and Port C contains the other 13. These ports can be configured as GPIO pins or dedicated peripheral interface pins.

4.4 Test

4.4.1 JTAG Test Interface Controller (JTIC)

The JTIC interface offers full JTAG and boundary scan capabilities for debug and production test purposes, as well as access to the JTAG interface on the ARM.

5 Pin Assignment Listing

The following table (Table 2-1) shows the pin assignment listing for the MC71000 IC. The pins are organized into functional groups.

- The Pin Name and Description columns show the actual name and a brief description of each pin.
- The Std Pad Drive column lists the typical (minimum) drive current required for the pin.
- The Power Group column lists the Supply Power Group assignment.
- The Reset State column lists the pin input/output direction at chip RESET.
- The Alternate Functions column lists each of the GPIO port alternate input and output selections available. Some selections are test- or development-mode specific.

Table 1. MC71000 Bluetooth Baseband Controller Pin Description

Pin Name	Description	Pin Type	Reset Pull U/D	Std Pad Drive	Power Group	Reset State	Alternate Functions
EIM							
A0	EIM - Address line	O		5 mA	EIMVDD	O/L	
A1	EIM - Address line	O		5 mA	EIMVDD	O/L	
A2	EIM - Address line	O		5 mA	EIMVDD	O/L	
A3	EIM - Address line	O		5 mA	EIMVDD	O/L	
A4	EIM - Address line	O		5 mA	EIMVDD	O/L	
A5	EIM - Address line	O		5 mA	EIMVDD	O/L	
A6	EIM - Address line	O		5 mA	EIMVDD	O/L	
A7	EIM - Address line	O		5 mA	EIMVDD	O/L	
A8	EIM - Address line	O		5 mA	EIMVDD	O/L	
A9	EIM - Address line	O		5 mA	EIMVDD	O/L	
A10	EIM - Address line	O		5 mA	EIMVDD	O/L	

Table 1. MC71000 Bluetooth Baseband Controller Pin Description (Continued)

Pin Name	Description	Pin Type	Reset Pull U/D	Std Pad Drive	Power Group	Reset State	Alternate Functions
A11	EIM - Address line	O		5 mA	EIMVDD	O/L	
D0	EIM - Data line	I/O	PU	5 mA	EIMVDD	Z/H	
D1	EIM - Data line	I/O	PU	5 mA	EIMVDD	Z/H	
D2	EIM - Data line	I/O	PU	5 mA	EIMVDD	Z/H	
D3	EIM - Data line	I/O	PU	5 mA	EIMVDD	Z/H	
D4	EIM - Data line	I/O	PU	5 mA	EIMVDD	Z/H	
D5	EIM - Data line	I/O	PU	5 mA	EIMVDD	Z/H	
D6	EIM - Data line	I/O	PU	5 mA	EIMVDD	Z/H	
D7	EIM - Data line	I/O	PU	5 mA	EIMVDD	Z/H	
CS0	EIM - Chip Select 0	O		5 mA	EIMVDD	O/H	
CS1	EIM - Chip Select 1	O		5 mA	EIMVDD	O/H	
OE	EIM - Output enable	O		5 mA	EIMVDD	O/H	
WE	EIM - Write enable	O		5 mA	EIMVDD	O/H	
MISC							
EXTAL	CLK - 32 kHz External crystal clock input	I		—	MISCVDD	I	
XTAL	CLK - 32 kHz Crystal output	O		?	MISCVDD	O	
TRST	JTAG - Test reset	ST[1]	PD	—-	MISCVDD	I	
TDI	JTAG - Test data input	I	PU	—-	MISCVDD	I	
TDO	JTAG - Test data output	Tri-O		3 mA	MISCVDD	O/L	
TMS	JTAG - Test mode select input	I	PU	—	MISCVDD	I	
TCK	JTAG - Test clock input	ST[1]	PD	—	MISCVDD	I	
RTCK	JTAG - Test clock output	O		—	MISCVDD	O	
TTS	JTAG - Test tap select	I		—	MISCVDD	I	
MODE0	Boot mode select pin 0	I	PU	—	MISCVDD	I	
MODE1	Boot mode select pin 1	I	PU	—	MISCVDD	I	
RESETIN	Reset input - POR	I	ST[1]	—	MISCVDD	I	
PORT A (BLUETOOTH)							
REFCTRL	RF Reference clock control	O		3 mA	AVDD	O/L	
REFCLK	RF Reference clock input	I		—	AVDD	I	
BT1	BT - Frame synch/ CSPI_di	I		—	AVDD	I	
BT2	BT - RXDATA	I		—	AVDD	I	
BT3	BT - TXDATA	Tri-O	PU	3 mA	AVDD	Z/H	
BT4	BT - RXTXEN/ HOP_STROBE	O		3 mA	AVDD	O/L	
BT5	BT - SPI_CLK	O		3 mA	AVDD	O/L	

Table 1. MC71000 Bluetooth Baseband Controller Pin Description (Continued)

Pin Name	Description	Pin Type	Reset Pull U/D	Std Pad Drive	Power Group	Reset State	Alternate Functions
BT6	BT - SPI_EN	O		3 mA	AVDD	O/H	
BT7	BT - SPI_DO/SPI_DI	I/O		3 mA	AVDD	O/L	
BT8	BT - PWM0/TX_EN/ GPO0	Tri-O		3 mA	AVDD	O/L	
BT9	BT - PWM1/PA_EN/ GPO1	O		3 mA	AVDD	O/L	
PORT B							
SSI_STCK	SSI - Serial Transmit Clock	I/O	PU	3 mA	BVDD	Z/H	GPIO_B0; BT_TP0
SSI_STFS	SSI - Serial Transmit Frame Sync	I/O	PU	3 mA	BVDD	Z/H	GPIO_B1; BT_TP1
SSI_STD	SSI - Serial Transmit Data	I/O	PU	3 mA	BVDD	Z/H	GPIO_B2; BT_TP2
SSI_SRCK	SSI - Serial Receive Clock	I/O	PU	3 mA	BVDD	Z/H	GPIO_B3; BT_TP3
SSI_SRFS	SSI - Serial Receive Frame Sync	I/O	PU	3 mA	BVDD	Z/H	GPIO_B4; BT_TP4
SSI_SRD	SSI - Serial Receive Data	I/O	PU	3 mA	BVDD	Z/H	GPIO_B5; BT_TP5
CSPI_0_SS	CSPI #0 - Slave Select	O	PU	3 mA	BVDD	Z/H	GPIO_B6; BT_TP6
CSPI_0_SCK	CSPI #0 - Serial Clock	O	PU	3 mA	BVDD	Z/H	GPIO_B7; BT_TP7
CSPI_0_MISO	CSPI #0 - Master In / Slave out	I/O	PU	3 mA	BVDD	O/L	GPIO_B8; BT_TP8;
CSPI_0_MOSI	CSPI #0 - Master Out / Slave in	I/O	PU	3 mA	BVDD	Z/H	GPIO_B9; BT_TP9
GPIO_B10	General Purpose I/O	I/O	PU	3 mA	BVDD	Z/H	GPIO_B10 UART-TXD
GPIO_B11	General Purpose I/O	I/O	PU	3 mA	BVDD	Z/H	GPIO_B11 UART-RTS
GPIO_B12	General Purpose I/O	I/O	PU	3 mA	BVDD	Z/H	GPIO_B12 UART-RXD
CLK0	Programmable Clock Output	I/O	PU	3 mA	BVDD	O/L	GPIO_B13 UART-CTS
PORT C							
TXD	UART - TXD	Tri-O	PU	3 mA	CVDD	Z/H	GPIO_C0; CSPI0_REQ
CTS_	UART - CTS	Tri-O	PU	3 mA	CVDD	Z/H	GPIO_C1; CSPI1_REQ
RXD	UART - RXD	I/O	PU	3 mA	CVDD	Z/H	GPIO_C2; TIM_0_I
RTS_	UART - RTS	I/O	PU	3 mA	CVDD	Z/H	GPIO_C3; TIM_1_I
CSPI_1_SS	CSPI #1 - Slave select	O	PU	3 mA	CVDD	O/H	GPIO_C4; SYSCLK

Table 1. MC71000 Bluetooth Baseband Controller Pin Description (Continued)

Pin Name	Description	Pin Type	Reset Pull U/D	Std Pad Drive	Power Group	Reset State	Alternate Functions
CSPI_1_SCK	CSPI #1 - Serial clock	O	PU	3 mA	CVDD	O/H	GPIO_C5; SH_STROBE
CSPI_1_MISO	CSPI #1 - Master In / Slave out	I/O	PU	3 mA	CVDD	O/L	GPIO_C6; ABORT
CSPI_1_MOSI	CSPI #1 - Master Out / Slave in	I/O	PU	3 mA	CVDD	Z/H	GPIO_C7; REFCLK
CLK1	Programmable clock output	I/O	PU	3 mA	CVDD	O/L	GPIO_C8; TIM_0_O
GPIO_C9	General Purpose I/O	I/O	PU	3 mA	CVDD	Z/H	GPIO_C9; XACK
OSC32K	Buffered Low Power 32 kHz Clock	I/O	PU	3 mA	CVDD	O/L	GPIO_C10; TIM_1_O
SYSCLK	Buffered System Clock	I/O	PU	3 mA	CVDD	O/L	GPIO_C11
BTCLK	Buffered Bluetooth Clock	I/O	PU	3 mA	CVDD	O/L	GPIO_C12
EIM POWER/GROUND							
GND_EIM2	GND	GND			EIMVDD		
GND_EIM3	GND	GND			EIMVDD		
GND_EIM4	GND	GND			EIMVDD		
GND_EIM6	GND	GND			EIMVDD		
GND_EIM7	GND	GND			EIMVDD		
PWR_EIM2	PWR	PWR			EIMVDD		
PWR_EIM3	PWR	PWR			EIMVDD		
PWR_EIM4	PWR	PWR			EIMVDD		
PWR_EIM6	PWR	PWR			EIMVDD		
PWR_EIM7	PWR	PWR			EIMVDD		
MISC POWER/GROUND							
GND_MISC	GND	GND			MISCVDD		
PWR_MISC	PWR	PWR			MISCVDD		
PORT A POWER/GROUND							
GND_PA	GND	GND			AVDD		
PWR_PA	PWR	PWR			AVDD		
PORT B POWER/GROUND							
GND_PB	GND	GND			BVDD		
PWR_PB	PWR	PWR			BVDD		
PORT C POWER/GROUND							
GND_PC	GND	GND			CVDD		
PWR_PC	PWR	PWR			CVDD		
CORE POWER/GROUND							
GND_CORE1	GND	GND			COREVDD		
GND_CORE2	GND	GND			COREVDD		
GND_CORE3	GND	GND			COREVDD		

Table 1. MC71000 Bluetooth Baseband Controller Pin Description (Continued)

Pin Name	Description	Pin Type	Reset Pull U/D	Std Pad Drive	Power Group	Reset State	Alternate Functions
GND_CORE4	GND	GND			COREVDD		
PWR_CORE1	PWR	PWR			COREVDD		
PWR_CORE2	PWR	PWR			COREVDD		
PWR_CORE3	PWR	PWR			COREVDD		
PWR_CORE4	PWR	PWR			COREVDD		

1.ST - Schmitt Trigger input

5.1 Pin Descriptions

The following table provides detailed pin descriptions for the external interface module (EIM); clock, reset, and JTAG; Bluetooth; SSI, SPI0, and UART; and UART, SPI1, and TIM including the GPIO shared package pins.

In the following table, the general purpose input/output (GPIO) is designed to share package pins with other peripheral modules on the chip. If the peripheral which normally controls a given pin is not required, then the pin may be programmed to be a general purpose input/output (GPIO) or alternate function 2 with programmable pullup. The GPIO module design has two available ports (Port B and Port C). The individual control for each pin can be in normal functional mode, alternate function mode 2, or GPIO mode. The individual direction control for each pin is in GPIO mode. The individual pullup enable control for each pin is in normal function mode, alternate function mode 2, or GPIO mode.

- **Normal mode.** The peripheral module controls the output enable and any output data to the pad and any input data from the pad is passed to the peripheral.
- **Alternate function 1 mode (GPIO).** The GPIO module controls the output enable to the pad and supplies any data to be output.
- **Alternate function 2 mode.** The peripheral module controls the output enable and any output data to the pad and any input data from the pad is passed to the peripheral.

Table 2. Pin Descriptions

EIM Signals	
D0-D7 (Data Bus)	Active high, bidirectional inputs/outputs. D0 is the least significant bit and D7 is the most significant. These pins provide the bidirectional data bus for external memory access. D0–D7 are held in the previous logic state when there is no external bus activity. This is done with weak “keepers” inside the I/O buffers. They are also kept in their previous state during hardware reset.
A0-A11 (Address Bus)	Active high outputs, specifies the address for external memory accesses. ADDR0 is the least significant bit and ADDR11 is the most significant. To minimize power dissipation, ADDR0–ADDR11 do not change state when external memory is not being accessed.
$\overline{\text{CS1}}$ (Chip Select 1)	This output signal is active low and is asserted based on the decode of the internal address bus.
$\overline{\text{CS0}}$ (Chip Select 0)	This active-low output signal is asserted based on the decode of the internal address bus.
$\overline{\text{OE}}$ (Output Enable)	This active low output signal is used to indicate that the bus access is a read and enables slave devices to drive the data bus with read data. OE is negated during hardware reset.
$\overline{\text{WE}}$ (Write Enable)	This active low output signal is used to indicate that the bus access is a write and enables slave devices to drive the address bus with the write data.

Table 2. Pin Descriptions (Continued)

Clock, Reset, and JTAG Signals	
EXTAL CLK	32 kHz external crystal clock input
XTAL CLK	32 kHz Crystal output
TDI (Test Data Input)	The test data input pin provides a serial input data stream to all TAP controllers. TDI is sampled on the rising edge of TCK.
TDO (Test Data Output)	The test data output pin is tri-statable, providing serial output data from the Master TAP or ARM Core TAP controller. It is actively driven in the shift-IR and shift-DR controller states of the TAP controller state machine. TDO changes on the falling edge of TCK.
$\overline{\text{TRST}}$ (Test Reset)	This active low Schmitt trigger input pin provides an asynchronously reset signal to all TAP controllers to initialize the test controller.
TMS (Test Mode Select)	The test mode select input pin is used to sequence all TAP controllers. The TAP sequenced is determined by the tap control module and the TTS device port. TMS is sampled on the rising edge of TCK.
TCK (Test Clock)	The test clock input pin is used to synchronize the JTAG test logic. It provides the clock to synchronize the test logic and shift serial data to and from all TAP controllers.
RTCK (Return Test Clock)	The return test clock input pin returns the synchronization test clock to ARM development tools to be entered from the serial debug input line.
TTS (Test TAP select)	The test tap select input pin directly controls the multiplexing logic to select between the chip TAP and the core TAP. A logic 1 applied to the tap select input will select the chip TAP.
MODE[1:0]	Test/boot mode select pins. In order to support a flexible development system, the system must be capable to boot from different memories during system reset and power-up. The four different memory maps can be selected by these two pins. All the different boot modes start reading data at address 0x0000_0000, since this is where the ARM7 reset vector is located.
$\overline{\text{RESETIN}}$ (Reset In)	The reset in pin is an active low Schmitt trigger input that provides reset to the internal circuitry. The RESET input will be qualified as valid if it will be asserted for at least 3 CLK cycles.
Bluetooth Signals	
REFCTRL (Reference Control)	The reference control pin is a dedicated output from the CRM which enables/disables the reference clock.
REFCLK (Reference Clock)	The reference clock pin is a dedicated input into the CRM from the RF interface. (12-32 MHz)
BT1	Input from the RF front end. Frame sync for the MC13180 RF IC; CSPI_din for Silicon Wave
BT2	RXDATA: Input from the MC13180 RF IC and Silicon Wave RF Front End
BT3	TXDATA: Output to the MC13180 RF IC and Silicon Wave RF Front End
BT4	Dedicated RF control output to the RF Front Ends. RXTX_EN for the MC13180 RF IC Radio or HOP_STROBE for the Silicon Wave Radio.
BT5	CSPI_CLK: One of the three CSPI signals which program the MC13180 RF IC Radio or one of the four CSPI signals which program the Silicon Wave Radio.
BT6	CSPI_EN: One of the three CSPI signals which program the MC13180 RF IC Radio or one of the four CSPI signals which program the Silicon Wave Radio.
BT7	CSPI_DOUT/CSPI_DIN: One of the three CSPI signals which program the MC13180 RF IC Radio (CSPI_DIN or CSPI_DOUT) or one of the four CSPI signals which program the Silicon Wave Radio (CSPI_DOUT)

Table 2. Pin Descriptions (Continued)

BT8	The BT8 pin is a RF control output which can be programmed for different purposes, such as TX_EN, PWM0 (Pulse Width modulator output), or as GPO0.	
BT9	The BT9 pin is an RF control output which can be programmed for different purposes, such as PA_EN (power amplifier enable), PWM1 (pulse width modulator output) or as GPO1.	
SSI, SPI0, and UART Signals		
SSI_STCK/GPIO_B0/BT_TP0		
Normal Mode	SSI_STCK	The serial transmit clock signal is used by the transmitter and can be either continuous or gated.
Alternate Function 1 (GPIO)	GPIO_B0	GPIO 0 on Port B
Alternate Function 2	BT_TP0	Bluetooth test port
SSI_STFS/GPIO_B1/BT_TP1		
Normal Mode	SSI_STFS	The serial transmit frame sync signal is used by the transmitter to synchronize the transfer of data. The frame sync signal can be one bit or one word in length.
Alternate Function 1 (GPIO)	GPIO_B1	GPIO 1 on Port B
Alternate Function 2	BT_TP1	Bluetooth test port signal
SSI_STD/GPIO_B2/BT_TP2		
Normal Mode	SSI_STD	The serial transmit data signal is used to transmit serial data.
Alternate Function 1 (GPIO)	GPIO_B2	GPIO 2 on Port B
Alternate Function 2	BT_TP2	Bluetooth test port signal
SSI_SRCK/GPIO_B3/BT_TP3		
Normal Mode	SSI_SRCK	The serial receive clock signal is used by the receiver and is always continuous, however, it is not used in synchronous mode.
Alternate Function 1 (GPIO)	GPIO_B3	GPIO 3 on Port B
Alternate Function 2	BT_TP3	Bluetooth test port signal
SSI_SRFS/GPIO_B4/BT_TP4		
Normal Mode	SSI_SRFS	The serial receive frame sync signal is used by the receiver to synchronize the transfer of data. The frame sync signal can be one bit or one word in length.
Alternate Function 1 (GPIO)	GPIO_B4	GPIO 4 on Port B
Alternate Function 2	BT_TP4	Bluetooth test port signal
SSI_SRD/GPIO_B5/BT_TP5		
Normal Mode	SSI_SRD	The serial receive data signal is used to receive serial data.
Alternate Function 1 (GPIO)	GPIO_B5	GPIO 5 on Port B
Alternate Function 2	BT_TP5	Bluetooth test port signal
CSPI_0_SS/GPIO_B6/BT_TP6		

Table 2. Pin Descriptions (Continued)

Normal Mode	CSPI_0_SS	The CSPI0 slave select bidirectional signal is an output in master mode and an input in slave mode.
Alternate Function 1 (GPIO)	GPIO_B6	GPIO 6 on Port B
Alternate Function 2	BT_TP6	Bluetooth test port signal
CSPI_0_SCK/GPIO_B7/BT_TP7		
Normal Mode	CSPI0 Clock	This bidirectional signal is the CSPI0 clock output in master mode. In slave mode, CSPI_0_SCK is an input clock signal to the CSPI.
Alternate Function 1 (GPIO)	GPIO_B7	GPIO 7 on Port B
Alternate Function 2	BT_TP7	Bluetooth test port signal
CSPI_0_MISO/GPIO_B8/BT_TP8		
Normal Mode	CSPI0	Master In Slave Out: In master mode, this bidirectional signal is the RXD input signal. In slave mode, MISO is the TXD output signal.
Alternate Function 1 (GPIO)	GPIO_B8	GPIO 8 on Port B
Alternate Function 2	BT_TP8	Bluetooth test port signal
CSPI_0_MOSI/GPIO_B9/BT_TP9		
Normal Mode	CSPI0	Master Out Slave In: In master mode, this bidirectional signal is the TXD output signal. In slave mode, MOSI is the RXD input signal.
Alternate Function 1 (GPIO)	GPIO_B9	GPIO 9 on Port B
Alternate Function 2	BT_TP9	Bluetooth test port signal; Bluetooth 4 MHz clock
GPIO_B10/UART_TxD		
Alternate Function 1 (GPIO)	GPIO_B10	GPIO 10 on Port B
Alternate Function 2	UART_TxD	Transmit data serial (output signal)
GPIO_B11/UART_RTS		
Alternate Function 1 (GPIO)	GPIO_B11	GPIO 11 on Port B
Alternate Function 2	UART_RTS	UART ready to send (RTS) This input signal, when asserted, indicates that the remote device is ready to accept new data and that the MC71000 Bluetooth Baseband Controller can transmit when it has data to send.
GPIO_B12/UART_RxD		
Alternate Function 1 (GPIO)	GPIO_B12	GPIO 12 on Port B
Alternate Function 2	UART_RxD	Receive data serial (input signal)
CLK0/GPIO_B13/UART_CTS		
Normal Mode	CLK0	Output to external devices generated by the fractional clock divider in the CRM. CLK0 is a programmable clock and derivative of REFCLK. Frequencies are programmable in the range of REFCLK/127 to REFCLK. CLK0 can be used to feed an external USB, a CODEC, or whatever the applications need. The fractional divider has 16-bit resolution; writing 0x000 to the divisor disables the timer.

Table 2. Pin Descriptions (Continued)

Alternate Function 1 (GPIO)	GPIO_B13	GPIO 13 on Port B
Alternate Function 2	UART_CTS	UART clear to send (CTS) This output signal, when asserted, indicates that the MC71000 Bluetooth Baseband Controller is ready to accept new data and the remote device can transmit when it has data to send.
UART, SPI1, and TIM Signals		
TXD/GPIO_C0/CSPI0_REQ		
Normal Mode	TXD	UART transmit data serial (output signal)
Alternate Function 1 (GPIO)	GPIO_C0	GPIO 0 on Port C
Alternate Function 2	CSPI0_REQ	External data transfer rate control for CSPI0
$\overline{\text{CTS}}$/GPIO_C1/CSPI1_REQ		
Normal Mode	CTS	UART clear to send (CTS) output signal, when asserted, indicates that the MC71000 is ready to accept new data and the remote device can transmit when it has data to send.
Alternate Function 1 (GPIO)	GPIO_C1	GPIO 1 on Port C
Alternate Function 2	CSPI1_REQ	External data transfer rate control for CSPI1
RXD/GPIO_C2/TIM_0_I		
Normal Mode	RXD	UART receive data serial (input signal)
Alternate Function 1 (GPIO)	GPIO_C2	GPIO 2 on Port C
Alternate Function 2	TIM_0_I	Input signal to timer 0
$\overline{\text{RTS}}$/GPIO_C3/TIM_1_I		
Normal Mode	RTS	UART ready to send (RTS) input signal, when asserted, indicates that the remote device is ready to accept new data and that the MC71000 can transmit when it has data to send.
Alternate Function 1 (GPIO)	GPIO_C3	GPIO 3 on Port C
Alternate Function 2	TIM_1_I	Input signal to timer 1
CSPI_1_SS/GPIO_C4/SYSCLK		
Normal Mode	CSPI1	Slave Select: This bidirectional signal is an output in master mode and an input in slave mode.
Alternate Function 1 (GPIO)	GPIO_C4	GPIO 4 on Port C
Alternate Function 2	SYSCLK	System clock used by the entire ARM7 platform and all peripherals attached to the IP and AHB bus. Some of the peripherals (for example, UART) will also use this clock signal to generate their own module clock.
CSPI_1_SCK/GPIO_C5/SH_STROBE		
Normal Mode	CSPI Clock	This bidirectional signal is the CSPI clock output in master mode. In slave mode, CSPI1_SCK is an input clock signal to the CSPI.
Alternate Function 1 (GPIO)	GPIO_C5	GPIO 5 on Port C

Table 2. Pin Descriptions (Continued)

Alternate Function 2	SH_STROBE	Indicates data is valid on the external bus when show cycle is used.
CSPI_1_MISO/GPIO_C6/ABORT		
Normal Mode	CSPI1	Master In Slave Out (MISO): In master mode, this bidirectional signal is the RXD input signal. In slave mode, MISO is the TXD output signal.
Alternate Function 1 (GPIO)	GPIO_C6	GPIO 6 on Port C
Alternate Function 2	ABORT	Indicates the current memory access can not be completed.
CSPI_1_MOSI/GPIO_C7/REFCLK		
Normal Mode	CSPI1	Master Out Slave In (MOSI): In master mode, this bidirectional signal is the TXD output signal. In slave mode, MOSI is the RXD input signal.
Alternate Function 1 (GPIO)	GPIO_C7	GPIO 7 on Port C
Alternate Function 2	REFCLK	RF reference clock input (12-32 MHz)
CLK1/GPIO_C8/TIM_0_O		
Normal Mode	CLK1	Output to external devices generated by the integer divider. CLK1 is a programmable clock and derivative of REFCLK. Frequencies are programmable in the range of REFCLK/64 to REFCLK. CLK1 can be used to feed an external USB, a CODEC, or whatever device the applications need. The integer divider should divide REFCLK with (1, 2, 4, 8, 16, 32, or 64). The value 0 disables the timer.
Alternate Function 1 (GPIO)	GPIO_C8	GPIO 8 on Port C
Alternate Function 2	TIM_0_O	Output signal from timer 0
GPIO_C9/XACK		
Alternate Function 1 (GPIO)	GPIO_C9	GPIO 9 on Port C
Alternate Function 2	XACK	External acknowledge signal
OSC32K/GPIO_C10/TIM_1_O		
Normal Mode	OSC32K	Buffered output from 32 kHz on chip oscillator
Alternate Function 1 (GPIO)	GPIO	GPIO 10 on Port C
Alternate Function 2	TIM_1_O	Output signal from timer 1
SYSCLK/GPIO_C11/A20		
Normal Mode	SYSCLK	System clock used by the processor as well as most peripherals attached to the IP and AHB bus. Some of the peripherals (for example, BTLC) will derive their internal clock based on the SYSCLK.
Alternate Function 1 (GPIO)	GPIO_C11	GPIO 11 on Port C
Alternate Function 2	A20	Address line signal used for debugging
BTCLK/GPIO_C12/A21		

Table 2. Pin Descriptions (Continued)

Normal Mode	BTCLK	The Bluetooth 4 MHz system clock, used internally in all Bluetooth-related calculations.
Alternate Function 1 (GPIO)	GPIO_C12	GPIO 12 on Port C
Alternate Function 2	A21	Address line signal used for debugging

5.1.1 Power and Ground

The following table shows the power and ground supplies.

Table 3. Power and Ground Supplies

Name	Description	Value
COREVDD	Core Supply	1.8 V
AVDD	Port A Noise Sensitive Bluetooth Supply	1.8 V
BVDD	Port B Supply	1.8 - 3.3 V
CVDD	Port C Supply	1.8 - 3.3 V
MISCVDD	Clock and JTAG Supply	1.8 V
EIMVDD	EIM Supply	2.7 V[1]

1.Can run at 1.8 V with degraded performance in timing and pull-ups

NOTE:

All pads are tolerant to 3.6 V. All ground supplies are tied together.

5.2 Functional Grouping of Signals

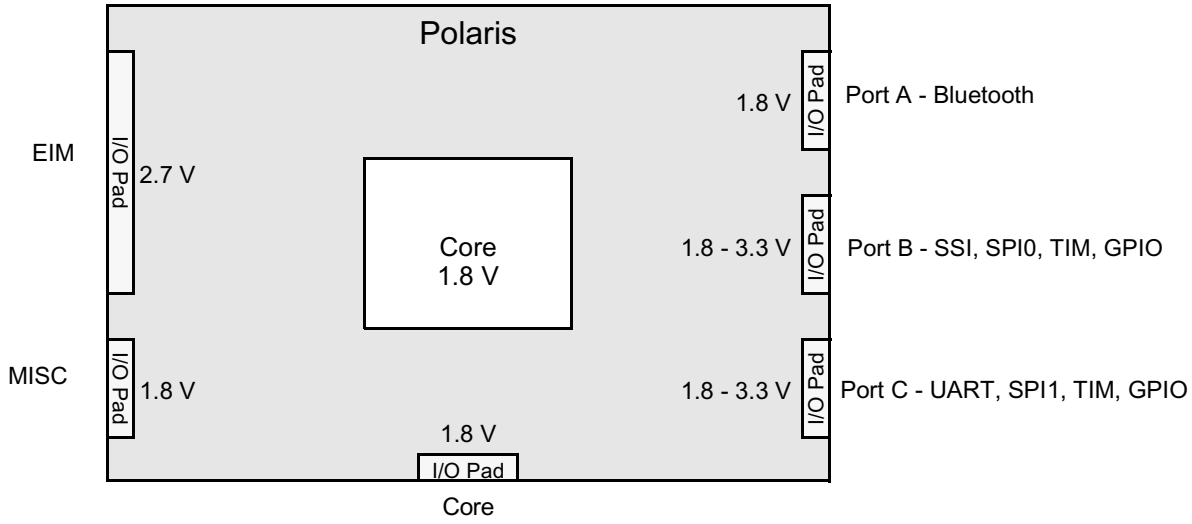


Figure 3. Functional Grouping of Signals

6 General Characteristics

Absolute maximum ratings given in Table 4 are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The MC71000 DC/AC electrical specifications are preliminary and are from design simulations and analysis. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

WARNING:

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to the high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either or V_{CC} or GND).

Table 4. Absolute Maximum Ratings (GND = 0 V)

Rating	Symbol	Value	Unit
Core supply voltage	V_{DD}	(GND–0.3) to 2.0	V
All other input voltages	V_{IN}	(GND – 0.3) to 3.6	V
Storage temperature range	T_{STG}	–55 to 150	°C

Table 5. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Core supply voltage	V_{DD}	1.65	1.8	1.95	V
Ambient temperature	T_A	–40	—	85	°C

Table 6. Package Thermal Characteristics

Thermal Resistance	Symbol	181-pin PGA	100-pin MAPBGA	Unit
Junction-to-ambient (estimated)[1]	$R_{\theta JA}$	105.38	22	C/W
Junction-to-case (estimated)[2]	$R_{\theta JC}$	28.76	1.6	C/W

1.Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided Printed Circuit Board.
2.Junction-to-case thermal resistance is based on measurements using a cold plate per with the exception that the cold plate temperature is used for the case temperature.

6.1 DC Electrical Characteristics

Table 7. DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
EIM supply voltage	EIMVDD	—	2.7	—	V
MISC supply voltage	MISCVDD	1.8	—	3.3	V
Bluetooth supply voltage (Port A)	AVDD	—	1.8	—	V

Table 7. DC Electrical Characteristics (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage (level shift I/O)	BVDD CVDD	1.8	—	3.3	V
High-level DC input voltage					
EIMVDD (2.7 V)	V_{IH}	1.90	2.7	3.6	V
MISCVDD		MISCVDD *	1.8	3.6	
AVDD		AVDD * 0.8	—	3.6	
BVDD		BVDD * 0.8	—	3.6	
CVDD		CVDD * 0.8	—	3.6	
High-level DC output voltage					
(2.7 V) EIMVDD	V_{OH}	2.2	—	2.7	V
MISCVDD		MISCVDD *	—	1.8	
AVDD		AVDD * 0.8	—	AVDD	
BVDD		BVDD * 0.8	—	BVDD	
CVDD		CVDD * 0.8	—	CVDD	
Low-level DC output voltage	V_{OL}	0	—	VDD * 0.2	V
Low-level DC input voltage	V_{IL}	-.3	—	VDD * 0.2	V
Current drain (run mode) @ 24 MHz, 1.8V	IDD_{ACTIVE}	—	17	—	mA
Current drain (stop mode) @ 1.8V	IDD_{SLEEP}	—	25	—	µA
Input capacitance (estimated)	C_{IN}	—	5	—	pF

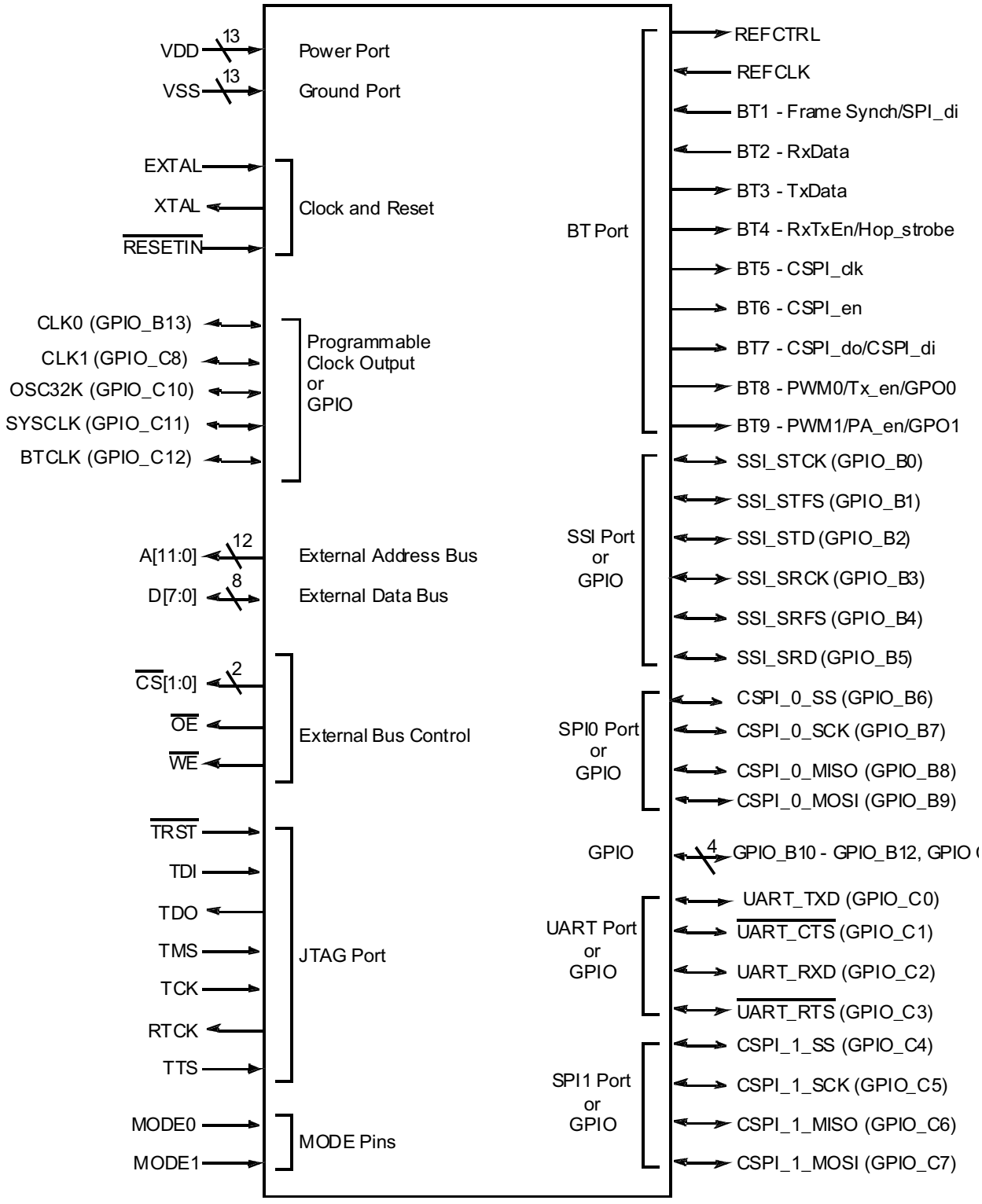


Figure 4. 100 MAPBGA Standard Configuration

7 Mechanical Specifications

7.1 Packaging

MAPBGA, 100-pin

- 7 mm x 7 mm x 1.35 mm
- 0.65 mm pitch

Table 8. MC71000 Bluetooth Baseband Controller 100 MAPBGA Ball Pad to Signal Name Net List

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	A6	D5	OSC32K	G9	MODE0
A2	A2	D6	SPI1_SS	G10	PWR_IO_I1_MISC
A3	CS0	D7	BTCLK	H1	D6
A4	WE	D8	GND_PB2	H2	D7
A5	CTS	D9	SPI0_SCK	H3	D5
A6	SPI1_SCK	D10	SPI0_MOSI	H4	GND_CORE2
A7	RXD	E1	PWR_EIM2	H5	PWR_PA1
A8	RTS	E2	GND_EIM2	H6	BT8
A9	SSI_STCK	E3	PWR_EIM7	H7	BT9
A10	SSI_SRCK	E4	A1	H8	TMS
B1	A7	E5	CLK1	H9	TDO
B2	A5	E6	SYSCLK	H10	RTCK
B3	A0	E7	GPIO_B11	J1	GND_EIM3
B4	OE	E8	SPI0_MISO	J2	GND_EIM4
B5	TXD	E9	CLK0	J3	GND_CORE2
B6	SPI1_MISO	E10	GPIO_B12	J4	PWR_CORE2
B7	PWR_PC3	F1	D0	J5	BT7
B8	SPI0_SS	F2	PWR_CORE1	J6	REFCLK
B9	SSI_STD	F3	GND_CORE1	J7	BT2
B10	SSI_SRD	F4	GND_EIM7	J8	BT4
C1	A9	F5	A4	J9	EXTAL
C2	A8	F6	MODE1	J10	TDI
C3	CS1	F7	GPIO_B10	K1	PWR_EIM3
C4	PWR_CORE4	F8	PWR_CORE3/	K2	PWR_EIM4
C5	GPIO_C9	F9	GND_CORE3/	K3	PWR_CORE2
C6	SPI1_MOSI	F10	RESETIN	K4	REFCTRL
C7	GND_PC3	G1	D3	K5	BT6
C8	PWR_PB2	G2	D4	K6	BT5
C9	SSI_STFS	G3	D2	K7	BT1
C10	SSI_SRFS	G4	D1	K8	BT3
D1	A11	G5	GND_PA1	K9	XTAL
D2	A10	G6	GND_MISC1	K10	TRST
D3	A3	G7	TCK		
D4	GND_CORE4	G8	TTS		

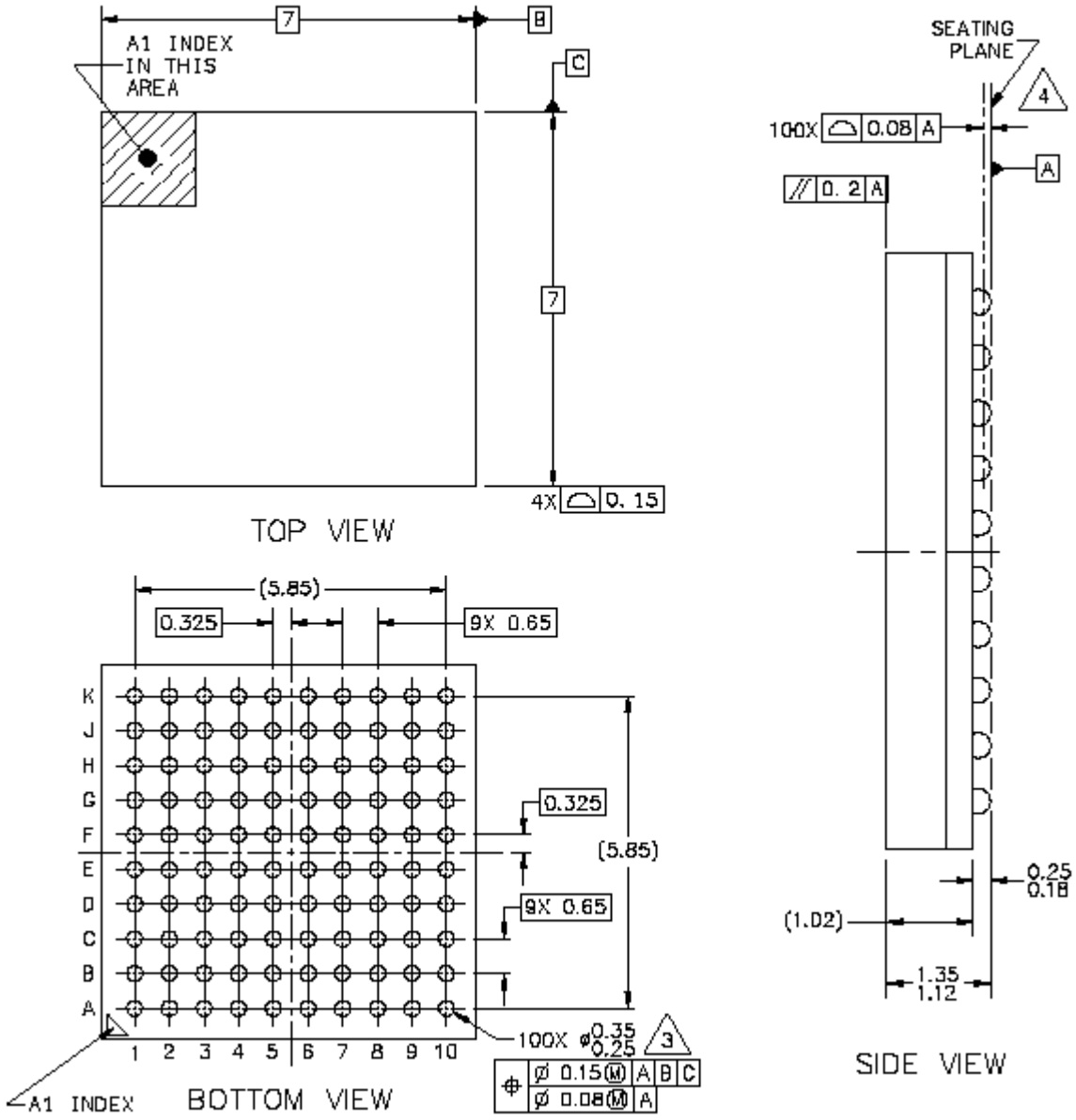


Figure 5. 100 MAPBGA Package Diagram 7 mm x 7 mm x 1.35 mm

8 Functionality Overview

The following section describes the link control and link manager features in detail and provides information on when those features will be supported (if not supported in this version).

8.1 Link Control Features

The following table lists, in detail, the supported link controller features of the MC71000. With only slight modification, the table has been prepared so that it closely parallels the Bluetooth SIG's PICS Proforma Annex B, Version 0.91.

Table 9. Overview of Link Controller Features

Feature	ROM V0.92 and ROM V2.0[1]	Planned Future Features	Support Not Currently Planned
Frequency Hopping Systems			
79-channel frequency hopping system	x		
23-channel frequency hopping system[2]	x		
Link Types			
ACL link support	x		
SCO link support	x		
Piconet Capabilities			
Max simultaneous ACL links[3]	7	7	
Point-to-point connection	x		
Point-to-multipoint connections	x		
Scatternet Capabilities			
Master in one piconet and slave in another			
Slave in more than one piconet			
SCO Link Capabilities			
Max simultaneous SCO links[3]	1	3	
Multiple SCO links to same slave			
Multiple SCO links to different slaves			
Multiple SCO links from same master			
Multiple SCO links from different masters			x
Common Packet Types			
ID packet type	x		
NULL packet type	x		
POLL packet type	x		
FHS packet type	x		
DM1 packet type	x		
ACL Packet Types			
DH1 packet type	x		
DM3 packet type	x		
DH3 packet type	x		
DM5 packet type	x		
DH5 packet type	x		
AUX1 packet type			x
SCO Packet Types			

Table 9. Overview of Link Controller Features (Continued)

Feature	ROM V0.92 and ROM V2.0[1]	Planned Future Features	Support Not Currently Planned
HV1 packet type	x		
HV2 packet type	x		
HV3 packet type	x		
DV packet type	x		
Paging Procedures			
Paging, 79-channel system	x		
Page scan, 79-channel system	x		
Paging, 23-channel system[2]	x		
Page scan, 23-channel system[2]	x		
Paging Schemes			
Paging scheme 0 (Mandatory)	x		
Paging scheme 1 (Optional I)			
Page Scanning Modes			
Paging mode R0	x		
Paging mode R1	x		
Paging mode R2	x		
Paging Train Repetition			
$N_{page} \geq 1$	x		
$N_{page} \geq 128$	x		
$N_{page} \geq 256$	x		
Inquiry Procedures			
Inquiry, 79-channel system	x		
Inquiry scan, 79-channel system	x		
Inquiry, 23-channel system[2]	x		
Inquiry scan, 23-channel system[2]	x		
Inquiry support for all IACs	x		
Inquiry scan, max num simultaneous IACs	2	2	
Other Link Controller Features			
Transparent SCO data pass-through			
Adaptive Frequency Hopping			
Antenna diversity			

1.ROM V2.0 is the label assigned to the production-ready, qualified iteration of ROM Version 0.92. There is no plan for a “ROM V1.0”.
2.The 23-channel frequency hopping system is fully implemented in ROM Version 0.92, but as it is being discontinued by the Bluetooth SIG, extensive testing has not been performed.

3.This value can be adjusted down to reduce the amount of RAM consumed on the MC71000.

8.2 Link Manager Features

Table 10 lists the Link Manager features of the MC71000. The table parallels the Bluetooth SIG's PICS Proforma Annex C, Version 0.91.

Table 10. Overview of Link Manager Features

Feature	ROM V0.92 and ROM V2.0[1]	Planned Future Features	Support Not Currently Planned
Supported Features (General Statement)			
3-slot packets	x		
5-slot packets	x		
Encryption	x		
Slot offset	x		
Timing accuracy	x		
Role switch (master/slave)	x		
Hold mode	x		
Sniff mode	x		
Park mode		x	
Power control		x	
Channel quality driven data rate		x	
RSSI	x		
Authentication			
Initiate authentication before connection completed	x		
Initiate authentication after connection completed	x		
Respond to authentication request	x		
Pairing			
Initiate pairing before connection completed	x		
Initiate pairing after connection completed	x		
Respond to pairing request	x		
Use fixed PIN and request responder-to-initiator switch	x		
Use variable PIN	x		
Accept initiator-to-responder switch	x		
Link Keys			
Link key creation using a unit key (local device is configured with a unit key)			x
Link key creation using a unit key (remote device is configured with a unit key)	x		

Table 10. Overview of Link Manager Features (Continued)

Feature	ROM V0.92 and ROM V2.0[1]	Planned Future Features	Support Not Currently Planned
Link key creation using a combination key	x		
Initiate change of link key	x		
Accept change of link key	x		
Change to temporary key (i.e., master link key)	x		
Make semi-permanent link key the current link key (i.e., exit master link key)	x		
Encryption			
Initiate encryption	x		
Accept encryption requests	x		
Point-to-point encryption	x		
Point-to-point and broadcast encryption	x		
Key size negotiation (up to 128 bit)	x		
Start encryption	x		
Accept start of encryption	x		
Stop encryption	x		
Accept stop of encryption	x		
Information Requests/Status Requests			
Request clock offset information	x		
Respond to clock offset requests	x		
Send slot offset information	x		
Request timing accuracy information	x		
Respond to timing accuracy requests	x		
Request LM version information	x		
Respond to LM version requests	x		
Request supported features	x		
Respond to supported features requests	x		
Request name information	x		
Respond to name requests	x		
Get link quality	x		
Read RSSI	x		
Role Switch			
Request master/slave switch	x		
Accept master/slave switch requests	x		
Detach			

Table 10. Overview of Link Manager Features (Continued)

Feature	ROM V0.92 and ROM V2.0[1]	Planned Future Features	Support Not Currently Planned
Detach connection	x		
Hold Mode			
Request hold mode	x		
Respond to hold mode requests	x		
Force hold mode			x
Accept forced hold mode	x		
Sniff Mode			
Request sniff mode	x		
Respond to sniff mode requests	x		
Request un-sniff	x		
Accept un-sniff requests	x		
Park Mode			
Request park mode		x	
Respond to park mode request		x	
Set up broadcast scan window		x	
Accept change to the broadcast scan window		x	
Modify beacon parameters		x	
Accept modification of beacon parameters		x	
Request unpark using PM_ADDR		x	
Request unpark using BD_ADDR		x	
Slave requested unpark		x	
Accept unpark using PM_ADDR		x	
Accept unpark using BD_ADDR		x	
Power Control			
Request to increase power	x		
Request to decrease power	x		
Respond when max power reached		x	
Respond when minimum power reached		x	
Link Supervision Timeout			
Set link supervision timeout value	x		
Accept link supervision timeout setting	x		
Quality of Service			
Channel quality driven change between DM and DH packet types		x	

Table 10. Overview of Link Manager Features (Continued)

Feature	ROM V0.92 and ROM V2.0[1]	Planned Future Features	Support Not Currently Planned
Force/accept forced change of Quality of Service (QoS)	x[2]		
Request/accept change of QoS	x[2]		
Multi-Slot Packages			
Allow maximum number of slots to be used	x		
Request maximum number of slots to be used	x		
Accept request of maximum number of slots to be used	x		
Paging Scheme			
Request page mode to use		x	
Accept suggested page mode		x	
Request page scan mode to use		x	
Accept suggested page scan mode		x	
Test Mode			
Activate test mode (as tester)			x
Enable test mode (as DUT) and ability to accept activation of test mode	x		
Ability to reject activation of test mode if test mode is disabled	x		
Control test mode			x
Ability to reject test mode control commands if test mode is disabled	x		

1.ROM V2.0 is the label assigned to the production-ready, qualified iteration of ROM Version 0.92. There is no plan for a ROM V1.0.
2.ROM Version 0.92 supports Best-Effort Quality of Service (QoS) only. The Guaranteed and No Traffic QoS types are features planned for ROM Version 3.0.

9 Supported HCI Commands

The HCI provides a command interface to the baseband controller and link manager, and access to hardware status and control registers. This interface provides a uniform method of accessing the Bluetooth baseband capabilities. Table 11 shows the currently supported HCI commands. The commands are divided into the following major groupings: link control, link policy, host/baseband, events, informational parameters, status parameters, and testing. The following list shows some of the key features of the HCI:

- 23- and 79-channel frequency hopping
- Supports all connection types
- Supports all packet types
- Host controller HCI flow control

- Authentication and pairing
- Change packet type
- Encryption
- Master/slave role switch
- Hold/sniff modes
- Radio TX power status and control
- Test modes

Table 11. HCI Commands and Events

HCI Command Name	Currently Supported	ROM 3.0	Not Supported
Link Control Commands			
HCI_Inquiry	X		
HCI_Inquiry_Cancel	X		
HCI_Periodic_Inquiry_Mode	X		
HCI_Exit_Periodic_Inquiry_Mode	X		
HCI_Create_Connection	X		
HCI_Disconnect	X		
HCI_Accept_Connection_Request	X		
HCI_Reject_Connection_Request	X		
HCI_Change_Connection_Packet_Type	X		
HCI_Add_SCO_Connection	X		
HCI_Remote_Name_Request	X		
HCI_Read_Remote_Supported_Features	X		
HCI_Read_Clock_Offset	X		
HCI_Read_Remote_Version_Information	X		
HCI_Authentication_Requested	X		
HCI_Link_Key_Request_Reply	X		
HCI_Link_Key_Request_Negative_Reply	X		
HCI_Pin_Code_Request_Reply	X		
HCI_Pin_Code_Request_Negative_Reply	X		
HCI_Change_Connection_Link_Key	X		
HCI_Master_Link_Key	X		
HCI_Set_Connection_Encryption	X		
Link Policy Commands			
HCI_Read_Link_Policy_Settings	X		
HCI_Write_Link_Policy_Settings	X		
HCI_Switch_Role	X		
HCI_Role_Discovery	X		
HCI_Read_Link_Policy_Settings	X		
HCI_Write_Link_Policy_Settings	X		
HCI_Hold_Mode	X		
HCI_Sniff_Mode	X		

Table 11. HCI Commands and Events (Continued)

HCI Command Name	Currently Supported	ROM 3.0	Not Supported
HCI_Exit_Sniff_Mode	X		
HCI_Park_Mode		X	
HCI_Exit_Park_Mode		X	
HCI_QoS_Setup		X	
Host/Baseband Commands			
HCI_Read_Scan_Enable	X		
HCI_Write_Scan_Enable	X		
HCI_Read_Page_Scan_Activity	X		
HCI_Write_Page_Scan_Activity	X		
HCI_Read_Inquiry_Scan_Activity	X		
HCI_Write_Inquiry_Scan_Activity	X		
HCI_Read_Number_Of_Supported_IAC	X		
HCI_Read_Current_IAC_LAP	X		
HCI_Write_Current_IAC_LAP	X		
HCI_Read_Connection_Accept_Timeout	X		
HCI_Write_Connection_Accept_Timeout	X		
HCI_Read_Page_Timeout	X		
HCI_Write_Page_Timeout	X		
HCI_Flush	X		
HCI_Read_Automatic_Flush_Timeout	X		
HCI_Write_Automatic_Flush_Timeout	X		
HCI_Set_Event_Mask	X		
HCI_Set_Event_Filter	X		
HCI_Reset	X		
HCI_Read_Class_of_Device	X		
HCI_Write_Class_of_Device	X		
HCI_Read_Num_Broadcast_Retransmissions	X		
HCI_Write_Num_Broadcast_Retransmissions	X		
HCI_Read_Link_Supervision_Timeout	X		
HCI_Write_Link_Supervision_Timeout	X		
HCI_Read_Voice_Setting	X		
HCI_Write_Voice_Setting	X		
HCI_Read_SCO_Flow_Control_Enable	X		
HCI_Write_SCO_Flow_Control_Enable	X		
HCI_Host_Buffer_Size	X		
HCI_Set_Host_Controller_To_Host_Flow_Control	X		
HCI_Host_Number_Of_Completed_Packets	X		
HCI_Read_Authentication_Enable	X		
HCI_Write_Authentication_Enable	X		
HCI_Read_PIN_Type	X		
HCI_Write_PIN_Type	X		

Table 11. HCI Commands and Events (Continued)

HCI Command Name	Currently Supported	ROM 3.0	Not Supported
HCI_Read_Stored_Link_Key	X		
HCI_Write_Stored_Link_Key	X		
HCI_Delete_Stored_Link_Key	X		
HCI_Read_Encryption_Mode	X		
HCI_Write_Encryption_Mode	X		
HCI_Read_Hold_Mode_Activity	X		
HCI_Write_Hold_Mode_Activity	X		
HCI_Read_Transmit_Power_Level	X		
HCI_Read_Page_Scan_Mode	X		
HCI_Write_Page_Scan_Mode		X	
HCI_Read_Page_Scan_Period_Mode	X		
HCI_Write_Page_Scan_Period_Mode		X	
Informational Parameters			
HCI_Read_BD_ADDR	X		
HCI_Read_Buffer_Size	X		
HCI_Read_Local_Supported_Features	X		
HCI_Read_Country_Code	X		
HCI_Read_Local_Version_Information	X		
Status Parameters			
HCI_Read_Failed_Contact_Counter	X		
HCI_Reset_Failed_Contact_Counter	X		
HCI_Get_Link_Quality	X		
HCI_Read_RSSI	X		
Testing			
HCI_Read_Loopback_Mode	X		
HCI_Read_RSSI	X		
HCI_Enable_Device_Under_Test_Mode	X		

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217
1-303-675-2140 or 1-800-441-2447

JAPAN:

Motorola Japan Ltd.; SPS, Technical Information Center,
3-20-1, Minami-Azabu Minato-ku, Tokyo 106-8573 Japan
81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.; Silicon Harbour
Centre, 2 Dai King Street, Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
852-26668334

TECHNICAL INFORMATION CENTER:

1-800-521-6274

HOME PAGE:

http://www.motorola.com/semiconductors

MOTOROLA

MC71000TB/D

Preliminary