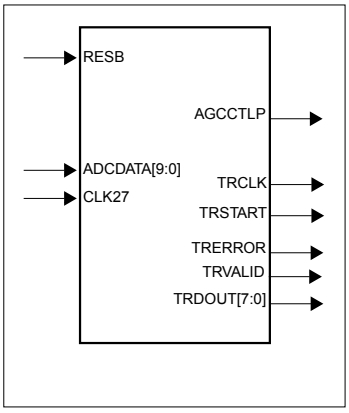
Order Number: MC92315AI/D
Rev. 1.1, 17 Feb 2000

MC92315

Advance Information

MC92315

2K/8K Integrated DVB-T Demodulator

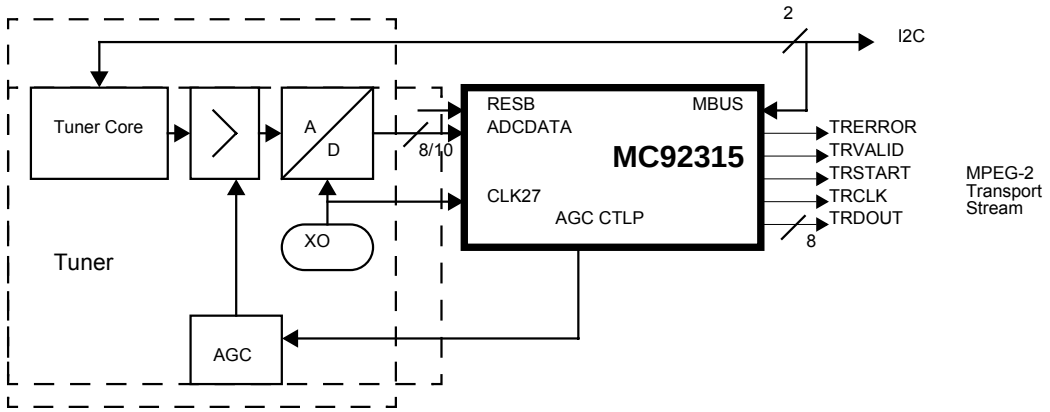


The MC92315 is a DVB-T compliant demodulator for 2K/8K transmission mode according to the ETSI specification for digital terrestrial broadcasting (ETS 300744). The MC92315 contains all the functionality required to demodulate and decode DVB-T compliant broadcast signals.

Feature Summary

- Automatic detection of 2K/8K mode
- Usable for 8MHz/7MHz/6MHz channels
- Digital I/Q separation on-chip
- Digital AFC on chip
- No VCXO required, free running XO at 27MHz sufficient
- Supports QPSK, 16-QAM and 64-QAM (non-hierarchical and hierarchical)
- Supports all guard interval lengths (1/32, 1/16, 1/8, 1/4)
- Automatic locking to any DVB-T guard interval
- 10-bit CMOS input for 2's-complement or offset-binary ADC data
- Provides control signals for AGC clock frequency control
- Viterbi Decoder for DVB convolutional code rates 1/2, 2/3, 3/4, 5/6 and 7/8
- Reed/Solomon Decoder for DVB Reed-Solomon code (204,188,8)
- I^2C serial bus compatible interface (M-Bus) for external programming and control
- Operating voltage 1.8V for the core and 3.3V for the I/O
- Power requirement 0.8W
- Package 160PQFP and 100TQFP
- Pin-compatible to MC92314 2K DVB-T demodulator

Ordering Information	
Device	**Package**
MC92315DH	160PQFP
MC92315NY	100TQFP



MC92315 Pinout (160PQFP)

The pinout for this package is given in the figure below:

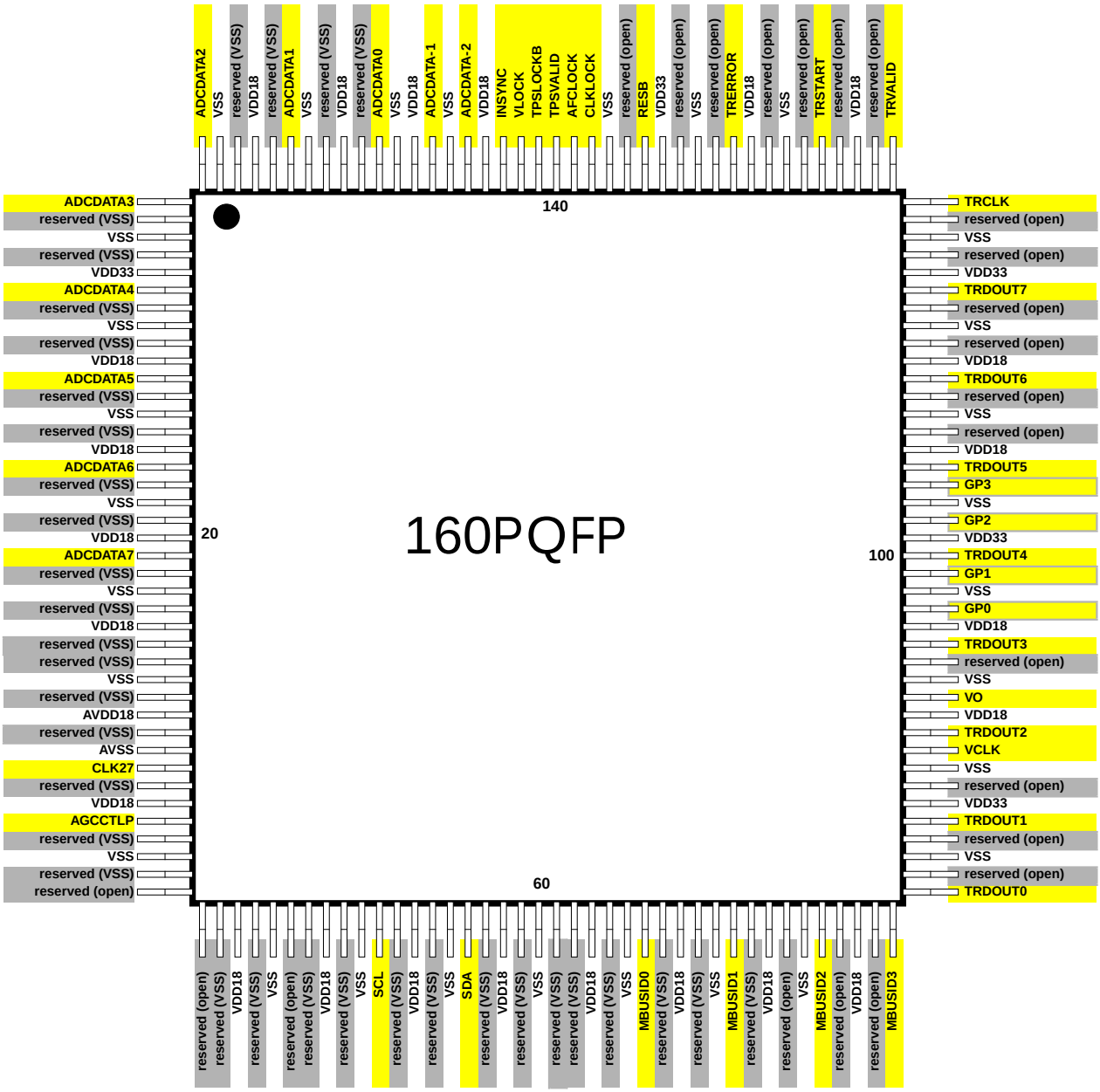


Figure 1. MC92315 Pinout (160PQFP)

Table 1: MC92315 Pin List (160PQFP)

SIGNAL	PIN-NR.	FUNCTIONALITY	TYPE	ACTIVE
RESB	135	Reset (asynchronous)	TTL - IN	low
CLK27	33	27 MHz Clock input	TTL - IN	high
ADCDATA[7:0]	21, 16, 11, 6, 1, 160, 155, 150	ADC input for 8-Bit ADCs	TTL - IN	high
ADCDATA[-1:-2]	147, 145	10-Bit extension for 10-Bit ADCs	reserved (VSS)	N/A
AGCCTLP	36	Analogue AGC control (+)	TTL - OUT	high
SDA	56	I^2C compatible control bus, data pin	TTL - OD	N/A
SCL	51	I^2C compatible control bus, clock pin	TTL - IN	high
MBUSID[3:0]]	80, 76, 71, 66	I^2C compatible control bus, variable ID selector	TTL - IN	high
VO	92	Output of Viterbi Decoder	TTL - OUT	high
VCLK	89	Clock for Viterbi Output	TTL - OUT	high
GP[3:0]	104, 102, 99, 97	General Purpose output pins, accessible via I^2C	TTL - OUT	high
TRERROR	130	MPEG-2 Frame Error Indicator	TTL - OUT	high
TRVALID	121	MPEG-2 Byte Valid Indicator	TTL - OUT	high
TRSTART	125	MPEG-2 Sync Byte Indicator	TTL - OUT	high
TRCLK	120	MPEG-2 Byte Clock	TTL - OUT	high
TRDOUT[7:0]	115, 110, 105, 100, 95, 90, 85, 81	MPEG-2 Transport Stream Byte Output	TTL - OUT	high
INSYNC	143	FEC Frame Synchronization Status	TTL - OUT	high
VLOCK	142	Viterbi Decoder Synchronization Status	TTL - OUT	high
TPSLOCKB	141	TPS demodulator in lock (active L)	TTL - OUT	low
TPSVALID	140	TPS data detected	TTL - OUT	high
AFCLCK	139	AFC status indicator	TTL - OUT	high
CLKLCK	138	Time Synchronization state indicator	TTL - OUT	high
VDD33	5, 86, 101, 116, 134	3.3 V Supply Voltage for I/O		N/A

SIGNAL	PIN-NR.	FUNCTIONALITY	TYPE	ACTIVE
VDD18	**10, 15, 20, 25, 35, 43, 48, 53, 58, 63, 68, 73, 78, 91, 96, 106, 111, 123, 129, 144, 148, 152, 157**	**1.8 V Supply Voltage for core**		**N/A**
VSS	**3, 8, 13, 18, 23, 28, 38, 45, 50, 55, 60, 65, 70, 75, 83, 88, 93, 98, 103, 108, 113, 118, 127, 132, 137, 146, 149, 154, 159**	**Ground pins**		**N/A**
AVDD18	**30**	**1.8 V analogue VDD (Integrated PLL)**		
AVSS	**32**	**Analogue VSS (Integrated PLL)**		

- VDD18 denotes the V_{DD} pins for the core in 1.8 V technology.
- VDD33 denotes the V_{DD} pins for the I/O in 3.3 V technology.
- AVDD18 denotes the supply voltage for the integrated PLL. It must be LC-filtered according to the 2K/8K Compatibility Schematic distributed in August 1998.
- AVSS denotes the ground pin of the integrated PLL. It must be connected with a low-impedance connection to the system ground plane.
- VDD18 denotes the V_{DD} pins for the core in 1.8 V technology.
- VDD33 denotes the V_{DD} pins for the I/O in 3.3 V technology.
- AVSS denotes the ground pin of the integrated PLL. It must be connected with a low-impedance connection to the system ground plane.
- **NOTE: Signal functions (e.g. MBUSID[3:0]) in the MC92315 Pin List are grouped in sequential order from the highest bit to the lowest bit.**

MC92315 Pinout (100TQFP)

The pinout for the smaller package is given in the figure below:

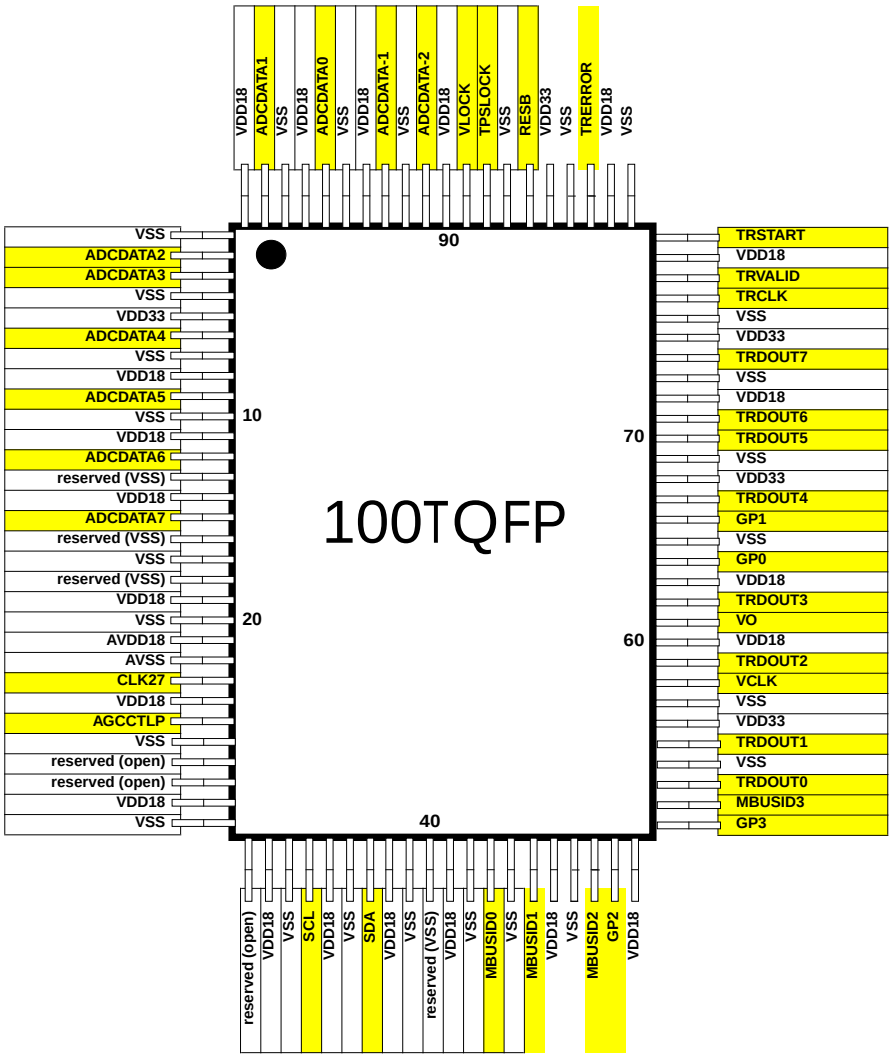


Figure 2. MC92315 Pinout (100TQFP)

Table 2: MC92315 Pin List (100TQFP) List

SIGNAL	PIN-NR.	FUNCTIONALITY	TYPE	ACTIVE
RESB	86	Reset (asynchronous)	IN	low
CLK27	23	27 MHz Clock input	IN	high

SIGNAL	PIN-NR.	FUNCTIONALITY	TYPE	ACTIVE
ADCDATA[7:0]	15, 12, 9, 6, 3, 2, 99, 96	ADC input for 8-Bit ADCs	IN	high
ADCDATA[-1:-2]	93, 91	10-Bit extension for 10-Bit ADCs	reserved (VSS)	N/A
AGCCTLP	25	Analogue AGC control (+)	OUT	high
SDA	37	I^2C compatible control bus, data pin	OD	N/A
SCL	34	I^2C compatible control bus, clock pin	IN	high
MBUSID[3:0]]	52, 48, 45, 43	I^2C compatible control bus, variable ID selector	IN	high
VO	61	Output of Viterbi Decoder	OUT	high
VCLK	58	Clock for Viterbi Output	OUT	high
GP[3:0]	51, 49, 66, 64	General Purpose output pins, accessible via I^2C	OUT	high
TRERROR	83	MPEG-2 Frame Error Indicator	OUT	high
TRVALID	78	MPEG-2 Byte Valid Indicator	OUT	high
TRSTART	80	MPEG-2 Sync Byte Indicator	OUT	high
TRCLK	77	MPEG-2 Byte Clock	OUT	high
TRDOUT[7:0]	74, 71, 70, 67, 62, 59, 55, 53	MPEG-2 Transport Stream Byte Output	OUT	high
VLOCK	89	Viterbi Decoder Synchronization Status	OUT	high
TPSLOCK	88	TPS demodulator in lock (active H)	OUT	high
VDD33	5, 56, 68, 75, 85	3.3 V Supply Voltage for I/O		N/A
VDD18	8, 11, 14, 19, 24, 29, 32, 35, 38, 41, 46, 50, 60, 63, 72, 79, 82, 90, 94, 97, 100	1.8 V Supply Voltage for core		N/A
VSS	1, 4, 7, 10, 17, 20, 26, 30, 33, 36, 39, 42, 44, 47, 54, 57, 65, 69, 73, 76, 81, 84, 87, 92, 95, 98	Ground pins		N/A

SIGNAL	PIN-NR.	FUNCTIONALITY	TYPE	ACTIVE
AVDD18	21	1.8 V analogue VDD for the analog part of the ntegrated PLL		
AVSS	22	Analogue VSS for the analog part of the integrated PLL		

NOTE: For the description of the supply voltages see Table 1 on page 3.

DC ELECTRICAL CHARACTERITICS

The MC92315 DC Electrical Characteristics are given in the following tables:

Table 3: Electrical Considerations

ABSOLUTE MAXIMUM RATINGS			
Symbol	Parameter		Unit
V_{DD33}	DC Supply Voltage, I/O	-0.3 to 4	V
V_{DD18}	DC Supply Voltage, Core	-0.3 to 2	V
V_{DDAP}	DC Supply Voltage, Analog PLL	-0.3 to 2	V
V_{DDDP}	DC Supply Voltage, Digital PLL	-0.3 to 2	V
V_{in}	DC Input Voltage	-0.3 to 4	V
I	DC Current Drain per Pin, Any Single Input or Output	25	mA
I	DC Current Drain VDD and VSS Pins	TBD	mA
T_{stg}	Storage Temperature	-55 to +150	°C
T_L	Lead Temperature (10 second soldering)	300	°C

Note: Maximum ratings are those values beyond which damage to the device may occur.

RECOMMENDED OPERATING CONDITIONS (to guarantee functionality)				
Symbol	Parameter	Min	Max	Unit
V_{DD33}*	DC Supply Voltage, V_{DD33} = 3.3V (Nominal)	3.0	3.6	V
V_{DD18}*	DC Supply Voltage, V_{DD18} = 1.8V (Nominal)	1.65	1.95	V
V_{DDAP}	DC Supply Voltage, Analog PLL	1.65	1.95	V
V_{DDDP}	DC Supply Voltage, Digital PLL	1.65	1.95	V
T_A	Commercial Operating Temperature	0	70	°C
T_J	Junction Temperature	0	105	°C

* For testing, only. V_{DD} range is wider for simulation purposes.

NOTES:

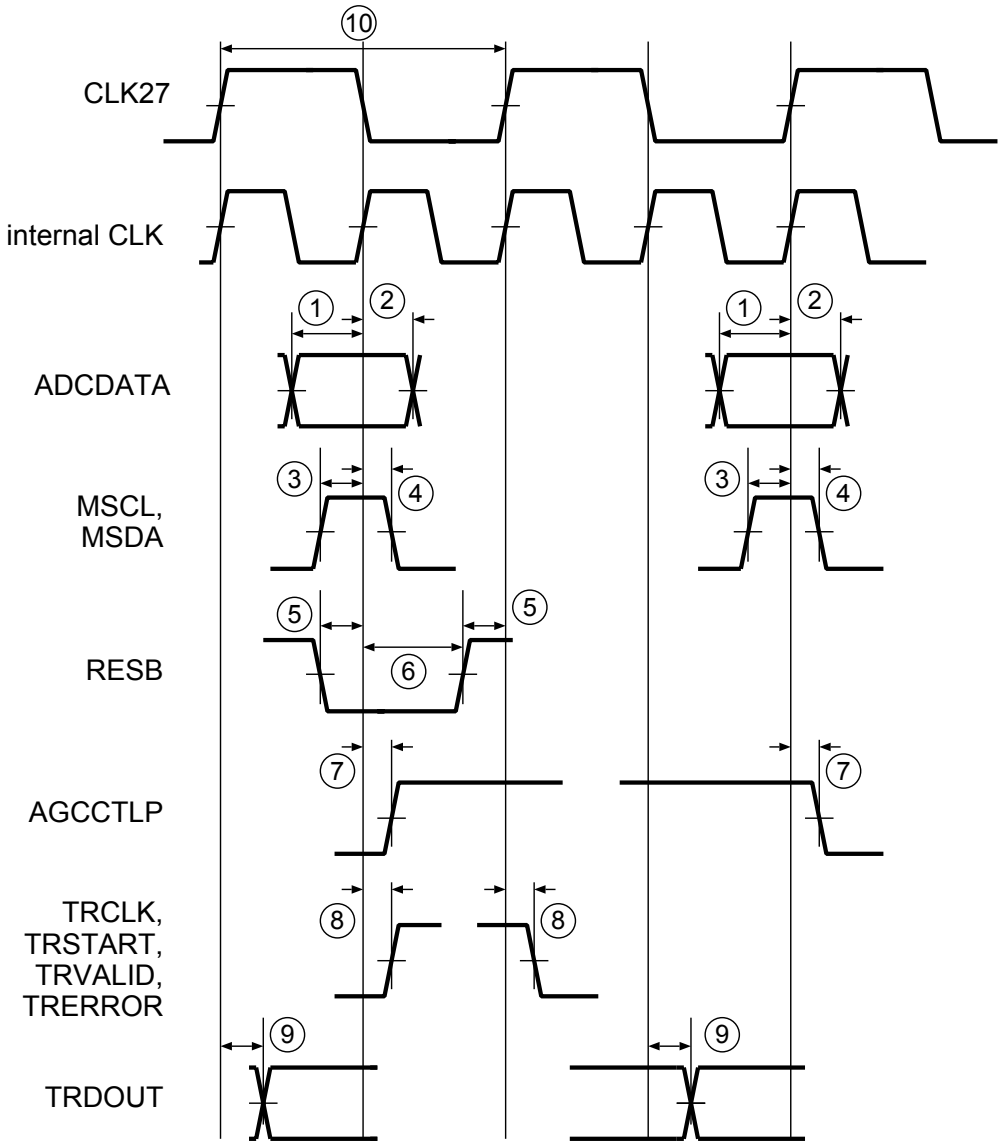
1. All parameters are characterized for DC conditions after thermal equilibrium has been established.
2. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Pins marked N/C are to be left unconnected. V_{DDAP} requires external lter ing of the supply. See details in the users manual.
3. Power sequencing precautions:
   - It is recommended that V_{DD18},V_{DDAP} and V_{DDDP} be applied before V_{DD33}.
   - Vin must not exceed V_{DD33} by more than 0.3 V at any time including during power-on reset.
   - V_{DD33} must not exceed V_{DD18} , V_{DDAP} or V_{DDDP} by more than 1.9V at any time including during power-on reset.
4. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD33}$.

Table 4: DC Electrical Characteristics (T_a = 0 C to 70 C)
V_{DD33} = 3.3V±0.3V

Sym.	Parameter	Condition	Min.	Max.	Unit
V_{IH}	LVTTL Inputs (3.3 V)		0.7*V_{DD33}	V_{DD33}	V
V_{IL}	LVTTL Inputs (3.3 V)		0	0.3*V_{DD33}	V
I_{in}	Input Leakage Current,No Pull Resistor	V_{in} = V_{DD33} or V_{SS}		1	µA
	with 100K Pullup Resistor		-18	-72	
	with 100K Pulldown Resistor		18	72	
I_{OH}	Output High Current, 5 mA LVTTL Output Type	V_{DD33} =Min, V_{OH} = 2.5 V	5		mA
	Output High Current, 10 mA LVTTL Output Type		10		
I_{OL}	Output Low Current, 5 mA LVTTL Output Type	V_{DD33} =Min, V_{OL}= 0.4 Volts	5		mA
	Output Low Current, 10 mA LVTTL Output Type		10		
V_{OH}	Output High Voltage, LVTTL	V_{DD33} = Min, I_{OH}= -100 mA	2.5		V
V_{OL}	Output Low Voltage, LVTTL	V_{DD33} = Min, I_{OH}= -100 mA		0.4	V
I_{OZ}	Output Leakage Current, 3-State Output	Output = Hi Impedance, V_{out} = V_{DD33} or V_{SS}		5	µA
	Output Leakage Current, Open Drain Output (Device Off)	Output = Hi Impedance, V_{out} = V_{DD33}		5	
I_{DD33}	Max Quiescent Supply Current	I_{out} = 0mA V_{in} = V_{DD33} or V_{SS}	TBD		mA

Switching Characteristics

The timing diagram of the MC92315 is shown below and additional timing information can be found in Table 5. The external clock CLK27 is multiplied by two to generate an ‘internal clock’ that is used for all registers of the MC92315. It should be noted that all timing relationships pertain to both edges of the clock CLK27 as both, rising and falling edges of CLK27 correspond to a rising edge of the internal clock. If CLK27 is used to clock the external ADC it will not matter which edge is used to trigger the ADC operation as longs as setup/hold requirements given in Table 5 are met.



Timing Diagram of the MC92315

Table 5: MC92315 Timing

No.	Characteristic	min	max	unit
1	ADCDATA to CLK setup time		2.2	ns
2	ADCDATA to CLK hold time		0.6	ns
3	MSCL, MSDA to CLK setup time		0.7	ns
4	MSCL, MSDA to CLK hold time		0	ns
5	RESB to CLK setup time		7.0	ns
6	RESB to CLK hold time		2.0	ns
7	CLK to AGCCTRLP out delay	3.2	6.6	ns
8	CLK to TRCLK, TRSTART, TRVALID, TRERROR out delay	3.2	7.6	ns
9	CLK to TRDOUT out delay	3.0	6.6	ns
10	CLK period	36.0	37.6	ns

Improvements included in the MC92315 device compared to the MC92314

In the following paragraphs the major improvements included in the 2K/8K OFDM demodulator MC92315 with respect to its predecessor MC92314 (2K only) are summarised:

Improvements concerning status information

Lock indicator register added

To improve the visibility of the internal functional blocks an additional I^2C register was added, showing all the lock indicator bits of the OFDM demodulator.

AGC lock indicator added

The visibility of the AGC functional block was improved by adding a status bit to the above mentioned register.

CSE information readable

To support reception quality measurement apart from BER measurement the appropriate value provided by the CSE block was made available. A new introduced 8 bit I^2C register provides this information intended especially for choosing the best antenna orientation by minimising the value reported in this register.

Improvements concerning the clock synchronisation

Full digital clock synchronisation

Instead of using an external VCXO all the clock synchronisation is done in the digital domain internally in the MC92315. The VCXO (running at 36.57 MHz) used in the MC92314 is simply replaced by a free running crystal oscillator running at 27 MHz (+/-1 MHz). The external ADC runs at this rate, too.

This concept avoids one of the external control loops employed in the MC92314.

The exact clock frequency of the crystal can be programmed into the MC92315, allowing faster clock synchronisation. The correction value can be read via I^2C, stored externally and used to speed up clock synchronisation after the next channel change of power up.

High efficiency clock synchronisation for the 8K mode

As the clock synchronisation in the 8K mode is much more difficult than in the 2K mode this block has been significantly reworked:

- Separate configuration of the clock synchronisation parameters for 2K and 8K reception.
- Programmable threshold to switch from acquisition to tracking mode.

- I In the 8K mode the tracking mode is separated additionally into two stages with different loop bandwidths (wide and narrow) with automatic changeover to ensure the best performance during acquisition **and** afterwards.

Improvements concerning other demodulator parameters

AFC range increased

The available correction range of the internal AFC was doubled. The user is able to select via I^2C the same range as before or double it by changing the internal coefficients.

Increased wordlength

The precision of the signal processing was increased, starting at the 10 bit ADC input. This provides a better overall SNR figure at the output of the MC92315.

No change of external clocking for different channel bandwidths

To make use of the different channel bandwidths specified by the DVB-T standard it is not necessary to use different clock frequencies like in the MC92314. The different channel bandwidths are programmable by I^2C, leaving the only difference between receivers for different channel bandwidths in the analog part.

Viterbi decoder takes code rate setting from OFDM demodulator

To avoid unneccesary long synchronisation times of the Viterbi decoder the most time consuming step (i.e. the selection of the coderate of the convolutional code) is replaced by using the TPS information from the OFDM demodulator. As a side effect the code rate for the whole device can be set (e.g. in applications with fixed code rate) by writing only into the OFDM part.

I^2C Register Map of the MC92315

As the single chip DVB-T demodulator MC92315 is the further development of Freescale's single chip 2K device, the register structure of its ancestor was preserved to allow as much reuse of the control software as possible. Therefore the registers are still grouped into the OFDM part and the FEC part, corresponding to Freescale's first generation DVB-T devices MC92308 and MC92309.

Register Map for the OFDM Part

The register map of the OFDM block is given in the table below with the registers changed or added w.r.t. its predecessor MC92314 marked.

The I^2C device address for the OFDM part is 010XXXX with XXXX beeing the logic levels at the external MBUSID pins.

Table 6: OFDM Block Register Map

Addr	Name	Type	Def/ Fmt	b7	b6	b5	b4	b3	b2	b1	b0
$0	TPS R0	R	*n/a*	S[7:0]							
$1	TPS R1	R	*n/a*	S[15:8]							
$2	TPS R2	R	*n/a*	S[23:16]							
$3	TPS R3	R	*n/a*	S[31:24]							
$4	TPS R4	R	*n/a*	S[39:32]							
$5	TPS R5	R	*n/a*	S[47:40]							
$6	TPS R 6	R	*n/a*	S[55:48]							
$7	TPS R7	R	*n/a*	S[63:56]							
$8	TPS R 8	R	*n/a*	AFCL	CLKL	TPSV	TPSL	S[67:64]			

Addr	Name	Type	Def/ Fmt	b7	b6	b5	b4	b3	b2	b1	b0
$9	TPS Idx	W	n/a	00000000							
$A	Reset	W	$00	AFC AGC	TSYNC	FE	FFT	CHAN	DEC	X	TOTAL
$B	OFDM R0	R/W	$12	X	CODERATE			GUARD		CONST	
$C	OFDM R1	W	$1F	CHANBW		XX		AFSY	ATPS	AFCM	TSM
$D	OFDM R2	W	$D3	FTSE	AFCS	AGCS	XX		UHFI	ADCM	MS2K
$E	CKFILT2K	W	$00 2's	CLKFILT2K_PROP				CLKFILT2K_INT			
$F	GAIN OFFS	W	$20 2's	AGC_GAIN				AFC_GAIN			
$10	AFCSWP0	W	$00	AFCSWPSTRT							
$11	AFCSWP1	W	$E8 2's								
$12	AFCTHRA	W	$15 Uns.	AFCTHRESH_A							
$13	AFCTHRB	W	$10 Uns.	AFCTHRESH_B							
$14	AGCTHR0	W	$96	AGCTHRESH							
$15	AGCTHR1	W	$2A Uns.								
$16	AFCSWS0	W	$80	AFCSWPSPEED							
$17	AFCSWS1	W	$00 2's								
$18	CSE R0	W	$40 Uns.	CSE_0							
$19	CSE R1	W	$20 Uns.	CSE_1							
$1A	CSE R2	W	$10 Uns.	CSE_2							
$1B	CSE R3	W	$00 2's	CSE_3							
$1C	CSE R4	W	$C6 Uns.	CSE_4							
$1D	CLKF8KWD	W	$1F 2's	CLKF8KWIDE_PROP				CLKF8KWIDE_INT			
§1E	CLKF8KNA	W	$1F 2's	CLKF8KNRW_PROP				CLKF8KNRW_INT			

Addr	Name	Type	Def/ Fmt	b7	b6	b5	b4	b3	b2	b1	b0
$1F	CLKOFS0	W	$00	CLKOFFSET							
$20	CLKOFS1	W	$00 2's								
$22	LOCKIN	R	*n/a*	STRV	AFCL	CLKL	TPSV	TPSL	AGCL	DEINT	INSYNC
$23	OFDMR3	R/W	$20	GIDET		AGI SE	AFCRG	ALPHA		STRM	8K
$35	AGCFIX0	W	$00	AGCFIX							
$36	AGCFIX1	W	$00 2's								
$3B	TSFB0	R	*n/a*	TS_FEEDBACK[7:0]							
$3C	TSFB1	R	*n/a 2's*	KDET	XXX			TS_FEEDBACK[11:8]			
$3F	AFCFB0	R	*n/a*	AFC_FEEDBACK							
$40	AFCFB1	R	*n/a 2's*								
$43	AGCFB0	R	*n/a*	AGC_FEEDBACK							
$44	AGCFB1	R	*n/a 2's*								
$48	FTFIX0	W	$00	FT_FIX[7:0]							
$49	FTFIX1	W	$E0 2's	ATSY	KENA	XX		FT_FIX[11:8]			

Note:

The bits marked 'X' are reserved bits.

Registers wider than 8 bits must be written LSB first, which is done in the most efficient way using the address auto-increment of the I^2C controller. **The value is stored internally not earlier than the MSB is written**.

Similar the reading of 2-byte read-only registers must start with the LSB. **The values provided by the internal blocks are latched only if the LSB is read**. If the user does an access to the MSB only no meaningful data are returned.

For more information see the MC92315 User Manual.

Register Map for the FEC Part

See the Table 7 on page 15 for the registers of the FEC block.

The I^2C device address for the FEC part is 001XXXX with XXXX beeing the logic levels at the external MBUSID pins

Table 7: FEC Block Register Map

Addr	Name	Type	Def	b7	b6	b5	b4	b3	b2	b1	b0
$00	CONFIG_VIT	W	$FF	DAP	DLT	DDEC	DTHR	IFS	VSYNC[2:0]		
$01	THRESHOLD	W	$00				THRES[4:0]				
$02	DECREMENT	W	$00				DEC[4:0]				
$03	TIMEOUT	W	$00					TIME[3:0]			
$04	AVG_PERIOD	W	$00					PERIOD[3:0]			
$08	QVALLSB	R		QVAL[7:0]							
$09	QVALMSB	R			QVAL[14:8]						
$0A	SYNC_VIT	R						VLCK	RIFO		R PHASE
$0B	SELECTEDRATE	R							SR[2:0]		
$0C	FIFO_STATE	R								VFF	VEF
$11	AQ_THRESH	W	$68	AQ_SYNC[2:0]			AQ_REF[4:0]				
$12	TR_THRESH	W	$7F	TR_SYNC[2:0]			TR_REF[4:0]				
$13	TIME_COUNT	W	$FF	TC[7:0]							
$18	BER_COUNT	R		BER_COUNT[7:0]							
$19	BAD_COUNT	R						BAD_COUNT[3:0]			
$1A	SYNC_RS	R		00000					STRV	DEINT	IN SYNC
$1F	SOFT_RESET	W	$00	GP[3:0]						SRRS	SRVIT

NOTE: The pecularities concerning the 2-byte registers of the OFMD part don't apply to the FEC block.

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