MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Product Preview

OC-3/STM-1 ATM Cell Processor (ATMC)

MC92501

The OC-3/STM-1 ATMC is a highly integrated ATM layer processor that combines such functions as OAM, policing, address translation, and statistics gathering. The single-chip device, capable of supporting full-duplex rates up to 155 Mbps, is composed of an ingress cell processor and egress cell processor. UTOPIA Level 2, intelligent memory, and host interfaces ensure easy system integration.

The second ATM cell processor family member adds TM4.0 and UNI4.0 compliance and full I.610 compliance on all 64K connections. For ease of migrating network management software, the MC92501 enhances the ATMC programming model while maintaining full compatibility with the other family members.

The OC-3 ATM cell processor's rich standards-based feature set supports such diverse applications as ATM core / edge switches, ATM LAN switches, digital cross-connects, add/drop muxes, multiservice access platforms, and base station controllers.

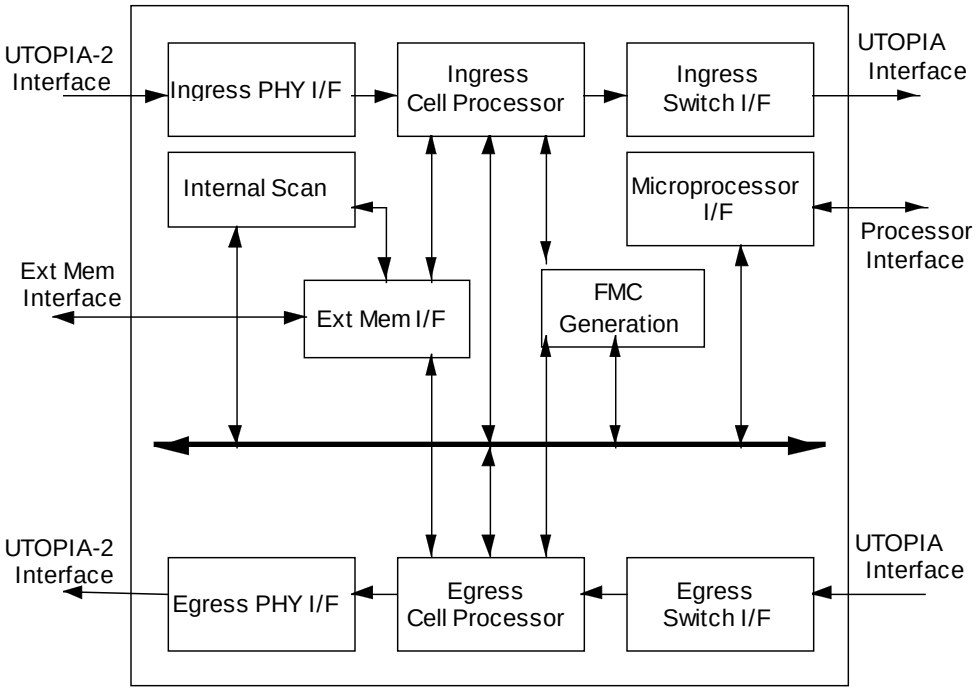

Figure 1: MC92501

Key Features:

- √ Full-duplex OC-3 (155 Mbps) cell processing
- √ UPC/NPC
- √ OAM
- √ Address translation
- √ Statistic gathering
- √ Easy upgrade from 92500
- √ Glueless interface to MC63XX and MPC8XX

Applications:

- ATM Core Switches
- ATM Edge Switches
- ATM Cross-Connects
- Multiservice Platforms
- Access Multiplexers

Complementary Products:

- CopperGold™ ADSL Modem
- MPC8XXSAR (PowerQUICC™)
- CAMs, NetRAMs, ZBTs

Features:

Overview:
- OC-3 (155 Mbps) line rates (full duplex)
- Support for up to 16 PHY UTOPIA Level 2 on the PHY interface
- Supports 64K VCs
- Implements ATM layer functions for broadband ISDN according to ANSI recommendations, ATM Forum specifications, and Bellcore recommendations

UPC/NPC:
- Four bucket per connection GCRA (leaky bucket algorithm)
- Either ingress or egress UPC/NPC
- Packet-based policing: partial packet discard (PPD), early packet discard (EPD)
- Selective discard for CLP = 1 and CLP = 0+1 flows
- CLP transparency / significance mode

Operation, Administration, and Maintenance (OAM):
- Fault Management
  - Continuity Check and Loopback on all connections
  - Virtual Path (VP) and Virtual Channel (VC) Alarm Surveillance (AIS/RDI) on all connections using an internal scan process to generate and insert OAM cells
- Performance Management
  - Performance Monitoring on all connections
  - Automatically performs PM block test once the microprocessor initiates block test request

Available Bit Rate (ABR):
- Supports Relative Rate ABR
- Supports changing RM cells' priority by marking the ingress switch parameters

Microprocessor Interface:
- Supports cell insertion / extraction using direct access registers by the microprocessor or by a DMA device
- Supports cell copying from the cell streams using direct access registers to the microprocessor or to a DMA device
- Provides indirect access to external memory
- Provides byte-swapping on cell payloads to and from the microprocessor bus to support both big-endian and little-endian buses
- Glueless connection to the MC68360 (QUICC), MPC860SAR and MPC860

Other Features:
- Configurable as a UNI (User-Network Interface) or NNI (Network-Network Interface)
- Uses external memory (up to 16 MB) to provide context management for all connections
- Supports point-to-multipoint operation on egress cell flow
- Uses 3.3 V power supply
- IEEE 1149.1 (JTAG) boundary scan test port

FUNCTIONAL SYSTEM DESCRIPTION

Figure 2 shows the MC92501 in a typical networking configuration. An ATM network is primarily composed of switching elements and access nodes. Within the ATM network core, the switches route multiple links to multiple links. A typical ATM core switch consists of a switch matrix and some line cards, one card for each physical link (or group of links). The switch matrix handles the actual routing of the cells. The line cards interface the physical lines to the switch matrix and perform ATM layer functions and cell queuing.

At the edges of the ATM network, access multiplexers aggregate multiple subscriber links to a single uplink. An access multiplexer line card consists of multiple PHYs, ATM layer functions, cell queuing, and a concentration matrix.

OPERATIONAL OVERVIEW

Figure 1 shows a block diagram of the MC92501. This diagram illustrates the integration of two independent cell processors, each capable of processing cells at an OC-3/STM-1 line rate.

Ingress Cell Flow

In the ingress direction, the MC92501 receives cells from the FIFO in the PHY. Cell discrimination is performed and uses pre-defined header field values to recognize unassigned and invalid cells. Unassigned and invalid cell slots may be used to insert OAM and messaging cells into the ingress cell flow. Cell rate decoupling is accomplished by discarding unassigned cells. In addition, the MC92501 operates at a true

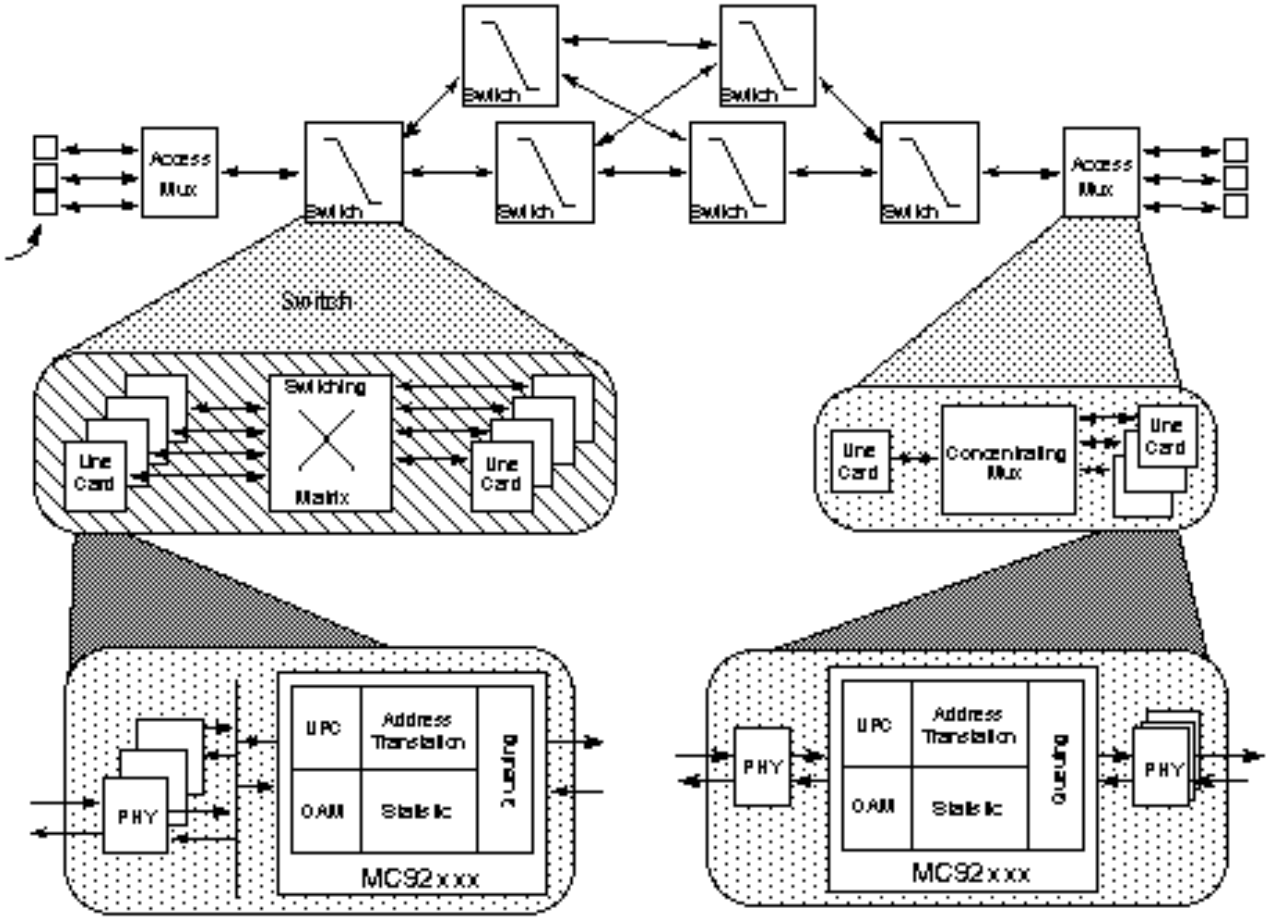

Figure 2: ATM Network Architecture

155 Mbps so the user is provided approximately 5 Mbps for cell flow insertion.

For VCCs, the 28-bit VPI/VCI address space (32-bit link/VPI/VCI if multiple physical links are supported) needs to be compressed into a 16-bit Ingress Connection Identifier (ICI). The MC92501 provides two methods for performing VPC or VCC address compression to generate the ICI:

- Table lookup based on reduced addressing (internal compression)
- External address lookup

The ICI is a pointer used to access the context parameters for the current ingress cell from the external context memory. Included in these parameters are cell counters, UPC/NPC traffic descriptors, OAM parameters, and switch parameters.

The UPC/NPC mechanism counts the arriving cells and, using a flexible arrangement of traffic enforcement algorithms, admits cells that do not violate the traffic characteristics established for that connection. Violating cells are tallied and may be tagged or discarded (i.e., removed from the cell flow).

The network operator may choose to have CLR (cell loss ratio) objective apply to either CLP=0 or CLP=0+1 cells. When CLP-Transparency is selected, the CLP bit in the cell's header is moved to the cell's overhead and the header CLP bit is set to 0. This process will allow all cells within the switch fabric to have equal loss priority (i.e., CLP=0). This copy is reversed in the egress processing path.

Frame discard is used during network congestion to increase the network's goodput. Three types of frame discard are supported: partial packet discard (PPD), early packet discard (EPD), and limited early packet discard (LEPD). The PPD algorithm discards all successive cells within the frame, except for the last cell, once the decision to discard a cell is made. The EPD algorithm discard decision occurs only at the beginning of the packet and either discards or passes the whole frame. In the case of big packets, the LEPD algorithm combines the benefits of PPD and EPD. In LEPD mode, the EPD algorithm is used until a pre-defined leaky bucket limit is reached; then the cells are discarded.

The OAM parameters are used to control how and when OAM cells are processed and to indicate if the current user cell belongs to a connection selected for a performance monitoring block test. If the ingress cell belongs to such a connection, the OAM table in external memory contains the relevant parameters.

Subsequent to the context processing, the ingress cells are transferred to the switch side UTOPIA interface. The associated user-defined switch overhead may be added to the cell before the header, and/or placed in the VPI/VCI fields of the header.

Egress Cell Flow

In the egress direction, the MC92501 receives cells from the switch, along with any associated parameters. The Egress Connection Identifier (ECI), which is contained in the cell header or extended header, is used for direct lookup into the context table to obtain the VPI/VCI, cell counters, and OAM flags.

If point-to-multipoint translation is enabled, the Multicast Identifier (MI) is received from the switch instead of the ECI, and the ECI is obtained from a lookup in the Multicast Translation Table. If enabled, the UPC function is executed. Cells are subject to processing as indicated by the OAM flags. If the egress cell belongs to a connection that has been selected for a performance monitoring test, the OAM Table in external memory contains the relevant parameters.

The egress cell header is generated by inserting the appropriate VPI/VCI fields obtained from the Address Translation Table. The PTI field is also updated in the case of an OAM cell or if signaled by the switch fabric. The cell is then forwarded to the appropriate PHY queue. Cell rate decoupling is performed in the egress direction (i.e., unassigned cells are optionally generated if no cells are available from the switch).

The cell's overhead, in the egress direction, moves the CLP bit from the extended overhead to the CLP field within the header when CLP-Transparent mode is enabled.

Other Functions

A general 32-bit slave system interface is provided for configuration, control, status monitoring, and insertion and extraction of cells. This interface provides for direct register access to the MC92501. The MC92501 also includes a standard JTAG Boundary Scan Architecture Test Access Port (TAP) for testing.

Upgrading from MC92500 or MC92501

When migrating from one device to another, modifying the network management software can be a concern. Motorola addressed this issue when upgrading the feature set of the MC92500 to create the MC92501. The two parts are pin and software compatible, which allows equipment vendors to enhance the software features as necessary.

Conclusion

The MC92501 is a full-duplex OC-3 ATM layer cell processor that includes OAM, UPC, address translation, and statistic gathering. By incorporating the ATM layer standard features within a single chip and providing configuration and driver software, the design cycle can be shortened.

Note: For the most current information regarding this device, contact Motorola on the World Wide Web at http://www.motorola.com/atmc

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