

## Product Preview

# 256K x 36 and 512K x 18 Bit ZBT<sup>®</sup> Fast Static RAM

**MCM64Z836**  
**MCM64Z918**

The ZBT RAM is an 8M-bit synchronous fast static RAM designed to provide Zero Bus Turnaround<sup>®</sup>. The ZBT RAM allows 100% use of bus cycles during back-to-back read/write and write/read cycles. The MCM64Z836 (organized as 256K words by 36 bits) and the MCM64Z918 (organized as 512K words by 18 bits) are fabricated in Motorola's high performance silicon gate CMOS technology. This device integrates input registers, an output register, a 2-bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in communication applications. Synchronous design allows precise cycle control with the use of an external positive-edge-triggered clock (CK). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

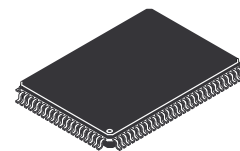
Addresses (SA), data inputs (DQ), and all control signals except output enable ( $\overline{G}$ ) and linear burst order ( $\overline{LBO}$ ) are clock (CK) controlled through positive-edge-triggered noninverting registers.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (CK) input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals. Write data is supplied to the memory one cycle after the write sequence initiation for the flow-through device, and two cycles after the write sequence initiation for the pipelined device.

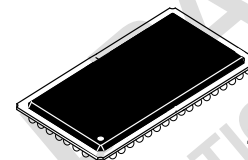
For flow-through read cycles, the SRAM allows output data to simply flow freely from the memory array. For pipelined read cycles, the SRAM output data is temporarily stored by an edge-triggered output register and then released to the output buffers at the next rising edge of clock (CK).

The MCM64Z836 and MCM64Z918 operate from a 2.5 V core power supply and all outputs operate on a 2.5 V power supply. All inputs and outputs are JEDEC Standard JESD8-5 compatible.

- 2.5 V  $\pm$ 200 mV Core Power Supply, 2.5 V I/O Supply
- MCM64Z836/918-7 = 7 ns Flow-Through Access/2.6 ns Pipelined Access (225 MHz)
- MCM64Z836/918-8 = 8 ns Flow-Through Access/3 ns Pipelined Access (200 MHz)
- MCM64Z836/918-8.5 = 8.5 ns Flow-Through Access/3.5 ns Pipelined Access (166 MHz)
- Selectable Read/Write Functionality (Flow-Through/Pipelined)
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self-Timed Write Cycle
- Two-Cycle Deselect (Pipelined)
- Byte Write Control
- ADV Controlled Burst
- Simplified JTAG
- 100-Pin TQFP and 119-Bump PBGA Packages



**TQ PACKAGE**  
**TQFP**  
**CASE 983A-01**



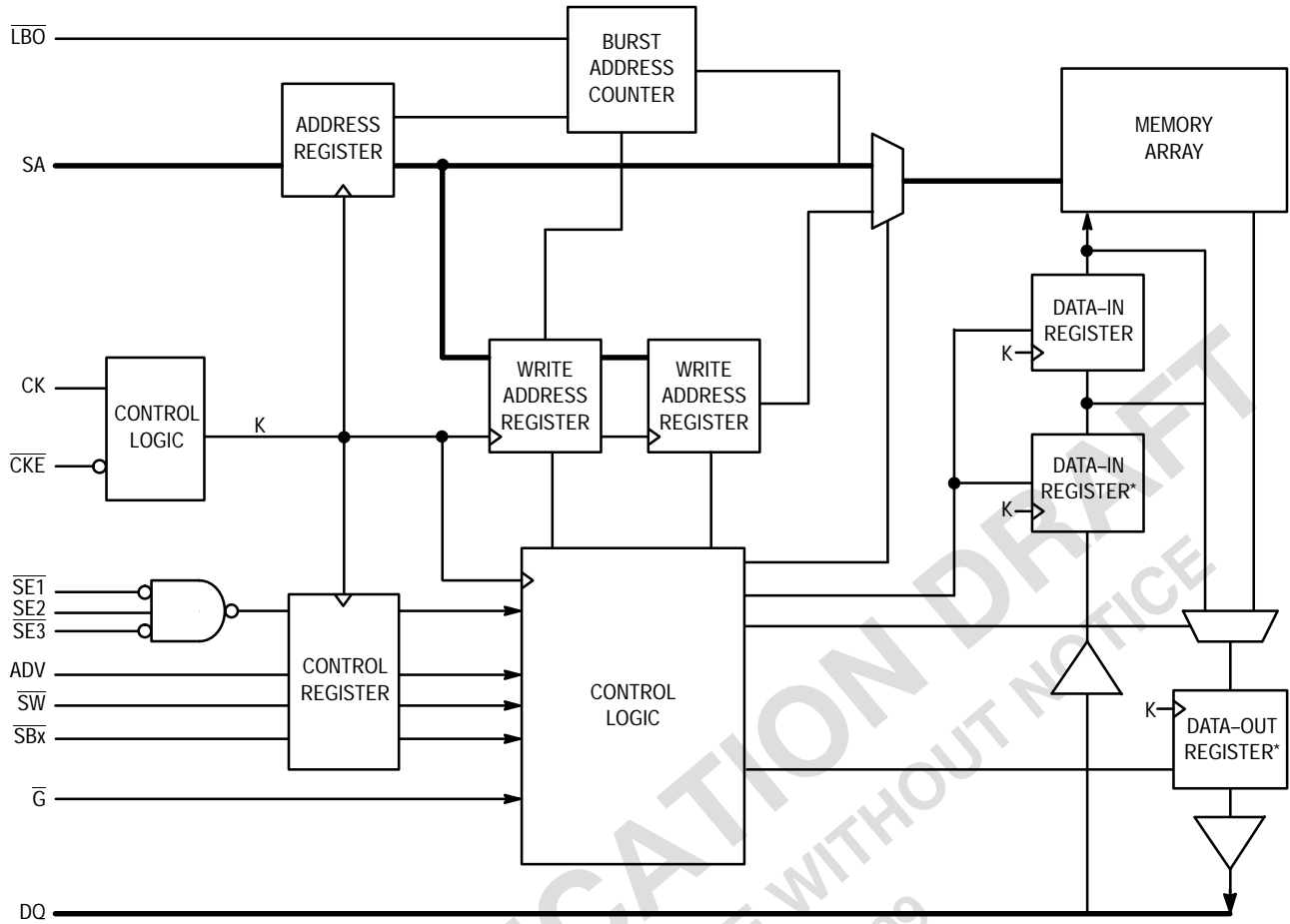
**ZP PACKAGE**  
**PBGA**  
**CASE 999-02**

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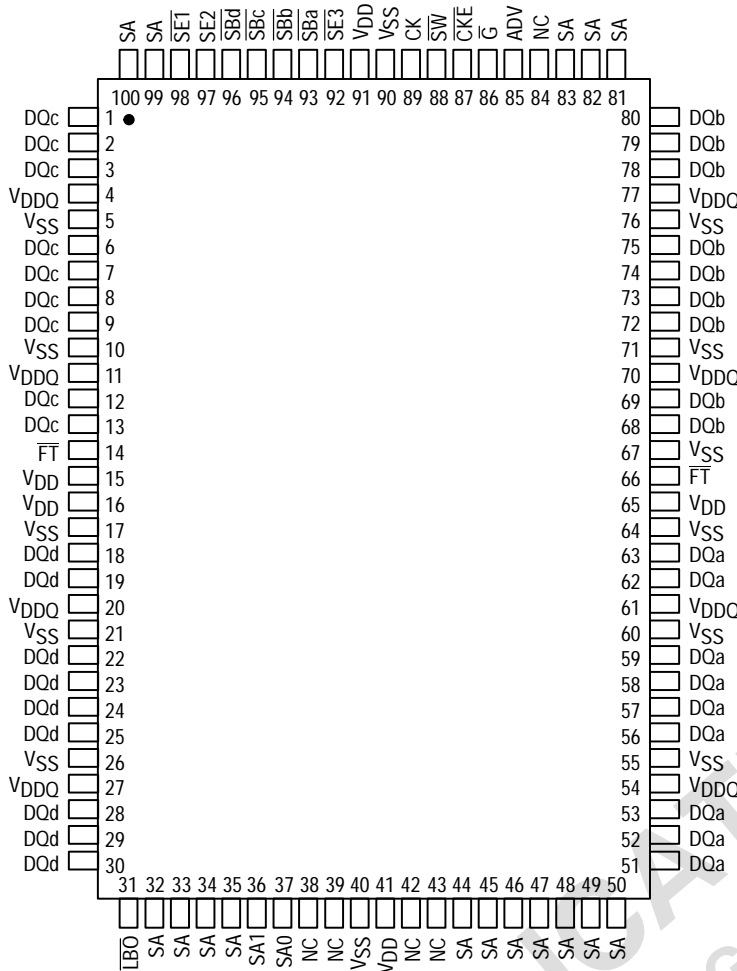
LOGIC BLOCK DIAGRAM



\* Valid only for pipelined device.

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## MCM64Z836 PIN ASSIGNMENTS



	1	2	3	4	5	6	7
A	○	○	○	○	○	○	○
B	VDDQ	SA	SA	NC	SA	SA	VDDQ
C	○	○	○	○	○	○	○
D	NC	SE2	SA	ADV	SA	SE3	NC
E	○	○	○	○	○	○	○
F	NC	SA	SA	VDD	SA	SA	NC
G	○	○	○	○	○	○	○
H	DQc	DQc	VSS	NC	VSS	DQb	DQb
J	○	○	○	○	○	○	○
K	DQc	DQc	VSS	SET	VSS	DQb	DQb
L	○	○	○	○	○	○	○
M	VDDQ	DQc	VSS	G	VSS	DQb	VDDQ
N	○	○	○	○	○	○	○
P	DQc	DQc	SBC	SA	SBB	DQb	DQb
R	○	○	○	○	○	○	○
T	DQc	DQc	VSS	SW	VSS	DQb	DQb
U	○	○	○	○	○	○	○
	VDDQ	VDD	VDD	VDD	FT	VDD	VDDQ
	○	○	○	○	○	○	○
	DQd	DQd	VSS	CK	VSS	DQa	DQa
	○	○	○	○	○	○	○
	DQd	DQd	SBD	NC	SBA	DQa	DQa
	○	○	○	○	○	○	○
	VDDQ	DQd	VSS	CKE	VSS	DQa	VDDQ
	○	○	○	○	○	○	○
	DQd	DQd	VSS	SA1	VSS	DQa	DQa
	○	○	○	○	○	○	○
	DQd	DQd	VSS	SA0	VSS	DQa	DQa
	○	○	○	○	○	○	○
	VDD	SA	LBO	VDD	FT	SA	NC
	○	○	○	○	○	○	○
	NC	NC	SA	SA	SA	NC	VSS
	○	○	○	○	○	○	○
	VDDQ	TMS	TDI	TCK	TDO	TRST	VDDQ

100-PIN TQFP  
TOP VIEW

119-BUMP PGBA  
TOP VIEW

Not to Scale

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## MCM64Z836 TQFP PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	ADV	Input	Synchronous Load/Advance: Loads a new address into counter when low. RAM uses internally generated burst addresses when high.
89	CK	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$ .
87	$\overline{CKE}$	Input	Clock Enable: Disables the CK input when $\overline{CKE}$ is high.
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
14, 66	$\overline{FT}$	Input	Flow-Through Option Input: This pin must remain in steady state (this signal is not registered or latched). It must be tied high or low. Low — flow-through functionality. High — pipelined functionality.
86	$\overline{G}$	Input	Asynchronous Output Enable.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter. High — interleaved burst counter.
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 81, 82, 83, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
37, 36	SA0, SA1	Input	Synchronous Burst Address Inputs: The two LSB's of the address field. These pins must preset the burst address counter values. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: Enables write to byte "x" (byte a, b, c, d) in conjunction with $\overline{SW}$ . Has no effect on read cycles.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins.
15, 16, 41, 65, 91	VDD	Supply	Core Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	VDDQ	Supply	I/O Power Supply.
5, 10, 17, 21, 26, 40, 55, 60, 64, 67, 71, 76, 90	VSS	Supply	Ground.
38, 39, 42, 43, 84	NC	—	No Connection: There is no connection to the chip.

## MCM64Z836 PBGA PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
4B	ADV	Input	Synchronous Load/Advance: Loads a new address into counter when low. RAM uses internally generated burst addresses when high.
4K	CK	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$ .
4M	$\overline{CKE}$	Input	Clock Enable: Disables the CK input when $\overline{CKE}$ is high.
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
5J, 5R	$\overline{FT}$	Input	Flow-Through Option Input: This pin must remain in steady state (this signal is not registered or latched). It must be tied high or low. Low — flow-through functionality. High — pipelined functionality.
4F	$\overline{G}$	Input	Asynchronous Output Enable.
3R	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter. High — interleaved burst counter.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4G, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
4N, 4P	SA1, SA0	Input	Synchronous Burst Address Inputs: The two LSBs of the address field. These pins must preset the burst address counter values. These inputs are registered and must meet setup and hold times.
5L, 5G, 3G, 3L (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: Enables write to byte "x" (byte a, b, c, d) in conjunction with $\overline{SW}$ . Has no effect on read cycles.
4E	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip.
2B	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
6B	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
4H	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins.
4U	TCK	Input	Boundary Scan Pin, Test Clock: If boundary scan is not used, TCK must be tied to $V_{DD}$ or $V_{SS}$ .
3U	TDI	Input	Boundary Scan Pin, Test Data In.
5U	TDO	Output	Boundary Scan Pin, Test Data Out.
2U	TMS	Input	Boundary Scan Pin, Test Mode Select.
6U	$\overline{TRST}$	Input	Boundary Scan Pin, Asynchronous Test Reset. If boundary scan is not used, $\overline{TRST}$ must be tied to $V_{SS}$ .
4C, 2J, 3J, 4J, 6J, 1R, 4R	$V_{DD}$	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	$V_{DDQ}$	Supply	I/O Power Supply.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 7T	$V_{SS}$	Supply	Ground.
4A, 1B, 7B, 1C, 7C, 4D, 7R, 1T, 2T, 6T	NC	—	No Connection: There is no connection to the chip.



## MCM64Z918 TQFP PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	ADV	Input	Synchronous Load/Advance: Loads a new address into counter when low. RAM uses internally generated burst addresses when high.
89	CK	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$ .
87	$\overline{CKE}$	Input	Clock Enable: Disables the CK input when $\overline{CKE}$ is high.
(a) 58, 59, 62, 63, 68, 69, 72, 73, 74 (b) 8, 9, 12, 13, 18, 19, 22, 23, 24	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b).
14, 66	$\overline{FT}$	Input	Flow-Through Option Input: This pin must remain in steady state (this signal is not registered or latched). It must be tied high or low. Low — flow-through functionality. High — pipelined functionality.
86	$\overline{G}$	Input	Asynchronous Output Enable.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter. High — interleaved burst counter.
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 80, 81, 82, 83, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
37, 36	SA0, SA1	Input	Synchronous Burst Address Inputs: The two LSB's of the address field. These pins must preset the burst address counter values. These inputs are registered and must meet setup and hold times.
93, 94 (a) (b)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: Enables write to byte "x" (byte a, b) in conjunction with $\overline{SW}$ . Has no effect on read cycles.
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins.
15, 16, 41, 65, 91	VDD	Supply	Core Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	VDDQ	Supply	I/O Power Supply.
5, 10, 17, 21, 26, 40, 55, 60, 64, 67, 71, 76, 90	VSS	Supply	Ground.
1, 2, 3, 6, 7, 25, 28, 29, 30, 38, 39, 42, 43, 51, 52, 53, 56, 57, 75, 78, 79, 84, 95, 96	NC	—	No Connection: There is no connection to the chip.

## MCM64Z918 PBGA PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
4B	ADV	Input	Synchronous Load/Advance: Loads a new address into counter when low. RAM uses internally generated burst addresses when high.
4K	CK	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$ .
4M	$\overline{CKE}$	Input	Clock Enable: Disables the CK input when $\overline{CKE}$ is high.
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b).
5J, 5R	$\overline{FT}$	Input	Flow-Through Option Input: This pin must remain in steady state (this signal is not registered or latched). It must be tied high or low. Low — flow-through functionality. High — pipelined functionality.
4F	$\overline{G}$	Input	Asynchronous Output Enable.
3R	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter. High — interleaved burst counter.
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4G, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
4N, 4P	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
5L, 3G (a) (b)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: Enables write to byte "x" (byte a, b) in conjunction with $\overline{SW}$ . Has no effect on read cycles.
4E	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip.
2B	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
6B	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
4H	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins.
4U	TCK	Input	Boundary Scan Pin, Test Clock: If boundary scan is not used, TCK must be tied to $V_{DD}$ or $V_{SS}$ .
3U	TDI	Input	Boundary Scan Pin, Test Data In.
5U	TDO	Output	Boundary Scan Pin, Test Data Out.
2U	TMS	Input	Boundary Scan Pin, Test Mode Select.
6U	$\overline{TRST}$	Input	Boundary Scan Pin, Asynchronous Test Reset. If boundary scan is not used, $\overline{TRST}$ must be tied to $V_{SS}$ .
4C, 2J, 3J, 4J, 6J, 1R, 4R	$V_{DD}$	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	$V_{DDQ}$	Supply	I/O Power Supply.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 7T	$V_{SS}$	Supply	Ground.
4A, 1B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 1K, 6K, 2L, 4L, 7L, 6M, 2N, 7N, 1P, 6P, 7R, 1T, 4T	NC	—	No Connection: There is no connection to the chip.



**TRUTH TABLE**

CK	$\overline{\text{CKE}}$	E	$\overline{\text{SW}}$	$\overline{\text{SBx}}$	ADV	SA0 – SAx	Next Operation	Input Command Code	Notes
L–H	1	X	X	X	X	X	Hold	H	1, 2
L–H	0	False	X	X	0	X	Deselect	D	1, 2
L–H	0	True	0	V	0	V	Load Address, New Write	W	1, 2, 3, 4, 5
L–H	0	True	1	X	0	V	Load Address, New Read	R	1, 2
L–H	0	X	X	V (W)	1	X	Burst	B	1, 2, 4, 6, 7
				X (R, D)			Continue		

**NOTES:**

1. X = don't care, 1 = logic high, 0 = logic low, V = valid signal, according to AC Operating Conditions and Characteristics.
2. E = true if SE1 and SE3 = 0, and SE2 = 1.
3. Byte write enables,  $\overline{\text{SBx}}$  are evaluated only as new write addresses are loaded.
4. No control inputs except  $\overline{\text{CKE}}$ ,  $\overline{\text{SBx}}$ , and ADV are recognized in a clock cycle where ADV is sampled high.
5. A write with  $\overline{\text{SBx}}$  not valid does load addresses.
6. A burst write with  $\overline{\text{SBx}}$  not valid does increment address.
7. ADV controls whether the RAM enters burst mode. If the previous cycle was a write, then ADV = 1 results in a burst write. If the previous cycle is a read, then ADV = 1 results in a burst read. ADV = 1 will also continue a deslect cycle.

**ASYNCHRONOUS TRUTH TABLE**

Operation	$\overline{\text{G}}$	I/O Status
Read	L	Data Out (DQx)
Read	H	High-Z
Write	X	High-Z
Deselected	X	High-Z

**WRITE TRUTH TABLE**

Cycle Type	$\overline{\text{SW}}$	$\overline{\text{SBa}}$	$\overline{\text{SBb}}$	$\overline{\text{SBc}}$ (See Note 1)	$\overline{\text{SBd}}$ (See Note 1)
Read	H	X	X	X	X
Write Byte a	L	L	H	H	H
Write Byte b	L	H	L	H	H
Write Byte c (See Note 1)	L	H	H	L	H
Write Byte d (See Note 1)	L	H	H	H	L
Write All Bytes	L	L	L	L	L

**NOTE:**

1. Valid only for the MCM64Z836.

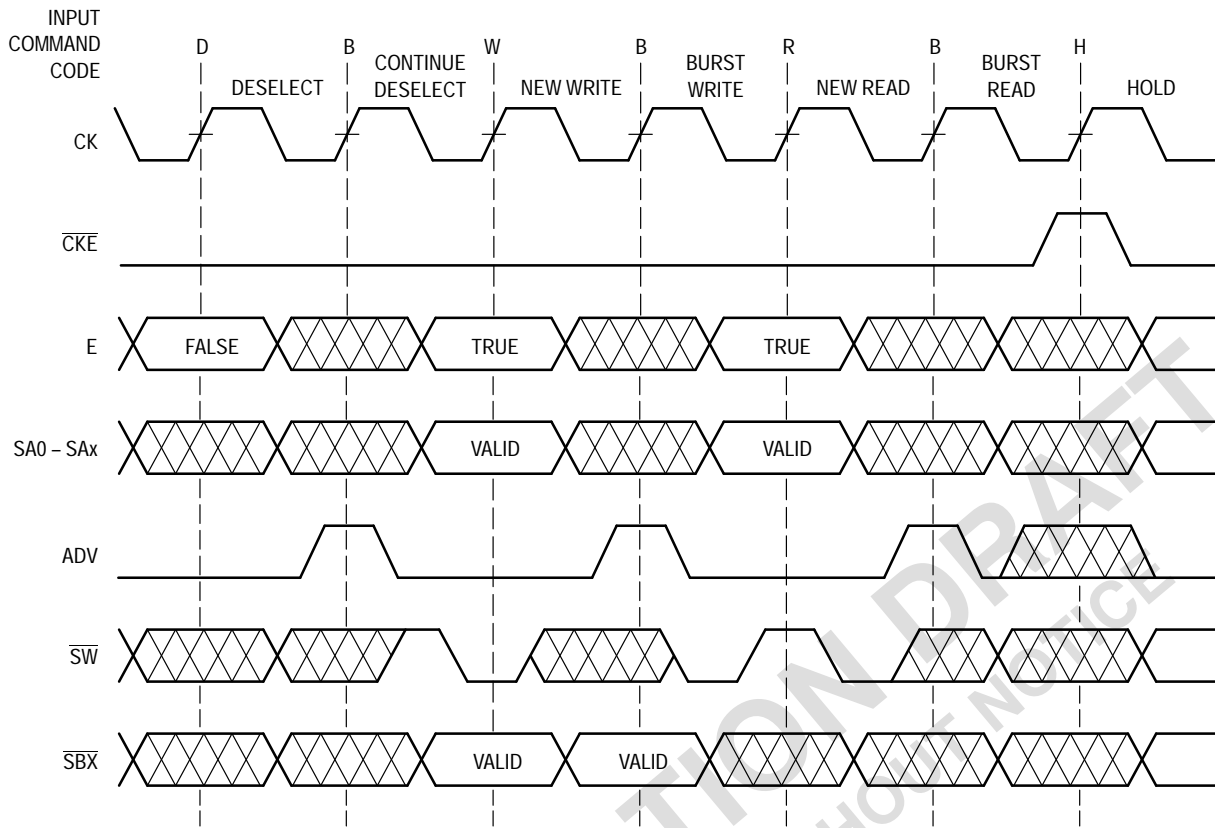
**LINEAR BURST ADDRESS TABLE ( $\overline{\text{LBO}} = V_{SS}$ )**

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X ... X00	X ... X01	X ... X10	X ... X11
X ... X01	X ... X10	X ... X11	X ... X00
X ... X10	X ... X11	X ... X00	X ... X01
X ... X11	X ... X00	X ... X01	X ... X10

**INTERLEAVED BURST ADDRESS TABLE ( $\overline{\text{LBO}} = V_{DD}$ )**

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X ... X00	X ... X01	X ... X10	X ... X11
X ... X01	X ... X00	X ... X11	X ... X10
X ... X10	X ... X11	X ... X00	X ... X01
X ... X11	X ... X10	X ... X01	X ... X00

**INPUT COMMAND CODE AND STATE NAME DEFINITION DIAGRAM**



NOTE: Cycles are named for their control inputs, not for data I/O state.

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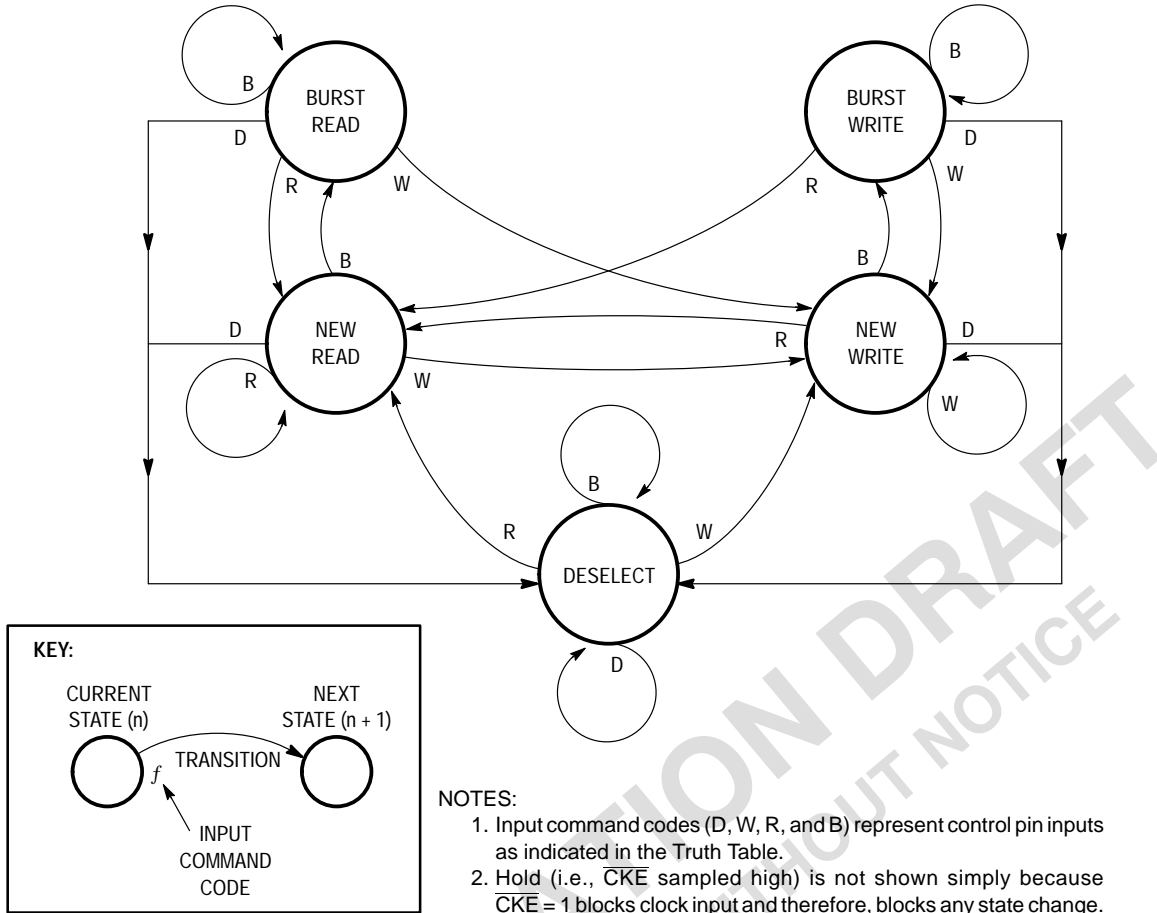
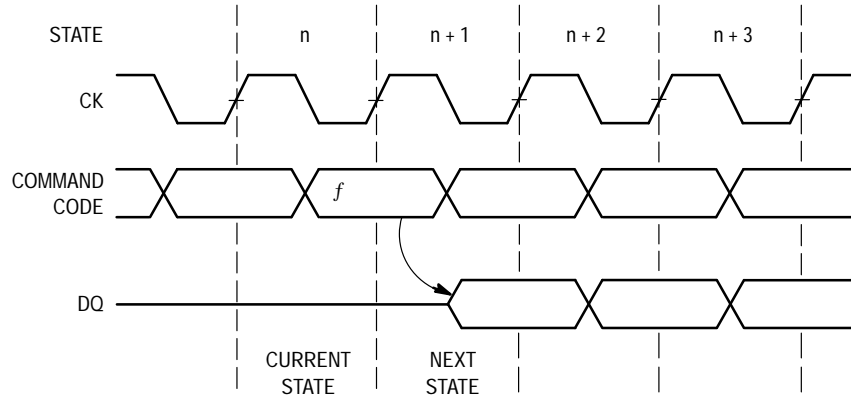
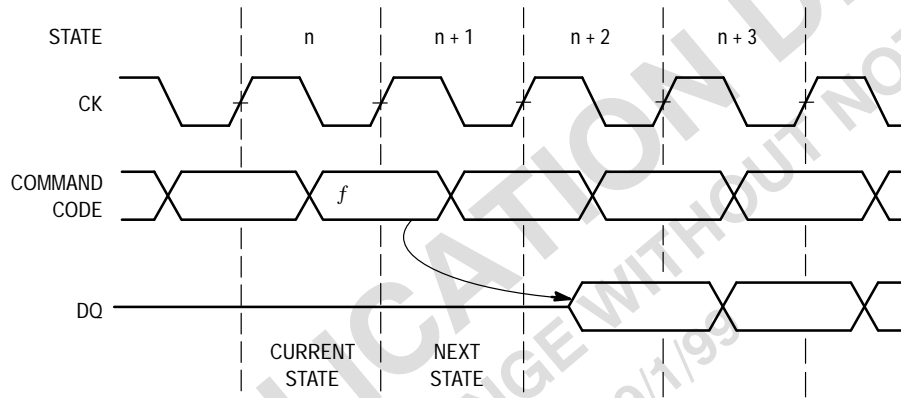


Figure 1. ZBT RAM State Diagram

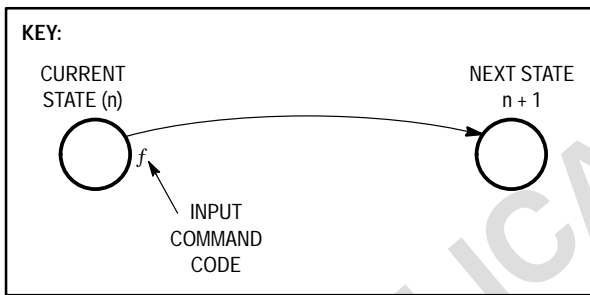
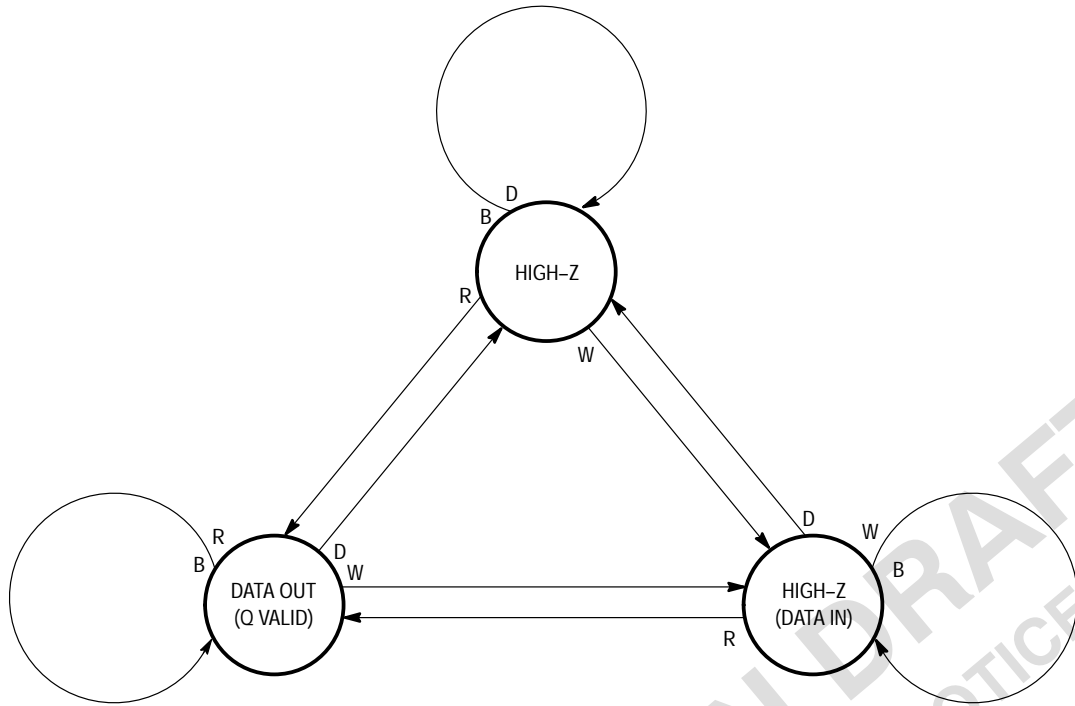


**Figure 2. State Definitions for ZBT RAM State Diagram (Flow-Through)**



**Figure 3. State Definitions for ZBT RAM State Diagram (Pipelined)**

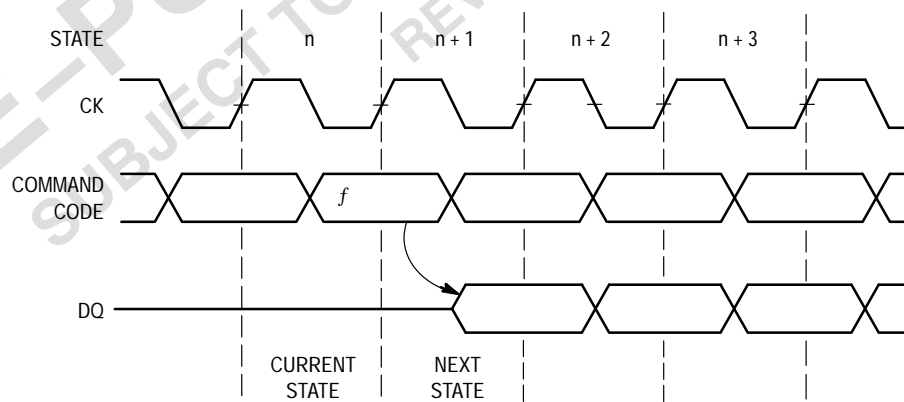
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**NOTES:**

1. Input command codes (D, W, R, and B) represent control pin inputs as indicated in the Truth Table.
2. Hold (i.e.,  $\overline{CKE}$  sampled high) is not shown simply because  $\overline{CKE} = 1$  blocks clock input and therefore, blocks any state change.

**Figure 4. Data I/O State Diagram (Flow-Through)**



**Figure 5. State Definitions for ZBT RAM State Diagram (Flow-Through)**

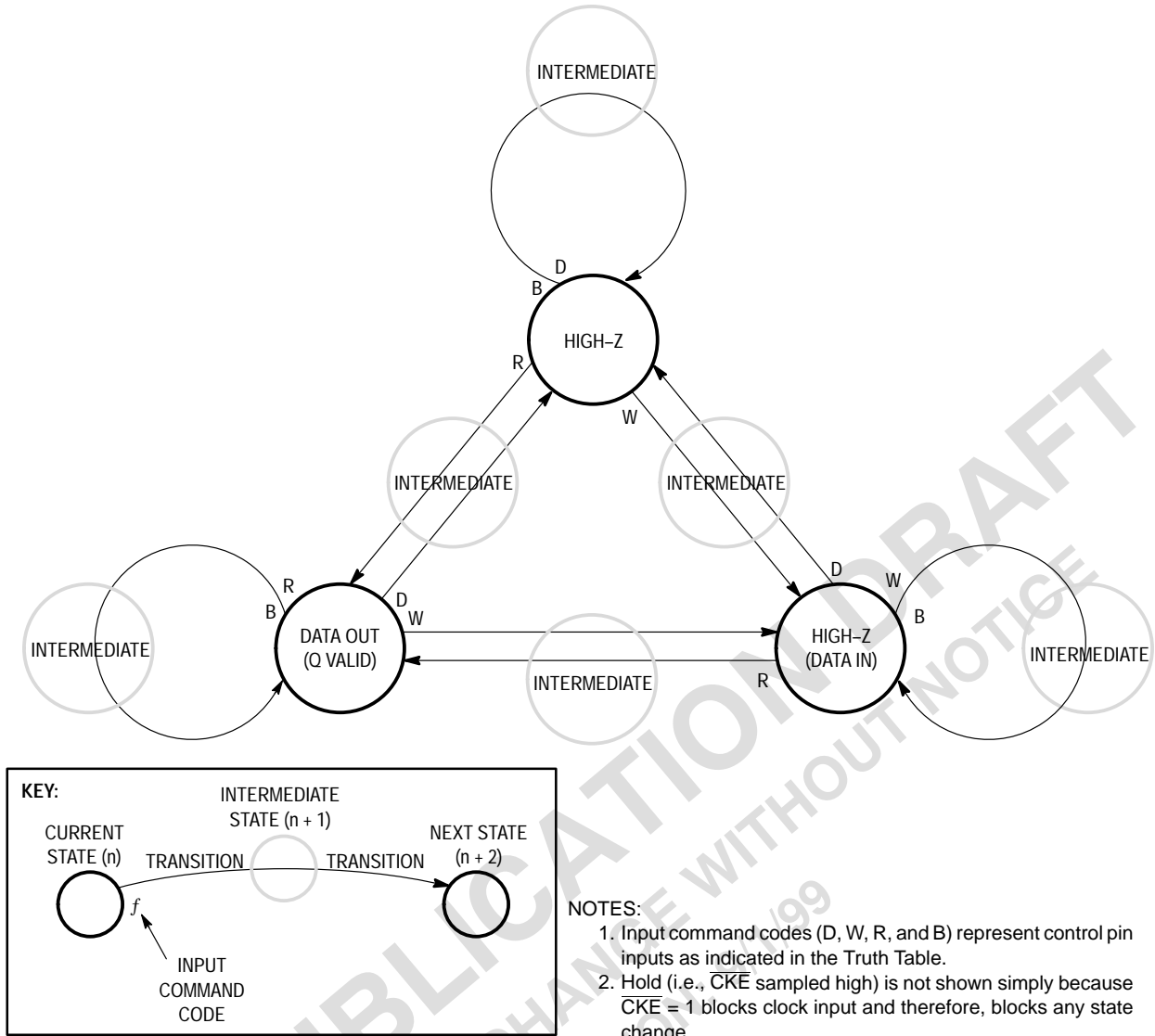


Figure 6. Data I/O State Diagram (Pipelined)

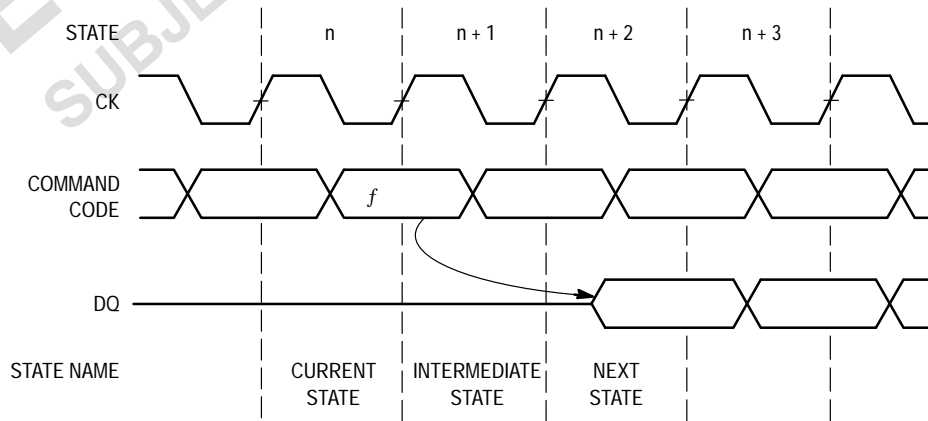


Figure 7. State Definitions for I/O State Diagram (Pipelined)

## ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit	Notes
Power Supply Voltage	$V_{DD}$	-0.5 to 3.6	V	
I/O Supply Voltage	$V_{DDQ}$	$V_{SS} - 0.5$ to $V_{DD}$	V	2
Input Voltage Relative to $V_{SS}$ for Any Pin Except $V_{DD}$	$V_{in}, V_{out}$	-0.5 to $V_{DD} + 0.5$	V	2
Input Voltage (Three State I/O)	$V_{IT}$	$V_{SS} - 0.5$ to $V_{DDQ} + 0.5$	V	2
Output Current (per I/O)	$I_{out}$	$\pm 20$	mA	
Package Power Dissipation	$P_D$	1.3	W	3
Temperature Under Bias	$T_{bias}$	-10 to 85	$^{\circ}C$	
Storage Temperature	$T_{stg}$	-55 to 125	$^{\circ}C$	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

### NOTES:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This is a steady-state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing is not necessary.
3. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

## PACKAGE THERMAL CHARACTERISTICS

Thermal Resistance	Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	$R_{\theta JA}$	40 25	$^{\circ}C/W$	1, 2
Junction to Board (Bottom)	$R_{\theta JB}$	17	$^{\circ}C/W$	3
Junction to Case (Top)	$R_{\theta JC}$	9	$^{\circ}C/W$	4

### NOTES:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38-87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC-883 Method 1012.1).

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## DC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{DD} = 2.5 \text{ V} \pm 200 \text{ mV}$ ,  $T_A = 0 \text{ to } 70^\circ\text{C}$  Unless Otherwise Noted)

### RECOMMENDED OPERATING CONDITIONS AND DC CHARACTERISTICS (Voltages Referenced to $V_{SS} = 0 \text{ V}$ )

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{DD}$	2.3	2.5	2.7	V
I/O Supply Voltage	$V_{DDQ}$	2.3	2.5	$V_{DD}$	V
Input Low Voltage	$V_{IL}$	-0.3	—	0.7	V
Input High Voltage	$V_{IH}$	1.7	—	$V_{DD} + 0.3$	V
Input High Voltage I/O Pins	$V_{IH2}$	1.7	—	$V_{DDQ} + 0.3$	V
Output Low Voltage ( $I_{OL} = 2 \text{ mA}$ )	$V_{OL}$	—	—	0.7	V
Output High Voltage ( $I_{OH} = -2 \text{ mA}$ )	$V_{OH}$	1.7	—	—	V

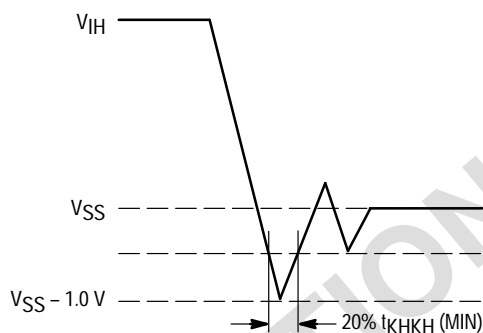


Figure 8. Undershoot Voltage

### DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input Leakage Current ( $0 \text{ V} \leq V_{in} \leq V_{DD}$ )	$I_{lkg(I)}$	—	—	$\pm 1$	$\mu\text{A}$	1
Output Leakage Current ( $0 \text{ V} \leq V_{in} \leq V_{DDQ}$ )	$I_{lkg(O)}$	—	—	$\pm 1$	$\mu\text{A}$	
AC Supply Current (Device Selected, All Outputs Open, Freq = Max) Includes Supply Current for Both $V_{DD}$ and $V_{DDQ}$	$I_{DDA-7}$ $I_{DDA-8}$ $I_{DDA-8.5}$	—	—	270/300 250/290 250/280	mA	2, 3, 4, 5
CMOS Standby Supply Current (Device Deselected, Freq = 0, $V_{DD} = \text{Max}$ , $V_{DDQ} = \text{Max}$ , All Inputs Static at CMOS Levels)	$I_{SB2}$	—	—	10	mA	6, 7
Clock Running (Device Deselected, Freq = Max, $V_{DD} = \text{Max}$ , All Inputs Toggling at CMOS Levels)	$I_{SB4-7}$ $I_{SB4-8}$ $I_{SB4-8.5}$	—	—	100/100 100/100 90/90	mA	5, 6, 8
Hold Supply Current (Device Selected, Freq = Max, $V_{DD} = \text{Max}$ , $V_{DDQ} = \text{Max}$ , $CKE \geq V_{DD} - 0.2 \text{ V}$ , All Inputs Static at CMOS Levels)	$I_{DD1}$	—	—	15	mA	7

NOTES:

1. LBO has an internal pull-up will exhibit leakage currents of  $\pm 5 \mu\text{A}$ .
2. Reference AC Operating Conditions and Characteristics for input and timing.
3. All addresses transition simultaneously low (LSB) then high (MSB).
4. Data states are all zero.
5. Flow-through/pipelined current.
6. Device in deselected mode as defined by the Truth Table.
7. CMOS levels for I/Os are  $V_{IT} \leq V_{SS} + 0.2 \text{ V}$  or  $\geq V_{DDQ} - 0.2 \text{ V}$ . CMOS levels for other inputs are  $V_{in} \leq V_{SS} + 0.2 \text{ V}$  or  $\geq V_{DD} - 0.2 \text{ V}$ .
8. TTL levels for I/Os are  $V_{IT} \leq V_{IL}$  or  $\geq V_{IH2}$ . TTL levels for other inputs are  $V_{in} \leq V_{IL}$  or  $\geq V_{IH}$ .



**CAPACITANCE** (f = 1.0 MHz, T<sub>A</sub> = 0 to 70°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C <sub>in</sub>	—	2	4	pF
Input/Output Capacitance	C <sub>I/O</sub>	—	3	5	pF

## AC OPERATING CONDITIONS AND CHARACTERISTICS

(V<sub>DD</sub> = 2.5 V ±5%, T<sub>A</sub> = 0 to 70°C Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.25 V  
 Input Pulse Levels ..... 0 to 2.5 V  
 Input Rise/Fall Time (Flow-Through) ..... 1.0 V/ns (20% to 80%)  
 Input Rise/Fall Time (Pipelined) ..... 2.5 V/ns (20% to 80%)  
 Output Timing Reference Level ..... 1.25 V  
 Output Load ..... See Figure 9 Unless Otherwise Noted

## FLOW-THROUGH READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM64Z836-7 MCM64Z918-7		MCM64Z836-8 MCM64Z918-8		MCM64Z836-8.5 MCM64Z918-8.5		Unit	Notes	
		Min	Max	Min	Max	Min	Max			
Cycle Time	t <sub>KHKH</sub>	8.5	—	10.5	—	11	—	ns		
Clock High Pulse Width	t <sub>KHKL</sub>	3.4	—	4.2	—	4.4	—	ns	3	
Clock Low Pulse Width	t <sub>KLKH</sub>	3.4	—	4.2	—	4.4	—	ns	3	
Clock Access Time	t <sub>KHQP</sub>	—	7	—	8	—	8.5	ns		
Output Enable to Output Valid	t <sub>GLQV</sub>	—	3.5	—	3.5	—	5	ns		
Clock High to Output Active	t <sub>KHQX1</sub>	4	—	4	—	4	—	ns	4, 5	
Output Hold Time	t <sub>KHQX</sub>	2	—	2	—	2	—	ns	4	
Output Enable to Output Active	t <sub>GLQX</sub>	0	—	0	—	0	—	ns	4, 5	
Output Disable to Q High-Z	t <sub>GHQZ</sub>	—	3.5	—	3.5	—	5	ns	4, 5	
Clock High to Q High-Z	t <sub>KHQZ</sub>	1.5	3.5	1.5	4	1.5	4	ns	4, 5	
Setup Times:	Address	t <sub>ADKH</sub>	1.5	—	1.5	—	2	—	ns	
	ADV	t <sub>LVKH</sub>	1.5	—	1.5	—	2	—	ns	
	Data In	t <sub>DVKH</sub>	1.5	—	1.5	—	2	—	ns	
	Write	t <sub>WVKH</sub>	1.5	—	1.5	—	2	—	ns	
	Chip Enable	t <sub>EVKH</sub>	1.5	—	1.5	—	2	—	ns	
	Clock Enable	t <sub>CVKH</sub>	1.5	—	1.5	—	2	—	ns	
Hold Times:	Address	t <sub>KHAX</sub>	0.5	—	0.5	—	0.5	—	ns	
	ADV	t <sub>KHLX</sub>	—	—	—	—	—	—	ns	
	Data In	t <sub>KHDX</sub>	—	—	—	—	—	—	ns	
	Write	t <sub>KHWX</sub>	—	—	—	—	—	—	ns	
	Chip Enable	t <sub>KHEX</sub>	—	—	—	—	—	—	ns	
	Clock Enable	t <sub>KHCX</sub>	—	—	—	—	—	ns		

**NOTES:**

1. Write is defined as any  $\overline{SBx}$  and  $\overline{SW}$  low. Chip enable is defined as  $\overline{SE1}$  low,  $\overline{SE2}$  high, and  $\overline{SE3}$  low whenever ADV is low.
2. All read and write cycle timings are referenced from CK or  $\overline{G}$ .
3. In order to reduce test correlation issues and to reduce the effects of application specific input edge rate variations on correlation between data sheet parameters and actual system performance, FSRAM AC parametric specifications are always specified at V<sub>DDQ</sub>/2. In some design exercises, it is desirable to evaluate timing using other reference levels. Since the maximum test input edge rate is known and is given in the AC Test Conditions section of the data sheet as 1 V/ns, one can easily interpolate timing values to other reference levels.
4. This parameter is sampled and not 100% tested.
5. Measured at ±200 mV from steady state.

## PIPELINED READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM64Z836-7 MCM64Z918-7 225 MHz		MCM64Z836-8 MCM64Z918-8 200 MHz		MCM64Z836-8.5 MCM64Z918-8.5 166 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t <sub>KHKH</sub>	4.4	—	5	—	6	—	ns	
Clock High Pulse Width	t <sub>KHKL</sub>	1.7	—	2	—	2.4	—	ns	3
Clock Low Pulse Width	t <sub>KLKH</sub>	1.7	—	2	—	2.4	—	ns	3
Clock Access Time	t <sub>KHQV</sub>	—	2.6	—	3	—	3.5	ns	
Output Enable to Output Valid	t <sub>GLQV</sub>	—	2.6	—	3	—	3.5	ns	
Clock High to Output Active	t <sub>KHQX1</sub>	0.8	—	0.8	—	0.8	—	ns	4, 5
Output Hold Time	t <sub>KHQX</sub>	0.7	—	0.7	—	0.7	—	ns	4
Output Enable to Output Active	t <sub>GLQX</sub>	0	—	0	—	0	—	ns	4, 5
Output Disable to Q High-Z	t <sub>GHQZ</sub>	—	2.3	—	3	—	3.5	ns	4, 5
Clock High to Q High-Z	t <sub>KHQZ</sub>	0.8	2.4	1	2.5	1	3	ns	4, 5
Setup Times:									
Address	t <sub>ADKH</sub>	1.3	—	1.3	—	1.3	—	ns	
ADV	t <sub>LVKH</sub>	1.3	—	1.3	—	1.3	—	ns	
Data In	t <sub>DVKH</sub>	1.2	—	1.2	—	1.2	—	ns	
Write	t <sub>WVKH</sub>	1.3	—	1.3	—	1.3	—	ns	
Chip Enable	t <sub>EVKH</sub>	1.3	—	1.3	—	1.3	—	ns	
Clock Enable	t <sub>CVKH</sub>	1.3	—	1.3	—	1.3	—	ns	
Hold Times:									
Address	t <sub>KHAX</sub>	0.5	—	0.5	—	0.5	—	ns	
ADV	t <sub>KHLX</sub>	—	—	—	—	—	—	ns	
Data In	t <sub>KHDX</sub>	—	—	—	—	—	—	ns	
Write	t <sub>KHWX</sub>	—	—	—	—	—	—	ns	
Chip Enable	t <sub>KHEX</sub>	—	—	—	—	—	—	ns	
Clock Enable	t <sub>KHCX</sub>	—	—	—	—	—	—	ns	

### NOTES:

1. Write is defined as any  $\overline{SBx}$  and  $\overline{SW}$  low. Chip Enable is defined as  $\overline{SE1}$  low,  $SE2$  high, and  $\overline{SB3}$  low whenever  $ADV$  is low.
2. All read and write cycle timings are referenced from  $CK$  or  $\overline{G}$ .
3. In order to reduce test correlation issues and to reduce the effects of application specific input edge rate variations on correlation between data sheet parameters and actual system performance, FSRAM AC parametric specifications are always specified at  $V_{DDQ}/2$ . In some design exercises, it is desirable to evaluate timing using other reference levels. Since the maximum test input edge rate is known and is given in the AC test conditions section of the data sheet as 2.5 V/ns, one can easily interpolate timing values to other reference levels.
4. This parameter is sampled and not 100% tested.
5. Measured at  $\pm 200$  mV from steady state.

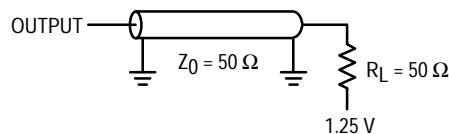


Figure 9. AC Test Loads

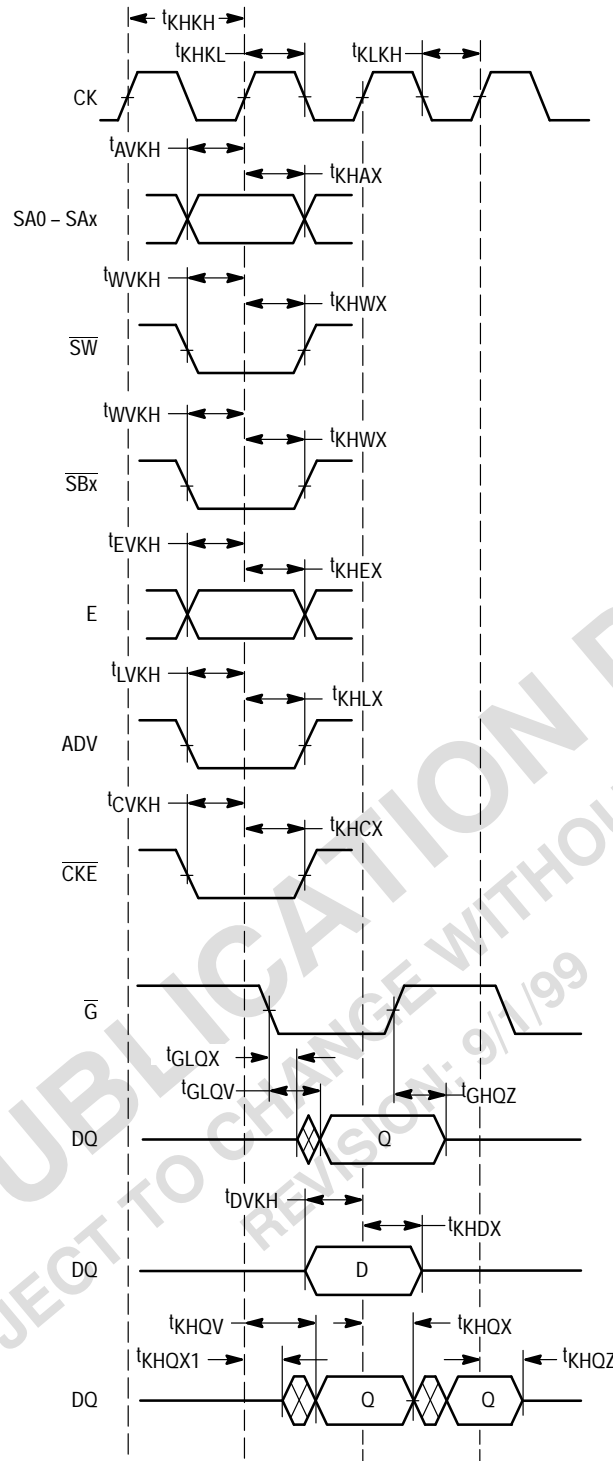
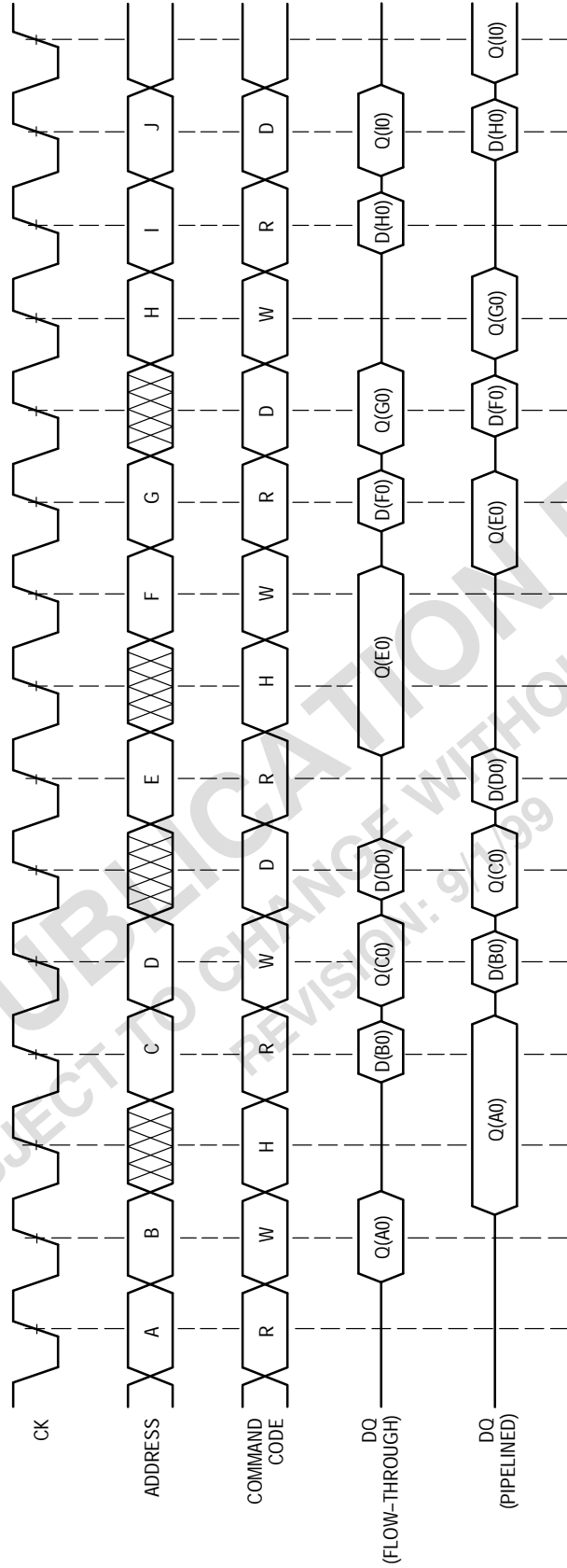


Figure 10. AC Timing Parameter Definitions (Flow-Through)

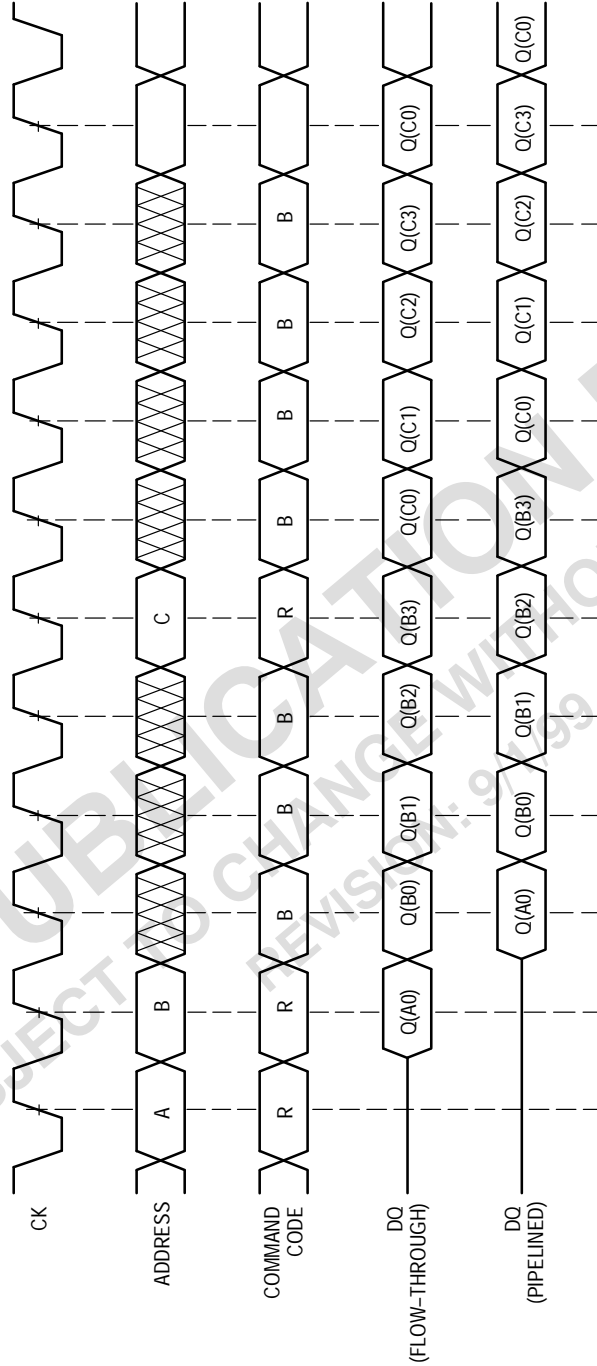


READ/WRITE CYCLES WITH HOLD AND DESELECT CYCLES



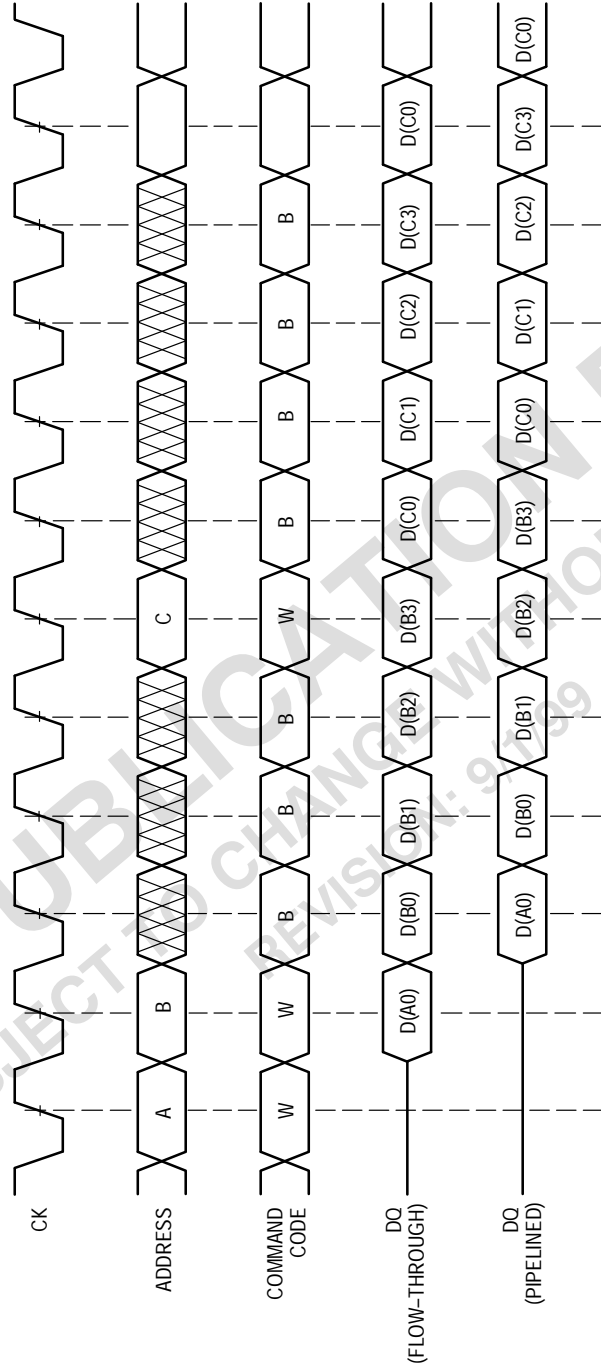
NOTE: Command code definitions are shown in Truth Table.

READ CYCLES (SINGLE, BURST, AND BURST WRAP-AROUND)



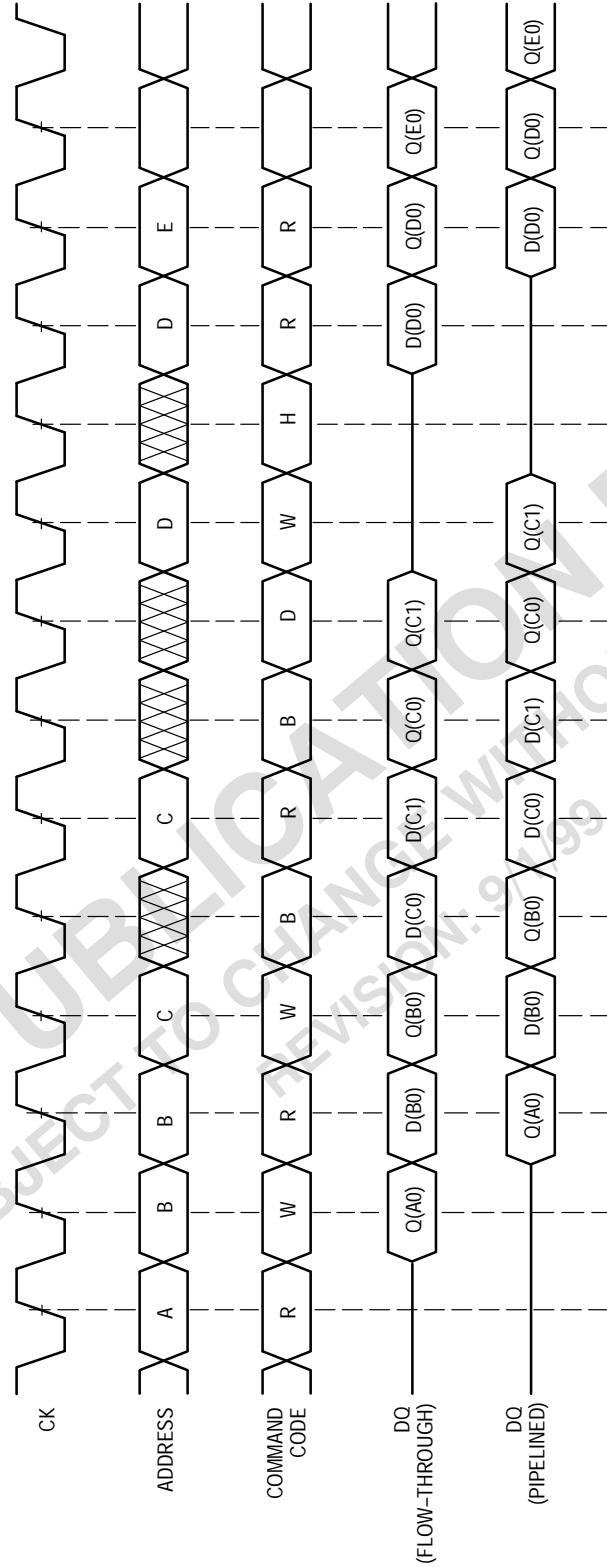
NOTE: Command code definitions are shown in Truth Table.

WRITE CYCLES (SINGLE, BURST, AND BURST WRAP-AROUND)



NOTE: Command code definitions are shown in Truth Table.

READ, WRITE, READ COHERENCY WITH HOLD, AND DESELECT CYCLES



NOTE: Command code definitions are shown in Truth Table.



## SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

### OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for IEEE 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture (the TAP controller is the state machine that controls the

TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with IEEE Standard 1149.1 compliant TAPs. The TAP operates using a 2.5 V tolerant logic level signaling.

### DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfering with normal operation of the device,  $\overline{\text{TRST}}$  should be tied low and TCK, TDI, and TMS should be pulled through a resistor to 2.5 V. TDO should be left unconnected.

### TAP DC OPERATING CHARACTERISTICS

( $T_A = 0$  to  $70^\circ\text{C}$ , Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Notes
Input Logic Low	$V_{IL1}$	-0.5	0.7	V	
Input Logic High	$V_{IH1}$	1.7	3	V	
Input Leakage Current	$I_{lkg}$	—	$\pm 10$	$\mu\text{A}$	1
Output Logic Low	$V_{OL1}$	—	0.7	V	2
Output Logic High	$V_{OH1}$	1.7	—	V	

#### NOTES:

- $0\text{ V} \leq V_{in} \leq V_{DDQ}$  for all logic input pins.
- For  $V_{OL} = 0.4\text{ V}$ ,  $14\text{ mA} \leq I_{OL} \leq 28\text{ mA}$ .

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## TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(T<sub>A</sub> = 0 to 70°C, Unless Otherwise Noted)

### AC TEST CONDITIONS

Parameter	Value	Unit
Input Timing Reference Level	1.25	V
Input Pulse Levels	0 to 2.5	V
Input Rise/Fall Time (20% to 80%)	1	V/ns
Output Timing Reference Level	1.25	V
Output Load (See Figure 6 Unless Otherwise Noted)	—	—

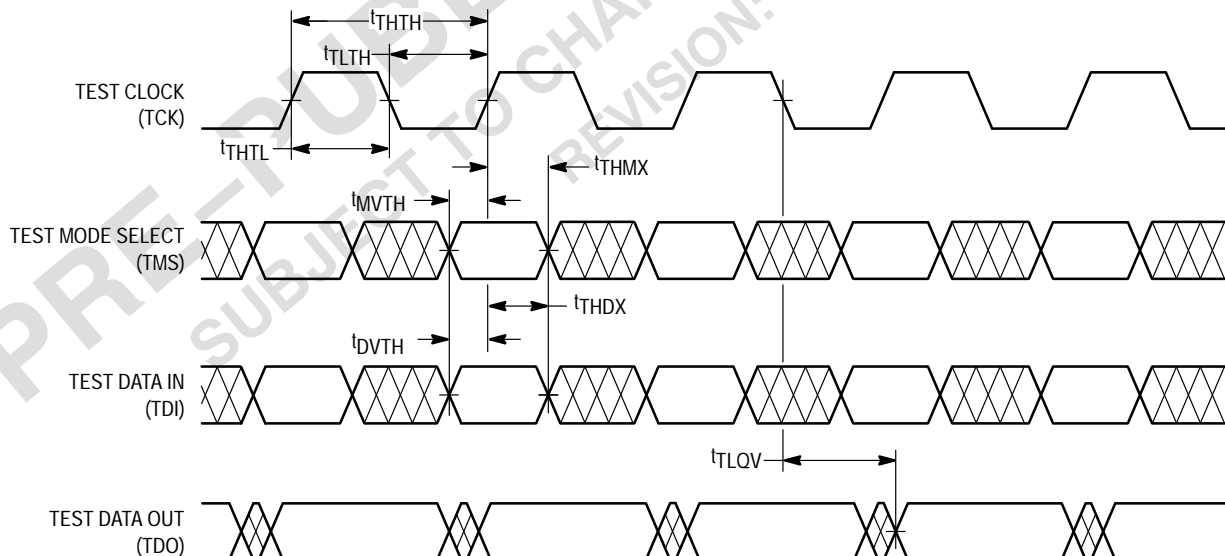
### TAP CONTROLLER TIMING

Parameter	Symbol	Min	Max	Unit	Notes	
TCK Cycle Time	t <sub>THTH</sub>	60	—	ns		
TCK Clock High Time	t <sub>TH</sub>	25	—	ns		
TCK Clock Low Time	t <sub>TL</sub>	25	—	ns		
TDO Access Time	t <sub>TLQV</sub>	1	10	ns		
TRST Pulse Width	t <sub>SRT</sub>	40	—	ns		
Setup Times	Capture	t <sub>CS</sub>	5	—	ns	1
	TDI	t <sub>DVTH</sub>	5	—	ns	
	TMS	t <sub>MVTH</sub>	5	—	ns	
Hold Times	Capture	t <sub>CH</sub>	13	—	ns	1
	TDI	t <sub>THDX</sub>	14	—	ns	
	TMS	t <sub>THMX</sub>	14	—	ns	

NOTE:

- t<sub>CS</sub> and t<sub>CH</sub> define the minimum pauses in RAM I/O transitions to assure accurate pad data capture.

### TAP CONTROLLER TIMING DIAGRAM



## MCM64Z836 BOUNDARY SCAN ORDER

Bit No.	Signal Name	Bump ID
1	SA	TBD
2	SA	TBD
3	SA	TBD
4	SA	TBD
5	SA	TBD
6	SA	TBD
7	SA	TBD
8	DQa	TBD
9	DQa	TBD
10	DQa	TBD
11	DQa	TBD
12	DQa	TBD
13	DQa	TBD
14	DQa	TBD
15	DQa	TBD
16	DQa	TBD
17	VSS	TBD
18	DQb	TBD
19	DQb	TBD
20	DQb	TBD
21	DQb	TBD
22	DQb	TBD
23	DQb	TBD
24	DQb	TBD
25	DQb	TBD
26	DQb	TBD
27	SA	TBD
28	SA	TBD
29	SA	TBD
30	ADV	TBD
31	$\bar{G}$	TBD
32	$\bar{CKE}$	TBD
33	$\bar{SW}$	TBD
34	$\bar{CK}$	TBD
35	SE3	TBD

Bit No.	Signal Name	Bump ID
36	$\bar{SBa}$	TBD
37	$\bar{SEb}$	TBD
38	$\bar{SBc}$	TBD
39	$\bar{SBd}$	TBD
40	SE2	TBD
41	$\bar{SE1}$	TBD
42	SA	TBD
43	SA	TBD
44	DQc	TBD
45	DQc	TBD
46	DQc	TBD
47	DQc	TBD
48	DQc	TBD
49	DQc	TBD
50	DQc	TBD
51	DQc	TBD
52	DQc	TBD
53	VDD	TBD
54	DQd	TBD
55	DQd	TBD
56	DQd	TBD
57	DQd	TBD
58	DQd	TBD
59	DQd	TBD
60	DQd	TBD
61	DQd	TBD
62	DQd	TBD
63	LBO	TBD
64	SA	TBD
65	SA	TBD
66	SA	TBD
67	SA	TBD
68	SA1	TBD
69	SA0	TBD

**MCM64Z918 BOUNDARY SCAN ORDER**

Bit No.	Signal Name	Bump ID
1	SA	TBD
2	SA	TBD
3	SA	TBD
4	SA	TBD
5	SA	TBD
6	SA	TBD
7	SA	TBD
8	DQa	TBD
9	DQa	TBD
10	DQa	TBD
11	DQa	TBD
12	VSS	TBD
13	DQa	TBD
14	DQa	TBD
15	DQa	TBD
16	DQa	TBD
17	DQa	TBD
18	SA	TBD
19	SA	TBD
20	SA	TBD
21	SA	TBD
22	ADV	TBD
23	$\bar{G}$	TBD
24	$\bar{CKE}$	TBD
25	$\bar{SW}$	TBD

Bit No.	Signal Name	Bump ID
26	CK	TBD
27	$\bar{SE3}$	TBD
28	$\bar{SBa}$	TBD
29	$\bar{SBb}$	TBD
30	SB2	TBD
31	$\bar{SE1}$	TBD
32	SA	TBD
33	SA	TBD
34	DQb	TBD
35	DQb	TBD
36	DQb	TBD
37	DQb	TBD
38	VDD	TBD
39	DQb	TBD
40	DQb	TBD
41	DQb	TBD
42	DQb	TBD
43	DQb	TBD
44	LBO	TBD
45	SA	TBD
46	SA	TBD
47	SA	TBD
48	SA	TBD
49	SA1	TBD
50	SA0	TBD

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## TEST ACCESS PORT PINS

### TCK — TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

### TMS — TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will not produce the same result as a logic 1 input level (not IEEE 1149.1 compliant).

### TDI — TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 13). An undriven TDI pin will not produce the same result as a logic 1 input level (not IEEE 1149.1 compliant).

### TDO — TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 13). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

### TRST — TAP RESET

The TRST is an asynchronous input that resets the TAP controller and preloads the instruction register with the IDCODE command. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

## TEST ACCESS PORT REGISTERS

### OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of 1s and 0s input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on the subsequent falling edge of TCK. When a register is selected, it is “placed” between the TDI and TDO pins.

### INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are 3 bits long. The register can be loaded when it is placed between the TDI and TDO pins. The parallel outputs of the instruction register are automatically preloaded with the IDCODE instruction when TRST is asserted or whenever the controller is placed in the test–logic–reset state. The two least significant bits of the serial instruction register are loaded with a binary “or” pattern in the capture–IR state.

### BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

## BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 0) reserved for density upgrade address pins. There are a total of 67 bits in the case of the x36 device and 48 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state.

The Bump/Bit Scan Order table describes which device bump connects to each boundary scan register location. The first column defines the bit’s position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

## IDENTIFICATION (ID) REGISTER

The ID register is a 32–bit register that is loaded with a device and vendor specific 32–bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32–bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

### ID Register Presence Indicator

Bit No.	0
Value	1

### Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1–1990)

Bit No.	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

### Reserved For Future Use

Bit No.	17	16	15	14	13	12
Value	x	x	x	x	x	x

### Device Width

Bit No.	22	21	20	19	18
256K x 36	0	0	1	0	0
512K x 18	0	0	0	1	1

### Device Depth

Bit No.	27	26	25	24	23
256K x 36	0	0	1	1	0
512K x 18	0	0	1	1	1

### Revision Number

Bit No.	31	30	29	28
Value	0	0	0	0

Figure 12. ID Register Bit Meanings

## TAP CONTROLLER INSTRUCTION SET

## OVERVIEW

There are two classes of instructions defined in the IEEE Standard 1149.1–1990; the standard (public) instructions and device specific (private) instructions. Some public instructions, are mandatory for IEEE 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the IEEE 1149.1 conventions, it is not IEEE 1149.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but can not be used to load address, data, or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform IEEE 1149.1 EXTEST, INTEST, or the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in capture–IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state the instruction register is placed between TDI and TDO. In this state, the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

## STANDARD (PUBLIC) INSTRUCTIONS

## BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

## SAMPLE/PRELOAD

SAMPLE/PRELOAD is an IEEE 1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the instruction register, moving the TAP controller out of the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK), it is

possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results can not be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time ( $t_{CS}$  plus  $t_{CH}$ ). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE/PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not IEEE 1149.1 compliant.

## EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device.

## IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at  $\overline{TRST}$  assertion and any time the controller is placed in the test–logic–reset state.

## THE DEVICE SPECIFIC (PUBLIC) INSTRUCTION

## SAMPLE–Z

If the HIGH–Z instruction is loaded in the instruction register, all DQ pins are forced to an inactive drive state (High–Z) and the bypass register is connected between TDI and TDO when the TAP controller is moved to the shift–DR state.

## THE DEVICE SPECIFIC (PRIVATE) INSTRUCTION

## NO OP

Do not use these instructions; they are reserved for future use.

## STANDARD AND DEVICE SPECIFIC (PUBLIC) INSTRUCTION CODES

Instruction	Code*	Description
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
HIGH-Z	010	Captures I/O ring contents. Places the bypass register between TDI and TDO. Forces all DQ pins to High-Z. <b>NOT IEEE 1149.1 COMPLIANT.</b>
BYPASS	011	Places bypass register between TDI and TDO. Does not affect RAM operation. <b>NOT IEEE 1149.1 COMPLIANT.</b>
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement IEEE 1149.1 Preload function. <b>NOT IEEE 1149.1 COMPLIANT.</b>

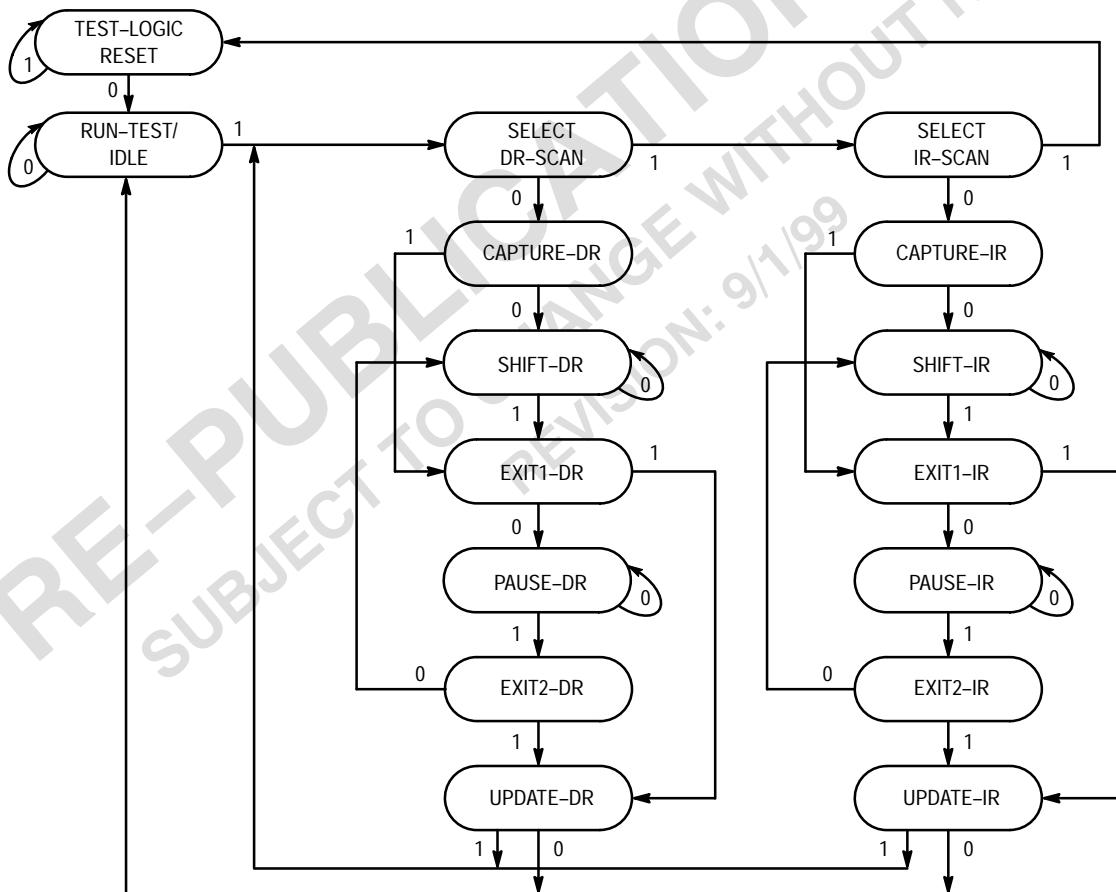
\* Instruction codes expressed in binary, MSB on left, LSB on right.

\*\* Default instruction automatically loaded when TRST asserted or in test-logic-reset state.

## STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	000	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.
NO OP	111	Do not use these instructions; they are reserved for future use.

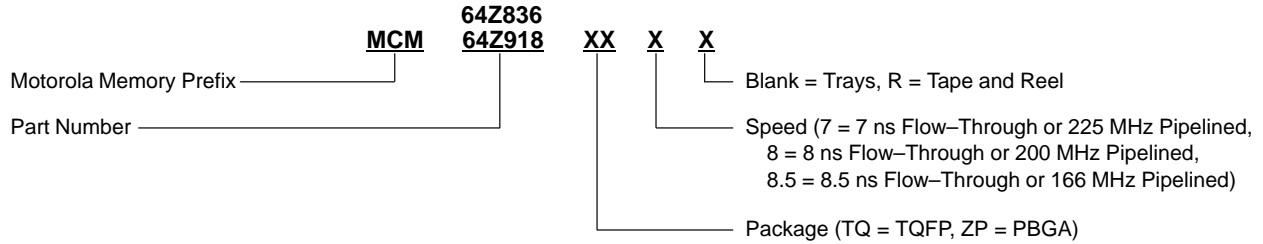
\* Instruction codes expressed in binary, MSB on left, LSB on right.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 13. TAP Controller State Diagram

## ORDERING INFORMATION (Order by Full Part Number)



Full Part Numbers —	MCM64Z836TQ7	MCM64Z836TQ8	MCM64Z836TQ8.5
	MCM64Z836TQ7R	MCM64Z836TQ8R	MCM64Z836TQ8.5R
	MCM64Z918TQ7	MCM64Z918TQ8	MCM64Z918TQ8.5
	MCM64Z918TQ7R	MCM64Z918TQ8R	MCM64Z918TQ8.5R
	MCM64Z836ZP7	MCM64Z836ZP8	MCM64Z836ZP8.5
	MCM64Z836ZP7R	MCM64Z836ZP8R	MCM64Z836ZP8.5R
	MCM64Z918ZP7	MCM64Z918ZP8	MCM64Z918ZP8.5
	MCM64Z918ZP7R	MCM64Z918ZP8R	MCM64Z918ZP8.5R

PRE-PUBLICATION DRAFT

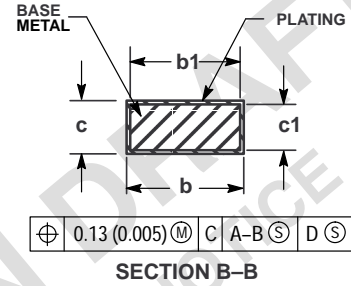
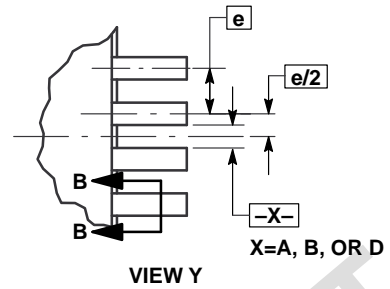
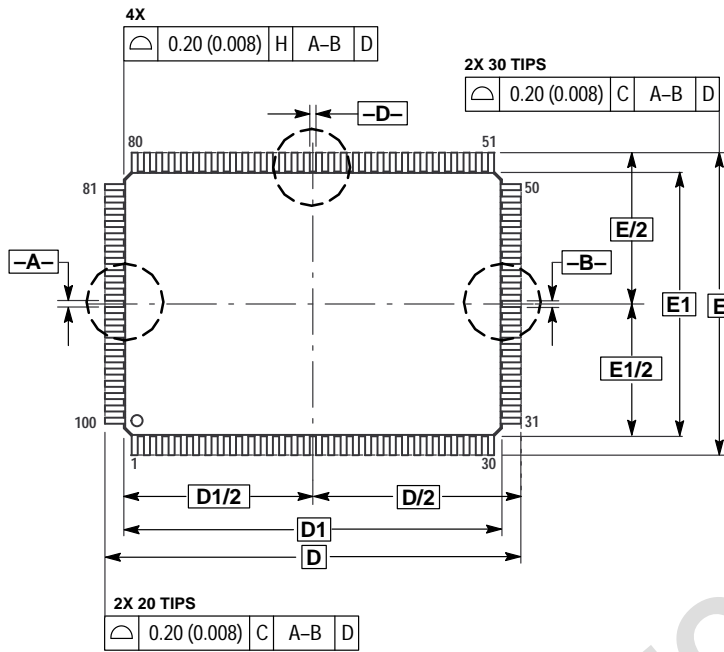
SUBJECT TO CHANGE WITHOUT NOTICE

REVISION: 9/1/99



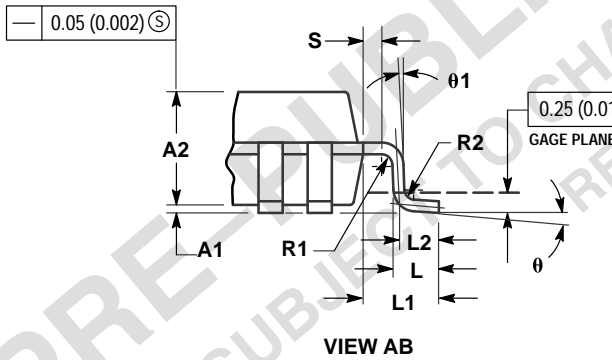
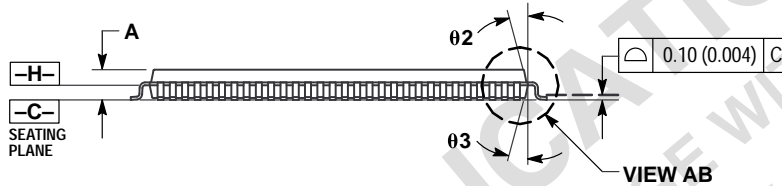
## PACKAGE DIMENSIONS

TQ PACKAGE  
TQFP  
CASE 983A-01



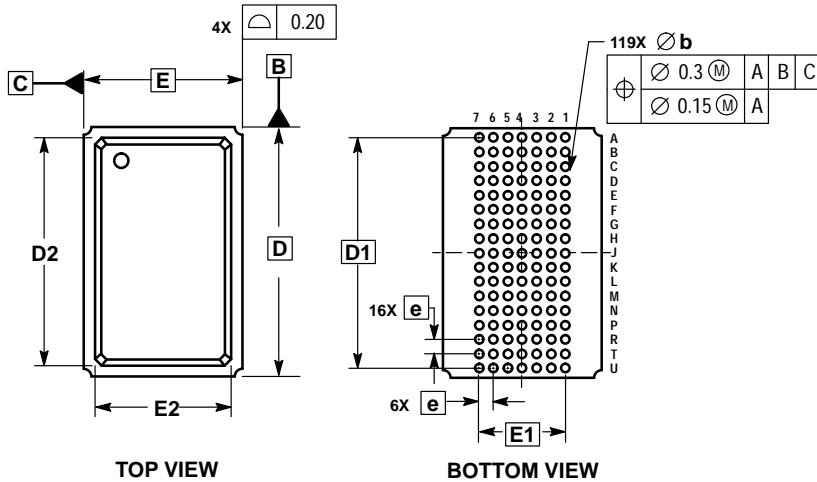
NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
- DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
- DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE -C-.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS D1 AND B1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.45 (0.018).



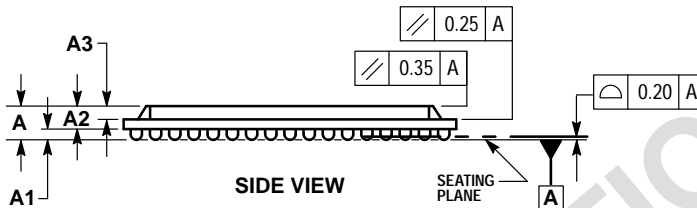
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	1.60	---	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015
b1	0.22	0.33	0.009	0.013
c	0.09	0.20	0.004	0.008
c1	0.09	0.16	0.004	0.006
D	22.00 BSC		0.866 BSC	
D1	20.00 BSC		0.787 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.039 REF	
L2	0.50 REF		0.020 REF	
S	0.20	---	0.008	---
R1	0.08	---	0.003	---
R2	0.08	0.20	0.003	0.008
theta	0°	7°	0°	7°
theta 1	0°	---	0°	---
theta 2	11°	13°	11°	13°
theta 3	11°	13°	11°	13°

**ZP PACKAGE**  
**7 x 17 BUMP PBGA**  
**CASE 999-02**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. ALL DIMENSIONS IN MILLIMETERS.
  3. DIMENSION b IS THE MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
  4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	---	2.40
A1	0.50	0.70
A2	1.30	1.70
A3	0.80	1.00
D	22.00 BSC	
D1	20.32 BSC	
D2	19.40	19.60
E	14.00 BSC	
E1	7.62 BSC	
E2	11.90	12.10
b	0.60	0.90
e	1.27 BSC	



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