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MOTOROLA

MCVVQ201

Product Preview

VirtuoVue™ Digital Display Driver

The MCVVQ201 VirtuoVue™ Digital Driver IC is designed to drive the MCVVQ420 Color LCD Display Panel, or the MCVVQ410 Monochrome Display Panel, in conjunction with the MCVVQ101 Analog Display and Backlight Driver IC. The MCVVQ201 interfaces to the host system's microprocessor to receive the digitized video information, and control information, via an SPI port.

The MCVVQ201 provides all the necessary timing signals to the LCD Display Panel. It also provides the digital video information to the 8–bit DAC in the MCVVQ101 Analog Driver, as well as the backlight control information.

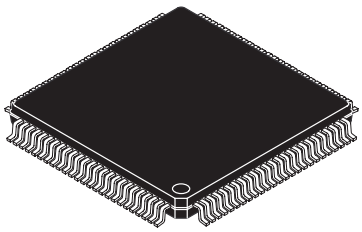
The MCVVQ201 interfaces to a 512 k × 8 SRAM, which provides for image storage. All address, data, and control lines for the SRAM are included. It can additionally interface to an optional external LUT.

The MCVVQ201 is designed to operate from 2.7 to 4.2 volts. It is available in a 100 pin LQFP package.

- Supports RGB and Monochrome VirtuoVue™ QVGA Display Panels
- Host Interface is via 5 Wire SPI Port
- Interfaces Directly to a 512 k × 8 SRAM for Image Storage
- Interfaces Directly to MCVVQ101 Analog Display and Backlight Driver
- Interfaces Directly to a 1.0 k × 8 LUT (Look Up Table)
- Single Supply Required: +2.7 to +4.2 Volts DC
- Operating Ambient Temperature Range: –20 to +70°C
- 100 Pin LQFP Package

VirtuoVue™ DIGITAL DISPLAY DRIVER

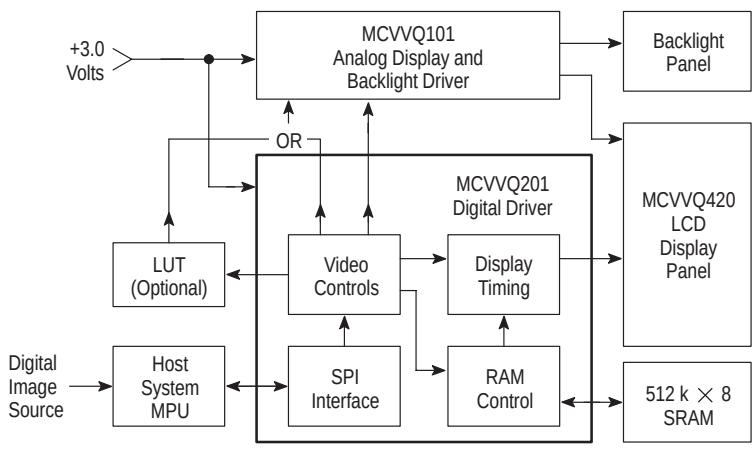
SEMICONDUCTOR TECHNICAL DATA



100 1

FB SUFFIX
PLASTIC PACKAGE
CASE 842F–01

Simplified System Diagram

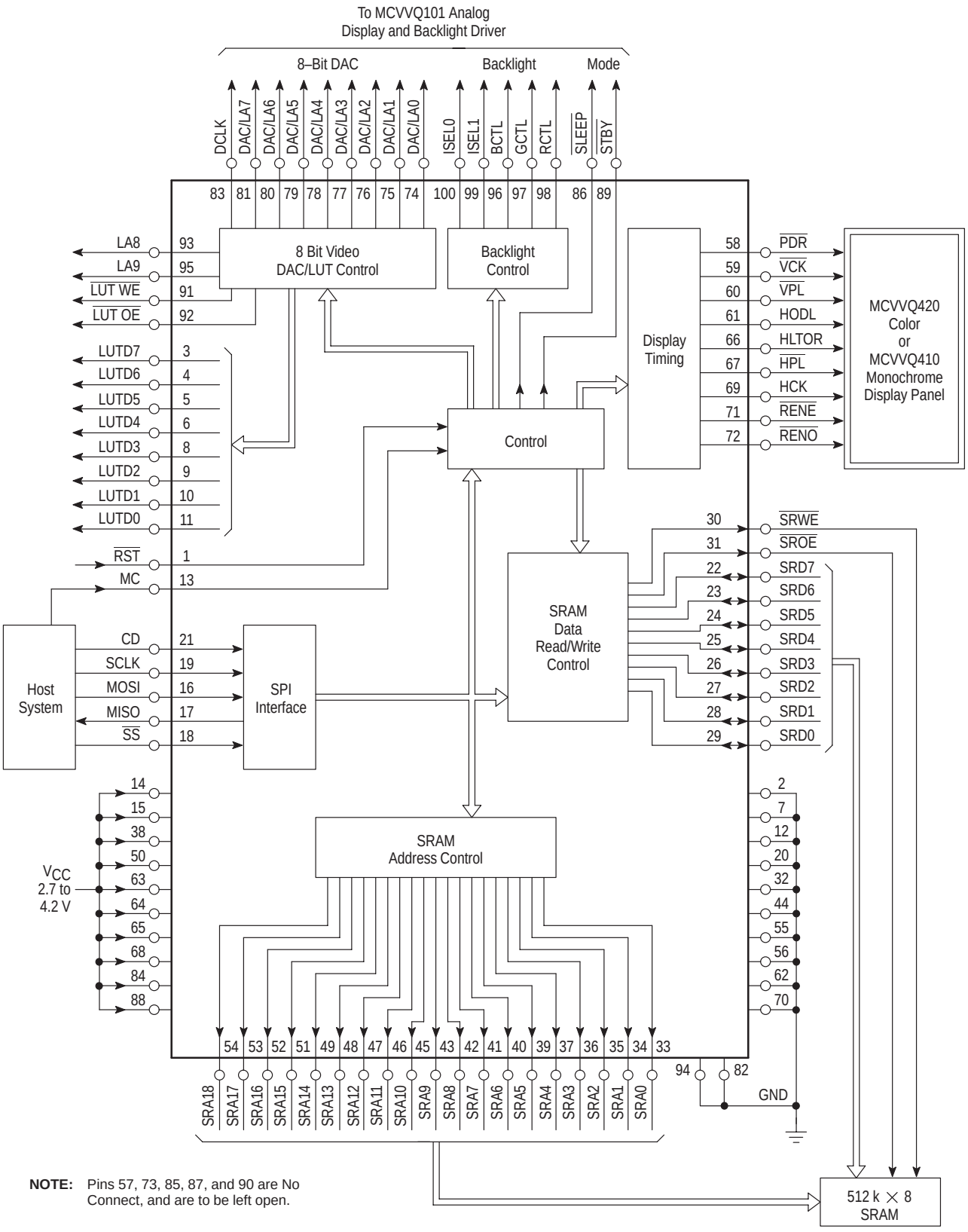


ORDERING INFORMATION

Device	Package
MCVVQ201FB	100 Pin LQFP

Rev 0

Figure 1. Block Diagram



NOTE: Pins 57, 73, 85, 87, and 90 are No Connect, and are to be left open.

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5, +6.0	Vdc
Voltage at All Logic Inputs	Vi	–0.5, V_{CC}+0.5	Vdc
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–65, +150	°C

NOTE: Devices should not be operated at these limits. The “Recommended Operating Conditions” provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Voltage (All V_{CC} Pins must be within 0.5 volt of each other.)		V_{CC}	2.7	3.0	4.2	Vdc
Digital Input High		Vinh	0.67 × V_{CC}	—	V_{CC}	Volts
Digital Input Low		Vinl	0	—	0.33 × V_{CC}	Volts
Frequency at Master Clock	Color	fMC	—	—	20	MHz
	Monochrome		—	—	5.0	
Frequency at SClk (SPI Interface)		fSCK	—	—	3.2	MHz
Operating Ambient Temperature		T_A	–20	—	+70	°C

NOTE: All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.0 V)

Characteristic		Min	Typ	Max	Unit
MISCELLANEOUS					
Total Supply Current – All Outputs Open, Pin 1 = High		TBD	TBD	TBD	mA
Reset Threshold (Pin 1)		—	TBD	—	Volts
Logic Output Level	High	TBD	TBD	V_{CC}	Volts
	Low	0	TBD	TBD	

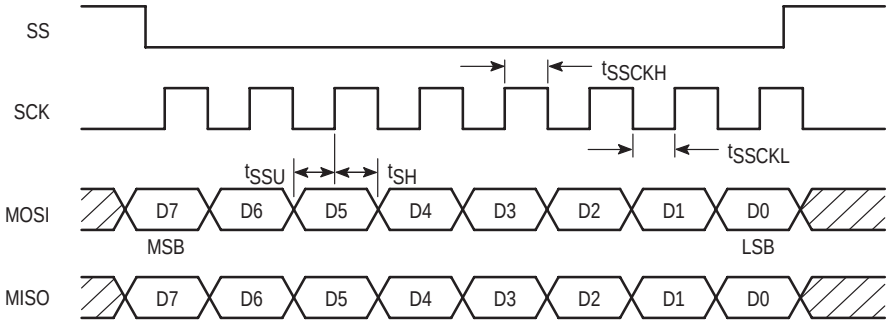
TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.0 V)

Parameter	Symbol	Min	Typ	Max	Unit
SPI INTERFACE (Figure 2)					
Maximum Data Rate	f_{SMAX}	—	—	3.2	MHz
SCLK High Time	t_{SSCKH}	190	—	—	nS
SCLK Low Time	t_{SSCKL}	190	—	—	nS
Data Setup Time	t_{SSU}	100	—	—	nS
Data Hold Time	t_{SH}	100	—	—	nS
Output Rise Time (C_L = 200 pF)	t_{SR}	—	—	100	nS
Output Fall Time (C_L = 200 pF)	t_{SF}	—	—	100	nS
EXTERNAL RAM INTERFACE (See Figure 3)					
Maximum Frequency of Operation	f_{RMAX}	—	—	20	MHz
Clock to Address Valid	t_{CAV}	15	—	—	nS
Address Out Valid to Data In Valid	t_{RACC}	—	—	30	nS
Data In Valid Setup Time	t_{RSU}	3.0	—	—	nS
Data In Valid Hold Time	t_{RH}	—	—	3.0	nS
LUT INTERFACE (See Figure 10)					
Maximum Frequency of Operation	f_{LMAX}	—	—	20	MHz
Clock to Address Valid	t_{LCAV}	—	—	30	nS
Clock to Data Valid	t_{LACC}	—	—	30	nS

TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.0 V)

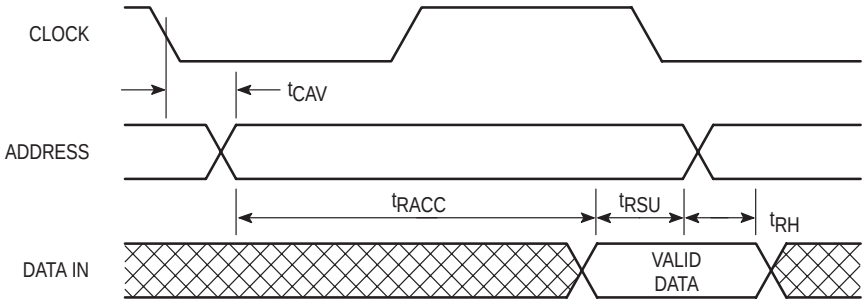
Parameter	Symbol	Min	Typ	Max	Unit
MONOCHROME DISPLAY PANEL INTERFACE TIMING (See Figures 4, 5, 7)					
VCK Period	t_{VC}	101.4	—	—	µS
VCK High Time	t_{VCH}	290	—	—	nS
VCK Low Time	t_{VCL}	290	—	—	nS
VPL Setup Time	t_{VPS}	140	—	—	nS
VPL Hold Time	t_{VPH}	140	—	—	nS
VCK to RENE/RENO Delay Time	t_{VCRD}	440	—	—	nS
RENE/RENO to VCK Delay Time	t_{VRCD}	440	—	—	nS
RENE/RENO to RENO/RENE Delay Time	t_{VRED}	890	—	—	nS
HODL to VCK Time	t_{HOV}	140	—	—	nS
HCK Period	t_{HC}	150	—	—	nS
HCK High Time	t_{HCH}	65	—	—	nS
HPL Setup Time	t_{HPS}	65	—	—	nS
HPL Hold Time	t_{HPH}	40	—	—	nS
Output Transition Time (Rise or Fall)	t_T	3.0	—	5.0	nS
HCK to Video Setup Time	t_{HVS}	—	—	40	nS
HCK to Video Hold Time	t_{HVH}	150	—	—	nS
Video Delay Time	t_{VD}	890	—	—	nS
Video Lead Time	t_{VL}	890	—	—	nS
RENE/RENO Power Down Pulse Width	t_{VRP}	6.0	—	—	µS
COLOR DISPLAY PANEL INTERFACE TIMING (See Figures 4, 5, 7)					
VCK Period	t_{VC}	35	—	—	µS
VCK High Time	t_{VCH}	140	—	—	nS
VCK Low Time	t_{VCL}	140	—	—	nS
VPL Setup Time	t_{VPS}	42	—	—	nS
VPL Hold Time	t_{VPH}	42	—	—	nS
VCK to RENE/RENO Delay Time	t_{VCRD}	240	—	—	nS
RENE/RENO to VCK Delay Time	t_{VRCD}	240	—	—	nS
RENE/RENO to RENO/RENE Delay Time	t_{VRED}	490	—	—	nS
HODL to VCK Time	t_{HOV}	140	—	—	nS
HCK Period	t_{HC}	50	—	—	nS
HCK High Time	t_{HCH}	20	—	—	nS
HPL Setup Time	t_{HPS}	20	—	—	nS
HPL Hold Time	t_{HPH}	10	—	—	nS
Output Transition Time (Rise or Fall)	t_T	—	—	10	nS
HCK to Video Setup Time	t_{HVS}	—	—	40	nS
HCK to Video Hold Time	t_{HVH}	80	—	—	nS
Video Delay Time	t_{VD}	490	—	—	nS
Video Lead Time	t_{VL}	490	—	—	nS
RENE/RENO Power Down Pulse Width	t_{VRP}	3.0	—	—	µS

Figure 2. SPI Interface Timing



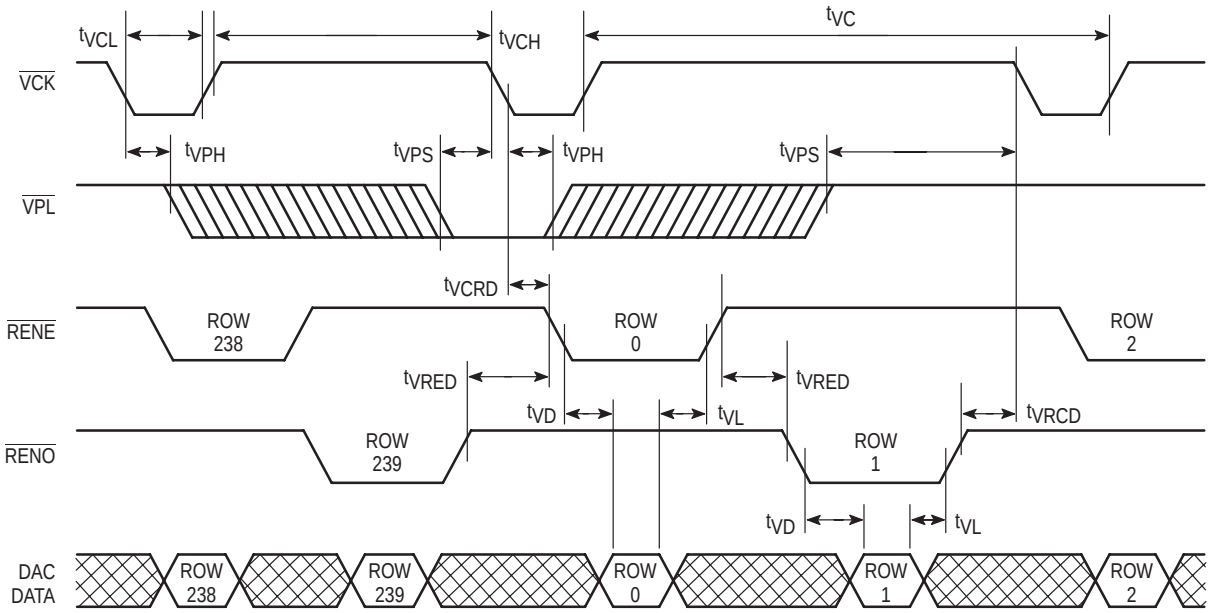
1) Maximum clock and data rate is 3.2 MHz. There is no required minimum rate.
2) D7 is to be entered first, D0 last.
3) Data is entered on the clock rising edge.

Figure 3. External RAM Read Cycle



1) Clock is the internal system clock, set by MC.
2) $\overline{\text{SRWE}}$ (Write Enable) = High.
3) $\overline{\text{SROE}}$ (Output Enable) = Low.

Figure 4. Vertical Timing to LCD Display Panel (Color and Monochrome)



NOTES: 1) All transition times measured from V_{IH} and V_{IL}.

Figure 5. Horizontal Timing to LCD Display Panel (Color and Monochrome)

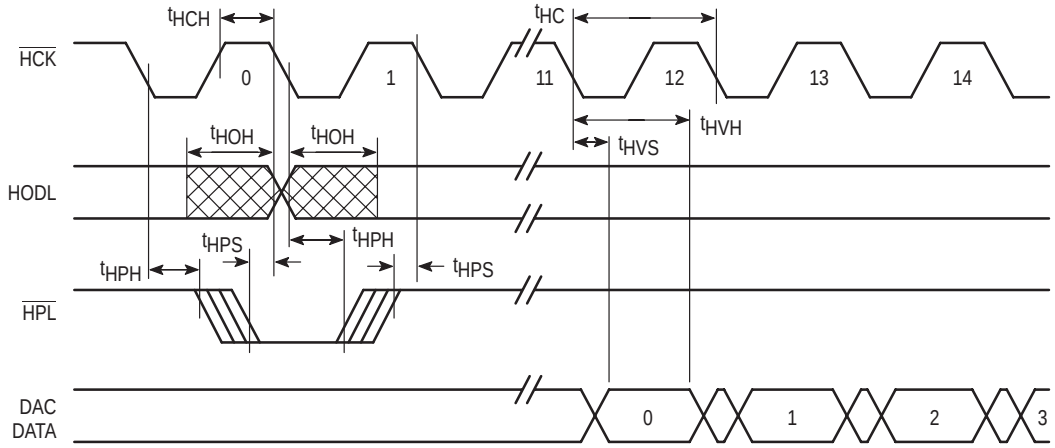
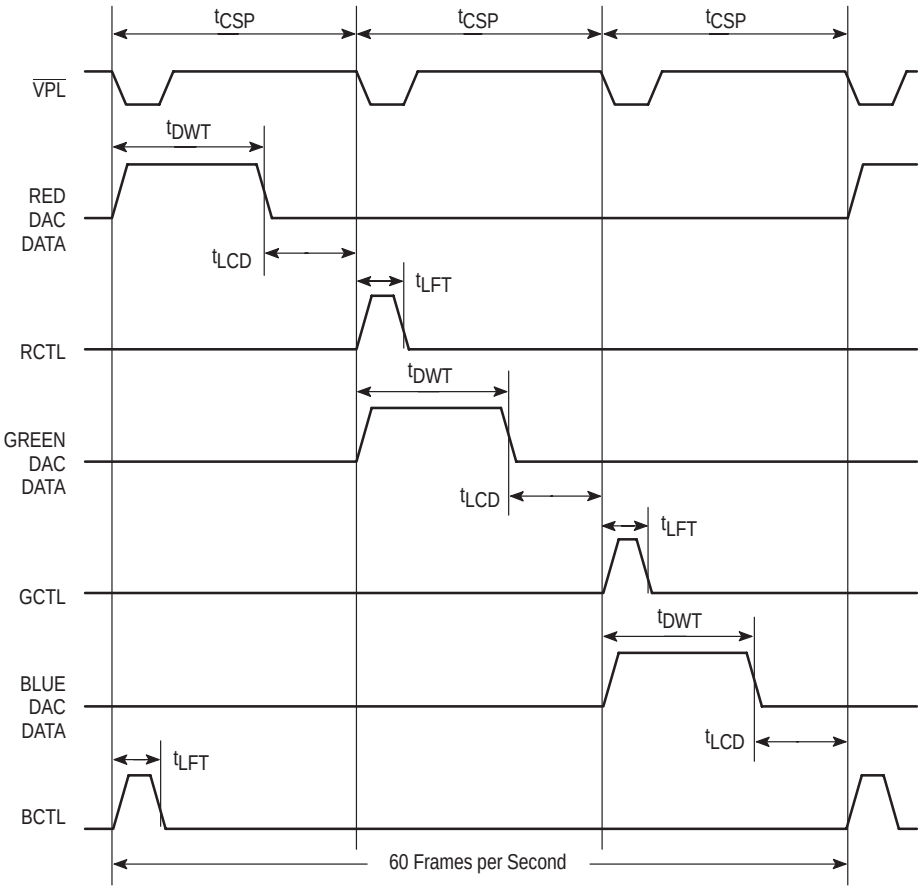


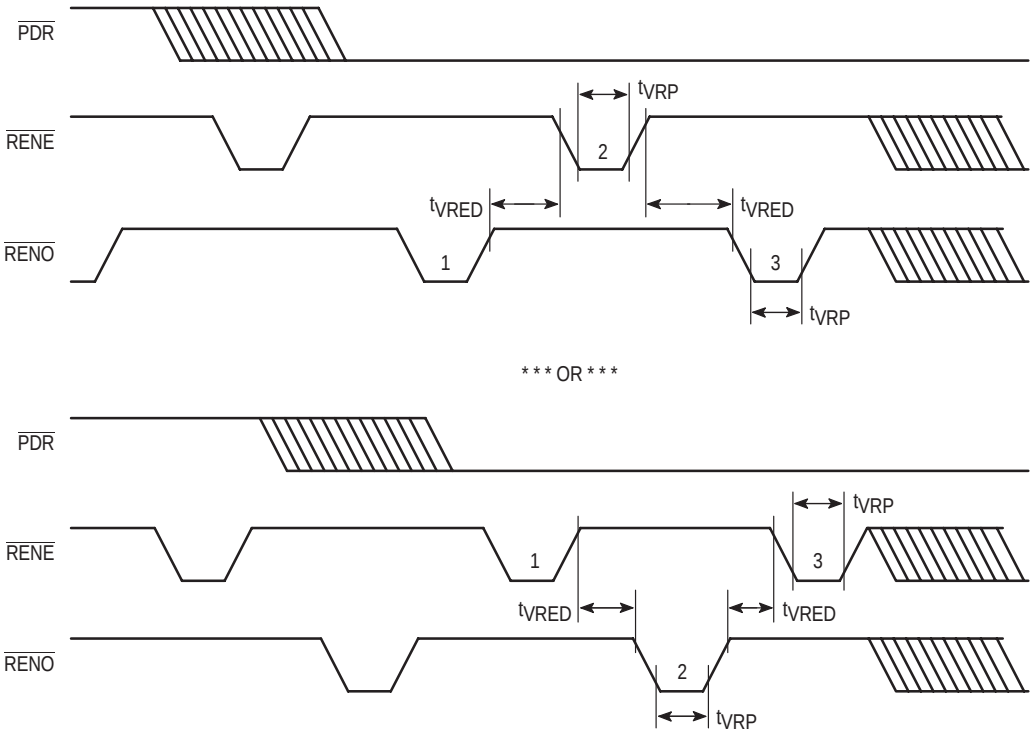
Figure 6. Backlight Color Sequential Timing



COLOR SEQUENTIAL TIMING (See Figure 6, MC = 20 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Color Subframe Period	t_{CSP}	—	5.55	—	mS
Display Write Time	t_{DWT}	—	4.2	—	mS
LC Display Delay	t_{LCD}	—	1.3	—	mS
Backlight LED Flash Time	t_{LFT}	—	1.0	—	mS
LED Duty Cycle	DCY	—	6.0	—	%
Sub Frame Rate	SFR	—	180	—	Hz

Figure 7. Power Down Cycle Timing



PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	$\overline{RST}$	Power–on Reset input. Connect to external RC, or controlling output from the host. When low, outputs to the LCD display panel are low.
2, 7, 12, 20, 32, 44, 55–56, 62, 70, 82, 94	GND	Ground. All ground pins are to be connected to circuit ground, preferably a ground plane.
3–6, 8–11	LUTD7 – LUTD0	Data outputs used to load an external 1.0 k × 8 LUT (Look Up Table). Use of a LUT is optional. LUTD7 is the MSB, LUTD0 is the LSB. See Figures 1, 10, and Table 9.
13	MC	Master Clock input. Nominally 20 MHz for color applications, 5.0 MHz for monochrome.
14, 15, 38, 50, 63–65, 68, 84, 88	V_{CC}	Power supply input. Nominal range is 2.7 to 4.2 volts. Bypassing is required. All V_{CC} pins are to be within ±0.5 volts of each other.
16	MOSI	Master Out Slave In input. Connect to MOSI output at host's microcontroller.
17	MISO	Master In Slave Out output. Connect to MISO input at host's microcontroller.
18	$\overline{SS}$	Slave select input for SPI slave mode. When low, enables shifting of data.
19	SCLK	Clock input for the SPI interface. Maximum frequency is 3.2 MHz. Data is shifted in/out on the clock rising edge.
21	CD	Control/Data Input. When high, data is directed to the Address Control registers. When low, data is directed to the SRAM or LUT.
22–29	SRD7 – SRD0	Bi–directional data lines for the external SRAM. SRD7 is the MSB. See Figure 1 for specific pinouts.
30	$\overline{SRWE}$	Write Enable output to the external SRAM.
31	$\overline{SROE}$	Output Enable output to the external SRAM.
33–37, 39–43, 45–49, 51–54	SRA0 – SRA18	Address output lines for the external SRAM. SRA18 is the MSB. See Figure 1 for specific pinouts.
58	$\overline{PDR}$	Power Down Reset output to the LCD display panel. Active low.
59	$\overline{VCK}$	Vertical Clock output to the LCD display panel's vertical shift register. Active low.
60	$\overline{VPL}$	Output. Active low start pulses to the LCD display panel's vertical shift register. Each pulse defines the start of a frame.
61	HODL	Horizontal Odd Low output to the LCD display panel. Alternates each frame to provide the column inversion requirement of the LCD panel.
66	HLTOR	Horizontal Left to Right Output to the LCD display panel. High for left–to–right scan.
67	$\overline{HPL}$	Output. Active low start pulses to the display panel's horizontal shift register. Each pulse defines the start of a new row.
69	HCK	Clock output to the LCD display panel's horizontal shift register. Timing is referenced to this clock's falling edge. The frequency is the same as at MC (Pin 13).
71	$\overline{RENE}$	Even Row Enable output to the LCD display panel.
72	$\overline{RENO}$	Odd Row Enable output to the LCD display panel.
81–74	DAC7–0 or LA7–0	When an external LUT is not used, connect to the MCVVQ101 Analog Driver DAC inputs. When an external LUT is used, these pins are the lower 8 of the LUT's 10 address lines. See Figures 1, 9, and 10.
83	DCLK	DAC Clock output. Connect to DCLK input on the MCVVQ101 Analog Driver.
86	$\overline{SLEEP}$	Active low Sleep output. Connect to Sleep input on the MCVVQ101 Analog Driver.
89	$\overline{STBY}$	Active low Standby output. Connect to Standby input on the MCVVQ101 Analog Driver.
91	$\overline{LUTWE}$	Write Enable output to the external LUT (Look Up Table).
92	$\overline{LUTOE}$	Output Enable output to the external LUT (Look Up Table).
93, 95	LA8, LA9	Upper address lines for the 1.0 k × 8 LUT. Used for color page selection (See Table 9).
96	BCTL	Logic output to the BCTL input pin on the MCVVQ101 Analog Driver. Blue LED current is on when this pin is high
97	GCTL	Logic output to the GCTL input pin on the MCVVQ101 Analog Driver. Green LED current is on when this pin is high
98	RCTL	Logic output to the RCTL input pin on the MCVVQ101 Analog Driver. Red LED current is on when this pin is high

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
99–100	ISEL1, ISEL0	Logic outputs to the MCVVQ101 Analog Driver. Used to fine tune the three LED current values, and thereby the backlight intensity.
57, 73, 85, 87, 90	NC	No External Connection. These pins are to be left open.

DESCRIPTION

The MCVVQ201 VirtuoVue™ Digital Display Driver is designed to provide the digital signals associated with driving and controlling the MCVVQ420 Color Display panel, or the MCVVQ410 Monochrome display panel. The MCVVQ201 provides:

- A 5 wire SPI interface to/from the host microcontroller.
- All timing signals to the LCD display.
- Interface for an external 512 k × 8 SRAM for image storage.
- Interface for an optional external 1.0 k × 8 LUT (Look Up Table).
- Interface to the MCVVQ101 Analog Display and Backlight Driver.

The MCVVQ201 is designed to receive digitized video information from the host system (via the SPI port), store it, and format it in order to control the LCD display, and the backlight LEDs. The digital timing waveforms are provided to the LCD display from this IC, while the analog information and backlight controls are provided via the MCVVQ101 Analog Driver. The MCVVQ101 also provides all necessary power supply voltages to the LCD display by means of an on–board DC–DC converter.

The MCVVQ201 is designed to operate from a supply voltage of 2.7 to 4.2 volts, at a current consumption of xx mA.

SERIAL PERIPHERAL INTERFACE (SPI)

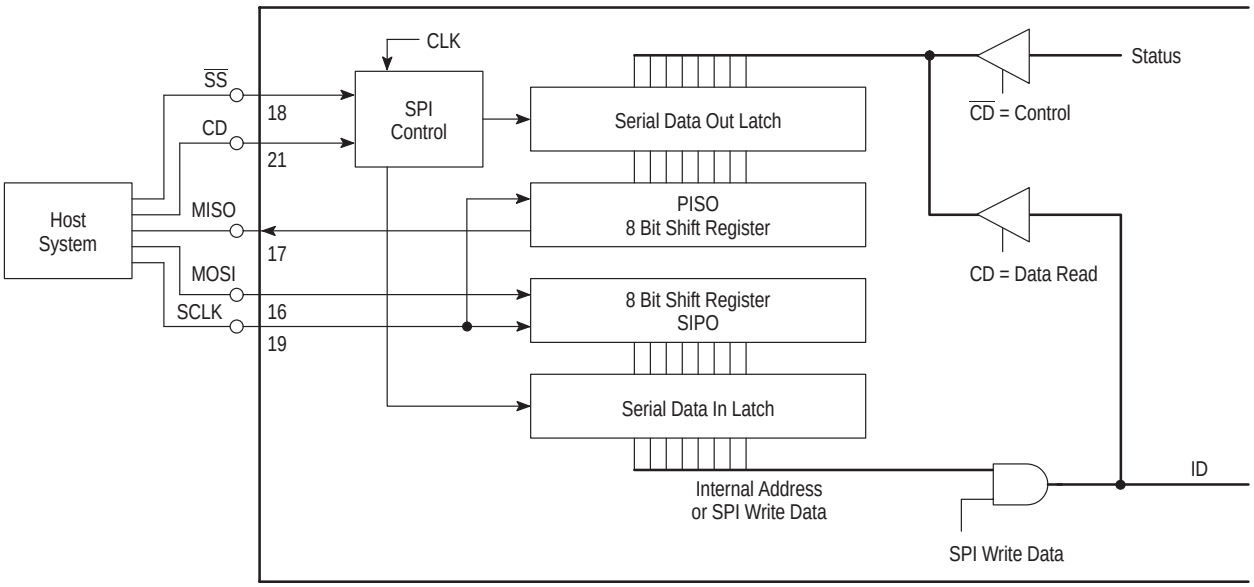
The SPI port provides the means for the host system to program and control the MCVVQ201 to drive the LCD display panel, and the MCVVQ101 Analog Driver. The port is a standard SPI arrangement, compatible with a wide array of microprocessors and controllers, such as the Motorola MC68HC11 series. The SPI block diagram is shown in Figure 8. Figure 2 indicates the basic timing diagram for this communication. Writing to/from the MCVVQ201 is done in 8 bit words.

The SPI port consists of five lines: SCK, MOSI, MISO, CD, and $\overline{SS}$. Their function is described in Table 1.

Table 1. SPI PIN DESCRIPTION

Pin No.	Pin Name	Description
19	SCK	Clock input for the SPI interface. Maximum frequency is 3.2 MHz. Data is shifted in/out on the clock rising edge.
16	MOSI	Master Out/Slave In. Data input from the host system.
17	MISO	Master In/Slave Out. Data output to the host system.
21	CD	Control/Data Input. When high, data is directed to the Address Control registers. When low, data is directed to/from memory.
18	$\overline{SS}$	Slave select input. When low, enables communicating with this IC.

Figure 8. SPI Block Diagram



CONTROL REGISTERS

There are 16 registers containing the control bits, and are accessed by setting CD (pin 21) high. The four MSBs of each byte written on the MOSI line (pin 16) designate the register ($0 through $F), and the four LSBs set the control bits for that register. Table 2 lists the control registers, and Table 3 provides a description of each control bit's function.

Table 2. Control Registers

Register	7	6	5	4	3	2	1	0
0	0	0	0	0	RD/WR	PARSER	DN/OVR	INIT
1	0	0	0	1	MAR	STBY	MOD1	MOD0
2	0	0	1	0	MA3	MA2	MA1	MA0
3	0	0	1	1	MA7	MA6	MA5	MA4
4	0	1	0	0	MA11	MA10	MA9	MA8
5	0	1	0	1	MA15	MA14	MA13	MA12
6	0	1	1	0	MA19	MA18	MA17	MA16
7	0	1	1	1	DA3	DA2	DA1	DA0
8	1	0	0	0	DA7	DA6	DA5	DA4
9	1	0	0	1	DA11	DA10	DA9	DA8
A	1	0	1	0	DA15	DA14	DA13	DA12
B	1	0	1	1	SP1	DA18	DA17	DA16
C	1	1	0	0	PD INH	HLTR	SWR	STOP
D	1	1	0	1	DCA3	DCA2	DCA1	DCA0
E	1	1	1	0	CLR/MONO	WHITE	ISEL1	ISEL0
F	1	1	1	1	SP2	SP3	SP4	SP5

Table 3. Control Bits Description

Name	Reg.	Bit(s)	Description
INIT	0	0	Initialize (not currently implemented).
DN/OVR	0	1	Down/Over – When 1, address counters increment down the LCD display for a data read/write. When 0, counters increment horizontally across display.
PARSER	0	2	Set to 1 for a parallel data transfer. Set to 0 for a serial data transfer.
RD/WR	0	3	Read/Write – Set to 1 for a read operation. Set to 0 for a write operation.
MOD1, 0	1	1, 0	Data Display Mode Select – Sets the number of levels of pixel control from dark to bright. 00 = 1 bit/ pixel (2 levels), 01 = 2 bits/pixel (4 levels), 10 = 4 bits/pixel (16 levels), 11 = 8 bits/pixel (256 levels). In color applications, this sets the number of bits/color, thereby tripling the number of bits/pixel.
STBY	1	2	Standby – When set to 1 causes immediate reset to standby mode, and Pin 89 is set low. When 0, allows display of data if MAR is low.
MAR	1	3	Memory Access Request – When high, generates a power–down cycle to the LCD display after the currently displayed frame is complete (see Figure 7). The LCD display is then held blank. Memory read/writes can then occur. When low, and if STBY is low, normal display operation is resumed.
MA19–MA0	6–2	0–3	Memory Address – Indicates starting address for SPI reads or writes to the external memory. Memory range is $00100 to $004FF for the LUT, and $80000 to $FFFFF for the SRAM . The address is internally latched in when register $6 is written to.
DA18–DA0	7–$B	3–0 2–0	Display Address – Indicates the SRAM starting address for data to be displayed via the DAC/LA7–0 pins.
STOP	C	0	Stop (Sleep) Mode – When 1, display is set to power down mode. All clock outputs are low. The Sleep pin (Pin 86) is set low.
SWR	C	1	Software Reset – When set to 1, generates a controlled reset to the LCD display panel. See Figure 7.
HLTR	C	2	Horizontal Left to Right – When 1, sets HLTOR (Pin 66) high, setting the LCD display to scan left to right. When 0, HLTOR is low, and the display scans right to left.
PD INH	C	3	Power Down Inhibit – When 1, prevents a power down sequence from occurring when Standby mode is set.
DCA3–0	D	3–0	DAC Clock Adjust – Sets the delay between valid data presented to the DAC/LA0–9 pins, and the falling edge of HCK (Pin 69). When $0, minimum delay is set. When $F, maximum delay is set.
ISEL1, 0	E	1, 0	Intensity Select – Adjusts the intensity of the backlight LEDs. Pins 99 and 100 follow bits ISEL1 and ISEL0, respectively. Backlight control is via the MCVVQ101 Analog Driver IC.
WHITE	E	2	Used in conjunction with CLR/MONO bit to select the color mode. See Table 10.
CLR/MONO	E	3	Used in conjunction with WHITE bit to select the color mode. See Table 10.
SP1 SP2–5	B F	3 3–0	These bits are unassigned. Register F is used in some software operations.

INITIALIZATION

When $\overline{\text{RST}}$ (Pin 1) is low the control registers cannot be written to. After $\overline{\text{RST}}$ goes high (after power–on or an intentional controlled reset), it is necessary to set both SWR and STOP = 1, thereby setting the internal logic arrays, and the display output pins, to a known state. The condition of the remaining control bits is unpredictable after reset, and therefore they must be initialized. SWR and STOP can be set to 0 when an image is to be displayed.

MEMORY INTERFACE

Following is a description of the interface to the SRAM and to the LUT:

SRAM Interface/Display Memory:

– The MCVVQ201 can interface to a high speed external 512k x 8 SRAM, using address lines SRA18–0 (Pins 54–33), data lines SRD7–0 (Pins 22–29), and control pins SRWE and SROE (Pins 30, 31). The Control Registers contain 20 address bits (MA19–0) in registers $6–2 to define a starting address for a read or write operation. The MSB (MA19) is always to be set to 1 when specifying an address for the SRAM, as the SRAM memory is mapped from $80000 to $FFFFF.

Areas of the memory map used for displaying images are segmented into 40 byte rows. One 40 byte row defines a single 320 pixel display row when MOD1,0 are set to 1 bit/pixel (Table 4). Note that the first pixel (pixel 0) is mapped into D7 of the first address, not D0. Table 5, 6, and 7 indicates the mapping when MOD1,0 are set to 2, 4, or 8 bits/pixel, respectively. Tables 4–7 indicate the mapping for one frame, with the starting address shown as $80000h as an example only. Other starting addresses are possible. The maximum number of images which can be stored in one 512 k $\times$ 8 SRAM is shown in Table 8.

When the non–indexed color mode is set, the memory requirement is tripled since each image requires one frame per color. In this mode, each image is stored in three contiguous frames, ordered red, green, blue.

Table 4. SRAM Display Data Mapping – 1 bit/pixel

	PIXEL 0							PIXEL 7		PIXEL 296		PIXEL 303		PIXEL 312		PIXEL 319	
	D7	D6	D5	D4	D3	D2	D1	D0	— — — —	D7	— — — —	D0	D7	— — — —	D0	D7	— — — —	D0
ROW 0	Address				80000 h				— — — —	80025 h			80026 h			80027 h		
ROW 1	80028 h								— — — —	8004D h			8004E h			8004F h		
ROW 2	80050 h								— — — —	80075 h			80076 h			80077 h		
—	—								— — — —	—			—			—		
—	—								— — — —	—			—			—		
ROW 239	82558 h									8257D h			8257E h			8257F h		

1st byte

40 bytes/row
Total of 9600 bytes.

Table 5. SRAM Display Data Mapping – 2 bits/pixel

	PIXEL 0							PIXEL 3		PIXEL 308		PIXEL 311		PIXEL 316		PIXEL 319	
	D7	D6	D5	D4	D3	D2	D1	D0	— — — —	D7	D6	– –	D1	D0	D7	D6	– –	D1	D0	D7	D6	– –	D1	D0
ROW 0	Address				80000 h				— — — —	8004D h					8004E h					8004F h				
ROW 1	80050 h								— — — —	8009D h					8009E h					8009F h				
ROW 2	800A0 h								— — — —	800ED h					800EE h					800EF h				
—	—								— — — —	—					—					—				
—	—								— — — —	—					—					—				
ROW 239	84AB0 h									84AFD h					84AFE h					84AFF h				

1st byte

80 bytes/row
Total of 19200 bytes.

Table 6. SRAM Display Data Mapping – 4 bits/pixel

	PIXEL 0							PIXEL 1		PIXEL 314		PIXEL 315		PIXEL 318		PIXEL 319	
	D7	D6	D5	D4	D3	D2	D1	D0	— — — —	D7– –D4		D3– –D0		D7– –D4		D3– –D0		D7– –D4		D3– –D0	
ROW 0	Address				80000 h				— — — —	8009D h				8009E h				8009F h			
ROW 1	800A0 h								— — — —	8013D h				8013E h				8013F h			
ROW 2	80140 h								— — — —	801DD h				801DE h				801DF h			
—	—								— — — —	—				—				—			
—	—								— — — —	—				—				—			
ROW 239	89560 h									895FD h				895FE h				895FF h			

1st byte

160 bytes/row
Total of 38400 bytes.

Table 7. SRAM Display Data Mapping – 8 bits/pixel

	PIXEL 0									PIXEL 317		PIXEL 318		PIXEL 319	
	D7	D6	D5	D4	D3	D2	D1	D0	— — — —	D7	— — — —	D0	D7	— — — —	D0	D7	— — — —	D0
ROW 0	Address				80000 h				— — — —	8013D h			8013E h			8013F h		
ROW 1	80140 h								— — — —	8027D h			8027E h			8027F h		
ROW 2	80280 h								— — — —	803BD h			803BE h			803BF h		
—	—								— — — —	—			—			—		
—	—								— — — —	—			—			—		
ROW 239	92AC0 h									92BFD h			92BFE h			92BFF h		

1st byte

320 bytes/row
Total of 76800 bytes.

Table 8. Maximum Number of Images in a 512 k × 8 SRAM

Mode	Bits/Pixel or Bits/Color	No. of Bytes/Image	Maximum No. of Images
Monochrome, Color–White, and Indexed Color (1 frame/image)	1	9600	54
	2	19200	27
	4	38400	13
	8	76800	6
Non–Indexed Color (3 frames/image)	1	28800	18
	2	57600	9
	4	115200	4
	8	230400	2

Indexed Color mode can only be set to 4 or 8 bits/pixel.

LUT (Look Up Table):

Use of a LUT is optional, and depends on the application. Use of a LUT reduces the amount of SRAM space required to store a complete color frame, since the SRAM will contain information for one frame, rather than three, and the LUT will create the color information for that image. The LUT is typically 1.0 k × 8, partitioned as 4 pages of 256 bytes each. Three pages contain the color information, with address bits LA9 and LA8 selecting the color page. See Table 9 and Figure 10. To use the color pages in the LUT, the indexed mode of operation must be selected (CLR/MONO = WHITE = 1).

If a color mode other than indexed mode is selected in a system which physically includes a LUT, the MCVVQ201 selects the fourth page within the LUT, allowing (e.g.) a pass through of the video DAC data to the DAC inputs on the MCVVQ101 Analog driver IC. The fourth page can also be used for inverting data, non–linear intensity mapping, and other data modifications.

The Memory Map information in Table 9 is used when loading the LUT via the SPI port.

Table 9. LUT Partitioning

Memory Map (for loading)	LA9 (Pin 95)	LA8 (Pin 93)	Color Page
$00400–004FF	0	0	Blue
$00100–001FF	0	1	Red
$00200–002FF	1	0	Green
$00300–003FF	1	1	Fourth page

COLOR/MONO DISPLAY MODES

There are 4 display modes, with variable resolution, as follows (summarized in Table 10):

Monochrome Mode (CLR/MONO = WHITE = 0):

This mode is intended for monochrome LCD display panels, and monochrome backlight panels. After a frame of data is written to the LCD display panel, then the backlight is strobed without any delay. The resolution may be set at 1, 2, 4, or 8 bits/pixel.

Color–White Mode (CLR/MONO = 0, WHITE = 1):

This mode is intended for color LCD display panels, and RGB backlight panels, displaying a monochrome picture. A frame of data is written to the LCD display panel. After a 1.3 ms delay, one of the three backlight LEDs is strobed. The same data frame is written twice more, and the two remaining LEDs are strobed in sequence after each frame. Resolution may be set at 1, 2, 4 or 8 bits/pixel.

Non–Indexed Color Mode (CLR/MONO = 1, WHITE = 0):

This mode is intended for color LCD display panels, and RGB backlight panels, displaying a color picture, without the use of an external Look Up Table. For this mode, the three color frames which make up the total image, are stored in the SRAM. The pixel information for the complete red frame is provided to the DAC outputs (Pins 81–74), followed by a strobe of the red backlight LED (via the RCTL pin) after a 1.3 ms delay. This is followed by the complete green frame information, followed by a strobe of the green backlight LED (via the GCTL pin) after a 1.3 ms delay. This is followed by the complete blue frame information, followed by a strobe of the blue backlight LED (via the BCTL pin) after a 1.3 ms delay. These steps constitute one full color frame. The resolution may be set at 1, 2, 4, or 8 bits/color (3, 6, 12, or 24 bits/pixel).

Indexed Color Mode (CLR/MONO = WHITE = 1):

This mode is intended for color LCD display panels, and RGB backlight panels, displaying a color picture using an external 1.0 k × 8 LUT (Look Up Table). The amount of SRAM space for a full color frame is less than that required in the Non–Indexed Color mode since one frame of information is stored in the SRAM. This information is then provided to the R, G, and B sections of the LUT to generate the color information.

The complete frame of data is provided to the LUT via the LA7–0 pins (Pins 81–74), with LA9 and LA8 = 00 to select the blue color page within the LUT. After a 1.3 ms delay, the blue LED is strobed via the BCTL pin. Then the complete frame of data is provided again to the LUT via the LA7–0 pins, with LA9 and LA8 = 01 to select the red color page within the LUT. After a 1.3 ms delay, the red LED is strobed via the RCTL pin. Then the complete frame of data is provided again to the LUT via the LA7–0 pins, with LA9 and LA8 = 10 to select the green color page within the LUT. After a 1.3 ms delay, the green LED is strobed via the GCTL pin. This sequence constitutes one complete color frame. The resolution may be set at 4 or 8 bits/color (12 or 24 bits/pixel). During this mode of display, the LUTD7 – LUTD0 pins are in a high impedance mode. See Table 9 and Figure 10.

Table 10. Color/Mono Mode Selection

Control Bit		Mode	Description
White	CLR/MONO		
0	0	Monochrome	For monochrome LCD panels and backlight panels. Resolution can be 1, 2, 4, or 8 bits/pixel.
1	0	Color–White	For color LCD panels and RGB backlight panels displaying a monochrome picture. Resolution can be 1, 2, 4, or 8 bits/pixel.
0	1	Non–Indexed Color	For color LCD panels and RGB backlight panels displaying a color picture, normally without the use of an external LUT. Resolution can be 1, 2, 4, or 8 bits/color (3, 6, 12, or 24 bits/pixel).
1	1	Indexed Color	For color LCD panels and RGB backlight panels displaying a color picture, with the use of an external LUT. Resolution can be 4 or 8 bits/color (12 or 24 bits/pixel).

MEMORY READ/WRITE AND DISPLAY OPERATIONS

Image Format:

Formatting of the image's digital data must be done externally so it can be properly loaded into the SRAM. Formatting will depend on the number of bits/pixel, and the color mode to be used. Refer to tables 4–8, and the section entitled "SRAM Interface/Display Memory" for formatting information.

Memory Access:

When CD = 1, D7 of the SPI bus readback data indicates the Memory Access Grant (MAG) status. When D7 = 1, system memory is available for system use, normally granted after the present frame is completed. Bits D6–0 supply the gate array version. When CD = 0, D7–0 represents data found in SRAM at the address specified by MA19–0.

Serial Data Write to SRAM Memory:

- Set CD = 1 (Pin 21).
- Set MAR (register $1) = 1 to indicate the system would like control of the memory after the current frame is complete.
- Set PARSER (register $0) = 0 to indicate a serial data transfer.
- Set RD/WR (reg. $0) = 0, to indicate a write operation.
- Set MA19–0 (registers $6–2) to indicate the initial memory location to be written to. The address range is $80000 to $FFFFF. The address is internally latched in when register $6 is written.
- Set DN/OVR (register $0) = 1 to auto–increment the address vertically down the display. Set DN/OVR = 0 to auto–increment the address horizontally, left to right.
- The host then polls by repeatedly writing to register $F, and monitors D7 of the bytes returned on MISO (Pin 17). When the returned bytes indicates D7=1, memory access is granted.
- The host sets CD = 0, and writes the data byte for transfer to the first memory location. After this transfer, the address counter is autoincremented, and the next data byte can be written. The address counter will continue to autoincrement as long as data bytes are written.
- The host then sets CD = 1, and sets MAR = 0.

Memory access can also be requested by setting STBY (register $1) = 1. The current frame is interrupted, and grants memory access after resetting internal registers. The memory is loaded, and then STBY must be reset to 0 to resume normal display operation.

Serial Data Write to LUT Memory:

- Serial Data Write to LUT Memory: (Addressing the LUT is done by Pins 81–74, 93, and 95. Data is provided to the LUT by Pins 3–6, 8–11 via the SPI port.) See Table 9 and Figure 10.
- Set CD = 1 (Pin 21).
- Set MAR (register $1) = 1 to indicate the system would like control of the memory after the current frame is complete.
- Set PARSER (register $0) = 0 to indicate a serial data transfer.
- Set RD/WR (reg. $0) = 0, to indicate a write operation.
- Set DN/OVR = 0 to auto–increment the address horizontally, left to right.
- Set MOD1, 0 (register $1) to indicate the number of bits/color:
  - Set MOD1,0 = 10 to display data as 4 bits/color.
  - Set MOD1,0 = 11 to display data as 8 bits/color.
- Set MA19–0 to $00100 to indicate the initial memory location for the Red palette, which occupies 256 bytes when in 8 bits/pixel mode, and 16 bytes when in 4 bits/pixel mode. The address is internally latched in when register $6 is written.
- The host then polls by repeatedly writing to register $F, and monitors D7 of the bytes returned on MISO (Pin 17). When the returned bytes indicates D7=1, memory access is granted.
- The host sets CD = 0, and writes a data byte for transfer to the first red memory location. After this transfer, the address counter is autoincremented, and the next data byte can be written. The address counter will continue to autoincrement as long as data bytes are written.
- After the red palette is loaded with 16 or 256 bytes, set CD = 1, and set MA19–0 to $00200 to indicate the initial memory location for the Green palette, which occupies 256 bytes when in 8 bits/pixel mode, and 16 bytes when in 4 bits/pixel mode. The address is internally latched in when register $6 is written.
- The host sets CD = 0, and writes a data byte for transfer to the first green memory location. After this transfer, the address counter is autoincremented, and the next data byte can be written. The address counter will continue to autoincrement as long as data bytes are written.
- After the green palette is loaded, set CD = 1, and set MA19–0 to $00400 to indicate the initial memory location for the Blue palette, which occupies 256 bytes

when in 8 bits/pixel mode, and 16 bytes when in 4 bits/pixel mode. The address is internally latched in when register $6 is written.
— The host sets CD = 0, and writes a data byte for transfer to the first blue memory location. After this transfer, the address counter is autoincremented, and the next data byte can be written. The address counter will continue to autoincrement as long as data bytes are written.
— After the blue palette is loaded, the host then sets CD = 1, and sets MAR = 0.
— If the LUT's fourth page is to be used (for modes other than the Indexed Mode), it can be loaded using starting address $00300.

Memory access can also be requested by setting STBY (register $1) = 1. The current frame is interrupted, and grants memory access after resetting internal registers. The memory is loaded, and then STBY must be reset to 0 to resume normal display operation.

Parallel Data Write to SRAM Memory:

This procedure is similar to the Serial Data Write to SRAM Memory, except it can occur at a higher rate.
— Set CD = 1 (Pin 21).
— Set MAR (register $1) = 1 to indicate the system would like control of the memory after the current frame is complete.
— Set PARSER (register $0) = 1 to indicate a parallel data transfer.
— Set RD/WR (reg. $0) = 0, to indicate a write operation.
— Set MA19–0 (registers $6–2) to indicate the initial memory location to be written to. The address range is $80000 to $FFFFF. The address is internally latched in when register $6 is written.
— Set DN/OVR (register $0) = 1 to auto–increment the address vertically down the display. Set DN/OVR = 0 to auto–increment the address horizontally, left to right.
— The host then polls by repeatedly writing to register $F, and monitors D7 of the bytes returned on MISO (Pin 17). When the returned bytes indicates D7=1, memory access is granted.
— The host sets CD = 0, and writes a data byte onto the parallel bus (at Pins 29–22).
— After this transfer, the address counter is incremented by the host sending an active high pulse on the $\overline{SS}$ line (Pin 18). The next data byte is then written. The address counter will continue to increment each time the $\overline{SS}$ line is toggled low–to–high.
— When the writing is finished, the host then sets CD = 1, and sets MAR = 0.
— Memory access can also be requested by setting STBY (register $1) = 1. The current frame is interrupted, and grants memory access after resetting internal registers. The memory is loaded, and then STBY must be reset to 0 to resume normal display operation.

Serial Data Read from SRAM Memory:
— Set CD = 1 (Pin 21).
— Set MAR (register $1) = 1 to indicate the system would like control of the memory after the current frame is complete.
— Set PARSER (register $0) = 0 to indicate a serial data transfer.
— Set RD/WR (reg. $0) = 1, to indicate a read operation.
— Set MA19–0 (registers $6–2) to indicate the initial memory location to be read from. The address range is $80000 to $FFFFF. The address is internally latched in when register $6 is written.
— Set DN/OVR (register $0) = 1 to auto–increment the address vertically down the display. Set DN/OVR = 0 to auto–increment the address horizontally, left to right.
— The host then polls by repeatedly writing to register $F, and monitors D7 of the bytes returned on MISO (Pin 17). When the returned bytes indicate D7=1, memory access is granted.
— The host sets CD = 0, and writes to register $F. The data read back on the MISO line will be the data contained in the memory location designated by MA19–0.
— After this transfer, the address counter is incremented. Writing to register $F will read out the data from the next memory location.
— Repeatedly writing to register $F will increment the address counter, and read out the data.
— When the reading is complete, the host then sets CD = 1, and sets MAR = 0.

Memory access can also be requested by setting STBY (register $1) = 1. The current frame is interrupted, and grants memory access after resetting internal registers. The memory is read, and then STBY must be reset to 0 to resume normal display operation.

Parallel Data Read from SRAM Memory:

This procedure is similar to the Serial Data Read from SRAM Memory, except it occurs at a higher rate.
— Set CD = 1 (Pin 21).
— Set MAR (register $1) = 1 to indicate the system would like control of the memory after the current frame is complete.
— Set PARSER (register $0) = 1 to indicate a parallel data transfer.
— Set RD/WR (reg. $0) = 1, to indicate a read operation.
— Set MA19–0 (registers $6–2) to indicate the initial memory location to be read from. The address range is $80000 to $FFFFF. The address is internally latched in when register $6 is written.
— Set DN/OVR (register $0) = 1 to auto–increment the address vertically down the display. Set DN/OVR = 0 to auto–increment the address horizontally, left to right.
— The host then polls by repeatedly writing to register $F, and monitors D7 of the bytes returned on MISO (Pin 17). When the returned bytes indicate D7=1, memory access is granted.
— The host sets CD = 0, and reads the data off the parallel data bus (at Pins 29–22). The data will be that at the location specified by MA19–0.
— After this transfer, the address counter is incremented by the host sending an active high pulse on the $\overline{SS}$ line (Pin 18). The next data byte is then read. The address counter will continue to increment each time the $\overline{SS}$ line is toggled low–to–high.
— When the reading is finished, the host then sets CD = 1, and sets MAR = 0.

Memory access can also be requested by setting STBY (register $1) = 1. The current frame is interrupted, and grants memory access after resetting internal registers. The

memory is read, and then STBY must be reset to 0 to resume normal display operation.

Display from SRAM Memory Location:

— Set CD = 1 (Pin 21).
— Set STBY (register $1) = 1 to stop display activity.
— Set MOD1, 0 (register $1) to indicate the number of bits/pixel (monochrome applications), or the number of bits/color (color applications):
  – Set MOD1,0 = 00 to display data as 1 bit/pixel or color.
  – Set MOD1,0 = 01 to display data as 2 bits/pixel or color.
  – Set MOD1,0 = 10 to display data as 4 bits/pixel or color.
  – Set MOD1,0 = 11 to display data as 8 bits/pixel or color.
— Set the CLR/MONO and White bits (register $E) to set the desired color mode (table 10).
— Set DA18–0 (register $7–B) to indicate the initial SRAM memory address contents to be supplied to the display. The memory range is $00000 to $7FFFF.
— Set MAR (register $1) = 0 to permit display from memory.
— Set STBY (register $1) = 0 to permit display from memory. The display will now be active.

The MCVVQ201 will retrieve the SRAM data starting at the address specified by DA18–0, and will repeatedly cycle through that portion of the memory containing the image. The memory space allocated to the image is defined by the color mode, and the number of bits/pixel (tables 4–7, and 10).

The data is provided to Pins 81–74, which are connected to either the DAC inputs on the MCVVQ101 Analog Driver, or the address inputs on the LUT. The data at Pins 81–74 depends not only on the data retrieved from the SRAM, but also on the number of bits/pixel selected with control bits MOD1 and MOD0. Table 11 indicates how the data is output. Note that the gray scale increments are equal value for each bit/pixel selection.

If a LUT is part of the system, and the indexed mode is selected (CLR/MONO = WHITE = 1), the SRAM will contain one frame of image data. The MCVVQ201 will provide the image data to the LUT, with LA9 and LA8 set at 00 to select the Blue color palette (see Table 9). When the image is complete, and after a 1.3 msec delay, the blue LED is strobed via the BCTL pin. LA9 and LA8 will then change to select the Red color palette, and the same image data will again be provided to the LUT. When the image is complete, and after a 1.3 msec delay, the red LED is strobed via the RCTL pin. Then LA9 and LA8 will change to select the Green color palette, and the same image data will again be provided to the LUT. When the image is complete, and after a 1.3 msec delay, the green LED is strobed via the GCTL pin. Then the cycle will repeat.

If the non–indexed color mode is selected (CLR/MONO = 1, WHITE = 0), the SRAM will contain three frames, i.e., image data for each of the three colors. The first set of image data (red data) is retrieved from the SRAM starting at the address specified by DA18–0, and supplied out to Pins 81–74. When the red image data is complete, and after a 1.3 msec delay, the red backlight LED is strobed via the RCTL pin (Pin 98). Then the green image data is retrieved from the next memory space in the SRAM, and after a 1.3 msec delay, the green LED is strobed via the GCTL pin (Pin 97). Then the blue image data is retrieved from the next memory space in the SRAM, and after a 1.3 msec delay, the blue LED is strobed via the BCTL pin (Pin 96). Then the cycle will repeat.

If the Color–White mode is selected (CLR/MONO = 0, WHITE = 1), the SRAM will contain one frame of image data. The MCVVQ201 will provide the image data to Pins 81–74. After a 1.3 msec delay, the red LED is strobed via the RCTL pin (Pin 98). Then the same image data is provided to Pins 81–74, and after a 1.3 msec delay, the green LED is strobed via the GCTL pin (Pin 97). Then the same image data is provided to Pins 81–74 for a third time, and after a 1.3 msec delay, the blue LED is strobed via the BCTL pin (Pin 96). Then the cycle will repeat.

If the Monochrome mode is selected (CLR/MONO = WHITE = 0), the SRAM will contain one frame of image data. The MCVVQ201 will provide the image data to Pins 81–74, and with no delay, the backlight's single LED is strobed. Then the cycle will repeat.

If the non–indexed color mode, the color–white mode, or the monochrome mode is selected, and an external LUT is not part of the system, then Pins 81–74 (DAC7–DAC0) should be connected to the D7–D0 pins on the MCVVQ101 Analog Driver, and the DCLK output (Pin 83) should be connected to the DCLK input on the MCVVQ101 (see Figure 9). If a LUT is part of the system when selecting one of these three modes, then Pins 81–74 will connect to the address input pins on the LUT, and the LUT's data output will connect to the D7–D0 input pins on the MCVVQ101. The DCLK output will connect to the DCLK input on the MCVVQ101 (see Figure 10). In these three modes, the color page selection pins (LA8,9, Pins 93, 95) will stay at 11 (see Table 9).

Table 11. Data Format at Pins 81–74

Bits/Pixel	Retrieved SRAM Data	Output at Pins 81–74	Hex Equivalent	Decimal Equivalent	LCD Display
8	D7 D6 – – D1 D0	D7 D6 – – D1 D0	00 – FF	0 – 255	256 Levels
4	0000	0000 0000	00	0	Black
	0001	0001 0001	11	17	14 Levels of Gray Scale
	0010	0010 0010	22	34	
	– –	– –	– –	– –	
	– –	– –	– –	– –	
	1110	1110 1110	EE	238	
	1111	1111 1111	FF	255	White
2	00	0000 0000	0	0	Black
	01	0101 0101	55	85	2 Levels of Gray Scale
	10	1010 1010	AA	170	
	11	1111 1111	FF	255	White
1	0	0000 0000	00	0	Black
	1	1111 1111	FF	255	White

Figure 9. System Configuration without LUT
(Typically for Monochrome, Color–White, and Non–Indexed Color Modes)

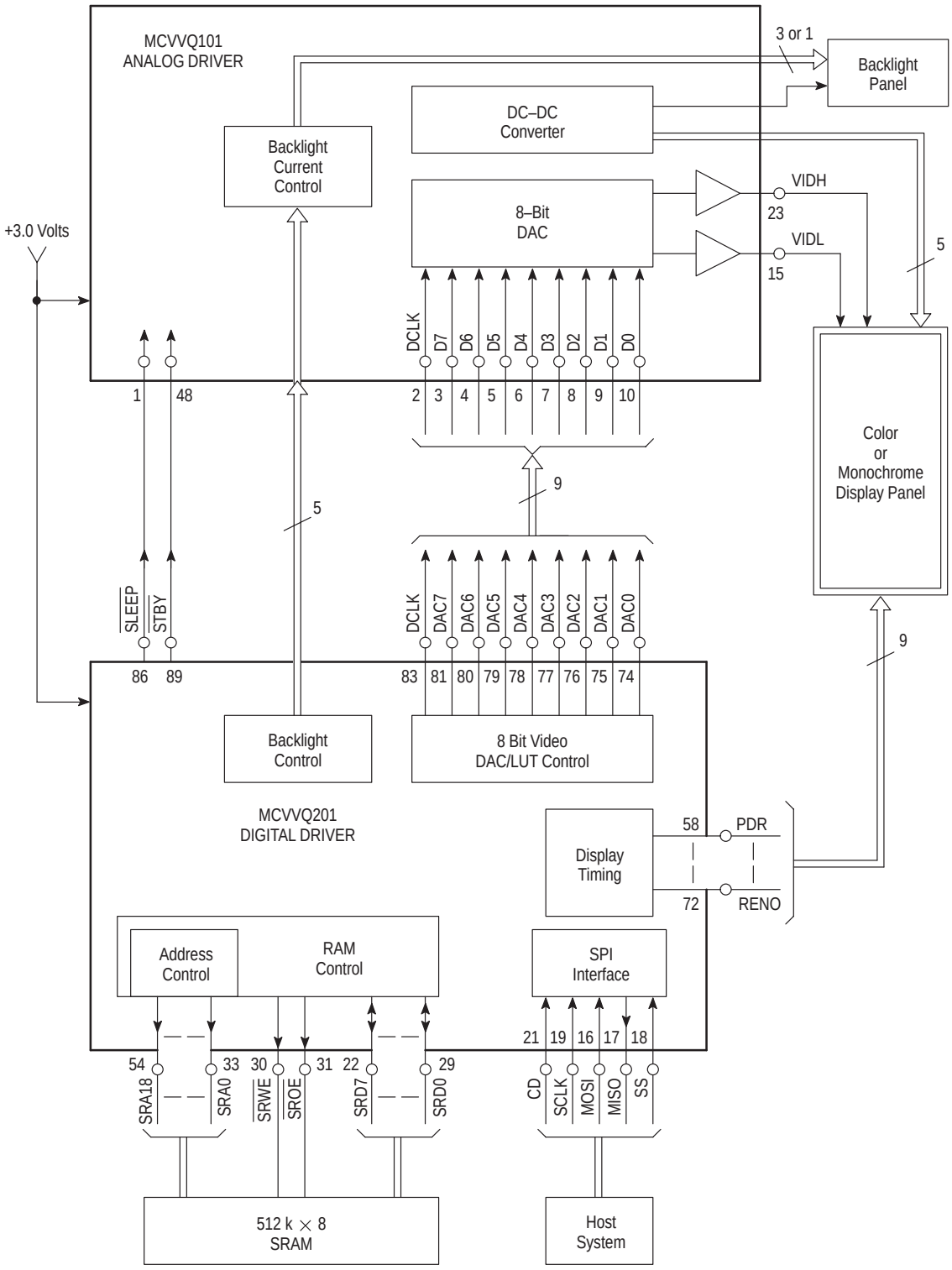
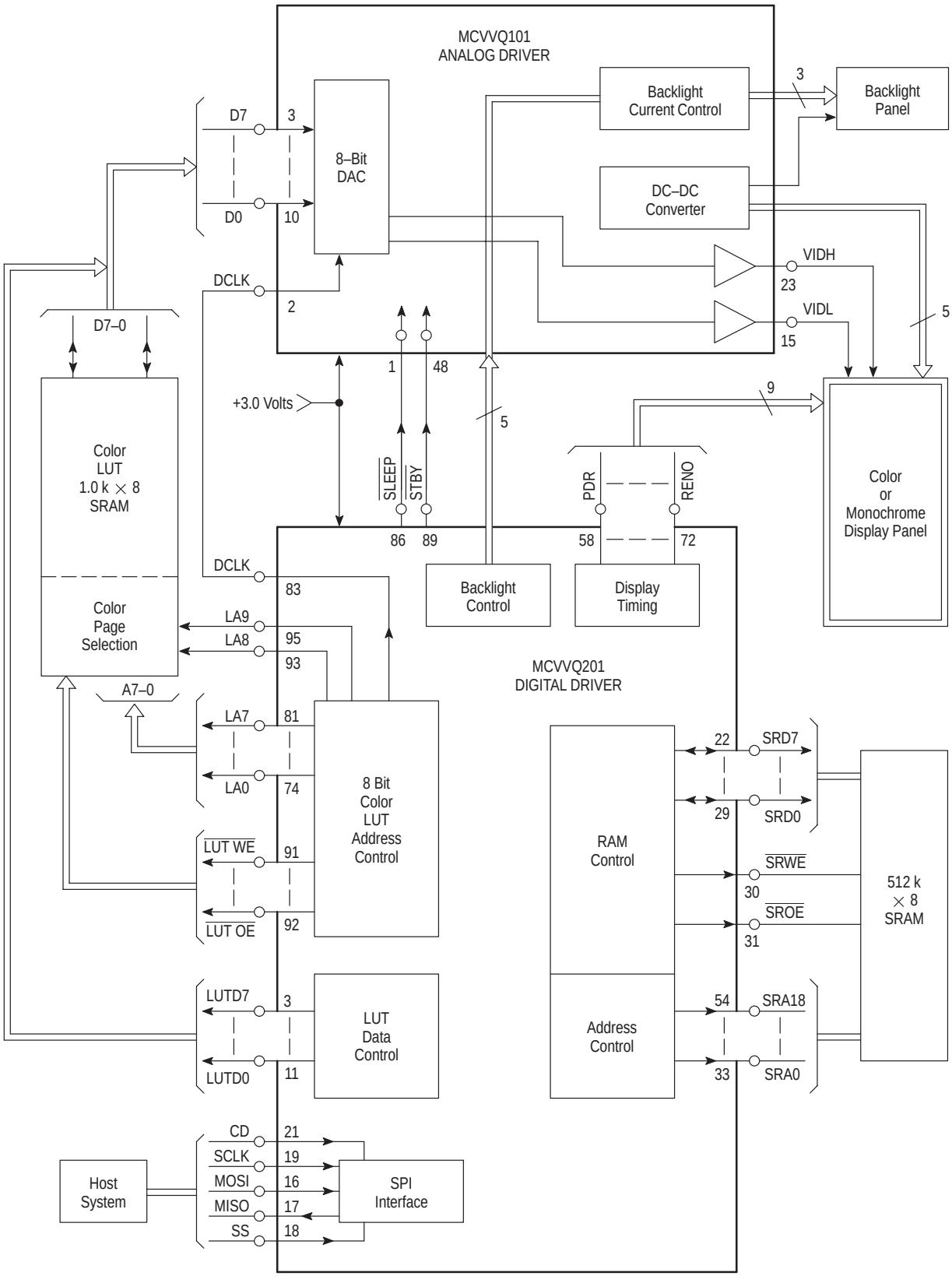


Figure 10. System Configuration with LUT (Typically for the Indexed Color Mode)



SLEEP, STANDBY MODES

The Standby and Sleep modes are set in control registers $1 and $C, respectively, and affect power consumption of the MCVVQ101 Analog Driver, the LCD panel, and the backlight panel. Refer to the MCVVQ101 data sheet for more details.

In the Standby mode (STBY = 1), Pin 89 is set low. Through the MCVVQ101 Analog Driver, the backlight LED(s) are shut off, and video information to the LCD panel is taken to white and held there. Recovery time to normal operation is minimal.

In the Sleep mode (STOP = 1), timing signals to the LCD display panel, and Pin 86, are held low. Through the MCVVQ101 Analog Driver, the backlight LED(s) are shut off, and the MCVVQ101's DC–DC converter is shut down, removing all power supply voltages from the LCD panel. All sections in the MCVVQ101 are unpowered. There is a recovery time to normal operation of approximately xx mS.

Power consumption within the MCVVQ201 is not changed when either mode is selected.

OPERATIONAL EXAMPLE

The following example illustrates the steps to serially load an image, and then display it, starting at SRAM's location $12345 (memory map location $92345), using 4 bits/pixel.

Loading memory:

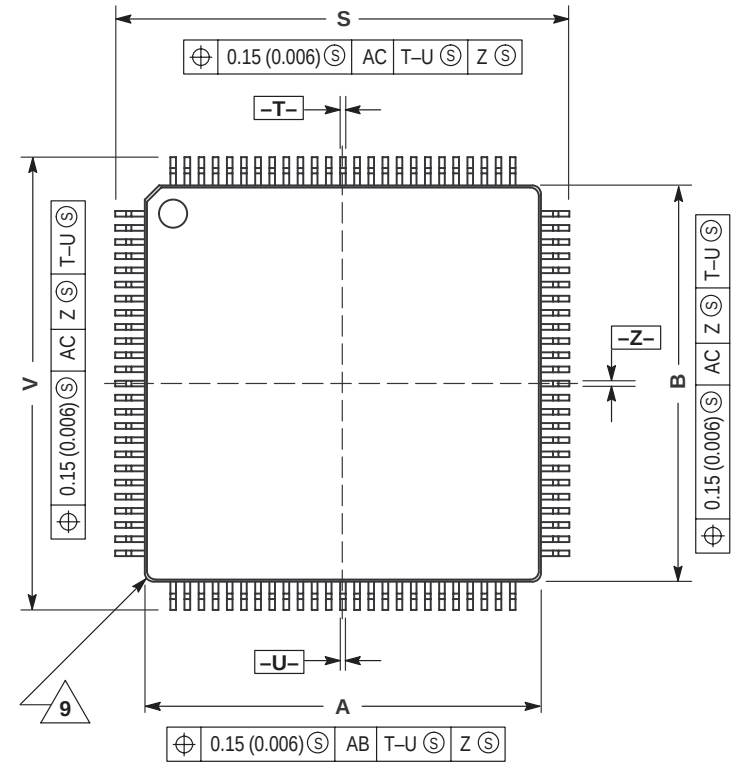
- Set CD = 1 (Pin 21) to allow writing to the control registers.
- Write 16h over the SPI bus. This writes 6h to register 1, setting STBY high, thereby clearing undefined counter states which may have occurred at power up. MOD1,0 are set to 10, selecting 4 bits/pixel. Memory access is not requested at this time.
- Write 25h over the SPI bus. Writes $5 into the least significant nibble of the starting memory location (MA3–0).
- Write 34h over the SPI bus. Writes 4 into the starting memory location (MA7–4).
- Write 43h over the SPI bus. Writes 3 into the starting memory location (MA11–8).
- Write 52h over the SPI bus. Writes 2 into the starting memory location (MA15–12).
- Write 69h over the SPI bus. Writes 9 into the most significant nibble of the starting memory location (MA19–16). The starting address (92345h) is internally latched when this register is written.
- Write 00h over the SPI bus. This sets a serial write operation, incrementing horizontally across the memory space.
- At this point, all pertinent controls bits have been set.
- Set CD = 0 (Pin 21). SPI writes will now be directed to the SRAM.
- Write 38400 bytes of image data over the SPI bus for loading into the SRAM. The internal memory address autoincrements after each byte is written. One QVGA monochrome picture is defined by these bytes.
- Set CD = 1 (Pin 21).

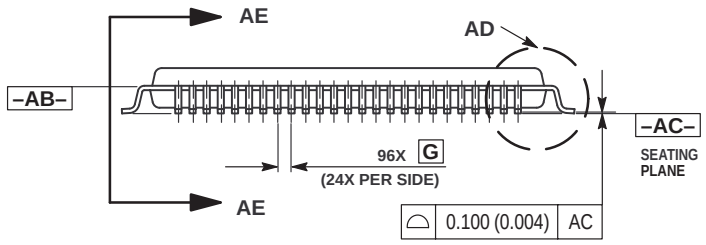
Displaying the image:

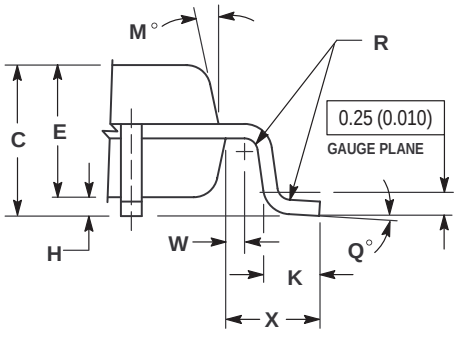
- With CD = 1, write C4h over the SPI bus. This sets HLTR = 1, establishing a left–to–right scanning order for the LCD display (Pin 66 is set high).
- Write 75h over the SPI bus. Writes 5 into the LSB of the starting memory location (DA3–0).
- Write 84h over the SPI bus. Writes 4 into the LSB of the starting memory location (DA7–4).
- Write 93h over the SPI bus. Writes 3 into the LSB of the starting memory location (DA11–8).
- Write A2h over the SPI bus. Writes 2 into the LSB of the starting memory location (DA15–12).
- Write B1h over the SPI bus. Writes 1 into the LSB of the starting memory location (DA18–16). This provides the starting SRAM address from which the display information will be drawn.
- Write D2h over the SPI bus. This sets a nominal clock delay value.
- Write E3h over the SPI bus. This selects the monochrome mode, and maximum intensity for the backlight LEDs.
- Write 12h over the SPI bus. This maintains MOD1,0 at 4 bits/pixel, while clearing the STBY bit. At this point, the MCVVQ201 begins feeding the image data from the SRAM to the display, at the rate of two pixels/byte. The MCVVQ201 will repeatedly cycle through the 38400 bytes which make up the full image.

OUTLINE DIMENSIONS

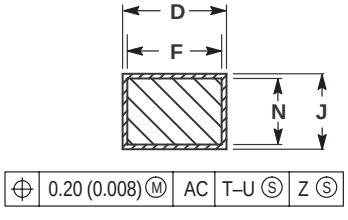
FB SUFFIX
PLASTIC PACKAGE
CASE 842F–01
ISSUE O







DETAIL AD



SECTION AE–AE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014). DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.070 (0.003).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	13.950	14.050	0.549	0.553
B	13.950	14.050	0.549	0.553
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BSC		0.020 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	15.950	16.050	0.628	0.632
V	15.950	16.050	0.628	0.632
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

NOTES

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