Document Number: MHVIC2115NR2
Rev. 5, 5/2006

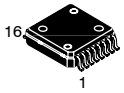
RoHS

RF LDMOS Wideband Integrated Power Amplifier

MHVIC2115NR2

The MHVIC2115NR2 wideband integrated circuit is designed for base station applications. It uses Freescale's newest High Voltage (26 to 28 Volts) LDMOS IC technology and integrates a multi-stage structure. Its wideband On-Chip matching design makes it usable from 1600 to 2600 MHz. The linearity performances cover W-CDMA modulation formats.

2170 MHz, 26 V, 23/34 dBm
W-CDMA
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIER



CASE 978-03
PFP-16

Final Application

- Typical W-CDMA Performance: -45 dBc ACPR, 2110-2170 MHz, V_{DD} = 27 Volts, I_{DQ1} = 56 mA, I_{DQ2} = 61 mA, I_{DQ3} = 117 mA, P_{out} = 34 dBm, 3GPP Test Model 1, Measured in 1.0 MHz BW @ 4 MHz offset, 64 DTCH
  Power Gain — 30 dB
  PAE = 16%

Driver Application

- Typical W-CDMA Performance: -53 dBc ACPR, 2110-2170 MHz, V_{DD} = 26 Volts, I_{DQ1} = 96 mA, I_{DQ2} = 204 mA, I_{DQ3} = 111 mA, P_{out} = 23 dBm, 3GPP Test Model 1, Measured in 3.84 MHz BW @ 5 MHz offset, 64 DTCH
  Power Gain — 34 dB
- Gain Flatness = 0.3 dB from 2110-2170 MHz
- P1dB = 15 Watts, Gain Flatness = 0.2 dB from 2110-2170 MHz
- Capable of Handling 3:1 VSWR, @ 26 Vdc, 2140 MHz, 15 Watts CW Output Power

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >5 Ohm Output)
- Integrated Temperature Compensation with Enable/Disable Function
- Integrated ESD Protection
- RoHS Compliant
- In Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Operating Junction Temperature	T_J	150	°C

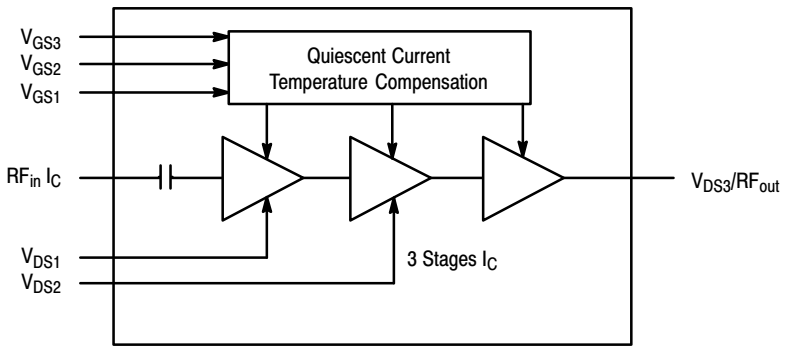
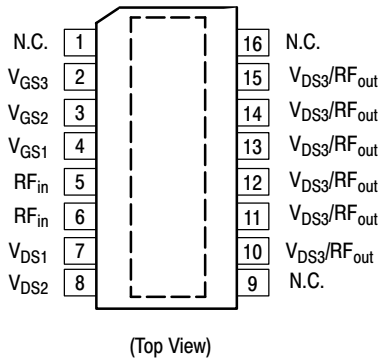


Figure 1. Block Diagram



(Top View)

Note: Exposed backside flag is source terminal for transistors.

Figure 2. Pin Connections

freescale semiconductor

Table 2. Thermal Characteristics

Characteristic		Symbol	Value	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
Driver Application (P_{out} = +0.2 W CW)	Stage 1, 26 Vdc, I_{DQ} = 96 mA Stage 2, 26 Vdc, I_{DQ} = 204 mA Stage 3, 26 Vdc, I_{DQ} = 111 mA		3.5	
Output Application (P_{out} = +2.5 W CW)	Stage 1, 27 Vdc, I_{DQ} = 56 mA Stage 2, 27 Vdc, I_{DQ} = 61 mA Stage 3, 27 Vdc, I_{DQ} = 117 mA		2.7	

Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)
Charge Device Model	C2 (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
W-CDMA Characteristics (In Freescale Test Fixture, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ1} = 96 mA, I_{DQ2} = 204 mA, I_{DQ3} = 111 mA, P_{out} = 23 dBm, 2110-2170 MHz					
Power Gain	G_{ps}	31	34	—	dB
Gain Flatness	G_F	—	0.3	0.5	dB
Input Return Loss	IRL	—	-12	-10	dB
Group Delay	—	—	1.7	—	ns
Phase Linearity	—	—	0.2	—	°
1-Carrier W-CDMA Conditions: Adjacent Channel Power Ratio @ P_{out} = 23 dBm, 5 MHz Offset	ACPR	—	-53	-50	dBc
1-Carrier W-CDMA Conditions: Adjacent Channel Power Ratio @ P_{out} = 28 dBm, 5 MHz Offset	ACPR	—	-50	—	dBc
W-CDMA Characteristics (In Freescale Test Fixture, 50 ohm system) V_{DD} = 27 Vdc, I_{DQ1} = 56 mA, I_{DQ2} = 61 mA, I_{DQ3} = 117 mA, P_{out} = 34 dBm, 2110-2170 MHz					
Power Gain	G_{ps}	—	30	—	dB
Gain Flatness	G_F	—	0.2	—	dB
Input Return Loss	IRL	—	-12	—	dB
Power Added Efficiency	PAE	—	16	—	%
1-Carrier W-CDMA Conditions: Adjacent Channel Power Ratio @ P_{out} = 34 dBm, 4 MHz Offset	ACPR	—	-45	—	dBc

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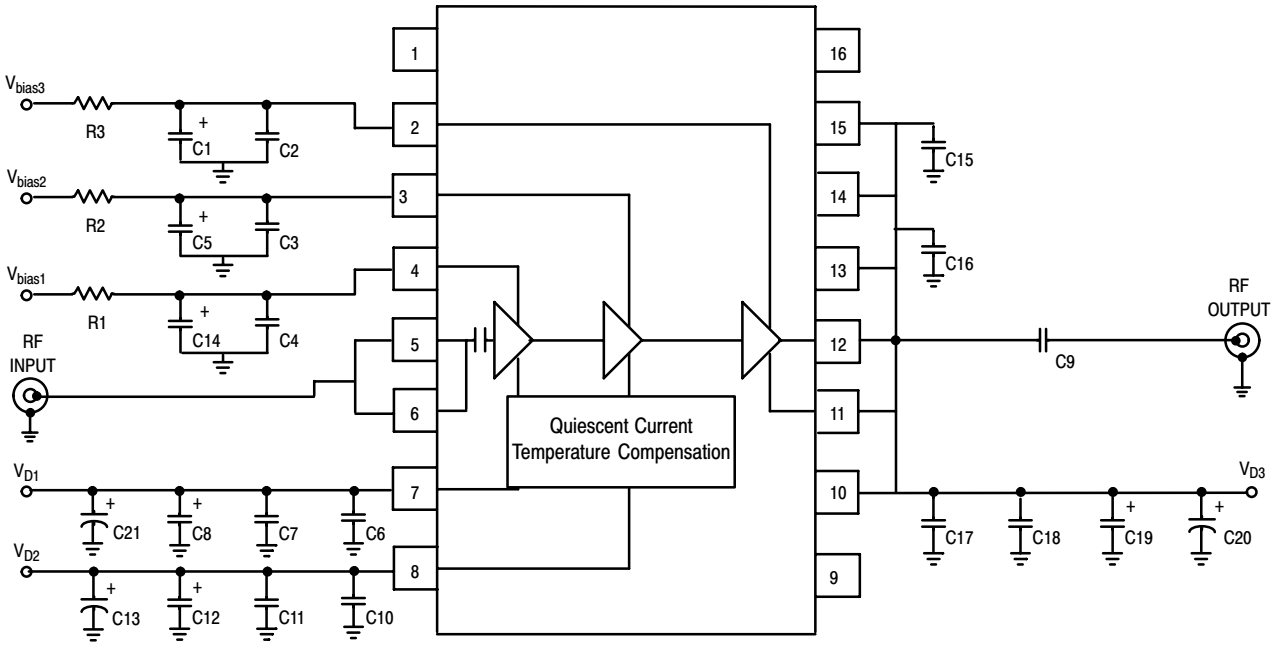

C1, C5, C8, C12, C14, C19	1 mF SMT Tantalum Chip Capacitors	C13, C20, C21	330 mF Electrolytic Capacitors (MCR35V337M10X16)
C2, C3, C4, C7, C11, C18	0.01 mF Chip Capacitors (0805C103K5RACTR)		
C6, C10, C17	6.8 pF Chip Capacitors, ACCU-P (AVX 08051J6R8BBT)	R1, R2, R3	1 kW Chip Resistors (0805)
C9, C15, C16	1.8 pF Chip Capacitors, ACCU-P (AVX 08051J1R8BBT)	PCB	Arlon, 0.020,, e_r = 2.55

Figure 3. MHVIC2115NR2 Demo Board Schematic

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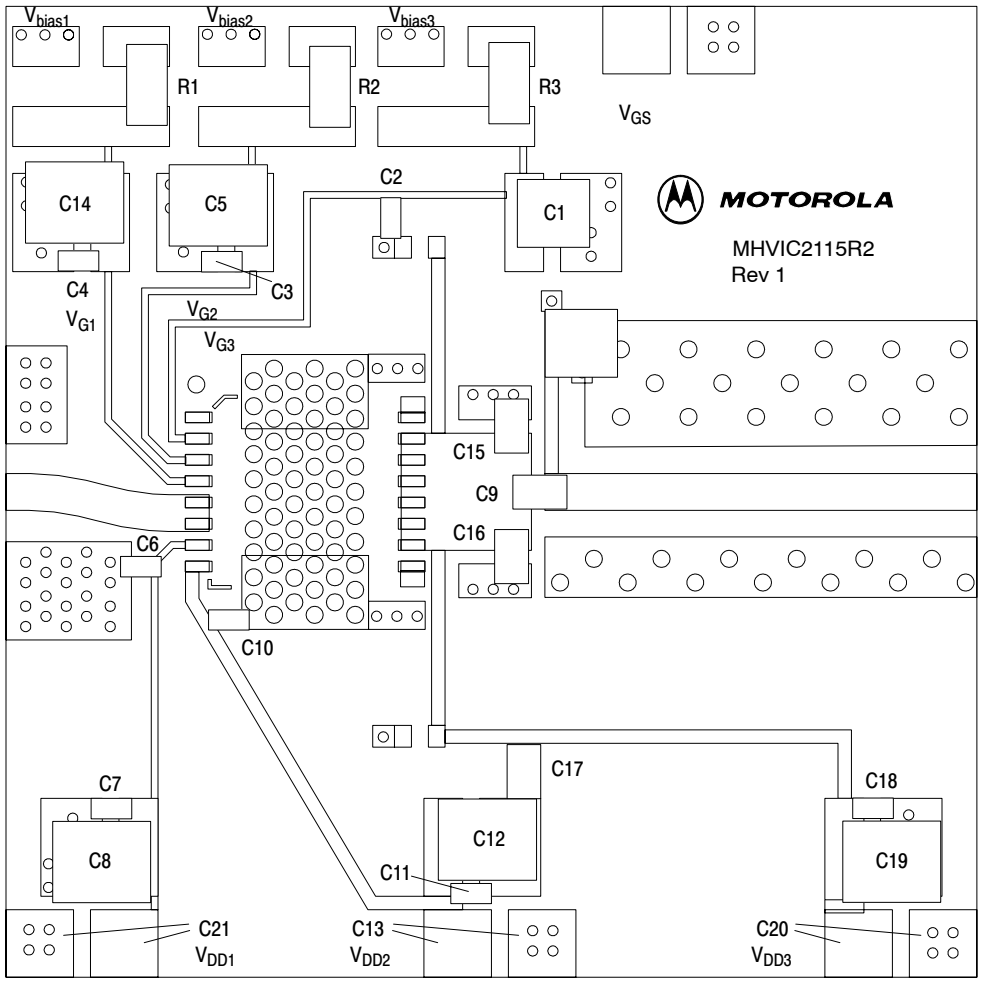

Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 4. MHVIC2115NR2 Demo Board Component Layout

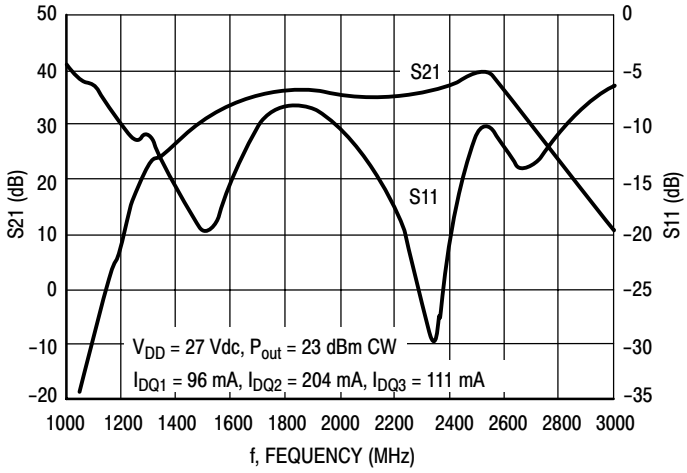

Figure 5. Broadband Frequency Response

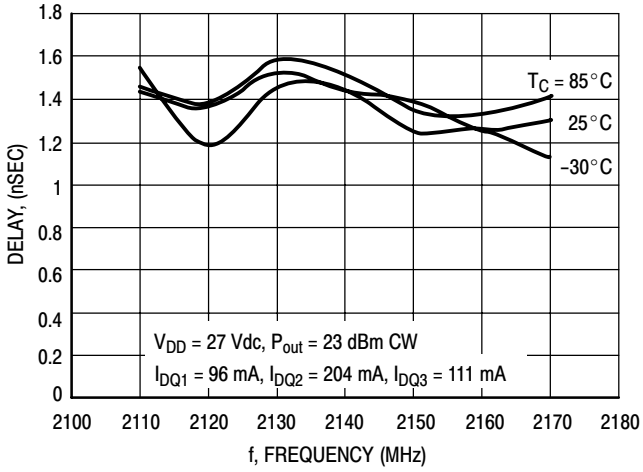

Figure 6. Delay versus Frequency

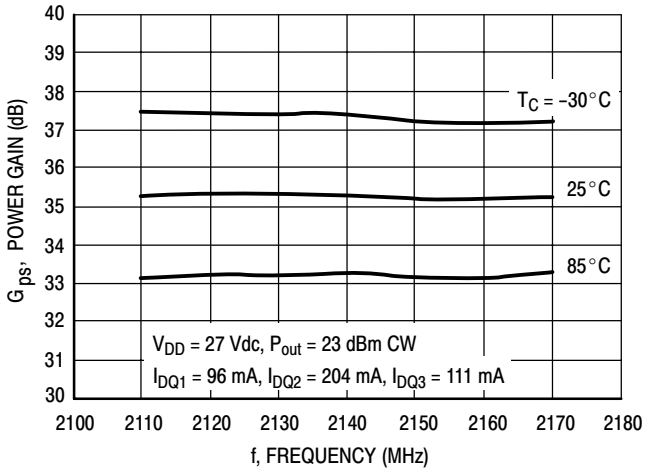

Figure 7. Power Gain versus Frequency

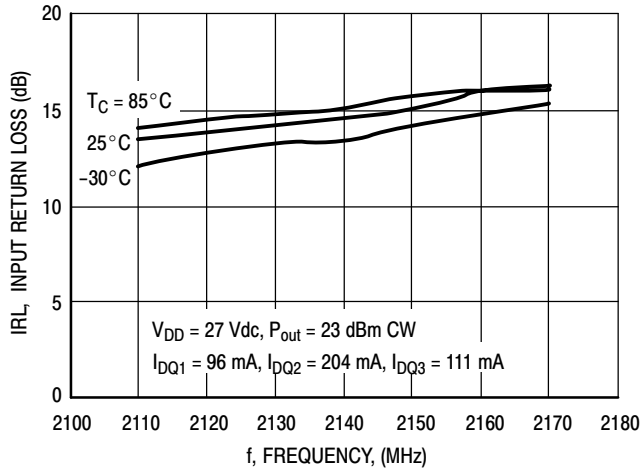

Figure 8. Input Return Loss versus Frequency

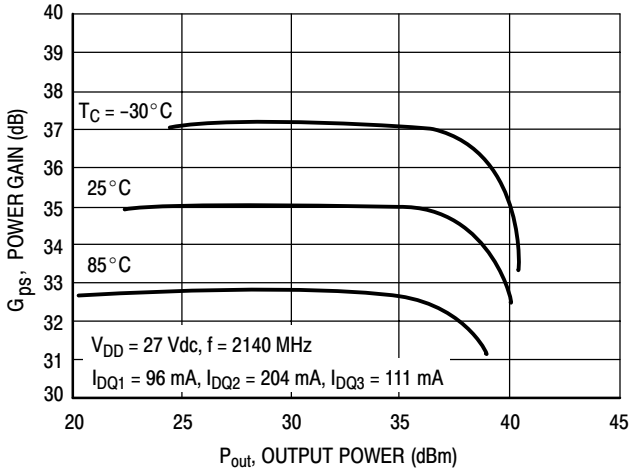

Figure 9. Power Gain versus Output Power

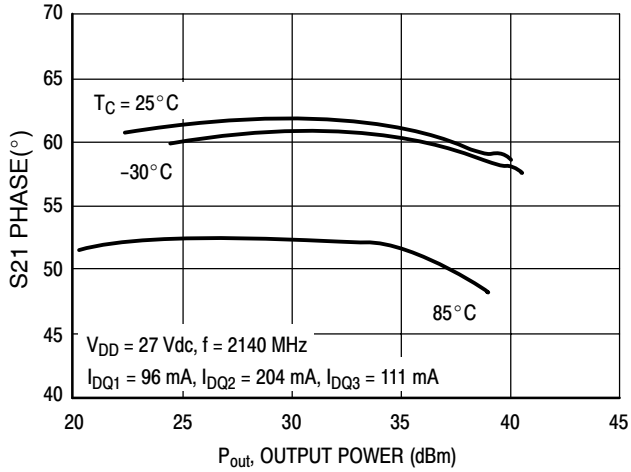

Figure 10. S21 Phase versus Output Power

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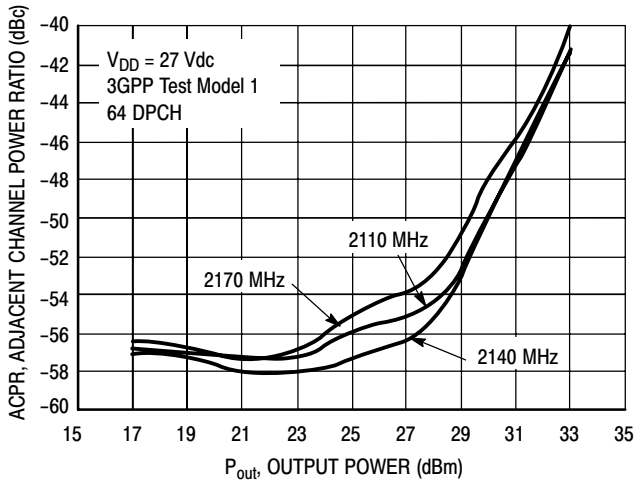

Figure 11. W-CDMA ACPR versus Output Power

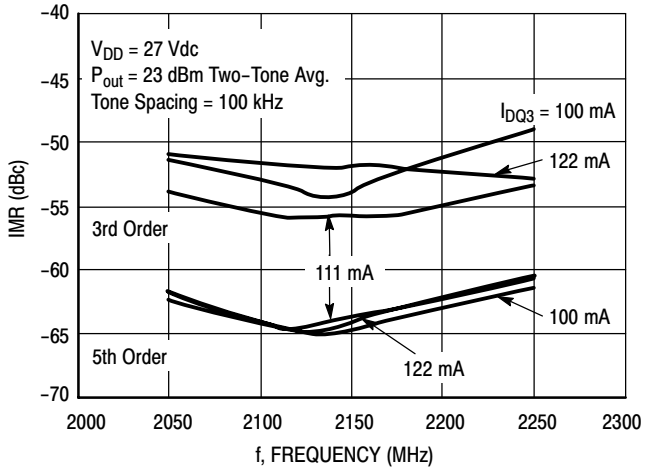

Figure 12. Two-Tone IMR versus Frequency

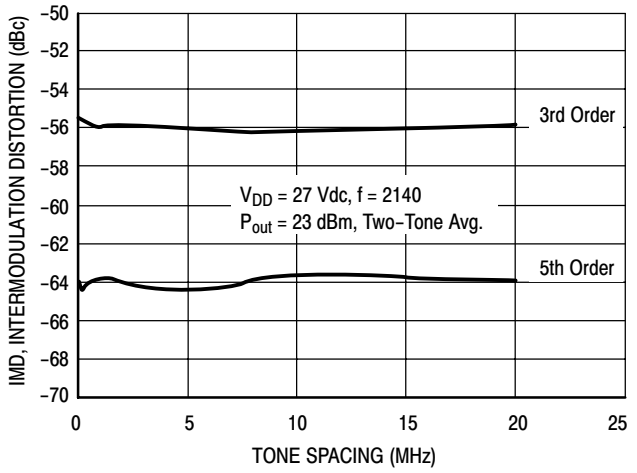

Figure 13. Two-Tone Broadband Performance

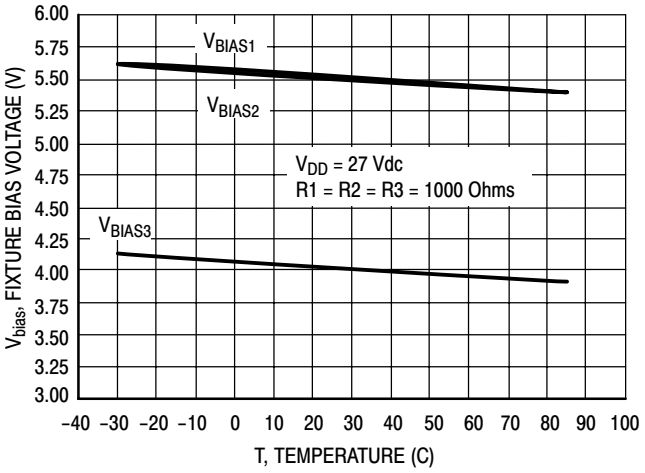

Figure 14. Fixture Bias versus Temperature

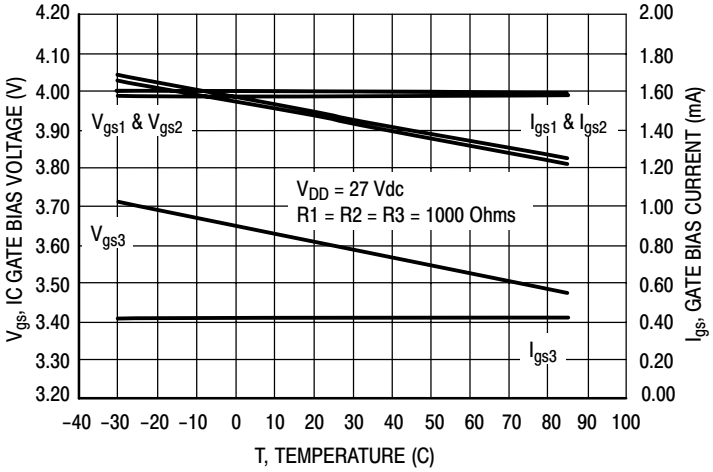

Figure 15. Gate Bias versus Temperature

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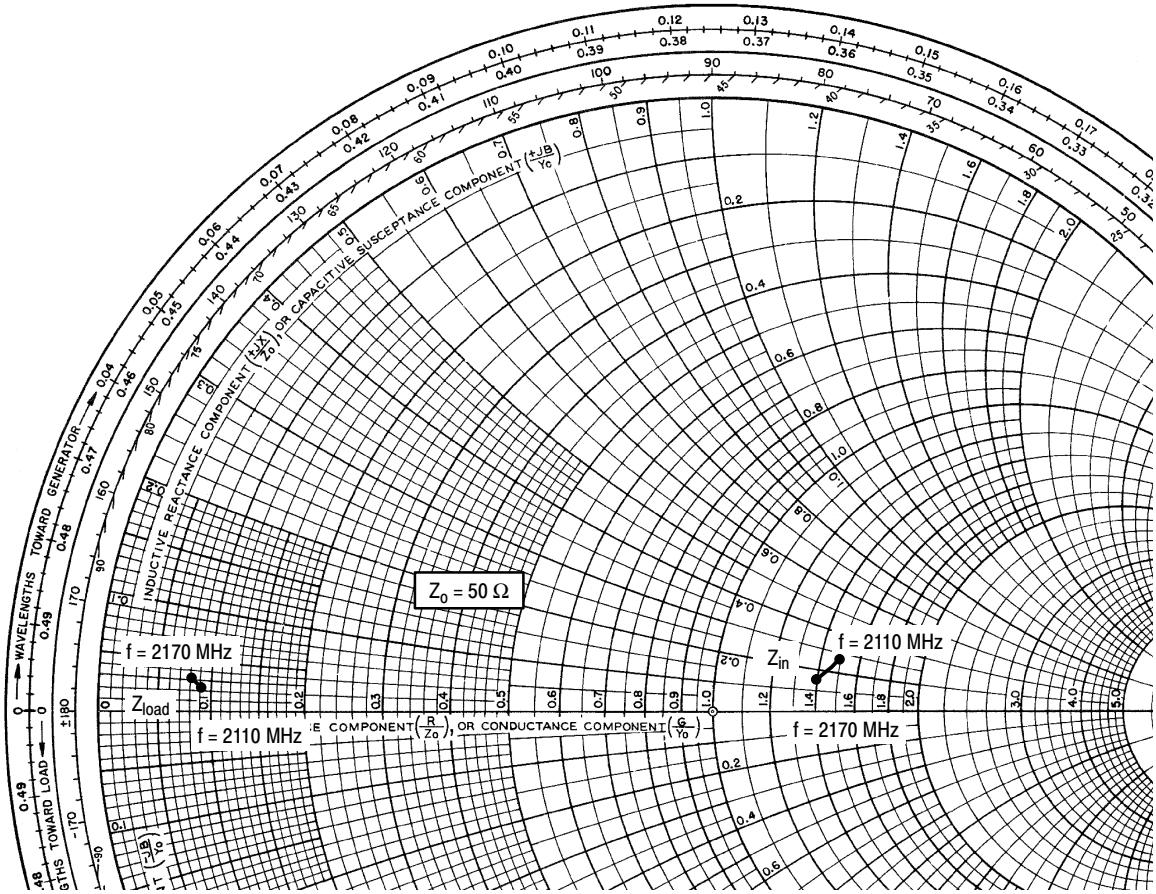

V_{DD} = 27 Vdc, I_{DQ} = 1411 mA, P_{out} = 15 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
2110	72.55 + j12.8	4.25 + j1.00
2140	71.40 + j9.9	4.13 + j1.37
2170	70.20 + j7.1	4.12 + j1.46

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

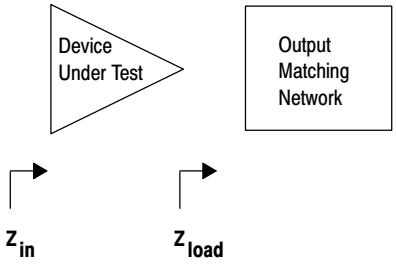

Figure 16. Series Equivalent Input and Load Impedance

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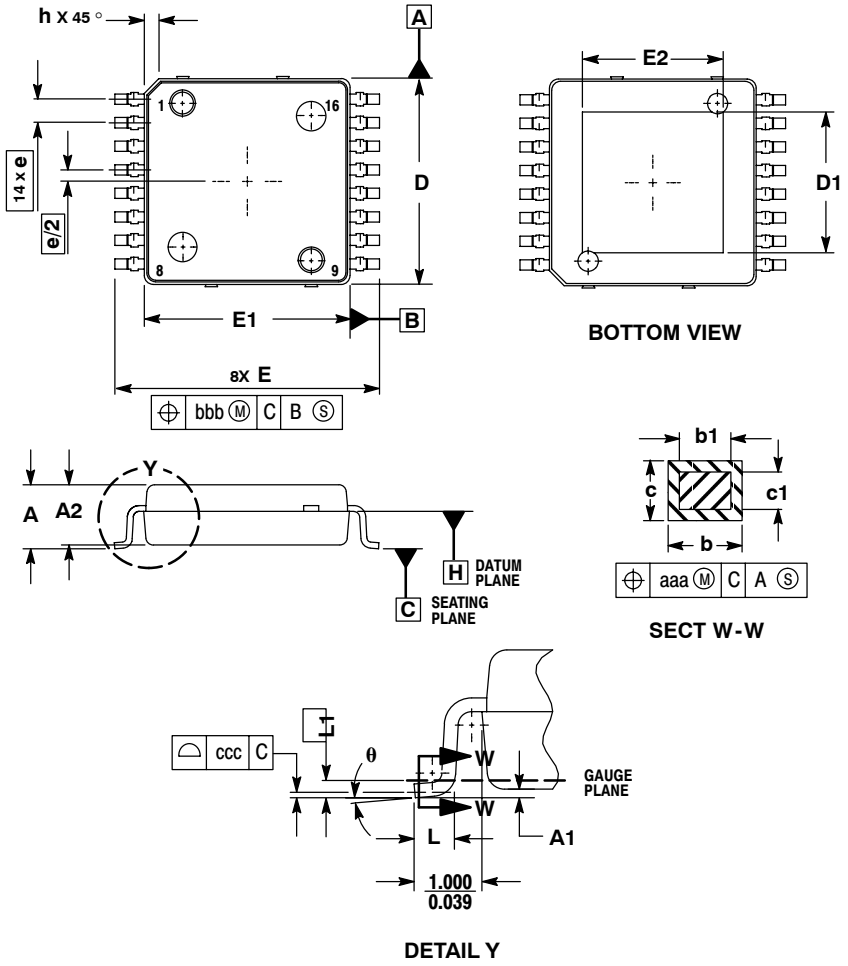
PACKAGE DIMENSIONS



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.300
A1	0.025	0.100
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	---	0.600
θ	0 °	7 °
aaa	0.200	
bbb	0.200	
ccc	0.100	

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