. .'eescale Semiconductor
Technical Data

Document Number: MMG20271H
Rev. 1, 9/2014

RoHS

Enhancement Mode pHEMT Technology (E-pHEMT)

High Linearity Amplifier

MMG20271HT1

1500-2700 MHz, 16 dB
27.5 dBm
E-pHEMT LNA/GPA

QFN 3 × 3

The MMG20271H is a high dynamic range, low noise amplifier MMIC, housed in a QFN 3 × 3 standard plastic package. It is ideal for Cellular, PCS, LTE, TD-SCDMA, W-CDMA base station, wireless LAN and other systems in the 1500 to 2700 MHz frequency range. With high OIP3 and low noise figure, it can be utilized as a driver amplifier in the transmit chain and as a second stage LNA in the receive chain.

Features

- Frequency: 1500-2700 MHz
- Noise Figure: 1.7 dB @ 2140 MHz
- P1dB: 27.5 dBm @ 2140 MHz
- Small-Signal Gain: 16 dB @ 2140 MHz
- Third Order Output Intercept Point: 42 dBm @ 2140 MHz
- Single 5 V Supply
- Supply Current: 180 mA
- 50 Ohm Operation (some external matching required)
- Cost-effective 12-pin, 3 mm QFN Surface Mount Plastic Package
- In Tape and Reel. T1 Suffix = 1,000 Units, 12 mm Tape Width, 7-inch Reel.

Table 1. Typical Performance (1)

Characteristic	Symbol	1500 MHz	2140 MHz	2700 MHz	Unit
Noise Figure	NF	2.0	1.7	1.9	dB
Input Return Loss (S11)	IRL	-16	-14	-17	dB
Output Return Loss (S22)	ORL	-20	-22	-17	dB
Small-Signal Gain (S21)	G_p	18	16	14	dB
Power Output @ 1dB Compression	P1db	27	27.5	28	dBm
Third Order Input Intercept Point	IIP3	22	26	28	dBm
Third Order Output Intercept Point	OIP3	40	42	42	dBm

1. V_{DD} = 5 Vdc, T_A = 25°C, 50 ohm system, application circuit tuned for specified frequency.

Table 2. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	6	V
Supply Current	I_{DD}	400	mA
RF Input Power	P_{in}	25	dBm
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature	T_J	175	°C

Table 3. Thermal Characteristics

Characteristic	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case Case Temperature 96°C, 5 Vdc, 190 mA, no RF applied	$R_{\theta JC}$	38	°C/W

2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

freescale

Table 4. Electrical Characteristics (V_{DD} = 5 Vdc, 2140 MHz, T_A = 25°C, 50 ohm system, in Freescale Application Circuit)

Characteristic	Symbol	Min	Typ	Max	Unit
Small-Signal Gain (S21)	G_p	13.9	16	—	dB
Input Return Loss (S11)	IRL	—	-14	—	dB
Output Return Loss (S22)	ORL	—	-22	—	dB
Power Output @ 1dB Compression	P1dB	—	27.5	—	dBm
Third Order Input Intercept Point	IIP3	—	26	—	dBm
Third Order Output Intercept Point	OIP3	—	42	—	dBm
Reverse Isolation (S12)	|S12|	—	-23	—	dB
Noise Figure	NF	—	1.7	—	dB
Supply Current	I_{DD}	148	180	227	mA
Supply Voltage	V_{DD}	—	5	—	V

Table 5. Functional Pin Description

Name	Pin Number	Description
RF_{in} (1)	3	RF input for the power amplifier. RF_{in} has an RF choke to ground internal to the package. No external blocking is necessary unless externally applied DC is present on the trace.
RF_{out}/ V_{DD}	8, 9	RF output for the power amplifier. This pin is DC coupled and requires a DC blocking capacitor.
V_{BA}	12	Bias voltage and current adjust pin.
GND	Backside Center Metal	The center metal base of the QFN package provides both DC and RF ground as well as the heat sink contact for the IC.

1. The RF input has a DC path to ground and therefore may require an external decoupling capacitor.

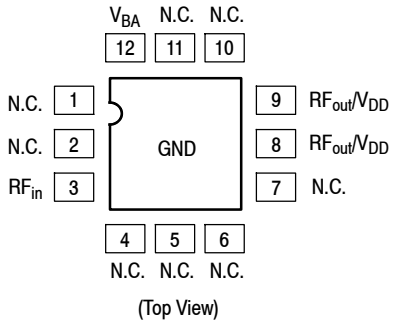


Figure 1. Pin Connections

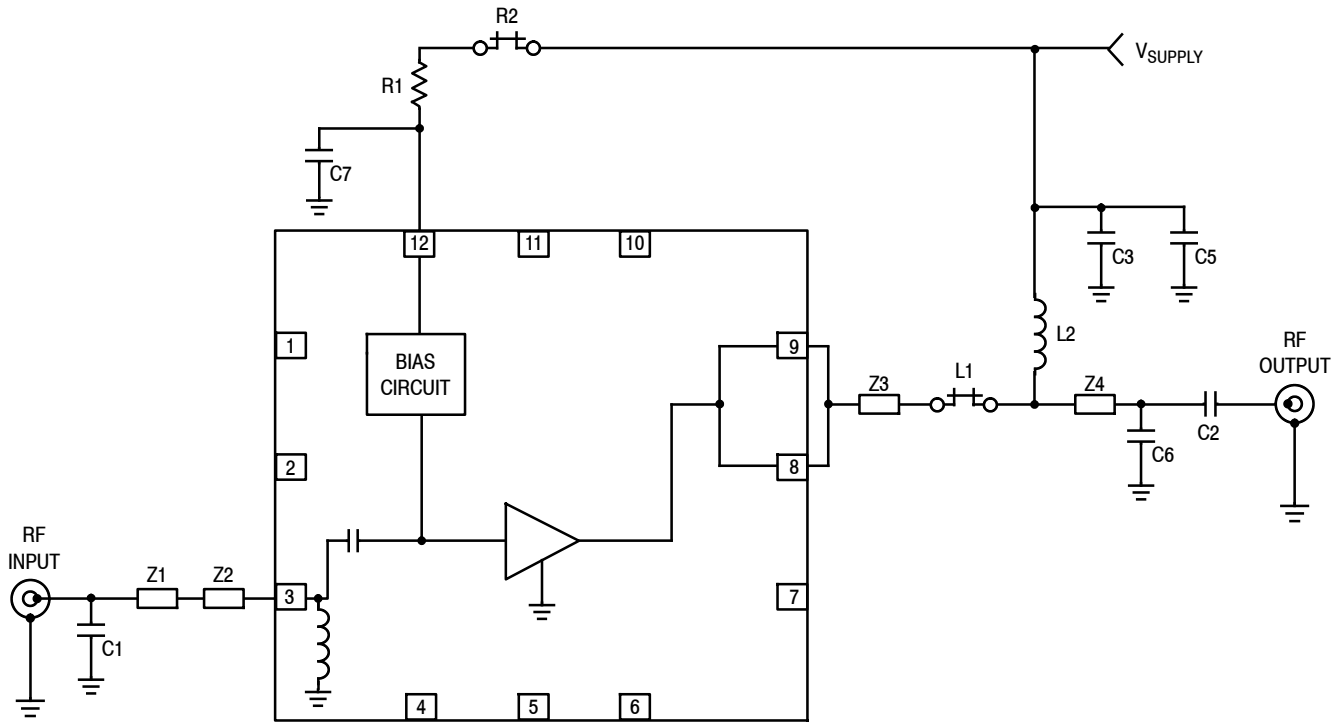
Table 6. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD 22-A114)	1B
Machine Model (per EIA/JESD 22-A115)	A
Charge Device Model (per JESD 22-C101)	IV

Table 7. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	1	260	°C

50 OHM APPLICATION CIRCUIT: 2140 MHz



Z1	0.139″ x 0.021″ Microstrip	Z3	0.041″ x 0.030″ Microstrip
Z2	0.026″ x 0.011″ Microstrip	Z4	0.198″ x 0.021″ Microstrip

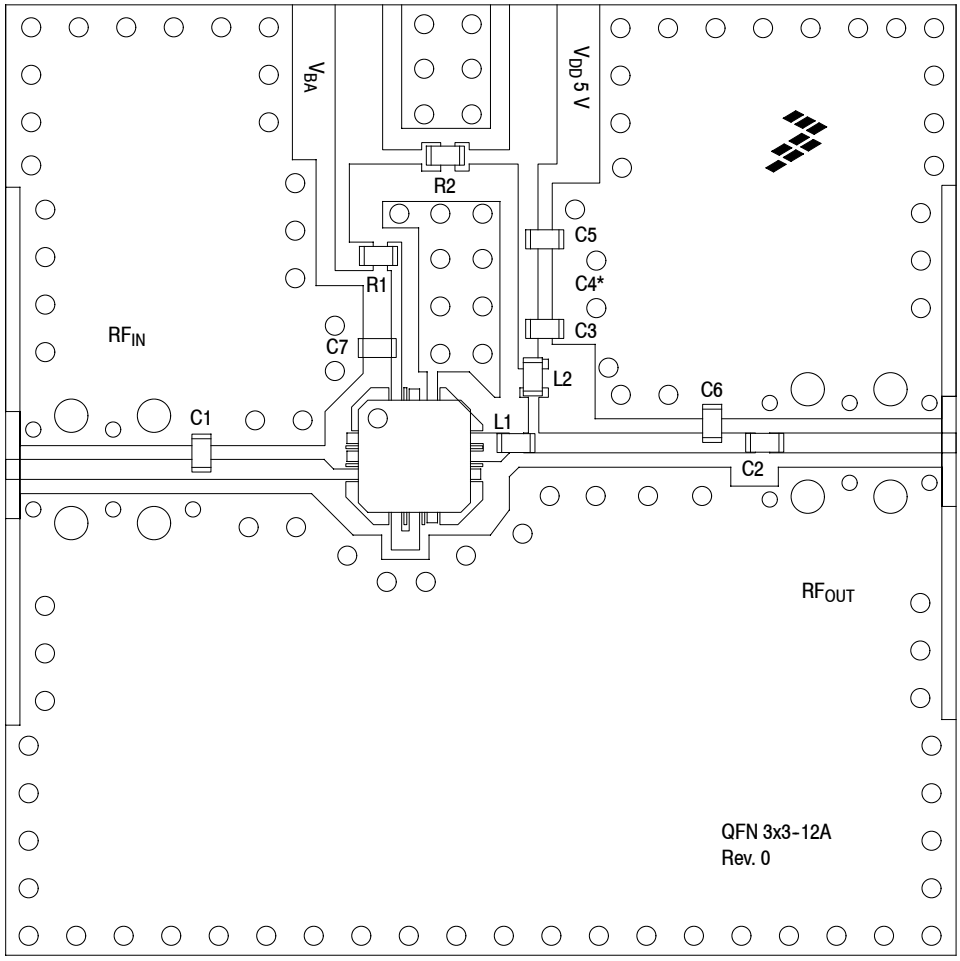
Figure 2. MMG20271HT1 Test Circuit Schematic

Table 8. MMG20271HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	1.8 pF Chip Capicitor	GJM1555C1H1R8BB01D	Murata
C2, C3, C7	18 pF Chip Capacitors	GJM1555C1H180GB01D	Murata
C4	Component Not Used		
C5	0.1 μF Chip Capacitor	GRM155R61A104K01D	Murata
C6	1.5 pF Chip Capacitor	GJM1555C1H1R5BB01D	Murata
L1, R2 (1)	0 Ω, 1 A Chip Resistor	ERJ2GE0R00X	Panasonic
L2	23 nH Chip Inductor	0402CS-23NXGL	Coilcraft
R1	220 Ω, 1/16 W Chip Resistor	RC0402FR-07220RL	Yageo
PCB	0.010″, ε_r = 3.38, Multilayer	IS680-338	Isola

1. Location L1 can be an inductor, resistor or jumper depending on frequency.

50 OHM APPLICATION CIRCUIT: 2140 MHz



*C4 component not used.

Figure 3. MMG20271HT1 Test Circuit Component Layout

Table 8. MMG20271HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	1.8 pF Chip Capicitor	GJM1555C1H1R8BB01D	Murata
C2, C3, C7	18 pF Chip Capacitors	GJM1555C1H180GB01D	Murata
C4	Component Not Used		
C5	0.1 μF Chip Capacitor	GRM155R61A104K01D	Murata
C6	1.5 pF Chip Capacitor	GJM1555C1H1R5BB01D	Murata
L1, R2 (1)	0 Ω, 1 A Chip Resistor	ERJ2GE0R00X	Panasonic
L2	23 nH Chip Inductor	0402CS-23NXGL	Coilcraft
R1	220 Ω, 1/16 W Chip Resistor	RC0402FR-07220RL	Yageo
PCB	0.010″, ε_r = 3.38, Multilayer	IS680-338	Isola

1. Location L1 can be an inductor, resistor or jumper depending on frequency.

(Component Designations and Values table repeated for reference.)

50 OHM TYPICAL CHARACTERISTICS: 2140 MHz

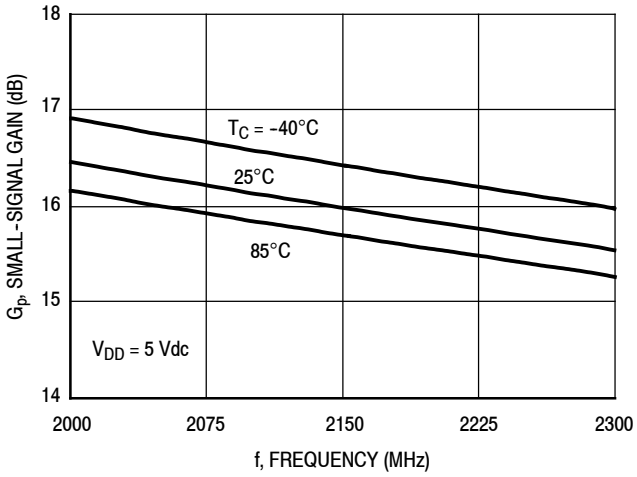


Figure 4. Small-Signal Gain (S21) versus Frequency

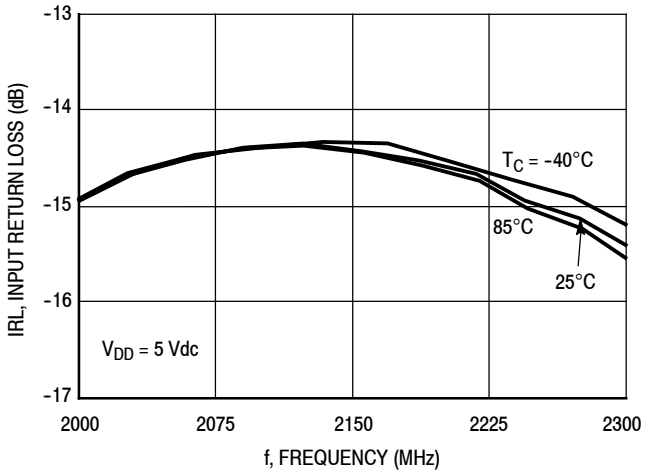


Figure 5. Input Return Loss (S11) versus Frequency

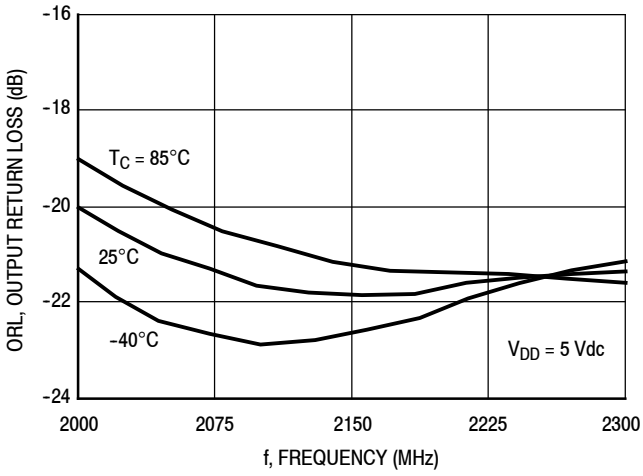


Figure 6. Output Return Loss (S22) versus Frequency

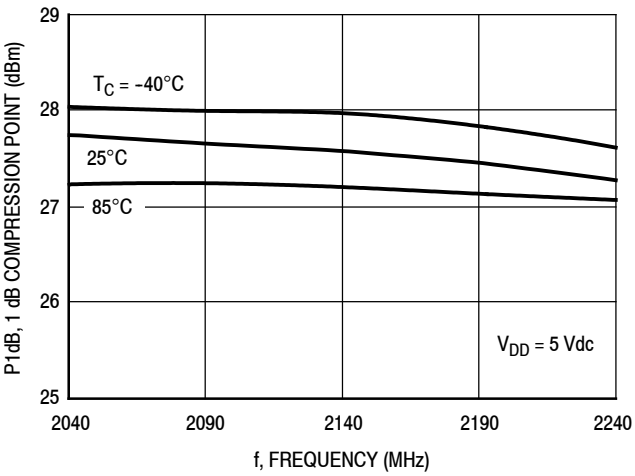


Figure 7. P1dB versus Frequency

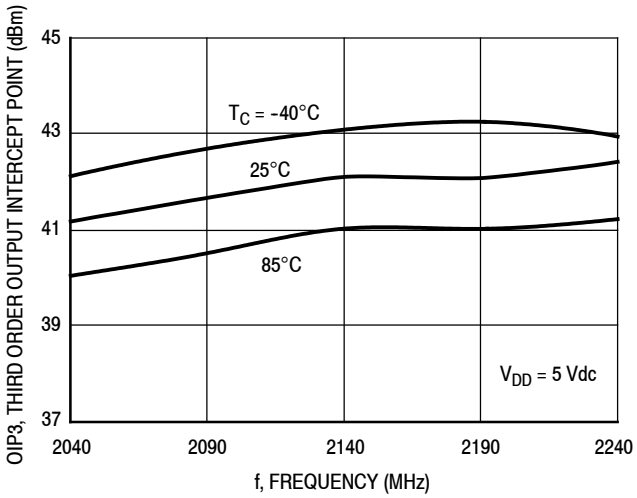


Figure 8. Third Order Output Intercept Point versus Frequency

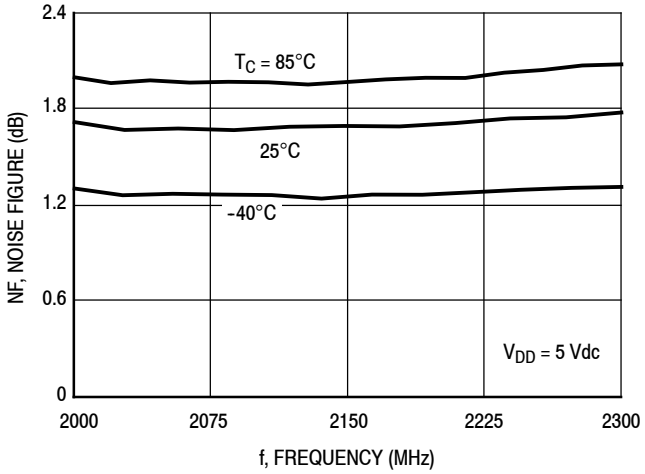


Figure 9. Noise Figure versus Frequency

50 OHM TYPICAL CHARACTERISTICS: 2140 MHz

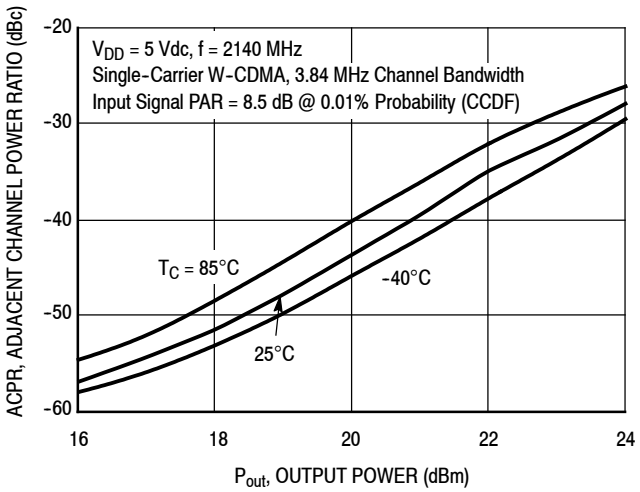
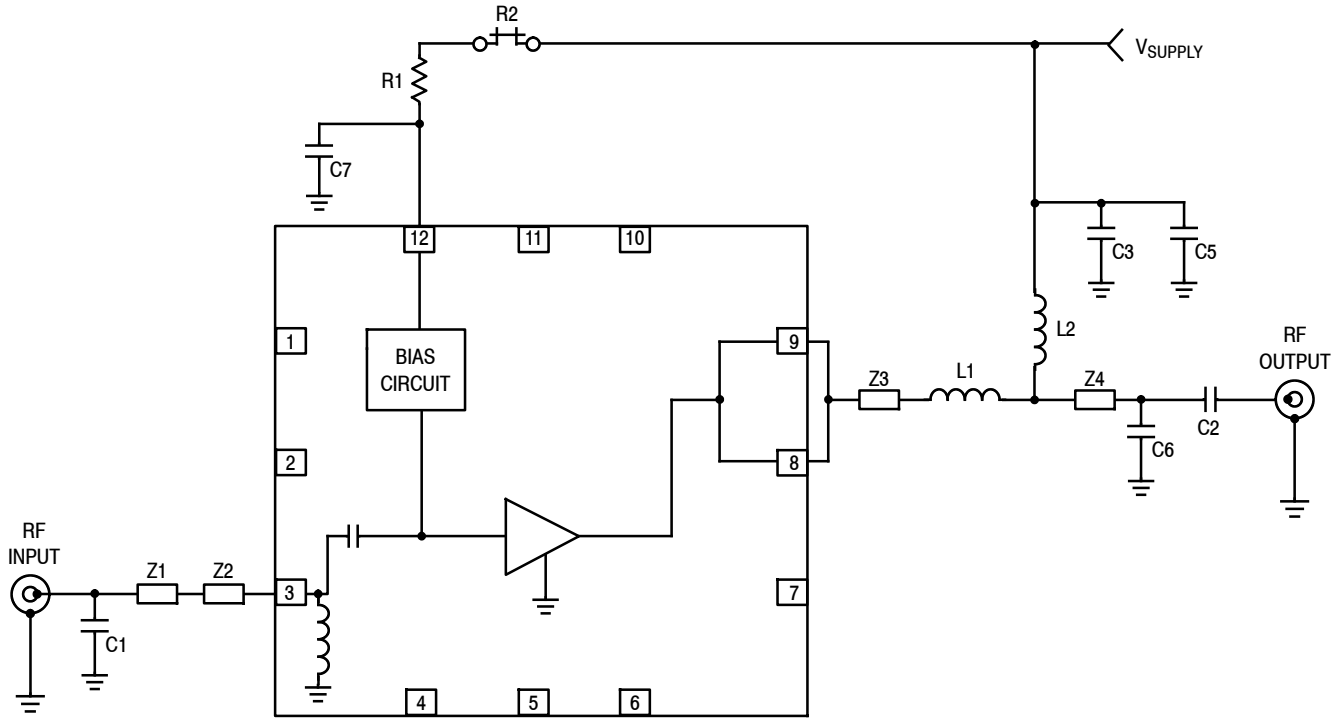


Figure 10. Single-Carrier W-CDMA Adjacent Channel Power Ratio versus Output Power

50 OHM APPLICATION CIRCUIT: 1900 MHz



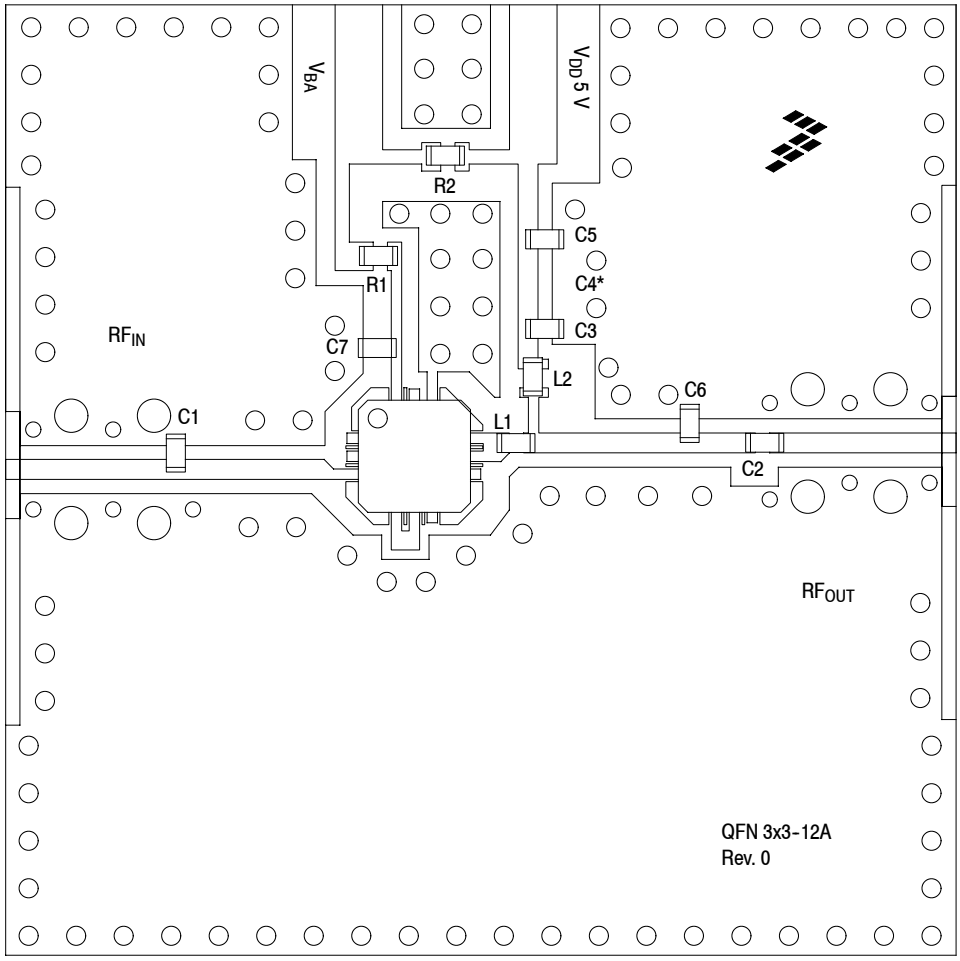
Z1	0.166″ x 0.021″ Microstrip	Z3	0.041″ x 0.030″ Microstrip
Z2	0.026″ x 0.011″ Microstrip	Z4	0.175″ x 0.021″ Microstrip

Figure 11. MMG20271HT1 Test Circuit Schematic

Table 9. MMG20271HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C6	1.6 pF Chip Capicitors	GJM1555C1H1R6BB01D	Murata
C2, C3, C7	18 pF Chip Capacitors	GJM1555C1H180GB01D	Murata
C4	Component Not Used		
C5	0.1 μF Chip Capacitor	GRM155R61A104K01D	Murata
L1	1 nH Chip Inductor	0402CS-1N0XGL	Coilcraft
L2	23 nH Chip Inductor	0402CS-23NXGL	Coilcraft
R1	220 Ω, 1/16 W Chip Resistor	RC0402FR-07220RL	Yageo
R2	0 Ω, 1 A Chip Resistor	ERJ2GE0R00X	Panasonic
PCB	0.010″, ε_r = 3.38, Multilayer	IS680-338	Isola

50 OHM APPLICATION CIRCUIT: 1900 MHz



*C4 component not used.

Figure 12. MMG20271HT1 Test Circuit Component Layout

Table 9. MMG20271HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C6	1.6 pF Chip Capicitors	GJM1555C1H1R6BB01D	Murata
C2, C3, C7	18 pF Chip Capacitors	GJM1555C1H180GB01D	Murata
C4	Component Not Used		
C5	0.1 μF Chip Capacitor	GRM155R61A104K01D	Murata
L1	1 nH Chip Inductor	0402CS-1N0XGL	Coilcraft
L2	23 nH Chip Inductor	0402CS-23NXGL	Coilcraft
R1	220 Ω, 1/16 W Chip Resistor	RC0402FR-07220RL	Yageo
R2	0 Ω, 1 A Chip Resistor	ERJ2GE0R00X	Panasonic
PCB	0.010″, ε_r = 3.38, Multilayer	IS680-338	Isola

(Component Designations and Values table repeated for reference.)

50 OHM TYPICAL CHARACTERISTICS: 1900 MHz

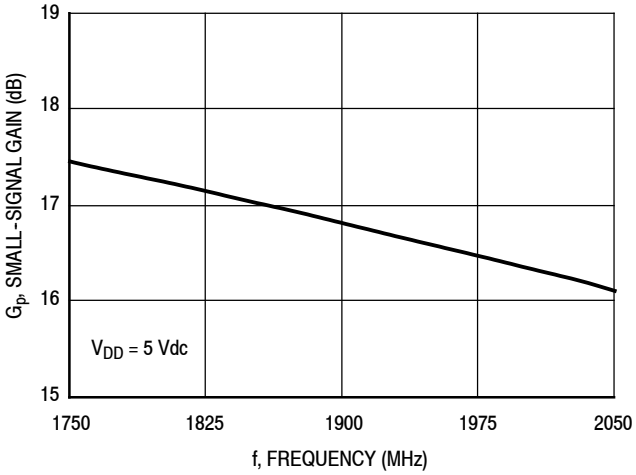


Figure 13. Small-Signal Gain (S21) versus Frequency

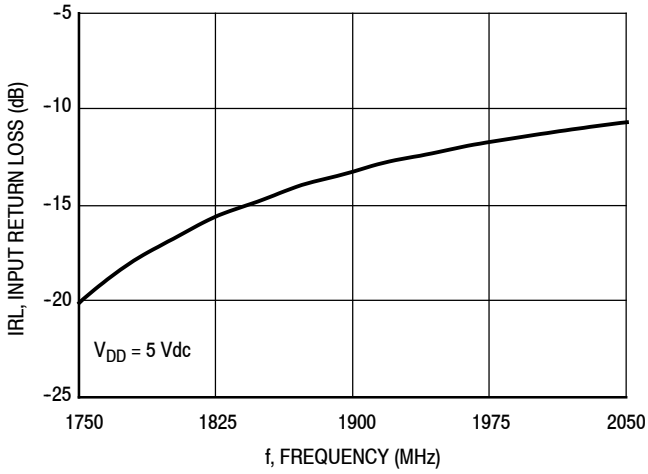


Figure 14. Input Return Loss (S11) versus Frequency

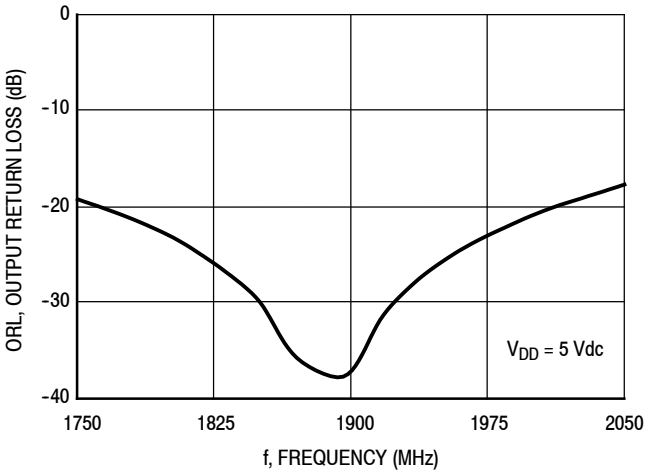


Figure 15. Output Return Loss (S22) versus Frequency

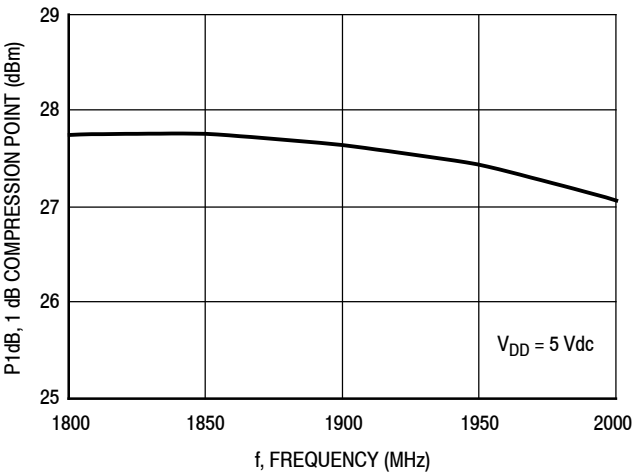


Figure 16. P1dB versus Frequency

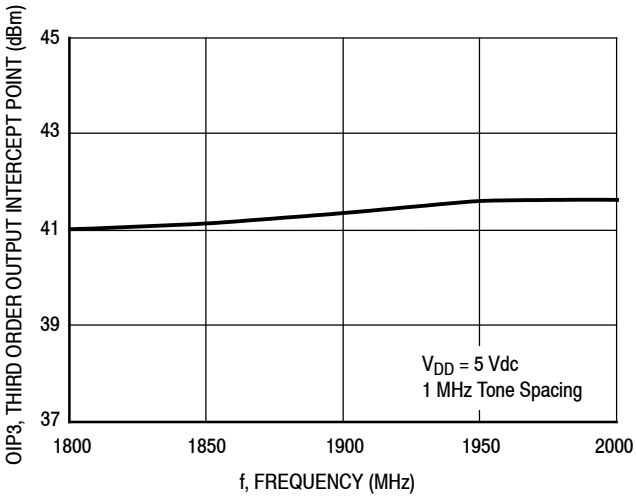


Figure 17. Third Order Output Intercept Point versus Frequency

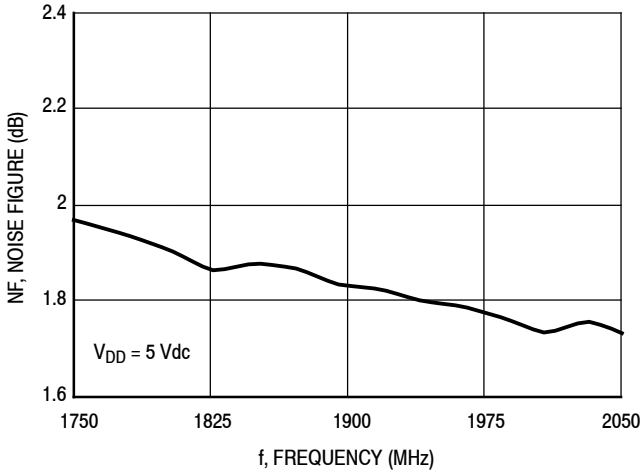
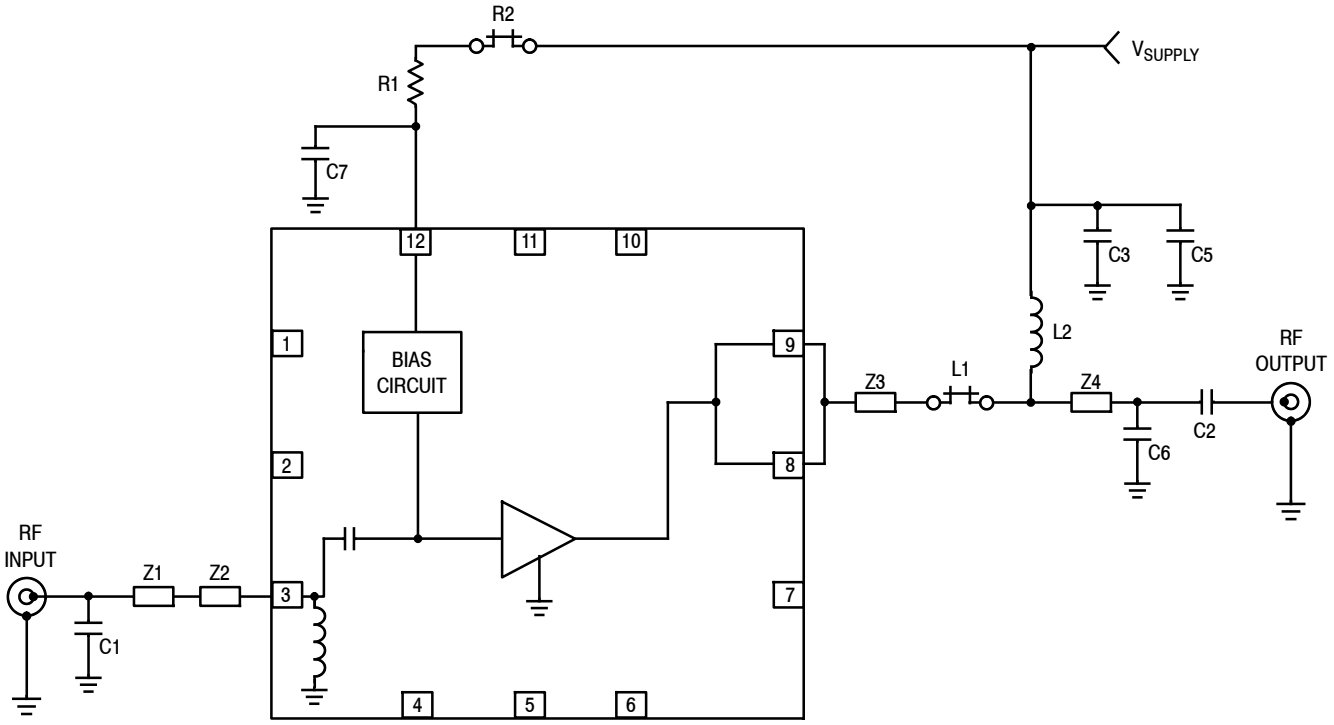


Figure 18. Noise Figure versus Frequency

50 OHM APPLICATION CIRCUIT: 2700 MHz



Z1	0.056″ x 0.021″ Microstrip	Z3	0.041″ x 0.030″ Microstrip
Z2	0.026″ x 0.011″ Microstrip	Z4	0.091″ x 0.021″ Microstrip

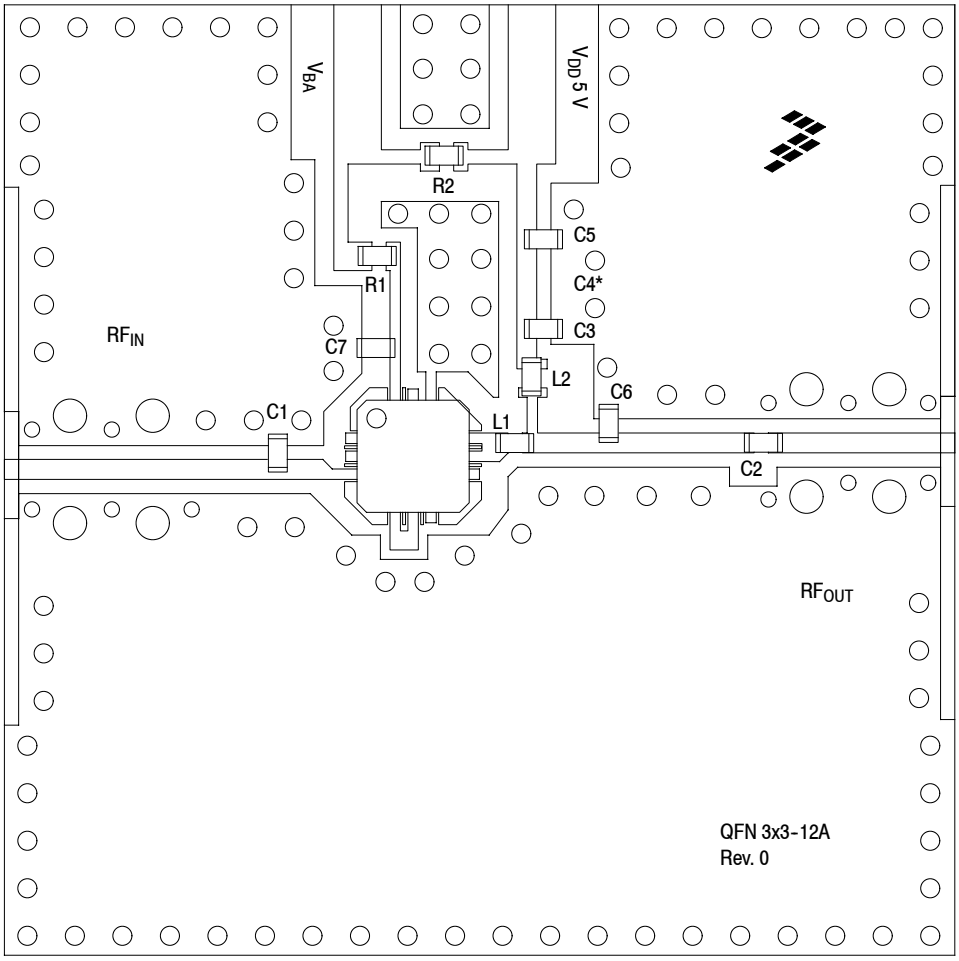
Figure 19. MMG20271HT1 Test Circuit Schematic

Table 10. MMG20271HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	1.8 pF Chip Capicitor	GJM1555C1H1R8BB01D	Murata
C2, C3, C7	18 pF Chip Capacitors	GJM1555C1H180GB01D	Murata
C4	Component Not Used		
C5	0.1 μF Chip Capacitor	GRM155R61A104K01D	Murata
C6	1.5 pF Chip Capacitor	GJM1555C1H1R5BB01D	Murata
L1, R2 (1)	0 Ω, 1 A Chip Resistor	ERJ2GE0R00X	Panasonic
L2	23 nH Chip Inductor	0402CS-23NXGL	Coilcraft
R1	220 Ω, 1/16 W Chip Resistor	RC0402FR-07220RL	Yageo
PCB	0.010″, ε_r = 3.38, Multilayer	IS680-338	Isola

1. Location L1 can be an inductor, resistor or jumper depending on frequency.

50 OHM APPLICATION CIRCUIT: 2700 MHz



*C4 component not used.

Figure 20. MMG20271HT1 Test Circuit Component Layout

Table 10. MMG20271HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	1.8 pF Chip Capicitor	GJM1555C1H1R8BB01D	Murata
C2, C3, C7	18 pF Chip Capacitors	GJM1555C1H180GB01D	Murata
C4	Component Not Used		
C5	0.1 μF Chip Capacitor	GRM155R61A104K01D	Murata
C6	1.5 pF Chip Capacitor	GJM1555C1H1R5BB01D	Murata
L1, R2 (1)	0 Ω, 1 A Chip Resistor	ERJ2GE0R00X	Panasonic
L2	23 nH Chip Inductor	0402CS-23NXGL	Coilcraft
R1	220 Ω, 1/16 W Chip Resistor	RC0402FR-07220RL	Yageo
PCB	0.010″, ε_r = 3.38, Multilayer	IS680-338	Isola

1. Location L1 can be an inductor, resistor or jumper depending on frequency.

(Component Designations and Values table repeated for reference.)

50 OHM TYPICAL CHARACTERISTICS: 2700 MHz

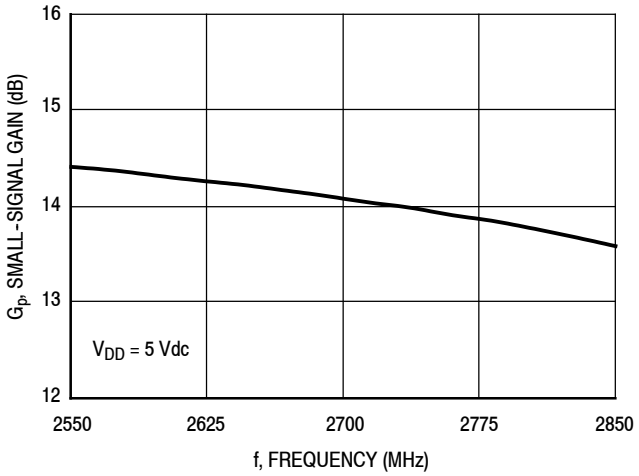


Figure 21. Small-Signal Gain (S21) versus Frequency

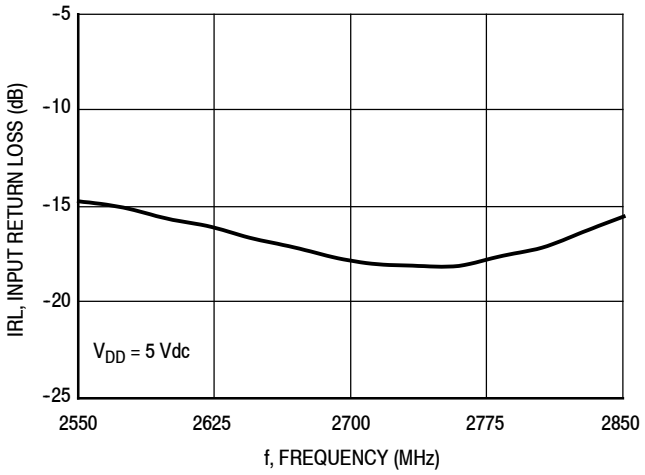


Figure 22. Input Return Loss (S11) versus Frequency

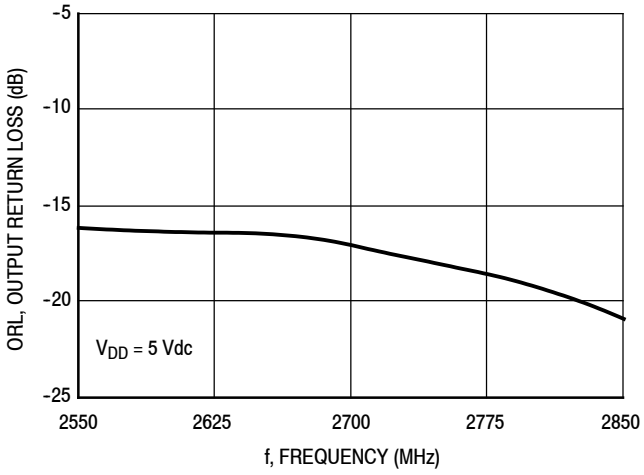


Figure 23. Output Return Loss (S22) versus Frequency

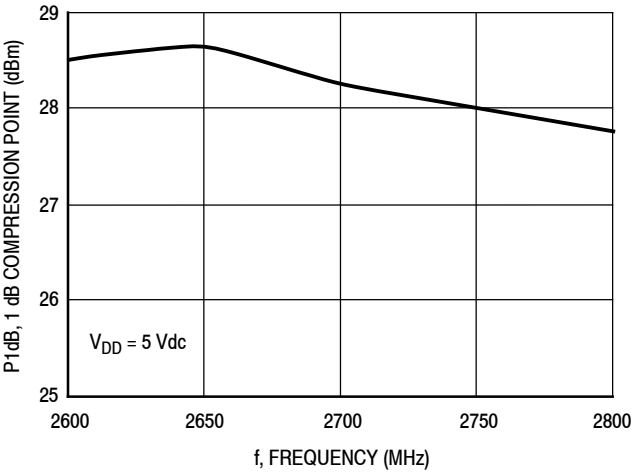


Figure 24. P1dB versus Frequency

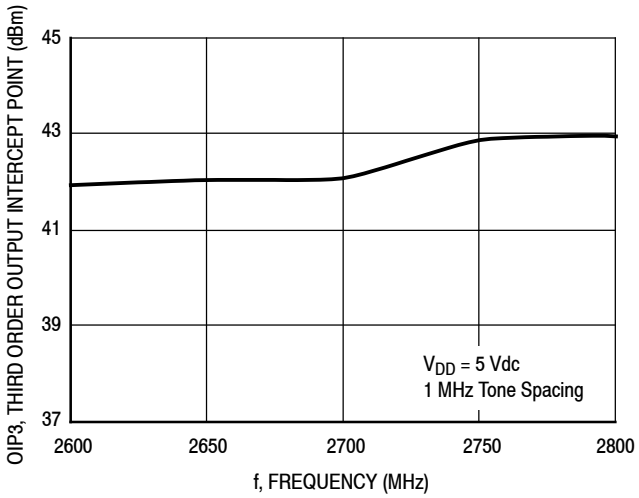


Figure 25. Third Order Output Intercept Point versus Frequency

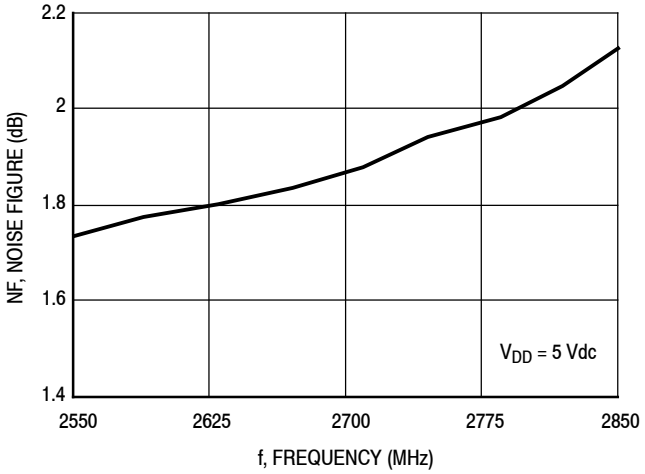


Figure 26. Noise Figure versus Frequency

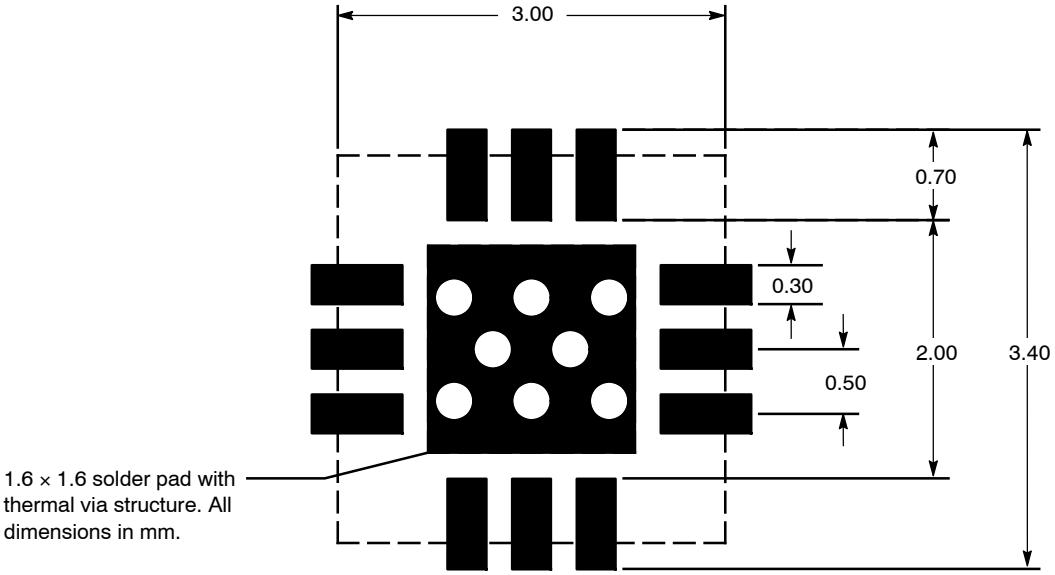
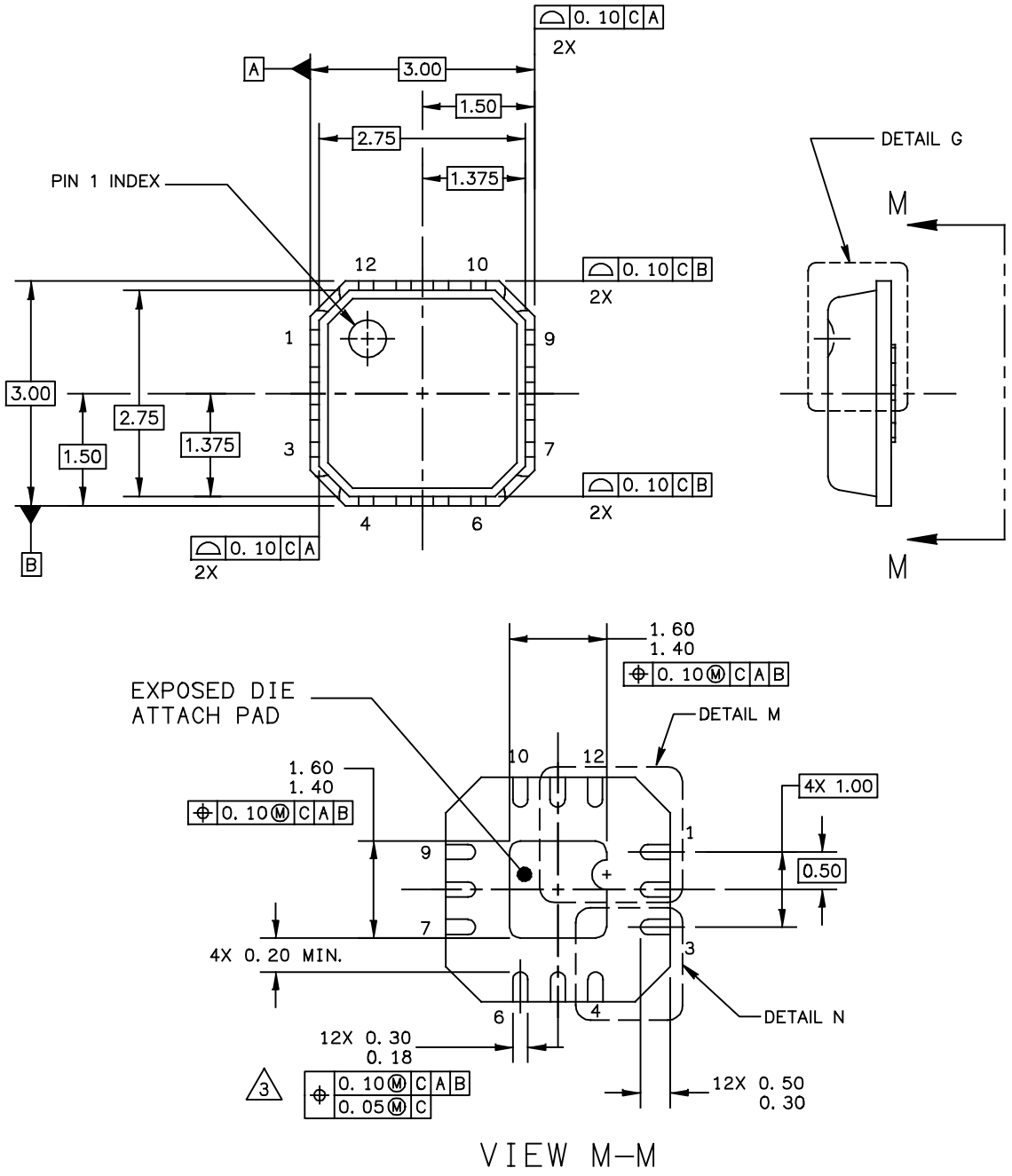


Figure 27. PCB Pad Layout for QFN 3 × 3

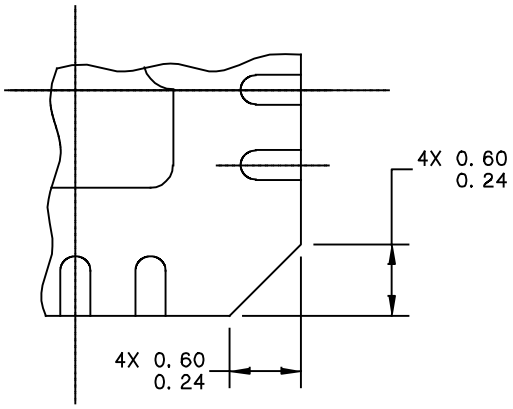
Figure 28. Product Marking

PACKAGE DIMENSIONS

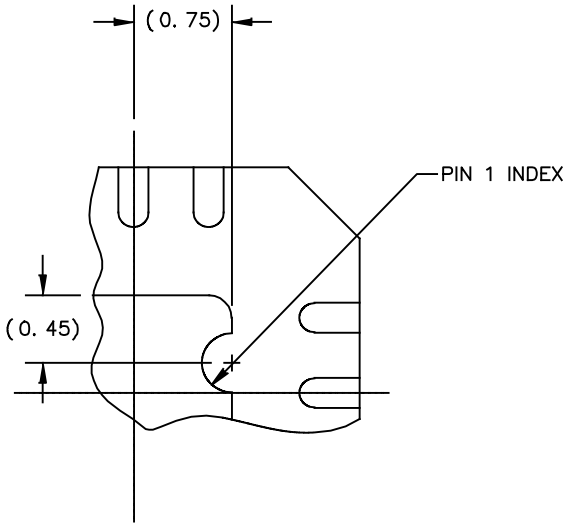


VIEW M–M

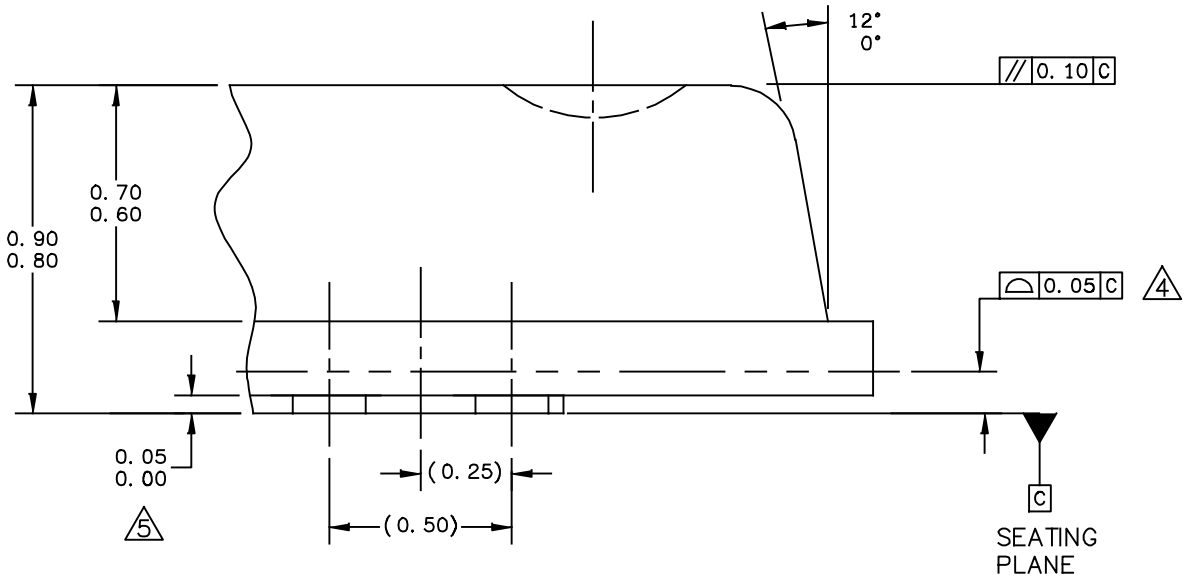
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 12 TERMINAL, 0.5 PITCH (3X3X0.85)	DOCUMENT NO: 98ASA00227D	REV: O
	CASE NUMBER: 2131–01	14 MAY 2010
	STANDARD: NON–JEDEC	



DETAIL N
CORNER CONFIGURATION



DETAIL M
PIN 1 BACKSIDE INDEX



DETAIL G
VIEW ROTATED 90° CW

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TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 12 TERMINAL, 0.5 PITCH (3X3X0.85)	DOCUMENT NO: 98ASA00227D	REV: O
	CASE NUMBER: 2131-01	14 MAY 2010
	STANDARD: NON-JEDEC	

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING & TOLERANCING PER ASME Y14.5 – 2009.

3. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.

4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

5. THIS DIMENSION APPLIED ONLY FOR TERMINALS.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 12 TERMINAL, 0.5 PITCH (3X3X0.85)	DOCUMENT NO: 98ASA00227D	REV: O
	CASE NUMBER: 2131–01	14 MAY 2010
	STANDARD: NON–JEDEC	

PRODUCT DOCUMENTATION, TOOLS AND SOFTWARE

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to Software & Tools on the part’s Product Summary page to download the respective tool.

FAILURE ANALYSIS

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where Freescale is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local Freescale Sales Office.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2010	• Initial Release of Data Sheet
1	Sept. 2014	• Table 2, Maximum Ratings: updated Junction Temperature from 150°C to 175°C to reflect recent test results of the device, p. 1 • Table 6, ESD Protection Characteristics, removed the word “Minimum” after the ESD class rating. ESD ratings are characterized during new product development but are not 100% tested during production. ESD ratings provided in the data sheet are intended to be used as a guideline when handling ESD sensitive devices, p. 2 • Revised Failure Analysis information, p. 17

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