Freescale Semiconductor
Advance Information

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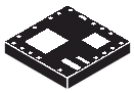
RoHS

MMM6035



Package Information
Plastic Package
Case 1561
(6 x 6 mm Module)

Ordering Information

Device	Device Marking or Operating Temperature Range	Package
MMM6035	MMM6035	Module

MMM6035

Quad-Band GSM/GPRS PA Module with Integrated Power Control

1 Introduction

The MMM6035 is a 50 Ω Power Amplifier module for quad-, tri-, and dual-band GSM handset applications, functioning over the GSM850, EGSM, DCS, and PCS frequency bands. This module is compatible with GSM/GPRS operating modes (up to 50% duty cycle). To simplify radio front-end design requirements, the power control function is integrated, removing the need for directional couplers and detector diodes. GSM burst shaping and power control is integrated on an internal control SmartMOS™ IC. The analog power control signal is smoothed by a low-pass filter included in the internal control SmartMOS chip, allowing over 45 dB dynamic range to be achieved.

The MMM6035 also prevents degradation of switching transients, regardless of battery conditions, due to an internal anti-saturation detection feature. Transmit Enable and Band Select functions are controlled through 0 to 2.8 V logic inputs. These functions are also compatible with 0 to 1.8 V logic inputs.

Contents

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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2 Functional Block Diagram

Figure 1 is a functional block diagram of the quad-band (GSM850, EGSM, DCS, and PCS power amplifier module.

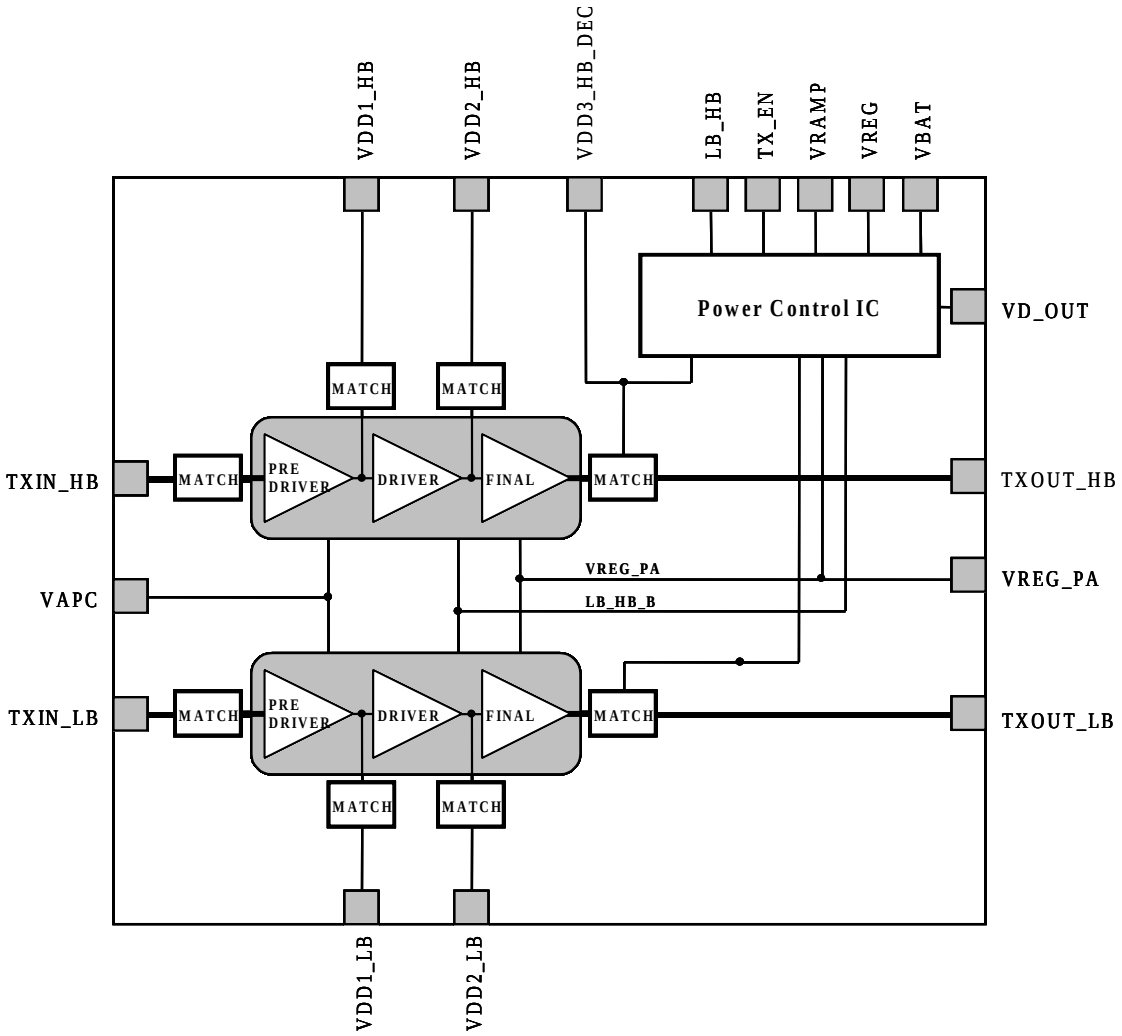


Figure 1. Functional Block Diagram

3 Electrical Characteristics

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain Supply Voltages	V_{DD}	5.5	V
Power Control IC Supply Voltage	V_{BAT}	5.5	V
External Regulated DC Supply Voltage	V_{REG}	5.5	V
RF Input Power	P_{in}	11	dBm
Operating Temperature Range	T_A	-20 to 85	°C
Storage Temperature	T_{stg}	-55 to 150	°C
Junction Temperature	T_J	150	°C
Moisture Sensitivity Level (Meets lead-free reflow profiles with peak temperature of 260 °C)	MSL	3	
Thermal Resistance (junction to mounting base)	R_{th}	20	°C/W

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions and Electrical Characteristics tables.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
External Regulated DC Supply Voltage	V_{REG}	2.6	2.8	3.0	V
Power Control IC Supply Voltage	V_{BAT}	3.1	-	4.5	V
RF Input Power	P_{in}	3.0	-	9.0	dBm
Mode Control Low Voltage (TX_EN, LB_HB)		0	-	0.4	V
Mode Control High Voltage (TX_EN, LB_HB)		1.4	-	V_{REG}	V
Power Control Ramp Voltage	V_{RAMP}	0.1	-	2.2	V

Table 3. DC Characteristics
(V_{REG} = 2.6 to 3 V, T_A = -20 to 85° C)

Characteristic	Symbol	Min	Typ	Max	Unit
External Regulate DC Supply Current TX_EN, LB_HB high	I_{reg}	-	5	10	mA
Standby Leakage Current Include current on all pins TX_EN, LB_HB low VRAMP = 0 V, Vreg = 2.8 V, VBAT = 4.5 V, TA = 85° C	I_{LKG}	-	-	50	µA
Mode Control Input Input Low Input High	 $I_{mci(L)}$ $I_{mci(H)}$	 -0.5 -	 - -	 - 50	µA

Table 3. DC Characteristics (continued)
(V_{REG} = 2.6 to 3 V, T_A = -20 to 85° C)

Characteristic	Symbol	Min	Typ	Max	Unit
Mode Control Input Resistance (High State) Resistance to GND	R_{mci}	-	250	-	kΩ
Vramp Input Current V_{RAMP} = 0 V Vramp = 2.2 V	 $I_{RAMP(L)}$ $I_{RAMP(H)}$	 -0.5 -	 - -	 - 50	µA

4 RF Specifications

Table 4. Mode GMSK Cellular Band Specifications
(TX_{IN_LB} = 3.0 dBm, V_{BAT} = 3.6 V, V_{RAMP} = 0.1 to 2.2 V pulsed, Period = 4.6 ms, Duty Cycle = 25%, LB_HB = 0 V, V_{REG} = 2.8 V, TX_EN = 2.8 V, T_A = 25°C ±5° C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Frequency	F_0	824	-	849	MHz
Output Power at High V_{RAMP}	$P_{O(H)}$	34.2	34.9	-	dBm
Output Power over V_{RNG}, T_{RNG} at High V_{RAMP}	P_O(HX)	32.2	-	-	dBm
Power Added Efficiency @ $P_{O(H)}$	PAE	46	52	-	%
Current Consumption at Low Output Power (P_O set to 6.0 dBm)	$I_{DD(L)}$	-	-	150	mA
Forward Isolation (V_{RAMP} = 0 V, TX_EN = 0 V) over V_{RNG}, T_{RNG}	Iso1	-	-	-20	dBm
Harmonics level over V_{RNG}, T_{RNG}	2 F_0 3 F_0	-	-	-10 -10	dBm
Tx Noise in Rx Cellular Band @ P_O=$P_{O(H)}$ RBW = 100 kHz	NRx1 F_{RX} = 869-894 MHz	-	-	-82	dBm
Input VSWR	Γ_{IN}	-	16	-	dB
Second Harmonic Leakage at DCS/PCS over V_{RNG}, T_{RNG} at High V_{RAMP}	X_{talk}	-	-	-15	dBm
Load mismatch stability All angles Set Vramp where Po(H) ≤ 34.2 dBm into 50 Ω load All spurious < -36 dBm, RBW = 3 MHz	VSWR	6:1	-	-	
Load mismatch ruggedness All angles Set Vramp where Po(H) ≤ 34.2 dBm into 50 Ω load No damage, no degradation	VSWR	20:1	-	-	
Power Control Range over V_{RNG}, T_{RNG}	R_{PC}	35	-	-	dB

Table 5. Mode GMSK E-GSM Band Specifications

(TX_{IN_LB} = 3.0 dBm, V_{BAT} = 3.6 V, V_{RAMP} = 0.1 to 2.2 V pulsed, Period = 4.6 ms, Duty Cycle = 25%, LB_HB = 0 V, V_{REG} = 2.8 V, TX_EN = 2.8 V, T_A = 25° C ±5° C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Frequency	F_0	880	-	915	MHz
Output Power at High V_{RAMP}	$P_{O(H)}$	34.2	34.9	-	dBm
Output Power over V_{RNG}, T_{RNG} at High V_{RAMP}	P_O(Hx)	32.2	-	-	dBm
Power Added Efficiency @ P_O(H)	PAE	50	56	-	%
Current Consumption at Low Output Power (P_O set to 6.0 dBm)	I_{DD}(L)	-	-	150	mA
Forward Isolation (V_{RAMP} = 0 V, TX_EN = 0 V) over V_{RNG}, T_{RNG}	Iso1	-	-	-20	dBm
Harmonics level over V_{RNG}, T_{RNG}	2 F_0 3 F_0	-	-	-10 -10	dBm
Tx Noise in Rx E-GSM Band @ P_O = $P_{O(H)}$ RBW = 100 kHz NRx1 F_{RX} = 925-935 MHz NRx2 F_{RX} = 935-960 MHz		 - -	 - -	 -77 -82	dBm
Input VSWR	Γ_{IN}	-	12	-	dB
Second Harmonic Leakage at DCS/PCS over V_{RNG}, T_{RNG} at High V_{RAMP}	X_{talk}	-	-	-15	dBm
Load mismatch stability All angles Set Vramp where Po(H) ≤ 34.2 dBm into 50 Ω load All spurious < -36 dBm, RBW = 3 MHz	VSWR	6:1	-	-	
Load mismatch ruggedness All angles Set Vramp where Po(H) ≤ 34.2 dBm into 50 Ω load No damage, no degradation	VSWR	20:1	-	-	
Power Control Range over V_{RNG}, T_{RNG}	R_{PC}	35	-	-	dB

Table 6. Mode GMSK DCS Band Specifications

(TX_{IN_HB} = 3 dBm, V_{BAT} = 3.6 V, V_{RAMP} = 0.1 to 2.2 V pulsed, Period = 4.6 ms, Duty Cycle = 25%, LB_HB = 2.8 V, V_{REG} = 2.8 V, TX_EN = 2.8 V, T_A = 25° C ±5° C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Frequency	F_0	1710	-	1785	MHz
Output Power at High V_{RAMP}	$P_{O(H)}$	31.5	33.0	-	dBm
Output Power over V_{RNG}, T_{RNG} at High V_{RAMP}	P_O(Hx)	29.5	-	-	dBm
Power Added Efficiency @ P_O(H)	PAE	40	46	-	%
Current Consumption at Low Output Power (P_O set to 1.5 dBm)	I_{DD}(L)	-	-	150	mA
Forward Isolation (V_{RAMP} = 0 V, TX_EN = 0 V) over V_{RNG}, T_{RNG}	Iso1	-	-	-28	dBm

Table 6. Mode GMSK DCS Band Specifications (continued)

(TX_{IN_HB} = 3 dBm, V_{BAT} = 3.6 V, V_{RAMP} = 0.1 to 2.2 V pulsed, Period = 4.6 ms, Duty Cycle = 25%, LB_HB = 2.8 V, V_{REG} = 2.8 V, TX_EN = 2.8 V, T_A = 25° C ±5° C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Harmonics level over V_{RNG}, T_{RNG}	$2F_0$ $3F_0$	- -	- -	-10 -10	dBm
Tx Noise in Rx DCS Band @ $P_O = P_{O(H)}$ RBW = 100 kHz	NRx1 F_{RX} = 1805-1880 MHz	-	-	-75	dBm
Input VSWR	Γ_{IN}	-	16	-	dB
Load mismatch stability All angles Set Vramp where Po(H) ≤ 31.5 dBm into 50 Ω load All spurious < -30 dBm, RBW = 3 MHz	VSWR	6:1	-	-	
Load mismatch ruggedness All angles Set Vramp where Po(H) ≤ 34.2 dBm into 50 Ω load No damage, no degradation	VSWR	20:1	-	-	
Power Control Range over V_{RNG}, T_{RNG}	R_{PC}	35	-	-	dB

Table 7. Mode GMSK PCS Band Specifications

(TX_{IN_HB} = 3 dBm, V_{BAT} = 3.6 V, V_{RAMP} = 0.1 to 2.2 V pulsed, Period = 4.6 ms, Duty Cycle = 25%, LB_HB = 2.8 V, V_{REG} = 2.8 V, TX_EN = 2.8 V, T_A = 25° C ±5° C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Frequency	F_0	1850	-	1910	MHz
Output Power at High V_{RAMP}	$P_{O(H)}$	31.5	32.8	-	dBm
Output Power over V_{RNG}, T_{RNG} at High V_{RAMP}	P_O(Hx)	29.5	-	-	dBm
Power Added Efficiency @ P_O(H)	PAE	40	46	-	%
Current Consumption at Low Output Power (P_O set to 1.5 dBm)	I_{DD}(L)	-	-	150	mA
Forward Isolation (V_{RAMP} = 0 V, TX_EN = 0 V) over V_{RNG}, T_{RNG}	Iso1	-	-	-28	dBm
Harmonics level over V_{RNG}, T_{RNG}	$2F_0$ $3F_0$	- -	- -	-10 -10	dBm
Tx Noise in Rx PCS Band @ $P_O = P_{O(H)}$ RBW = 100 kHz	NRx1 F_{RX} = 1930 -1990 MHz	-	-	-75	dBm
Input VSWR	Γ_{IN}	-	15	-	dB
Load mismatch stability All angles Set Vramp where Po(H) ≤ 31.5 dBm into 50 Ω load All spurious < -30 dBm, RBW = 3 MHz	VSWR	6:1	-	-	

Table 7. Mode GMSK PCS Band Specifications (continued)

(TX_{IN_HB} = 3 dBm, V_{BAT} = 3.6 V, V_{RAMP} = 0.1 to 2.2 V pulsed, Period = 4.6 ms, Duty Cycle = 25%, LB_HB = 2.8 V, V_{REG} = 2.8 V, TX_EN = 2.8 V, T_A = 25° C ±5° C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Load mismatch ruggedness All angles Set Vramp where Po(H) ≤ 34.2 dBm into 50 Ω load No damage, no degradation	VSWR	20:1	-	-	
Power Control Range over V_{RNG}, T_{RNG}	R_{PC}	35	-	-	dB

Table 8. Power Control Specifications

(V_{REG} = 2.8 V, Vrng = 3.0 to 4.5 V, -20 to 85° C)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Wake-up Time	V_{BAT} = 3.6 V T_A = 25° C, Time to reach stable VD_OUT after 0.3 V V_{RAMP} step	t_{wu}	-	12	-	µs
Vramp Input Voltage Offset	Voltage at which VD_OUT rises above 0 V	V_{offset}[1]	0.18	0.2	-	V
VD_OUT vs. V_{RAMP} Slope	V_{BAT} = 3.6 V T_A = 25° C, V_{RAMP} > V_{Offset}	V_{slope}[1]	-	2.0	-	V/V
Po versus V_{RAMP} Slope	V_{BAT} = 3.6 V T_A = 25° C, Po>5 dBm for TX CEL and EGSM, Po>0 dBm for TX DCS and PCS	Po_slope[1]	-	-	240	dB/V
V_{RAMP} Controller Enable Threshold	V_{BAT} = 3.6 V T_A = 25° C, Rising V_{RAMP}	$V_{ctrl(R)}$	-	160	-	mV
V_{RAMP} Controller Disable Threshold	V_{BAT} = 3.6 V T_A = 25° C, Falling V_{RAMP}	$V_{ctrl(F)}$	-	140	-	mV
Smoothing Filter Bandwidth (3 dB cutoff frequency)	V_{BAT} = 3.6 V T_A = 25° C	BW vramp	-	200	-	kHz
Smoothing Filter Attenuation (Atten at 1 MHz)	V_{BAT} = 3.6 V	αvramp	-	30	-	dB
Smoothing Filter Rise Time (Vdout rise time between 10% and 90% with V_{RAMP} step of Voffset 50 mV)	V_{BAT} = 3.6 V T_A = 25° C	t_r	-	2.5	-	µs

Table 8. Power Control Specifications (continued)

(V_{REG} = 2.8 V, Vrng = 3.0 to 4.5 V, -20 to 85° C)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Pout variation versus Temp Vramp adj for Pout(H)-10 dB < Pout < Pout(H) Vramp adj for Pout(H)-20 dB < Pout < Pout(H)-10 dB Vramp adj for Pout(H)-30 dB < Pout < Pout(H)-20 dB	V_{BAT} = 3.6 V T_A = 25° C	 ΔPo(H)_T ΔPo(M)_T ΔPo(L)_T	 -1.5 -2.0 -4.0	 - - -	 1.5 2.0 4.0	 dB dB dB
Pout variation versus Freq Vramp set for Power(H) at 836.5 MHz Vramp set for Power(H) at 897.5 MHz Vramp set for Power(H) at 1747.5 MHz Vramp set for Power(H) at 1880 MHz	V_{BAT} = 3.6 V T_A = 25° C	 ΔPo_CELL_f ΔPo_EGSM_f ΔPo_DCS_f ΔPo_PCS_f	 -0.5 -0.5 -0.5 -0.5	 - - - -	 0.5 0.5 0.5 0.5	 dB dB dB dB

1 See Figure 4.

5 Input/Output ESD Specifications

The MMM6035 meets Class 1B and Class 1C for the Human Body Model (HBM) Electrostatic Discharge (ESD) classification and it meets Class M2 for the Machine Model (MM) ESD classification. Table 9 and Table 10 show the ESD immunity level for each MMM6035 pin. The numbers shown in Table 9 and Table 10 specify the ESD threshold level for each pin where the I-V curve between the pin and ground begins to show degradation.

Table 9. ESD Human Body Model: EOS/ESD-S5.1 (Pin to Ground Stress)

Pin Number-Name	450 Volts	500 Volts	750 Volts	1000 Volts	1250 Volts	2000 Volts
1 - GND	NA	NA	NA	NA	NA	NA
2 - VDD2_HB						X
3 - VDD1_HB	X					
4 - Vapc	X					
5 - TXIn_HB						X
6 - TXIn_LB						X
7 - VDD1_LB	X					
8 - VDD2_LB					X	
9 - GND	NA	NA	NA	NA	NA	NA
10 - GND	NA	NA	NA	NA	NA	NA
11 - TXOut_LB						X
12 - Vreg_PA						X
13 - VD_OUT						X
14 - Vramp						X
15 - TXEn						X
16 - LB_HB						X
17 - Vreg						X
18 - Vbat						X
19 - VD3_HB_DEC						X
20 - TXOut_HB						X
21 - GND	NA	NA	NA	NA	NA	NA
22 - GND	NA	NA	NA	NA	NA	NA

Table 10. ESD Machine Model: EOS/ESD-S5.1, From 50 V up to 150 V (Destruction Voltage)

Pin Number/Name	50 Volts	75 Volts	100 Volts	150 Volts	200 Volts
1 - GND	NA	NA	NA	NA	NA
2 - VDD2_HB		X			
3 - VDD1_HB		X			
4 - Vapc			X		
5 - TXIn_HB				X	
6 - TXIn_LB				X	
7 - VDD1_LB	X				
8 - VDD2_LB				X	
9 - GND	NA	NA	NA	NA	NA
10 - GND	NA	NA	NA	NA	NA
11 - TXOut_LB				X	
12 - Vreg_PA				X	
13 - VD_OUT				X	
14 - Vramp				X	
15 - TXEn				X	
16 - LB_HB				X	
17 - Vreg				X	
18 - Vbat				X	
19 - VD3_HB_DEC				X	
20 - TXOut_HB				X	
21 - GND	NA	NA	NA	NA	NA
22 - GND	NA	NA	NA	NA	NA

6 Application Information

Figure 2 shows the typical application schematic and Figure 3 shows the printed circuit board for the MMM6035. The bill of materials are listed in Table 11 and the power up/down sequences are listed in Table 12.

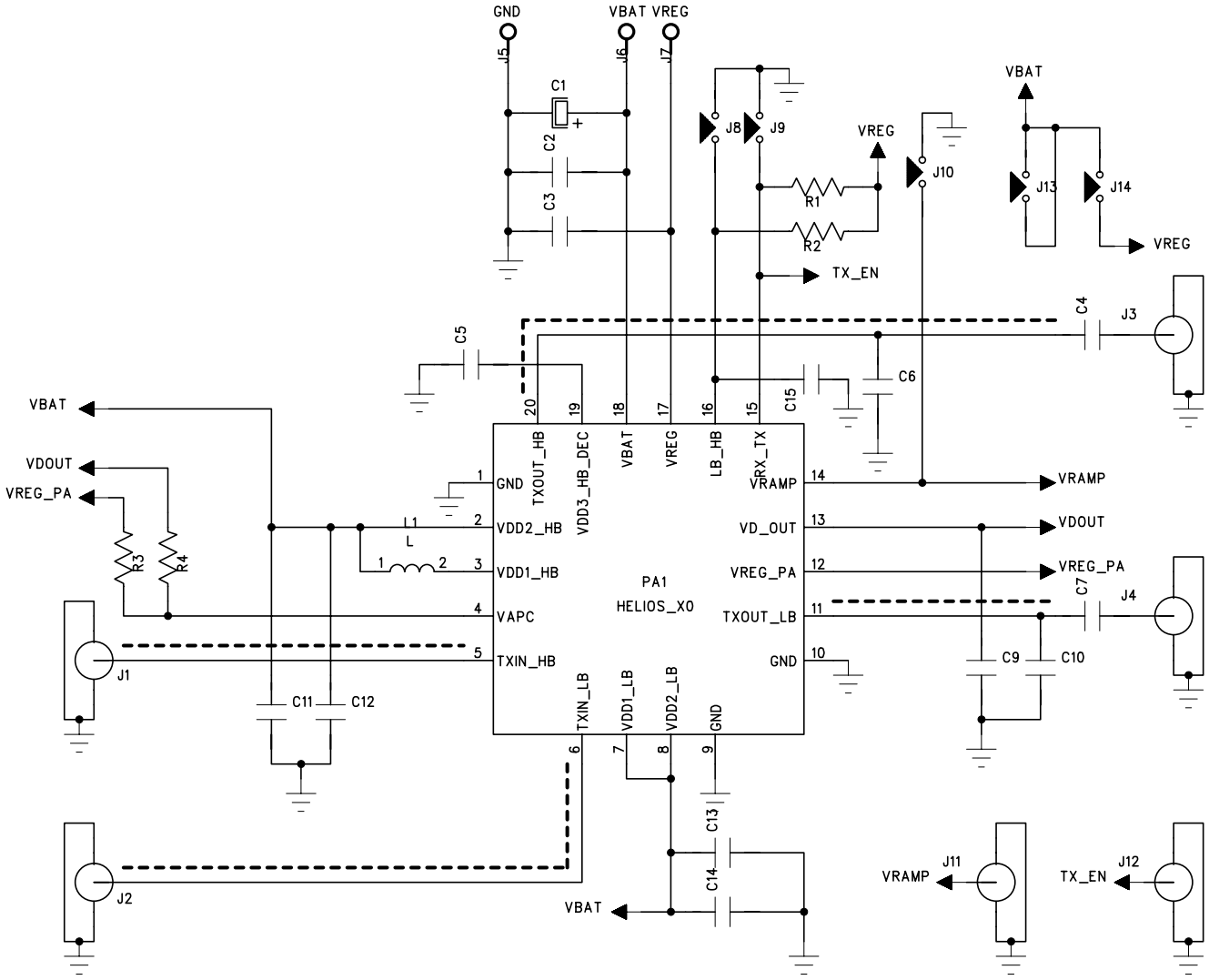


Figure 2. Typical Application Schematic

Table 11. Bill of Materials

Reference	Value	Size and Manufacturer
C1	68 uF 6 V	Sprague
C2	1000 nF	0402 Murata
C3	100 nF	0402 Murata
C4	22 pF	0402 Murata
C5	22 pF	0402 Murata
C6	2.7 pF	0402 Murata
C7	22 pF	0402 Murata
C9	33 pF	0402 Murata
C10	8.2 pF	0201 Johanson
C11	10 nF	0402 Murata
C12	10 nF	0402 Murata
C13	220 pF	0402 Murata
C14	10 nF	0402 Murata
C15	1 nF	0402 Murata
L1	3.9 nH	0402 Murata
R1	10 k	0402 NEOHM
R2	10k	0402 NEOHM
R3	1.8 k	0402 NEOHM
R4	1 k	0402 NEOHM

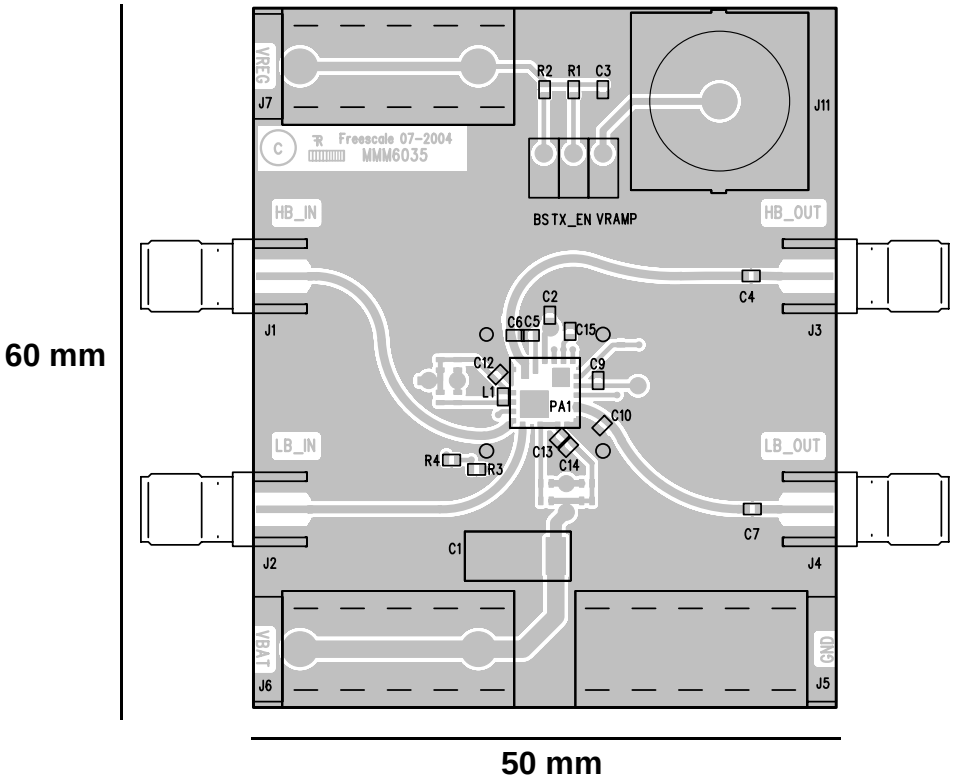


Figure 3. Printed Circuit Board

Table 12. Power Up/Down Sequences

SEQ	DESCRIPTION
Power Up Sequence for TX	
1	Set TX_EN, LB_HB low
2	Set VRAMP to 0 V
3	Apply VBAT
4	Apply RF drive to appropriate TXIN
5	Apply VREG
6	Set LB_HB for desired band
7	Set TX_EN high
8	Apply appropriate pulses to VRAMP
Power Down Sequence for TX	
1	Set VRAMP to 0 V
2	Set TX_EN low
3	Set LB_HB low
4	Remove VREG

Table 12. Power Up/Down Sequences (continued)

SEQ	DESCRIPTION
5	Remove RF drive
6	Remove VBAT

7 Design Information

7.1 Dual-, Tri- or Quad-band Application Optimization

The first step of the output matching for both low-band and high-band sections is integrated inside the MMM6035 module. The second step of the output matching is placed outside the module, allowing some flexibility for the customer to optimize the device for dual-, tri- or quad-band applications. This second step is achieved through the C6 and the C10 capacitors on the engineering board.

7.2 Power Control

The open loop power control of the power amplifier is enabled when TX_EN is set high. The PA drain voltage will then be proportional to the VRAMP input voltage over the range 200 mV to 2.2 V of VRAMP as shown in Figure 4.

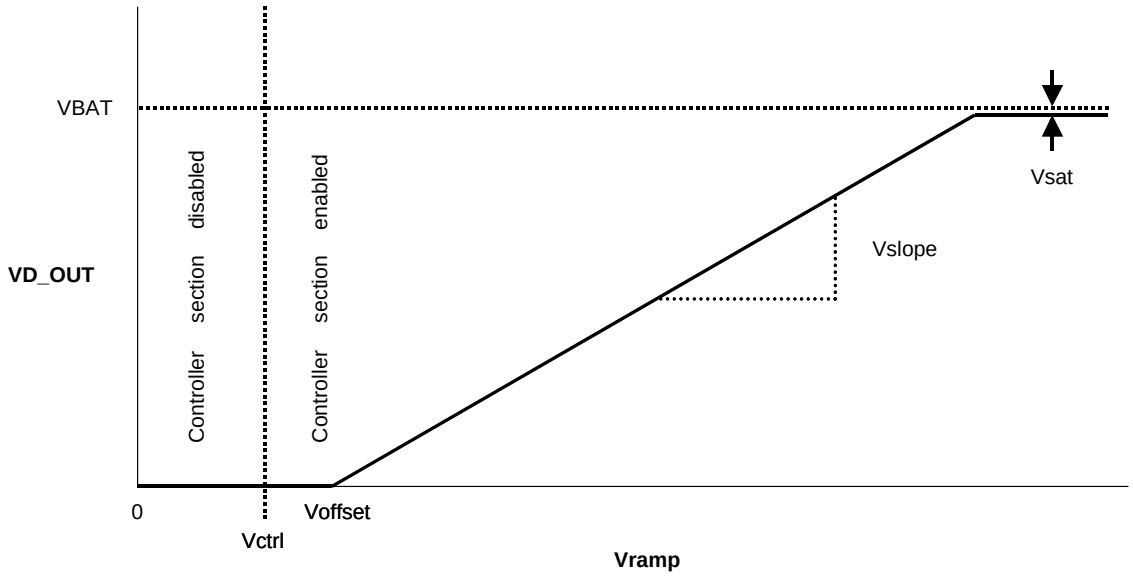
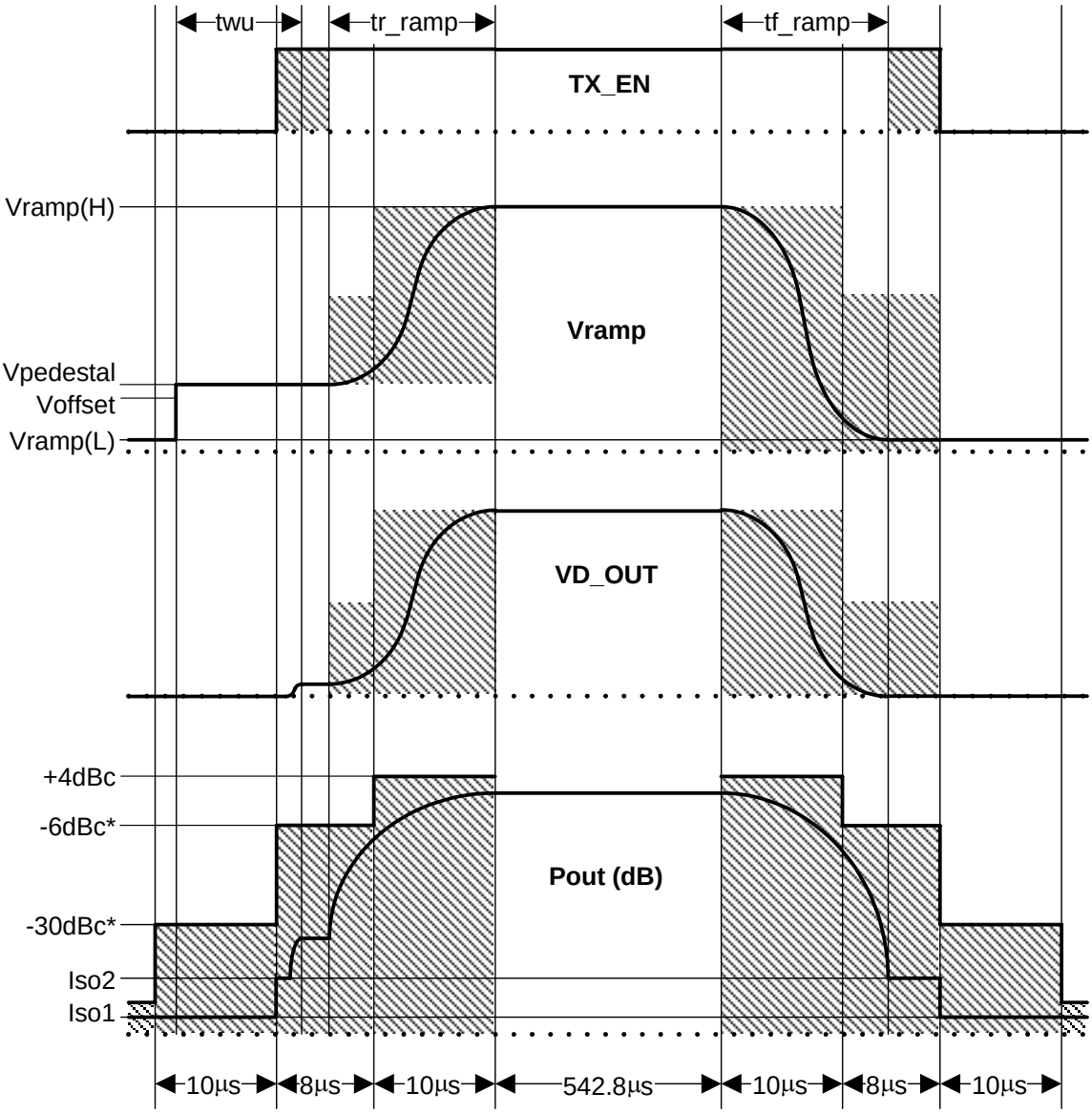


Figure 4. VD_OUT vs. VRAMP Characteristics

To meet the GSM power versus time mask and switching transient requirement, the MMM6035 must be provided with a DAC ramp profile on the VRAMP input, as well as proper timing on digital controls for the control loop circuitry as shown in Figure 5.



* Derated at low Pout

Figure 5. Recommended Power Control Timing

The ramp profile consists of a pedestal voltage, 12 to 16 discrete voltage steps on the rising edge of the burst, a constant region, 12 to 16 steps on the falling edge of the burst, and a final voltage. Generally, the same profile, scaled in amplitude, us used for all frequencies and power control levels.

A feature unique to the MMM6035 is the internal offset generator which functions to cancel any external offset associated with the DAC driving the VRAMP pin. In addition, the MMM6035 has a 200 kHz

two-pole Sallenkey filter included in the VRAMP path to remove DAC noise and to provide VRAMP signal smoothing.

7.3 Anti-Saturation Detection Feature

The MMM6035 prevents degradation of switching transients, regardless of battery conditions, due to an internal anti-saturation detection feature. The goal of this block is to maintain the RF output power ramp within the power versus time mask and to maintain acceptable spectral limits at specified offset frequencies.

The anti-saturation detection feature is implemented by a feedback loop inside the power control loop which detects when the power controller PMOS goes into the linear region. The feedback loop reduces VRAMP to maintain the pass device in its saturation region, even under low battery voltage conditions.

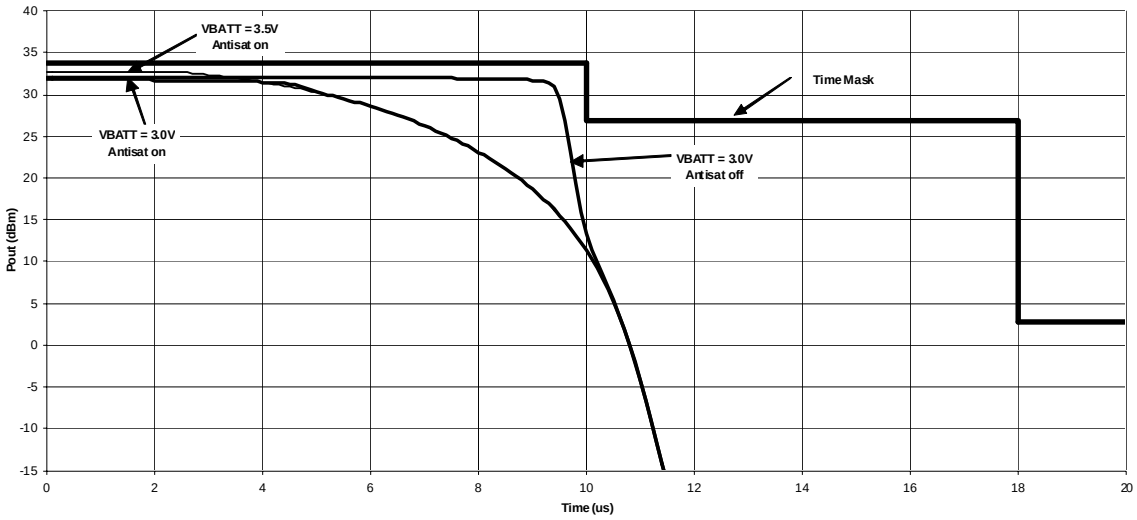


Figure 6. Anti-Saturation Detection

7.4 Recommended Power Control Calibration Procedure

Power control calibration is carried out at two points. The procedure first requires the measurement of output power (Po) calibration points at two values of Vramp (Vramp(1) and Vramp(2)). Figure 5 shows these points, after conversion (*), plotted on the RMS RF output voltage (Vrf) against the control voltage (Vramp) characteristic. Using these points, the Vramp voltage (Vramp(E)) can be estimated for any desired output power level. In order to meet the transmitted power level versus time requirement of GSM05.05 Specification, at the lowest power level, it is also necessary to determine the Vramp pedestal voltage (see Figure 4 and Figure 5) required to reach an acceptable power level when the controller section feedback loop has stabilized after wake-up.

As a reminder:

$$Vrf = 10^{(Po-13)/20} \qquad \textit{Eqn. 1}$$

where Po is in dBm into 50 Ω and Vrf is in Vrms.

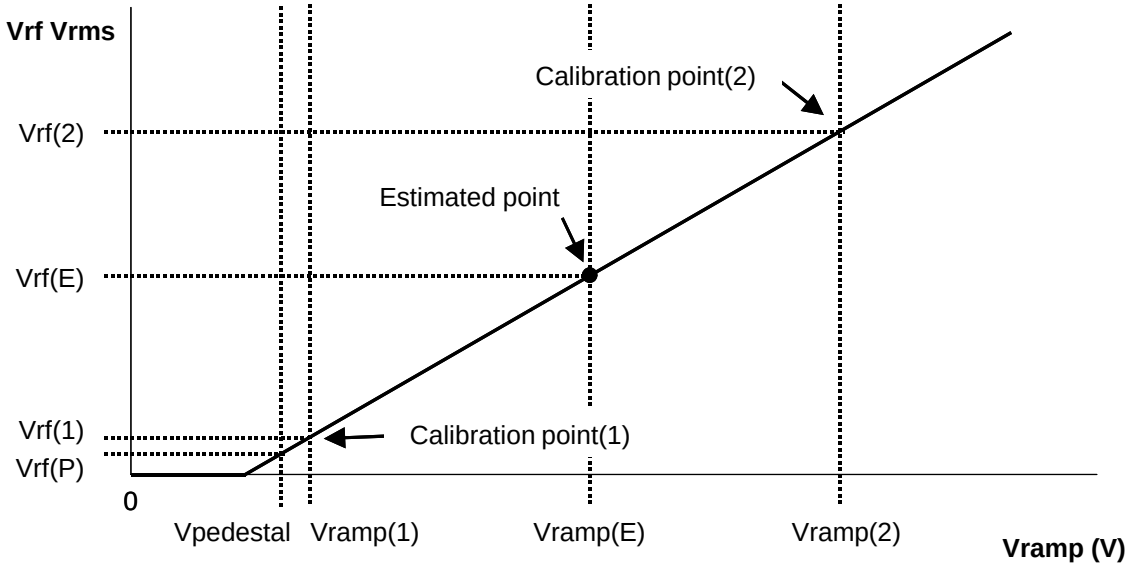


Figure 7. Vrf vs. Vramp characteristic

The calibration points Vrf(1) and Vrf(2) are each measured by forcing Vramp levels of Vramp(1) and Vramp(2) respectively. The estimated Vramp level for the required RF output voltage Vrf(E) is then calculated from the following:

$$Vramp(E) = \frac{Vramp(2)x[Vrf(E) - Vrf(1)] + Vramp(1)x[Vrf(2) - Vrf(E)]}{Vrf(2) - Vrf(1)} \quad \textit{Eqn. 1}$$

In a similar way Vpedestal can be calculated:

$$Vpedestal = \frac{Vramp(2)x[Vrf(P) - Vrf(1)] + Vramp(1)x[Vrf(2) - Vrf(P)]}{Vrf(2) - Vrf(1)} \quad \textit{Eqn. 2}$$

Table 13. Recommended Calibration Values

Description	Symbol	Value	Unit
Vramp at calibration point (1)	Vramp(1)	0.3	V
Vramp at calibration point (2)	Vramp(2)	1.5	V
Output power with Vramp=Vpedestal (Low band)	Po(P)_LB	1	dBm
Output power with Vramp=Vpedestal (High band)	Po(P)_HB	-3.5	dBm
Active Vramp rise time	Tr_ramp	14	µs
Active Vramp fall time	Tf_ramp	14	µs
Pedestal Width	-	12	µs

8 Package Information

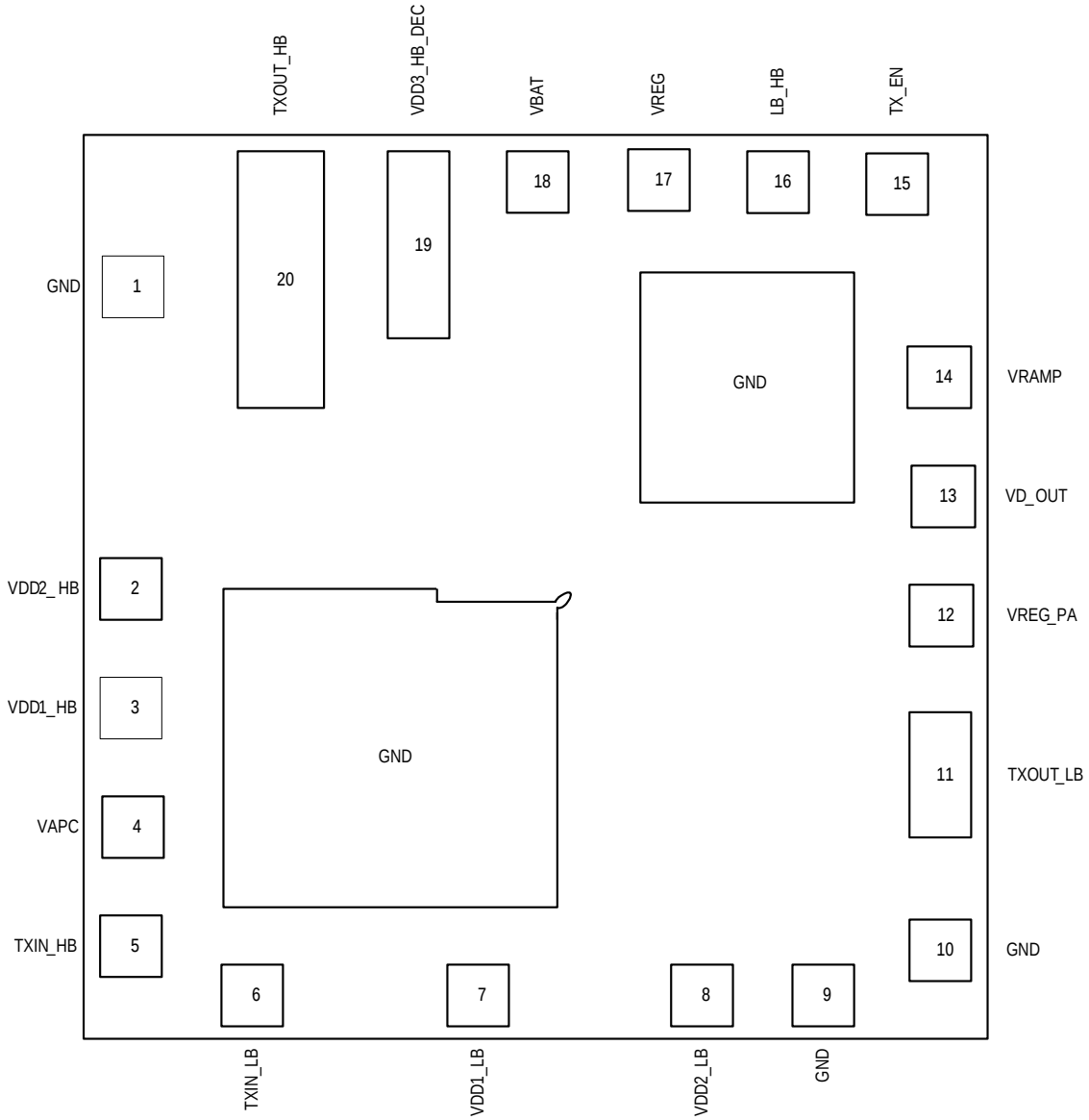


Figure 8. Package Footprint - Top View

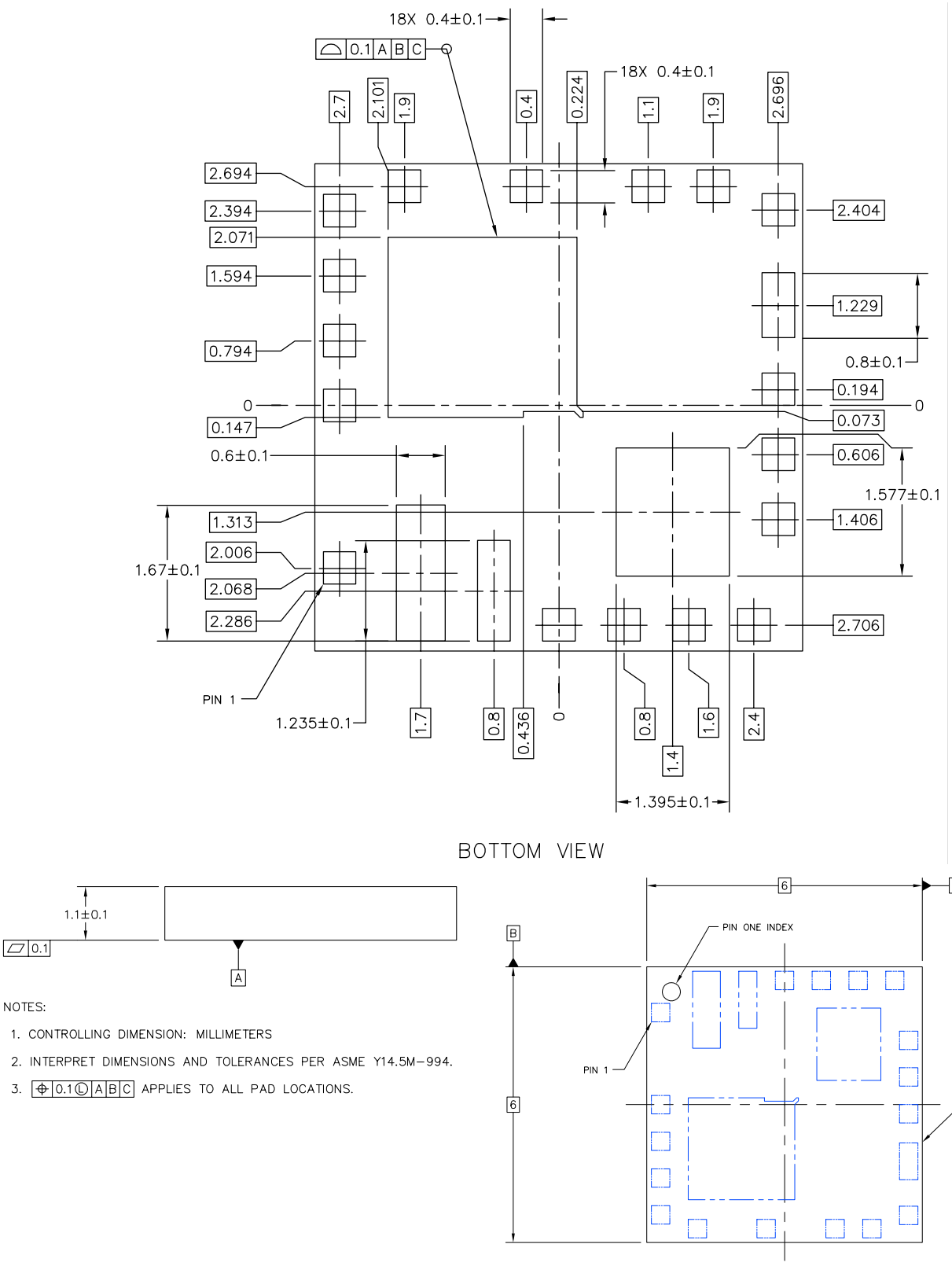


Figure 9. Outline Dimensions for 6x6 mm Module
(Case 1561-01, Issue O)

9 Signal Description

Table 14. Pin Connections

Number	Name	Description	Type	Impedance
1	GND	Ground	Ground	Ground
2	VDD2_HB	Drain Supply for Driver Stage, High-Band	Supply	
3	VDD1_HB	Drain Supply for Pre-Driver Stage, High-Band	Supply	
4	VAPC	Bias Control Voltage		
5	TX_IN_HB	TX Input High-Band	RF Input	50 Ω – DC Blocked
6	TX_IN_LB	TX Input Low-Band	RF Input	50 Ω – DC Blocked
7	VDD1_LB	Drain Supply for Pre-Driver Stage, Low-Band	Supply	
8	VDD2_LB	Drain Supply for Driver Stage, Low-Band	Supply	
9	GND	Ground	Ground	Ground
10	GND	Ground	Ground	Ground
11	TXOUT_LB	TX Output Low-Band		50 Ω – NOT DC Blocked
12	VREG_PA	Regulated DC supply output active only when TX_EN is high. Used for external biasing of the power amplifier section.	Supply	
13	VD_OUT	Power Control IC Output	Supply	
14	VRAMP	DAC power control ramp	Control	
15	TX_EN	Enable Power Control when set High	Control	
16	LB_HB	Low-Band/High-Band Select. Logic High for High-Band, Logic Low for Low-Band.	Control	
17	VREG	External Regulated Voltage	Supply	
18	VBAT	Drain supply for power control chip	Supply	
19	VDD3_HB_DEC	High-Band Final Stage RF Decoupling	RF	
20	TXOUT_HB	TX Output High-Band	RF Output	50 Ω – NOT DC Blocked

10 Product Documentation

This data sheet provides an abbreviated version of the full data sheet for the stated device. The full data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com on the Documentation page.

How to Reach Us:

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USA/Europe or Locations Not Listed:
Freescale Semiconductor
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1300 N. Alma School Road
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+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
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