MOTOROLA
Semiconductor Products Sector

Order Number: MPC106ARXTGPNS/D
Rev. 0, 8/2001

Motorola Part Number Affected:
MPC106ARXTG

PowerPC™

Application-Specific Information

PowerPC RISC Support and Peripheral Chips: MPC106 Part Number Specifications

This document defines a unique part number for a PowerPC™ MPC106 PCI Bridge/Memory Controller manufactured by Motorola. It describes changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the *MPC106 Hardware Specification*.

Specifications provided in this data sheet supersede those of the *MPC106 Hardware Specifications* (order # MPC106EC/D); specifications not addressed herein are unchanged.

Note that headings and tables in this data sheet are not numbered; however, they are intended to correspond directly to the heading or table affected in the general hardware specifications. Any additional information (including tables) not included in the hardware specifications are noted.

Part numbers addressed in this document and a summary of their differences from the general specification are listed in the following table. For more detailed ordering information, see Table 12.

Table 1. Part Numbers Addressed by this Part Number Specification

Motorola Part Number	Operating Condition	Significant Differences
	T_J (°C)	
MPC106ARXTG	-40 to 105	Extended temperature; VCO operating range

1.4 Electrical and Thermal Characteristics

This section provides any changes to the AC and DC electrical specifications and thermal characteristics for the MPC106 parts described herein.

1.4.1 DC Electrical Characteristics

The following table describes the changed thermal operating conditions for the MPC106 part numbers described herein.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit
Junction temperature	T_j	-40 to 105	ºC

Note: Parts with TG suffix only.

1.4.2.1 Clock AC Specifications

The following tables provides the revised VCO AC timing specifications for the parts described herein. Assume Vdd = AVdd = 3.3 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, and -40 ≤ T_j ≤ 105 °C.

Table 6. Clock AC Timing Specifications

Num	Characteristic	SYSCLK/Core 33/66 MHz		SYSCLK/Core 33/83.3 MHz		Unit
		Min	Max	Min	Max	
—	60x processor bus (core) frequency	16.67	66	16.67	83.3	MHz
—	VCO frequency	150	400	150	400	MHz
—	SYSCLK frequency	16.67	33.33	16.67	33.33	MHz
1	SYSCLK cycle time	30.0	60.0	30.0	60.0	ns
2, 3	SYSCLK rise and fall time	—	2.0	—	2.0	ns
4	SYSCLK duty cycle measured at 1.4 V	40	60	40	60	%
—	SYSCLK jitter	—	±200	—	±200	ps
—	106 internal PLL relock time	—	100	—	100	µs

1.8.1 PLL Configuration

Table 11. PLL Configuration

PLL[0–3][1]	Core/SYSCLK Ratio	VCO Multiplier	Core Frequency (VCO Frequency) in MHz			
			PCI Bus 16.6 MHz	PCI Bus 20 MHz	PCI Bus 25 MHz	PCI Bus 33.3 MHz
0010	1:1	x8	—	—	—	33.3 (266)
0101	2:1	x4	—	40 (160)	50 (200)	66.6 (266)
0110	5:2 [2]	x2	—	—	—	83.3 (166)
0111	5:2 [2]	x4	41.6 (166)	50 (200)	62.5 (250)	83.3 (333)
1000	3:1	x2	—	—	75 (150)	—

Table 11. PLL Configuration (Continued)

PLL[0–3][1]	Core/SYSCLK Ratio	VCO Multiplier	Core Frequency (VCO Frequency) in MHz			
			PCI Bus 16.6 MHz	PCI Bus 20 MHz	PCI Bus 25 MHz	PCI Bus 33.3 MHz
1001	3:1	x4	—	60 (240)	75 (300)	—
0011	PLL-bypass [3]		PLL off SYSCLK clocks core circuitry directly 1x core/SYSCLK ratio implied			
1111	Clock off [4]		PLL off no core clocking occurs			

Notes:

1 PLL[0–3] settings not listed are reserved. Some PLL configurations may select bus, CPU, or VCO frequencies which are not useful, not supported, or not tested. See Section 1.4.2.1, “Clock AC Specifications,” for valid SYSCLK and VCO frequencies.

2 5:2 clock modes are only supported by MPC106 Rev 4.0; earlier revisions do not support 5:2 clock modes. The 5:2 modes require a 60x bus clock applied to the 60x clock phase ($\overline{\text{LBCLAIM}}$) configuration input signal during power-on reset, hard reset, and coming out of sleep and suspend power-saving modes.

3 In PLL-bypass mode, the SYSCLK input signal clocks the internal circuitry directly, the PLL is disabled, and the core/SYSCLK ratio is set for 1:1 mode operation. This mode is intended for factory use and third-party tool vendors only. **Note also**: The AC timing specifications given in this document do not apply in PLL-bypass mode.

4 In clock-off mode, no clocking occurs inside the MPC106 regardless of the SYSCLK input.

1.10 Ordering Information

The following table provides the ordering information for the extended temperature MPC106 part numbers described herein.

Table 12. Ordering Information for the PowerPC 106

Package Type	Device Rev	Process	CPU Frequency (MHz)	Motorola Part Number
304 CBGAP	4.0	PPC1.4	66, 83	MPC106ARXTG

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