Advance Information

MPC107APXPNS/D
Rev. 1, 11/2002

MPC107 Part Number Specification for the XPC107APXnnnWx Series

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Motorola Part Numbers Affected:

XPC107APX133WD

This document describes part-number-specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the *MPC107 PCI Bridge/Memory Controller Hardware Specifications* (Order No. MPC107EC/D).

Specifications provided in this document supersede those in the *MPC107 PCI Bridge/Memory Controller Hardware Specifications*, Rev.1 or later, for the part numbers listed in Table A only. Specifications not addressed herein are unchanged. Because this document is frequently updated, refer to http://www.motorola.com/semiconductors or to your Motorola sales office for the latest version.

Note that headings and table numbers in this document are not consecutively numbered. They are intended to correspond to the heading or table affected in the general hardware specification.

Part numbers addressed in this document are listed in Table A. For more detailed ordering information, see Section 1.9, “Ordering Information.”

Table A. Part Numbers Addressed by This Data Sheet

Motorola Part Number	Operating Conditions			Significant Differences from Hardware Specification
	Memory Bus Frequency (MHz)	V_{DD}	T_j (°C)	
XPC107APX133WD	133	2.7 ± 100 mV	0 to 85	Modified voltage and temperature specifications to achieve 133 MHz

Note: The X prefix in a Motorola part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.3 General Parameters

This section summarizes changes to the general parameters of the MPC107 described in the *MPC107 PCI Bridge/Memory Controller Hardware Specifications*.

Core power supply 2.7 V ± 100 mV DC nominal

1.4.1 DC Electrical Characteristics

Table 2 provides the recommended operating conditions for the MPC107 part numbers described herein.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Supply voltage	V_{DD}	2.7 ± 100 mV	V	4
PLL supply voltage	AV_{DD}	2.7 ± 100 mV	V	5
DLL supply voltage	LAV_{DD}	2.7 ± 100 mV	V	5
Die-junction temperature	T_j	0 to 85	°C	

Cautions:

4. OV_{DD} must not exceed $V_{DD}/AV_{DD}//LAV_{DD}$ by more than 1.8 V at any time, including during power-on reset.
5. $V_{DD}/AV_{DD}//LAV_{DD}$ must not exceed OV_{DD} by more than 0.6 V at any time, including during power-on reset.

Table 5 provides the power consumption for the MPC107 part numbers described herein.

Table 5. Power Consumption

Mode	CI_SYNC_IN/Core Frequency (MHz)		Unit	Notes
	66/133			
	V_{DD} Power	I/O Power		
Typical	1230	1308	mW	1, 2
Doze	476	1022	mW	1, 2
Nap	356	1108	mW	1, 2
Sleep	149	1056	mW	1, 2

Notes:
1. Power is extrapolated at V_{DD} = 2.7 V, GV_{DD} = OV_{DD} = BV_{DD} = 3.45 V.
2. All clock drivers enabled.

Table 10 provides the processor bus AC timing specifications for the MPC107 part numbers described herein.

Table 10. Output AC Timing Specifications

Num	Characteristic [3, 6]	Min	Max	Unit	Notes
12b	Memory interface signals, SDRAM_SYNC_IN to output valid	—	4.5	ns	1
12e	60x Processor interface signals, SDRAM_SYNC_IN to output valid	—	4.5	ns	1

Notes:
1. All memory and related interface output signal specifications are specified from the VM = 1.4 V of the rising edge of the memory bus clock, SDRAM_SYNC_IN to the TTL level (0.8 or 2.0 V) of the signal in question. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 7 in the *MPC107 PCI Bridge/Memory Controller Hardware Specifications*.

Table 13 provides the I^2C frequency divider register (I2CFDR) information for the MPC107 133-MHz memory bus.

Table 13. MPC107 Maximum I^2C Input Frequency

FDR Hex [2]	Divider [2, 3] (Dec)	Max I^2C Input Frequency [1]
		SDRAM_CLK @ 133 MHz
20, 21	160, 192	4.58 MHz
22, 23, 24, 25	224, 256, 320, 384	2.95 MHz
0, 1	288, 320	2.18 MHz
2, 3, 26, 27, 28, 29	384, 448, 480, 512, 640, 768	1.72 MHz
4, 5	576, 640	1.22 MHz
6, 7, 2A, 2B, 2C, 2D	768, 896, 960, 1024, 1280, 1536	943
8, 9	1152, 1280	648
A, B, 2E, 2F, 30, 31	1536, 1792, 1920, 2048, 2560, 3072	494
C, D	2304, 2560	335
E, F, 32, 33, 34, 35	3072, 3584, 3840, 4096, 5120, 6144	253
10, 11	4608, 5120	170
12, 13, 36, 37, 38, 39	6144, 7168, 7680, 8192, 10240, 12288	128
14, 15	9216, 10240	85
16, 17, 3A, 3B, 3C, 3D	12288, 14336, 15360, 16384, 20480, 24576	64
18, 19	18432, 20480	43
1A, 1B, 3E, 3F	24576, 28672, 30720, 32768	32
1C, 1D	36864, 40960	21
1E, 1F	49152, 61440	16

Notes:
1. Values are in kHz unless otherwise specified.
2. FDR Hex and Divider (Dec) values are listed in corresponding order.
3. Multiple Divider (Dec) values will generate the same input frequency, but each Divider (Dec) value will generate a unique output frequency as shown in Table 14 of the *MPC107 PCI Bridge/Memory Controller Hardware Specifications* document.

1.6 PLL Configuration

The MPC107 internal PLLs are configured by the PLL_CFG[0:3] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. Table 18 provides the PLL configurations for the MPC107 part numbers described herein.

Table 18. MPC107 Bridge Controller PLL Configuration

Ref	PLL_CFG[0:3] [2]	133 MHz Part		PCI:Core Ratio	VCO Multiplier
		PCI_SYNC_IN Range (MHz)	Core/Mem/CPU Range (MHz)		
1	0001	25[5]–50[4]	25–50	1	4
2	0010	12.5[5]–25[4]	25–50	2	4
3	0011	Bypass [2]		Bypass	Bypass
5	0101	25[5]–66	50–133	2	2
8	1000	16[5]–44	50–132	3	2
9	1001	33[5]–66	50–100	1.5	2
C	1100	20[5]–53	50–133	2.5	2
D	1101	50[5]–66	50–66	1	2
F	1111	Clock off [3]	Not usable	Off	Off

Notes:
1. PLL_CFG[0:3] settings not listed (0000, 0100, 0110, 0111, 1010, 1011, and 1110) are reserved.
2. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal core directly, the PLL is disabled, and the PCI:core mode is set for 1:1 mode operation. The AC timing specifications given in this document do not apply in PLL bypass mode.
3. In clock off mode, no clocking occurs inside the MPC107 regardless of the PCI_SYNC_IN input.
4. Limited due to maximum memory VCO = 200 MHz.
5. Limited due to minimum memory VCO = 133 MHz.
6. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.

1.9 Ordering Information

1.9.1 Part Numbers Fully Addressed by This Document

Table 20 provides the ordering information for the MPC107 parts described in this document.

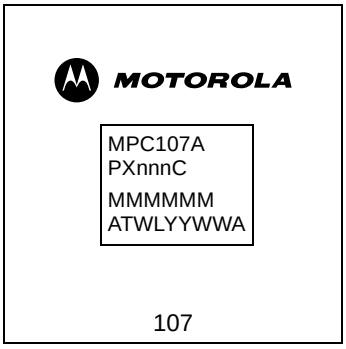
Table 20. Part Marking Nomenclature

XPC	*nnn*	*x*	*xx*	*nnn*	W	*x*
Product Code	**Part Identifier**	**Part Modifier**	**Package [1]**	**Frequency [2]**	**Process Descriptor**	**Revision Level**
XPC	107	A	PX = PBGA	133	W: 2.7 V ± 100 mV 0 to 85°C	D:1.4; Rev. ID:0x14

Notes:
1. See Section 1.5, “Package Description,” in the *MPC107 PCI Bridge/Memory Controller Hardware Specifications,* for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only.

1.9.3 Part Marking

Parts are marked as the example shown in Figure 26.



PBGA

Notes:
MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 26. Motorola Part Marking for PBGA Device

Document Revision History

Table B provides a revision history for this part number specification.

Table B. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release. Released as XPC.
1	Changed document number to MPC. Renumbered Notes in Table 2. Added Table 10. Added Section 1.9.3. Added Document Revision History table.

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