

Advance Information

700 mA Dual H-Bridge Motor Driver with 3.0 V Compatible Logic I/O

The 17530 is a monolithic dual H-Bridge power IC ideal for portable electronic applications containing bipolar step motors and/or brush DC-motors (e.g., cameras, disk drive head positioners, etc.).

The 17530 operates from 2.0 V to 6.8 V, with independent control of each H-Bridge via parallel MCU interface. The device features on-board charge pump, as well as built-in shoot-through current protection and an undervoltage shutdown function.

The 17530 has four operating modes: Forward, Reverse, Brake, and Tri-States (High Impedance). The 17530 has a low total $R_{DS(ON)}$ of 1.2 Ω (max @ 25°C).

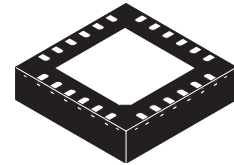
The 17530 efficiently drives many types of micromotors with low power dissipation owing to its low output resistance and high output slew rates. The H-Bridge outputs can be independently pulse width modulated (PWM'ed) at up to 200 kHz for speed/torque and current control.

Features

- Low Total $R_{DS(ON)}$ 0.8 Ω (Typ), 1.2 Ω (Max) @ 25°C
- Output Current 0.7 A (DC)
- Shoot-Through Current Protection Circuit
- PWM Control Input Frequency up to 200 kHz
- Built-In Charge Pump Circuit
- Low Power Consumption
- Undervoltage Detection and Shutdown Circuit
- Pb-Free Packaging Designated by Suffix Code EP

17530

3.0 V LOGIC COMPATIBLE 700 mA DUAL H-BRIDGE MOTOR DRIVER IC

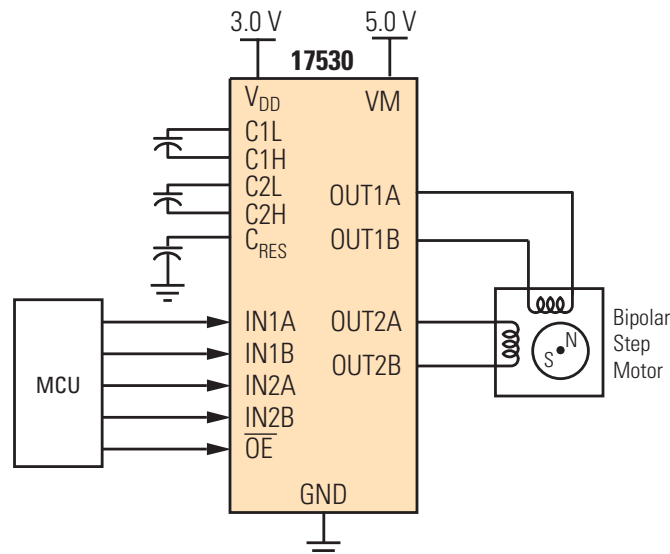


EP (Pb-FREE) SUFFIX
CASE 1508-01
24-LEAD QFN

ORDERING INFORMATION

Device	Temperature Range (T _A)	Package
MPC17530EP/R2	-20°C to 65°C	24 QFN

17530 Simplified Application Diagram



This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

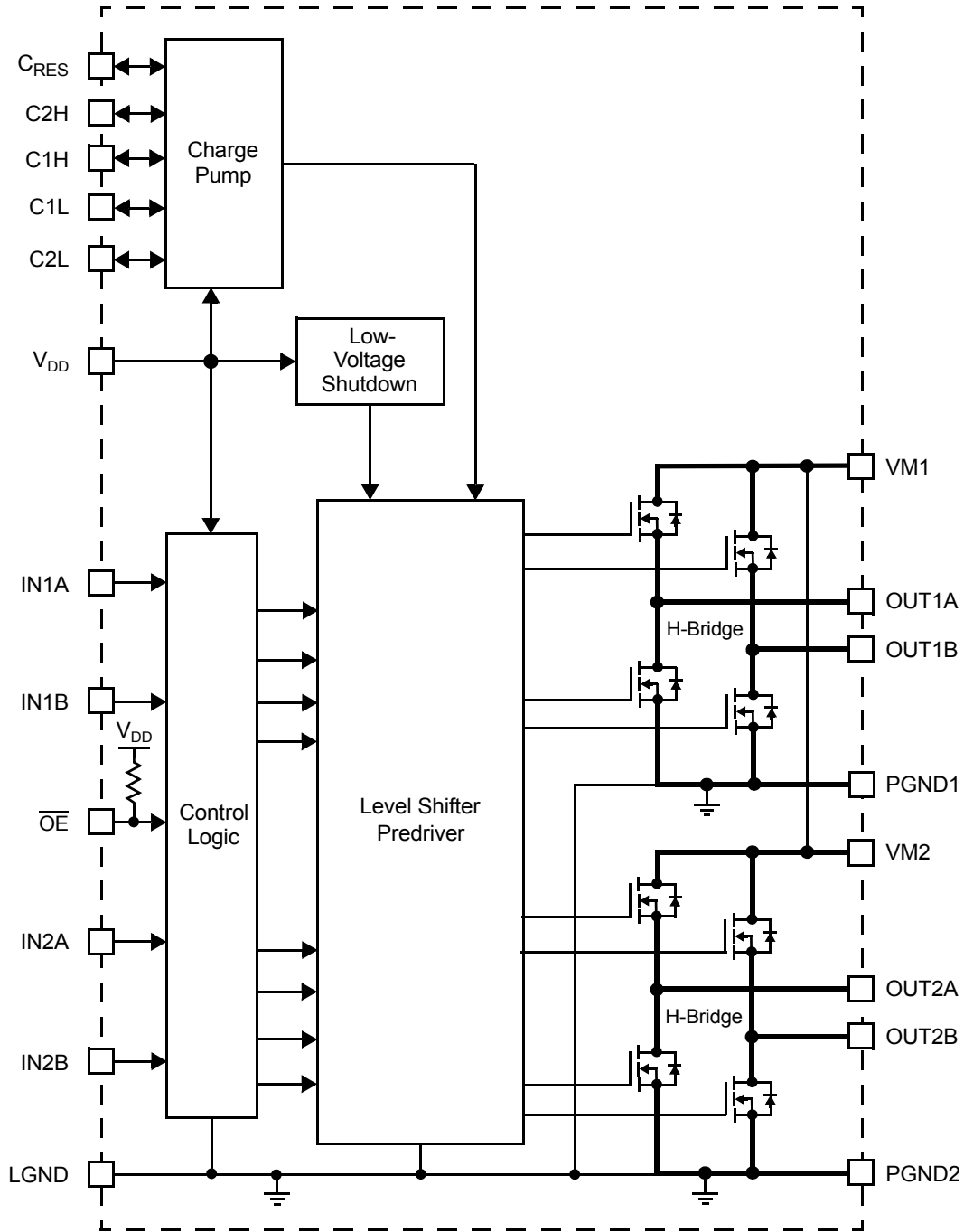
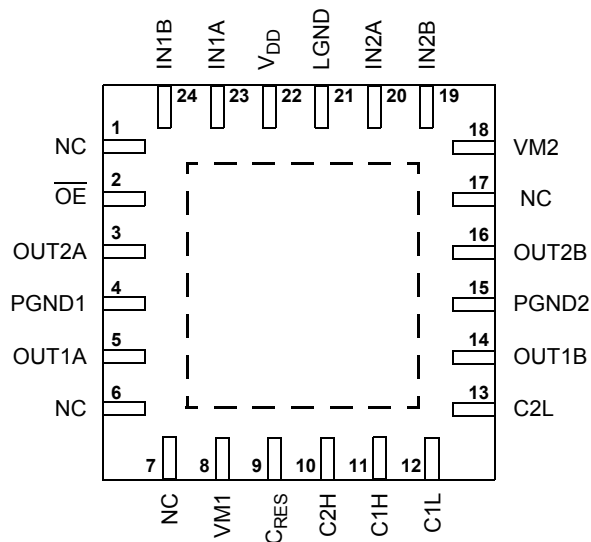


Figure 1. 17530 Simplified Internal Block Diagram



TERMINAL FUNCTION DESCRIPTION

Terminal	Terminal Name	Formal Name	Definition
1, 6, 7, 17	NC	No Connect	This terminal is not used.
2	\overline{OE}	Output Enable	Logic output Enable control of H-Bridges (Low = True).
3	OUT2A	H-Bridge Output 2A	Output A of H-Bridge channel 2.
4	PGND1	Power Ground 1	High-current power ground 1.
5	OUT1A	H-Bridge Output 1A	Output A of H-Bridge channel 1.
8	VM1	Motor Drive Power Supply 1	Positive power source connection for H-Bridge 1 (Motor Drive Power Supply).
9	C _{RES}	Predriver Power Supply	Internal triple charge pump output as pre-driver power supply.
10	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).
11	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
12	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).
13	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
14	OUT1B	H-Bridge Output 1B	Output B of H-Bridge channel 1.
15	PGND2	Power Ground 2	High-current power ground 2.
16	OUT2B	H-Bridge Output 2B	Output B of H-Bridge channel 2.
18	VM2	Motor Drive Power Supply 2	Positive power source connection for H-Bridge 2 (Motor Drive Power Supply).
19	IN2B	Logic Input Control 2B	Logic input control of OUT2B (refer to Table 1, Truth Table , page 7).
20	IN2A	Logic Input Control 2A	Logic input control of OUT2A (refer to Table 1, Truth Table , page 7).
21	LGND	Logic Ground	Low-current logic signal ground.
22	V _{DD}	Control Circuit Power Supply	Positive power source connection for control circuit.
23	IN1A	Logic Input Control 1A	Logic input control of OUT1A (refer to Table 1, Truth Table , page 7).
24	IN1B	Logic Input Control 1B	Logic input control of OUT1B (refer to Table 1, Truth Table , page 7).

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted. Exceeding the ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Motor Supply Voltage	V_M	-0.5 to 8.0	V
Charge Pump Output Voltage	V_{CRES}	-0.5 to 14	V
Logic Supply Voltage	V_{DD}	-0.5 to 5.0	V
Signal Input Voltage	V_{IN}	-0.5 to $V_{DD}+0.5$	V
Driver Output Current			A
Continuous	I_O	0.7	
Peak (Note 1)	I_{OPK}	1.4	
ESD Voltage			V
Human Body Model (Note 2)	V_{ESD1}	±1000	
Machine Model (Note 3)	V_{ESD2}	±100	
Operating Junction Temperature	T_J	-20 to 150	°C
Operating Ambient Temperature	T_A	-20 to 65	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C
Thermal Resistance (Note 4)	$R_{\theta JA}$	50	°C/W
Power Dissipation (Note 5)	P_D	2.5	W
Soldering Temperature (Note 6)	T_{SOLDER}	260	°C

Notes

- $T_A = 25^\circ\text{C}$, 10 ms pulse at 200 ms interval.
- ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP} = 100 \text{ pF}$, $R_{ZAP} = 1500 \ \Omega$).
- ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP} = 200 \text{ pF}$, $R_{ZAP} = 0 \ \Omega$).
- Mounted on 37 x 50 Cu area (1.6 mm FR-4 PCB).
- $T_A = 25^\circ\text{C}$.
- Soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

 Characteristics noted under conditions $T_A = 25^\circ\text{C}$, $V_{DD} = V_M = 5.0\text{ V}$, $\text{GND} = 0\text{ V}$ unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER					
Motor Supply Voltage	V_M	2.0	5.0	6.8	V
Logic Supply Voltage	V_{DD}	2.7	3.0	3.6	V
Driver Quiescent Supply Current (No Signal Input)	I_{QM}	–	–	100	μA
Logic Quiescent Supply Current (No Signal Input) (Note 7)	I_{QVDD}	–	–	1.0	mA
Operating Power Supply Current Logic Supply Current (Note 8) Charge Pump Circuit Supply Current (Note 9)	I_{VDD} I_{CRES}	– –	– –	3.0 0.7	mA
Low V_{DD} Detection Voltage (Note 10)	V_{DDDET}	1.5	2.0	2.5	V
Driver Output ON Resistance (Note 11)	$R_{DS(ON)}$	–	0.8	1.2	Ω

GATE DRIVE

Gate Drive Voltage (Note 9) No Current Load	V_{CRES}	12	13	13.5	V
Recommended External Capacitance (C1L–C1H, C2L–C2H, C_{RES} –GND)	C_{CP}	0.01	0.1	1.0	μF

CONTROL LOGIC

Logic Input Voltage	V_{IN}	0	–	V_{DD}	V
Logic Inputs ($2.7\text{ V} < V_{DD} < 3.3\text{ V}$)					
High-Level Input Voltage	V_{IH}	$V_{DD} \times 0.7$	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	$V_{DD} \times 0.3$	V
High-Level Input Current	I_{IH}	–	–	1.0	μA
Low-Level Input Current	I_{IL}	-1.0	–	–	μA
$\overline{\text{OE}}$ Terminal Input Current Low	$I_{IL-\overline{\text{OE}}}$	–	50	100	μA

Notes

- I_{QVDD} includes the current to pre-driver circuit.
- I_{VDD} includes the current to predriver circuit at $f_{IN} = 100\text{ kHz}$.
- At $f_{IN} = 20\text{ kHz}$.
- Detection voltage is defined as when the output becomes high-impedance after V_{DD} drops below the detection threshold. When the gate voltage V_{CRES} is applied from an external source, $V_{CRES} = 7.5\text{ V}$.
- $I_O = 0.7\text{ A}$ source + sink.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions $T_A = 25^\circ\text{C}$, $V_{DD} = V_M = 5.0\text{ V}$, $\text{GND} = 0\text{ V}$ unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

INPUT

Pulse Input Frequency	f_{IN}	–	–	200	kHz
Input Pulse Rise Time (Note 12)	t_R	–	–	1.0 (Note 13)	μs
Input Pulse Fall Time (Note 14)	t_F	–	–	1.0 (Note 13)	μs

OUTPUT

Propagation Delay Time (Note 15)					μs
Turn-ON Time	t_{PLH}	–	0.1	0.5	
Turn-OFF Time	t_{PHL}	–	0.1	0.5	
Charge Pump Wake-Up Time (Note 16)	t_{VGON}	–	1.0	3.0	ms
Low-Voltage Detection Time	t_{VDDDET}	–	–	10	ms

Notes

12. Time is defined between 10% and 90%.
13. That is, the input waveform slope must be steeper than this.
14. Time is defined between 90% and 10%.
15. Output load is $8.0\ \Omega$ DC.
16. $C_{CP} = 0.1\ \mu\text{F}$.

Timing Diagrams

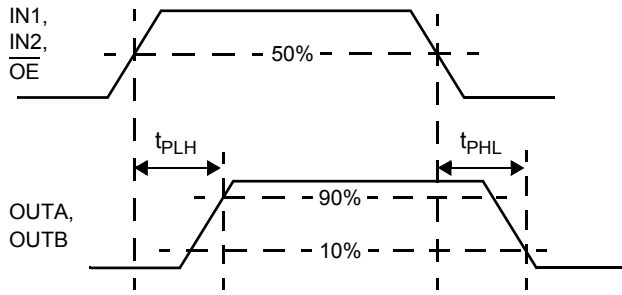


Figure 2. t_{PLH} , t_{PHL} , and t_{PZH} Timing

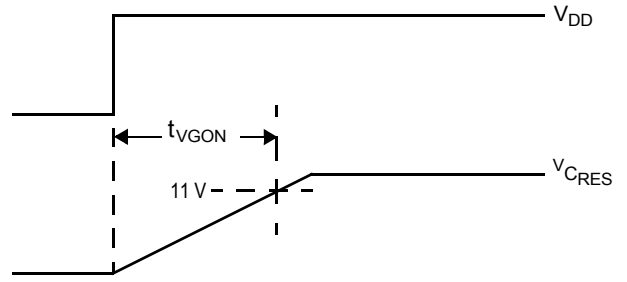


Figure 4. Charge Pump Timing

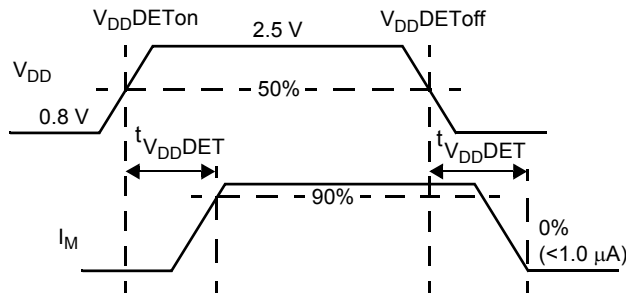


Figure 3. Low-Voltage Detection Timing

Table 1. Truth Table

INPUT			OUTPUT	
\overline{OE}	IN1A IN2A	IN1B IN2B	OUT1A OUT2A	OUT1B OUT2B
L	L	L	L	L
L	H	L	H	L
L	L	H	L	H
L	H	H	Z	Z
H	X	X	Z	Z

H = High.
 L = Low.
 Z = High impedance.
 X = Don't care.
 \overline{OE} terminal is pulled up to V_{DD} with internal resistance.

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 17530 is a monolithic dual H-Bridge ideal for portable electronic applications to control bipolar step motors and brush DC motors such as those found in camera lens assemblies, camera shutters, and optical disk drives. The device features an on-board charge pump, as well as built-in shoot-through current protection and undervoltage shutdown.

The 17530 has four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance). The MOSFETs comprising the output bridge have a total source + sink $R_{DS(ON)} \leq 1.2 \Omega$.

The 17530 can simultaneously drive two brush DC motors or one bipolar step motor. The drivers are designed to be PWM'ed at frequencies up to 200 kHz.

FUNCTIONAL TERMINAL DESCRIPTION

V_{DD}

The V_{DD} terminal carries the logic supply voltage and current into the logic sections of the IC. V_{DD} has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input terminals.

IN1A, IN1B, IN2A, and IN2B

These logic input terminals control each H-Bridge output. IN1A logic HIGH = OUT1A HIGH. However, if all inputs are taken HIGH, the outputs bridges are both tri-stated (refer to [Table 1, Truth Table](#), page 7).

 \overline{OE}

The \overline{OE} terminal is a LOW = TRUE enable input. When \overline{OE} = HIGH, all H-Bridge outputs (OUT1A, OUT1B, OUT2A, and OUT2B) are tri-stated (High-Z) regardless of logic inputs (IN1A, IN1B, IN2A, and IN2B) states.

OUT1A, OUT1B, OUT2A, and OUT2B

These terminals provide connection to the outputs of each of the internal H-Bridges (see [Figure 1, 17530 Simplified Internal Block Diagram](#), page 2).

VM1 and VM2

The VM terminals carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the loads attached between the OUTput terminals. All VM terminals must be connected together on the printed circuit board.

C1L and C1H, C2L and C2H

These two pairs of terminals, the C1L and C1H and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 μ F.

C_{RES}

The C_{RES} terminal is the output of the internal charge pump. Its output voltage is approximately three times of V_{DD} voltage. The V_{CRES} voltage is power supply for the internal predriver circuit of H-Bridges.

PGND

Power ground terminals. They must be tied together on the PCB.

LGND

Logic ground terminal.

APPLICATIONS

Typical Application

Figure 5 shows a typical application for the 17530. When applying the gate voltage to the C_{RES} terminal from an external source, be sure to connect it via a resistor equal to, or greater than, $R_G = V_{C_{RES}}/0.02 \Omega$.

The internal charge pump of this device is generated from the V_{DD} supply; therefore, care must be taken to provide sufficient gate-source voltage for the high-side MOSFETs when $V_M \gg V_{DD}$ (e.g., $V_M = 5.0 \text{ V}$, $V_{DD} = 3.3 \text{ V}$), in order to ensure full enhancement of the high-side MOSFET channels.

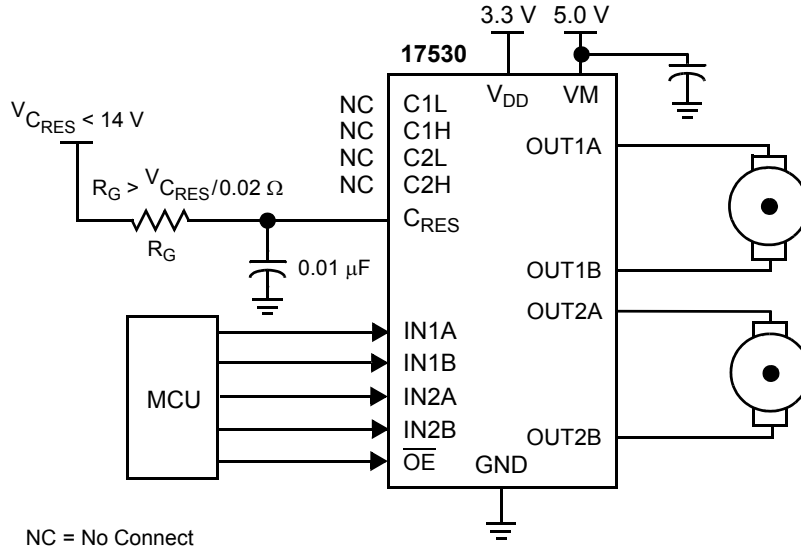


Figure 5. 17530 Typical Application Diagram

CEMF Snubbing Techniques

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients via placing a capacitor or zener at the supply terminal (VM) (see Figure 6).

PCB Layout

When designing the printed circuit board (PCB), connect sufficient capacitance between power supply and ground terminals to ensure proper filtering from transients. For all high-current paths, use wide copper traces and shortest possible distances.

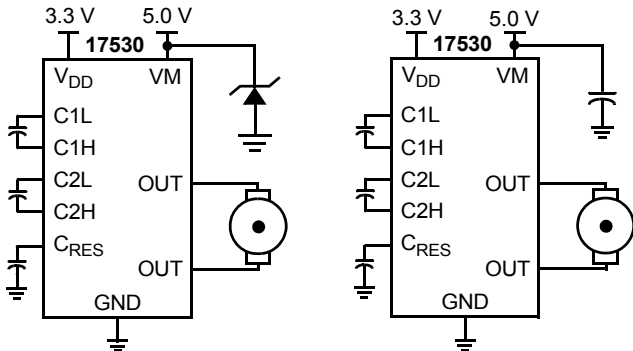
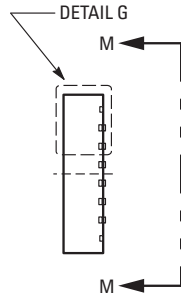
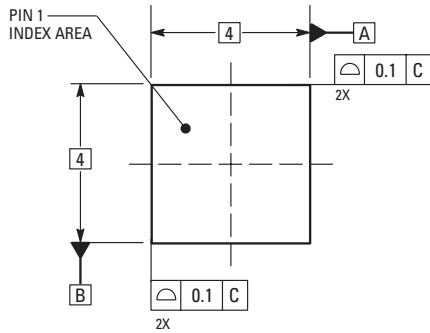


Figure 6. CEMF Snubbing Techniques

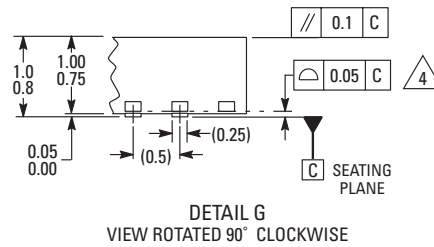
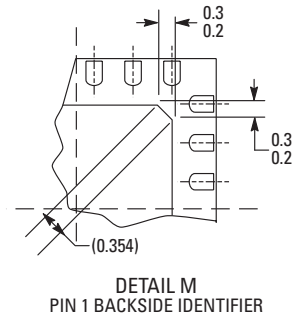
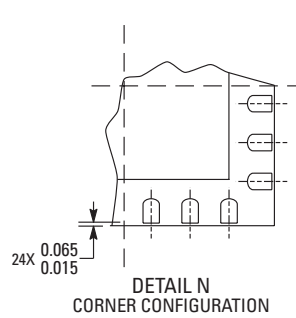
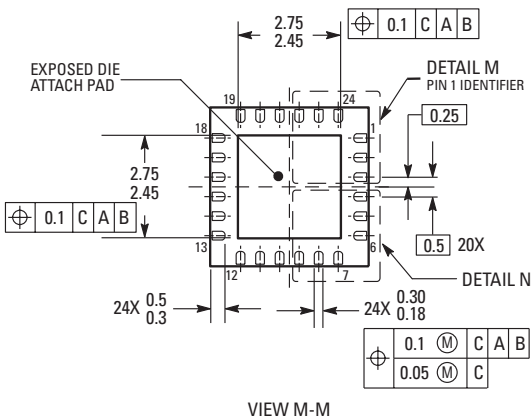
PACKAGE DIMENSIONS

EP (Pb-FREE) SUFFIX
 24-LEAD QFN
 NON-LEADED PACKAGE
 CASE 1508-01
 ISSUE O



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.



Freescale Semiconductor, Inc.



NOTES

Freescale Semiconductor, Inc.

Information in this document is provided solely to enable system and software implementers to use Motorola products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.

MOTOROLA and the Stylized M Logo are registered in the US Patent and Trademark Office. All other product or service names are the property of their respective owners.

© Motorola, Inc. 2004

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution
P.O. Box 5405, Denver, Colorado 80217
1-800-521-6274 or 480-768-2130

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center
3-20-1 Minami-Azabu, Minato-ku, Tokyo 106-8573, Japan
81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre
2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong
852-26668334

HOME PAGE: <http://motorola.com/semiconductors>



MOTOROLA

**For More Information On This Product,
Go to: www.freescale.com**

MPC17530